Powerline Modules

200Mbps Modules

The Bel Single In-line Package (SIP) module is HomePlug AV, open-standard-based MAC/PHY/AFE Powerline Communications (PLC) transceiver/modem.

The Module provides an integrated solution for Powerline communications. The "Black Box" design requires no external software and only a few external components to create a working solution. Operate as a Phy or Mac is selectable via Pull up/down resistor.

Communication is possible over any 2 wire system DC/AC/Dry wire and can provide real world data rates of up to 90Mbps.

Key Features & Benefits

- Based on Atheros' AR6400/AR1400 chipset
- Supports HomePlug® AV Standard with data rates of 200Mbps
- MII (Host & PHY) interface
- Supports1024/256/64/16/8-QAM, QPSK, BPSK, and ROBO modulation schemes
- 128-bit AES Link Encryption with key management for secure power line communications
- Windowed OFDM with noise mitigation based on patented line synchronization techniques improves data integrity in noisy conditions
- Dynamic channel adaptation and channel estimation maximizes throughput in harsh channel conditions
- Horizontal mounting configuration using standard 1.27mm pin header (50 way)
- Integrates all components necessary to add HomePlug AV functionality to any embedded system at low cost

RoHS Compliant

Part Number	Mount	Temp Range	interface
0804-5000-18	Horizontal	0 – 70°C	MII
0804-5000-24	Horizontal	-40 - +85°C Including Heatsink	MII

bel POWER SOLUTIONS & PROTECTION
a bel group

Bel Modules
28 Turkey Court, Turkey Mill, Ashford Road
Maidstone ME14 5PP UK

+44 1622 757 395
techhelp@belf.com
belfuse.com

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Rev A

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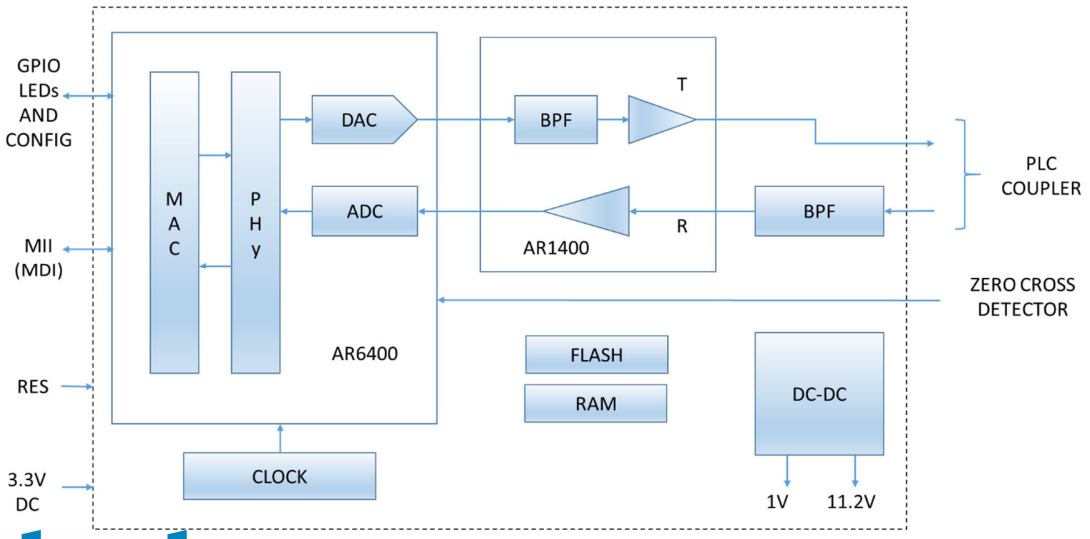
Module Interface
All module connectivity is provided via a 50 way 1.27mm pitch gold pin header.

Pin Number	Pin Name	Pin Number	Pin Name
1	VDD	26	MDC
2	VSS	27	Do not connect
3	VDD	28	Do not connect
4	VSS	29	VSS
5	VDD	30	MRX_D0
6	TX+	31	MRX_D1
7	TX-	32	MRX_D2
8	VSS	33	MRX_D3
9	RX+	34	COL
10	RX-	35	MRX_CLK
11	RESET/	36	VSS
12	GPIO0	37	MRX_ERR
13	GPIO1	38	MRX_DV
14	GPIO2	39	MTX_D0
15	GPIO3	40	MTX_D1
16	GPIO4	41	MTX_D2
17	GPIO5	42	MTX_D3
18	GPIO6	43	CRS
19	GPIO7	44	MTX_CLK
20	GPIO8	45	MTX_EN
21	GPIO9	46	VSS
22	GPIO10	47	PHY_RST/
23	GPIO11	48	VSS
24	ZC_IN	49	PHY_CLK
25	MDIO	50	VSS

Module Block Diagram
* Dotted line signifies Modules External connectivity.



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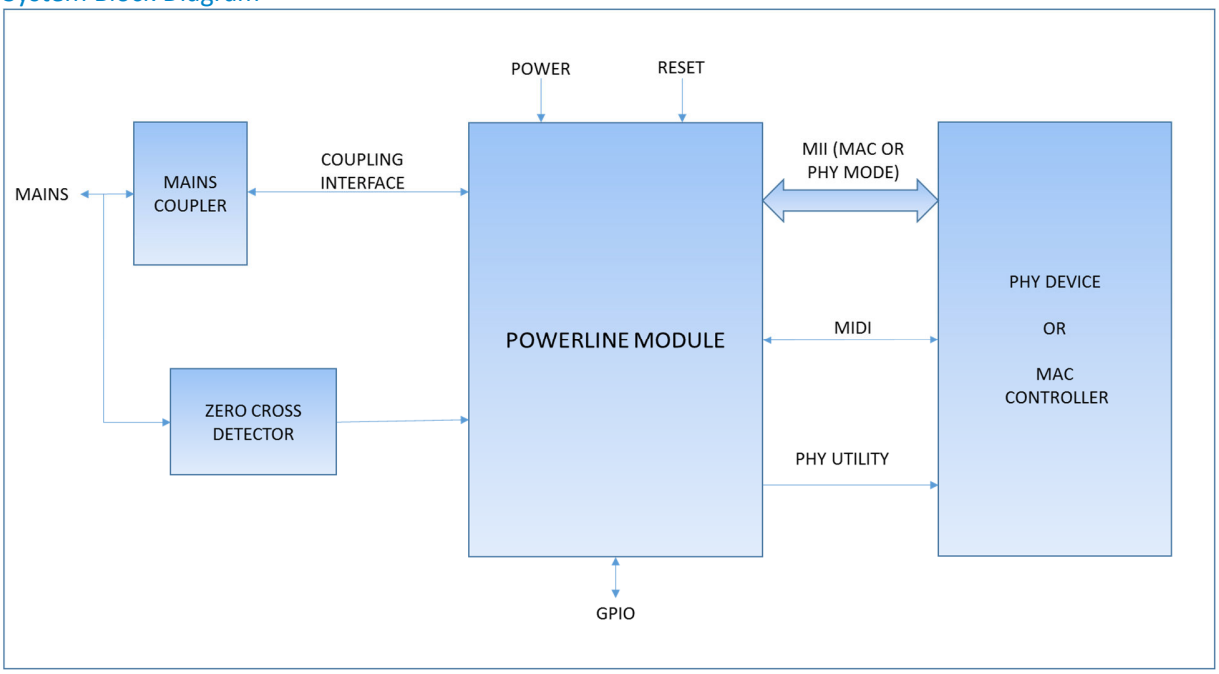
System Block Diagram



* The block diagram presents the Powerline module in a typical environment.

Media Independent Interface (MII)

The MII interface is configured as either an Ethernet Medium Access Controller (MAC) or a Physical Medium Dependent (PMD or PHY) controller. Medium Independent Interface (MII) is an industry standard, multi-vendor interface between the MAC and PHY sub-layers. It provides a simple connection between Ethernet PHY controllers and IEEE802.3 Ethernet MACs from a variety of sources.

MII consists of separate 4-bit data paths for transmit and receive data along with carrier sense and collision detection. Further details of the MII are available from the IEEE 802.3u Standard.

The configuration options section describes the straps required for MII operation to a MAC or PHY controller. The MAC and PHY configurations support 10 Mbps or 100 Mbps in half-duplex or full-duplex modes and flow control for half-duplex and full-duplex connections. The Ethernet MAC module implements standard Ethernet MAC functionality. The Ethernet MAC is connected to an external Ethernet PHY function. The MAC configuration provides bridging between Ethernet and the Powerline. The PHY configuration emulates Ethernet PHY functionality and provides HomePlug AV connectivity to devices designed to communicate over an Ethernet network.

The MII (Ethernet) interface has separate transmit and receive packet buffering. When operating as a MAC the MII transmit FIFO is 2 KB and the receive FIFO is 8 KB. When operating as a PHY controller, the MII transmit FIFO is 8 KB and the receive FIFO is 2 KB.

MII MAC Operation

The MII MAC configuration operates as an IEEE 802.3 10/100-Mbps Ethernet MAC connected to an external 10/100-Mbps Ethernet PHY.

When the Powerline module boots it attempts to configure the MII MAC interface. It will first scan all external MII PHYs starting from PHY #0 and will select the first PHY that responds with valid register contents.

The PHY's Link Status register will be read, and if the link is up, auto-negotiation will be performed. If the PHY's status indicates that auto-negotiation is not supported, auto-negotiation will not be performed.

Based upon the results of the PHY's status registers, or auto-negotiation results, the PHY will be configured in an operational mode (i.e. no loopback, no collision test, not in isolate etc.) The MII MAC within the Powerline module will be configured for the same speed and duplex. External devices do not have direct access to any MII MAC registers in the Powerline chipset.

MII PHY Operation

The MII PHY emulation hardware connects to an external 10/100-Mbps Ethernet MAC. The default PHY functionality is configured through standard management data interface communications (MDI interface) and may be overridden by the Powerline chipset. MAC firmware access to the PHY emulation registers. The interface supports the standard control and status register.

- Link speed at 10 Mbps or 100 Mbps
- Full-duplex or half-duplex operation
- Management data interface base address
- Isolate to disconnect the PHY from the MII port

In PHY mode, auto-negotiation is not supported. GPIO strapping on the Powerline module will determine the desired configuration, these straps will be reflected in the default settings in the MII PHY emulation registers.

Interface Signals

Pin Number	Pin Name	I/O		Description
		MAC Mode	PHY Mode	
30 31 32 33	MRX-D0 MRX-D1 MRX-D2 MRX-D3	I	O	MII Receive Data. The PHY controller drives MRX_D[3:0] and the MAC core receives MRX_D[3:0]. MRX_D[3:0] transition synchronously with respect to MRX_CLK. For each MRX_CLK period in which MRX_DV is asserted, MRX_D[3:0] is valid. MRX_D0 is the least-significant bit. The PHY controller tri-states MRX_D[3:0] in isolate mode.
34	COL	I	O	MII Collision Detected. The PHY controller asserts COL when it detects a collision on the medium. COL remains asserted while the collision condition persists. COL signal transitions are not synchronous to either the MTX_CLK or the MRX_CLK. The MAC core ignores the COL signal when operating in the full-duplex mode. The PHY controller tristates COL in isolate mode.
35	MRX_CLK	I	O	MII Receive Clock. MRX_CLK is a continuous clock that provides the timing reference for the transfer of the MRX_DV and MRX_D[3:0] signals from the PHY controller to the MAC core. The PHY controller sources MRX_CLK. MRX_CLK frequency is equal to 25% of the data rate of the received signal on the Ethernet cable. The PHY controller tri-states MRX_CLK in isolate mode.
37	MRX_ERR	I	O	MII Receive Error. The PHY controller asserts MRX_ERR high for one or more MRX_CLK periods to indicate to the MAC core that an error (a coding error or any error that the PHY is capable of detecting that is otherwise undetectable by the MAC) was detected somewhere in the current frame. MRX_ERR transitions synchronously with respect to MRX_CLK. While MRX_DV is de-asserted, MRX_ERR has no effect on the MAC core. The PHY controller tri-states MRX_ERR in isolate mode.

Pin Number	Pin Name	I/O		Description
		MAC Mode	PHY Mode	
38	MRX_DV	I	O	MII Receive Data Valid. The PHY controller asserts MRX_DV to indicate to the MAC core that it is presenting the recovered and decoded data bits on MRX_D[3:0] and that the data on MRX_D[3:0] is synchronous to MRX_CLK. MRX_DV transitions synchronously with respect to MRX_CLK. MRX_DV remains asserted continuously from the first recovered nibble of the frame through the final recovered nibble, and is de-asserted prior to the first MRX_CLK that follows the final nibble. The PHY controller tri-states MRX_DV in isolate mode.
39 40 41 42	MTX_D0 MTX_D1 MTX_D2 MTX_D3	O	I	MII Transmit Data. The MAC core drives MTX_D[3:0] and the PHY controller receives MTX_D[3:0]. MTX_D[3:0] transitions synchronously with respect to MTX_CLK. For each MTX_CLK period in which MTX_EN is asserted, MTX_D[3:0] is valid. MTX_D0 is the least significant bit. The PHY controller ignores MTX_D[3:0] in isolate mode.
43	CRS	I	O	MII Carrier Sense. The PHY controller asserts CRS when either transmit or receive medium is non-idle. The PHY de-asserts CRS when both transmit and receive medium are idle. The PHY must ensure that CRS remains asserted throughout the duration of a collision condition. The transitions on the CRS signal are not synchronous to either the MTX_CLK or the MRX_CLK. The PHY controller tri-states CRS in isolate mode.
44	MTX_CLK	I	O	MII Transmit Clock. MTX_CLK is a continuous clock that provides a timing reference for the transfer of the MTX_EN and MTX_D[3:0] signals from the MAC core to the PHY controller. The PHY controller sources MTX_CLK. The operating frequency of MTX_CLK is 25 MHz when operating at 100 Mbps and 2.5 MHz when operating at 10 Mbps. The PHY controller tri-states MTX_CLK in isolate mode.

MII Management Data Interface (MDI)

The MII interface has a two-wire bi-directional serial Management Data Interface (MDI). This interface provides access to the status and control registers in the Ethernet PHY logic. The MII and MDI pins are shared between the MAC and PHY interfaces.

Pin Number	Pin Name	I/O		Description
		MAC Mode	PHY Mode	
25	MDIO	I/O	I/O	MII Management Data In/Out. This is the data input signal from the PHY controller. The PHY drives the Read Data synchronously with respect to the MDC clock during the read cycles. This is also the data output signal from the MAC core that drives the control information during the Read/Write cycles to the PHY controller. The MAC core drives the MDO signal synchronously with respect to the MDC. An external pull-up resistor is needed on this pin.
26	MDC	O	I/O	MII Management Data Clock. The MAC core sources MDC as the timing reference for transfer of information on the MDIO signal. MDC signal has no maximum high or low times. MDC minimum high and low times are 160 ns each, and the minimum period for MDC is 400 ns.

General Purpose Input/Output (GPIO) Pins Interface

The GPIO Pins have two uses, firstly for configuration and secondly as status outputs and control inputs. The following table shows the provided default Pull Up/Pull Down configuration.

Pin Number	Pin Name	Configuration Strap Function	Internal Pull Up/Down
12	GPIO0	N/A	Up
13	GPIO1	N/A	Up
14	GPIO2	N/A	Up
15	GPIO3	ISODEF	Up
16	GPIO4	SPEED	Up
17	GPIO5	MD_A3	Up
18	GPIO6	CFG_SEL	Down
19	GPIO7	MD_A4	Down
20	GPIO8	MP_SEL	Up
21	GPIO9	N/A	Down
22	GPIO10	BM_SEL	Down
23	GPIO11	N/A	Down

The following table shows the GPIO usage for user input and lead status feedback.

GPIO	I/O	Default Function After Reset
GPIO1	I	Typically connected to a push-button. This GPIO is used to add a new device to, or remove an old device from, a HomePlug AC logical network.
GPIO2	I	Typically connected to a push-button. The factory default can be restored by applying a low-level digital voltage on GPIO2 for greater than 0.5 seconds and less than 3.0 seconds.
GPIO8	O	To be connected to an LED. The LED gives indications about Powerline link & activity. On: Powerline link detected. Flash: TX or RX Powerline activity (if the Powerline chipset is serving as a Station). Off: Powerline link not detected.
GPIO9	O	To be connected to an LED. The LED gives indications about Ethernet link & activity. On: Ethernet link detected. Flash: Transmit or receive activity. Off: No link detected.
GPIO10	O	To be connected to an LED. The LED gives indications about Powerline mode. On N/A Flash: HomePlug1.0trafficdetected. Off: Silence.
GPIO11	O	To be connected to an LED. The LED gives indication about power. On: Power ready. Flash: Load firmware. (Boot loader mode) Off: Power not ready.

1. The Powerline link LED indicator turns On when Powerline link is detected. If the Powerline chipset module is serving as a STATION (STA), the LED indicator will flash to indicate, transmit or receive Powerline activity. If the INT6400 module is serving as a CCO (central co-ordinator), the LED indicator will light steadily ON, even in the presence of Powerline activity.

2. The module flash memory is corrupted / blank, the module ROM based code will blink the POWER LED On and Off at a frequency of one cycle per second.

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PHY Utility Interface

Pin Number	Pin Name	I/O	Description
47	PHY_RST/	O	PHY device Reset (active low). Connect to an external Ethernet PHY. This reset output is a stretched version of the RESET/ input.
49	PHY_CLK	O	25MHz Clock Out. This output is a dedicated clock output that can be used to drive the clock input on an external Ethernet PHY. This clock output is only available when the Powerline chipset is configured in MAC mode, and not in PHY mode of operation. Note that if this output is used, it is strongly advised that the corresponding PHY_RST/ signal also be connected to the external Ethernet PHY.

Coupling Interface

Pin Number	Pin Name	I/O	Description
6	TX+	O	100R differential TX Line Driver output, connects to coupling transformer
7	TX-	O	100R differential TX Line Driver output, connects to coupling transformer
9	RX+	I	100R differential RX Line Filter input, connects to coupling transformer
10	RX-	I	100R differential RX Line Filter input, connects to coupling transformer

Special care must be taken during PCB layout of the coupling interface signals.

Route differential pairs close together and away from all other signals. Route each differential pair on the same PCB layer. Keep both traces of each differential pair as identical to each other as possible.

Wide copper is needed here to support current density of up to 30MHz. These high frequencies result in higher resistance due to skin effect. The wide traces also accommodate high transient currents caused by voltage spikes. Trace widths between the module and the coupling transformer must be no less than 0.020” (0.5 mm) and should be no greater than 0.030” (0.75 mm).

Use of the Bel Fuse 0557-7700-36, 0557-7700-40, 0557-7700-41 or 0557-7700-42 Powerline couplers is recommended. Details can be found on the Powerline Couplers datasheet.

Reset, Zero Crossing and Power connections

Pin Number	Pin Name	I/O	Description
1, 3, 5	VDD	I	+3.3V with respect to VSS
2, 4, 8, 29, 36, 46, 48, 50	VSS	I	Ground
11	RESET/	I	Resets all IC logic when low. Maintain this signal active for 100ms after the VDD rail is stable.
24	ZC_IN	I	Zero Cross Detector Input. This should be provided from a safety isolated source (opto isolator). The waveform is to correspond to the polarity of the AC live waveform. For dry wire or DC safety this should be connected to VCC via a pull up (10K). This information synchronizes the channel adaptation of the Powerline chipset to the line cycle periodic noise present on the power line.

Configuration Options

The Powerline chipset MII and boot options are selected by the initial condition of GPIO pins. If a GPIO pin is not used and its internal strapping resistor sets the booting option correctly, then the pin may be left unconnected. If a GPIO pin is not used but the internal strapping resistor sets the booting option incorrectly, then the pin must be pulled high or low to the correct booting option by an external resistor. This resistor can be 10 k-Ohms down to a few hundred Ohms. 3.3 k-Ohms is typical. Many GPIO pins are driven by firmware for LED output immediately after boot up so connecting these GPIO directly to ground or VDD is not permitted.

Pin Number	Pin Name	Strap Function	Internal Pull Up/Down	Default Function
15	GPIO3	ISODEF	Up	PHY MODE: Hi-Z MII interface
16	GPIO4	SPEED	Up	PHY MODE: 100Mbps
17	GPIO5	MD_A3	Up	PHY MODE: PHY address 0x0100
18	GPIO6	CFG_SEL	Down	BOOT: SDRAM parameters from Host
19	GPIO7	MD_A4	Down	PHY MODE: PHY address 0x0100
20	GPIO8	MP_SEL	Up	HOST: MAC mode
22	GPIO10	BM_SEL	Down	BOOT: Firmware from Host
49	PHY_CLK	DUPLEX	Up	PHY MODE: Full Duplex

MII Options

The MP_SEL strap is used to specify whether the Powerline chipset is configured for MII MAC mode, or in MII PHY mode (i.e. reverse-MII mode). The encoding of this signal is shown in the following table:

MP_SEL	Mode
0	MII in PHY mode
1	MII in MAC mode

MII PHY mode, there are 4 additional configuration straps that are unique to this mode of operation:

SPEED	MII Speed
0	10Mbps
1	100Mbps

DUPLEX	MII Duplex
0	Half Duplex
1	Full Duplex

ISODEF	Isolation
0	Normal Operation
1	Isolated

MD_A[3,4]	MII Management address
00	0x00
01	0x08
10	0x10
11	0x18

Boot Options

The BM_SEL strap is used to determine the source of the boot code for the embedded ARM processor. Similarly, the CFG_ SEL strap is used to determine the source of the SDRAM configuration applet. The encodings for these two signals is shown in the following table.

BM_SEL	CFG_SEL	Meaning
0	0	Load SDRAM configuration and boot code from external host. (Not recommended).
0	1	Load SDRAM configuration applet from Flash, and then load boot code from external host. (Not Recommended).
1	0	Not supported
1	1	Load SDRAM configuration and boot code from Flash. (Recommended).

Design Notes

Leave below lines unconnected if they are not unused:

- Pin 47: PHY_RST#
- Pin 49: PHY_CLK
- Pin 27: Reserved

Connect Pin 28 (Reserved) signal to the Ground.

Zero-cross detection circuit is not required for DC line connection, but to work correctly the PLC Module requires a pull-up resistor (10k) on ZC_IN line

Do not force other logic levels than default during the module boot on reserved GPIO strappings, GPIO 0-2 and 3.

When the Powerline module is in PHY mode, RX_ER signal should not be connected to the MII Bus. This line is NOT tri-stated. Use a 10k Ohm pull down resistor only.

General Specifications

Symbol	Parameter	Test Conditions	Min	Max	Units
VDD	Supply voltage (1)		3.0	3.6	V
VIL	Low-level input voltage			0.8	V
VIH	High-level input voltage		2.0		V
VOL	Low-level output voltage	IOL = 4 mA, 12 mA (2)		0.4	V
VOH	High-level output voltage	IOH = -4 mA, -12 mA (3)	2.4		V
IIL	Low-level input current	VI = Gnd	-1		µA
IIH	High-level input current	VI = 3.3 V		1	µA
IOZ	High-impedance output current	Gnd < VI < 3.3 V	-1	+1	µA
Top	Operating temperature range		-40	+85	° C

1. *A typical supply current, assuming a nominal operation of 50% transmit and 50% receive duty cycle, is 580 mA.*
2. *IOL=12 mA for all GPIOs. IOL = 4 mA for all other digital interfaces.*
3. *IOH = -12 mA for all GPIOs. IOH = -4 mA for all other digital interfaces.*

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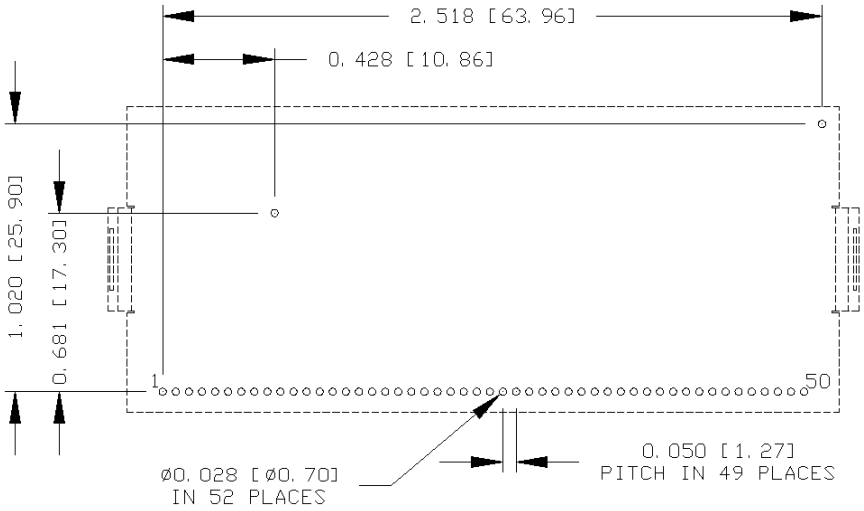
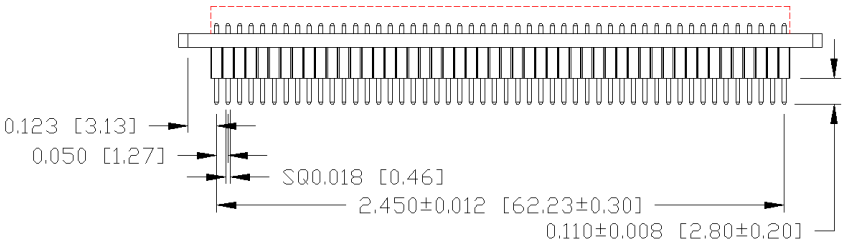
Mechanical

PCB Footprint





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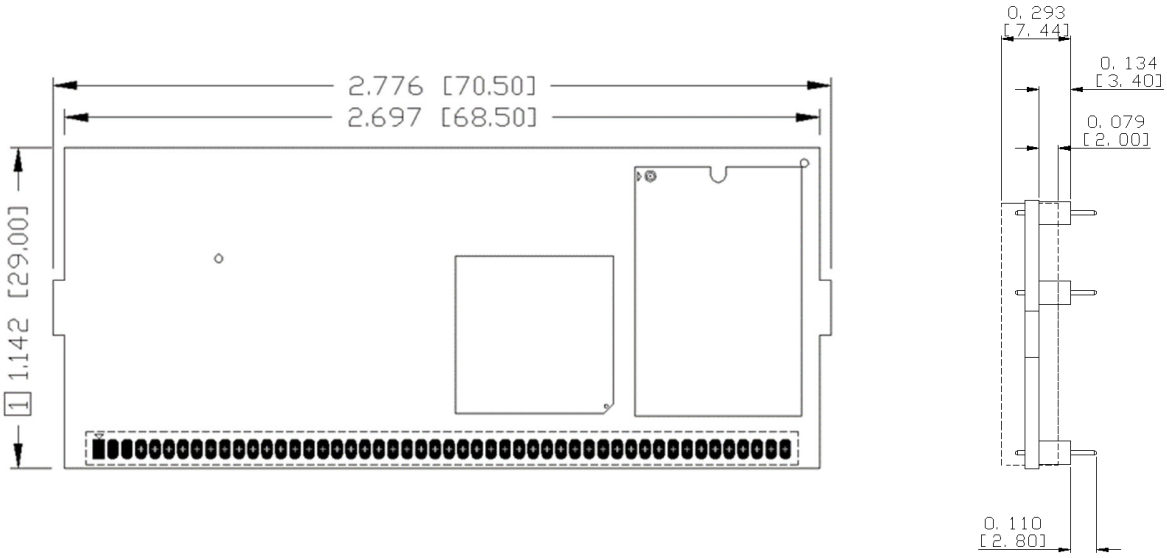
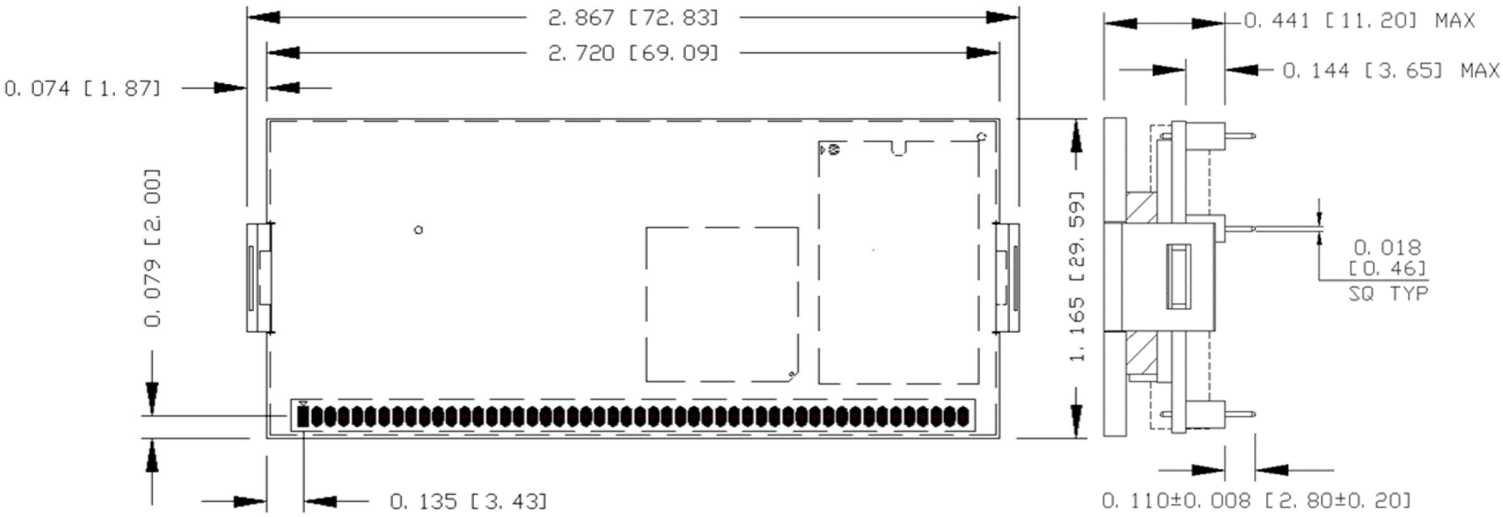
0804-5000-18 Horizontal Mount



0804-5000-24

Horizontal Mount - Industrial Temperature with Heatsink