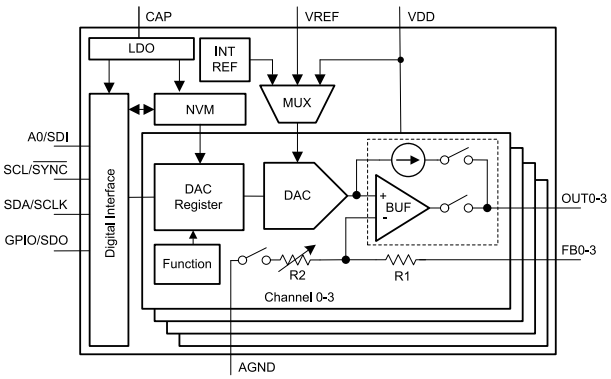
DACx3004 12-Bit and 10-Bit, Ultra-Low-Power, Quad Voltage and Current Output Smart DACs With Auto-Detected I²C, PMBus™, or SPI

1 Features

- Programmable voltage or current outputs with flexible configuration:
  - Voltage outputs:
    - 1 LSB INL and DNL (10-bit)
    - Gains of 1x, 1.5x, 2x, 3x, and 4x
  - Current outputs:
    - 1 LSB INL and DNL (8-bit)
    - Unipolar and bipolar output range options from 25 µA to 250 µA
- 50 µA/channel quiescent current in voltage-output mode
- Programmable comparator mode for all channels
- High-impedance output when VDD is off
- High-impedance and resistive pulldown power-down modes
- 25-MHz SPI-compatible interface
- Automatically detected I²C, PMBus™, or SPI interface
  - 1.62-V V_{IH} with V_{DD} = 5.5 V
- General-purpose input/output (GPIO) configurable as multiple functions
- Predefined waveform generation: sine wave, triangular, sawtooth
- User-programmable nonvolatile memory (NVM)
- Internal, external, or power-supply as reference
- Wide operating range:
  - Power supply: 1.8 V to 5.5 V
  - Temperature range: –40˚C to +125˚C
- Tiny package: 16-pin WQFN (3 mm × 3 mm)



Simplified Block Diagram

2 Applications

- Land mobile radio
- Pulse oximeter
- Optical module
- Standard notebook PC

3 Description

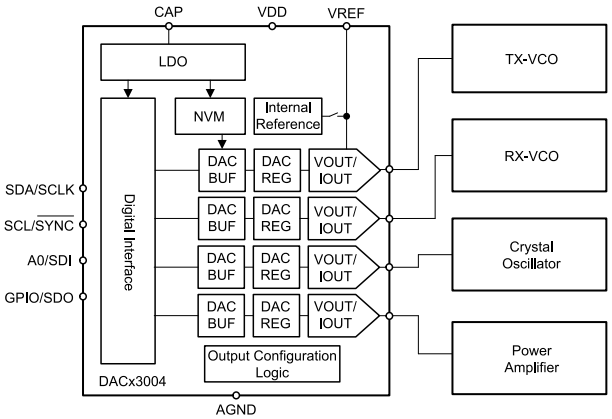
The 12-bit DAC63004 and 10-bit DAC53004 (DACx3004) are a pin-compatible family of ultra-low-power, quad-channel, buffered, voltage-output and current-output smart digital-to-analog converters (DACs). The DAC outputs are capable of both voltage and current output. These DACx3004 support Hi-Z power-down mode and Hi-Z output during power-off condition. The DAC outputs provide a force-sense option for use as a programmable comparator and current sink. The multifunction GPIO, function generation, and NVM enable these smart DACs for processor-less applications and design reuse. These devices also have an automatically detected I²C, PMBus, or SPI interface and an internal reference.

The feature set combined with the tiny package and ultra-low-power make these smart DACs an excellent choice for applications such as land mobile radio, pulseoximeter, notebook PCs, and other battery-operated applications for biasing, calibration, and waveform generation.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DACx3004	WQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DACx3004 for Biasing in Land Mobile Radio

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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4 Revision History

DATE	REVISION	NOTES
April 2021	*	Initial Release

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5 Pin Configuration and Functions

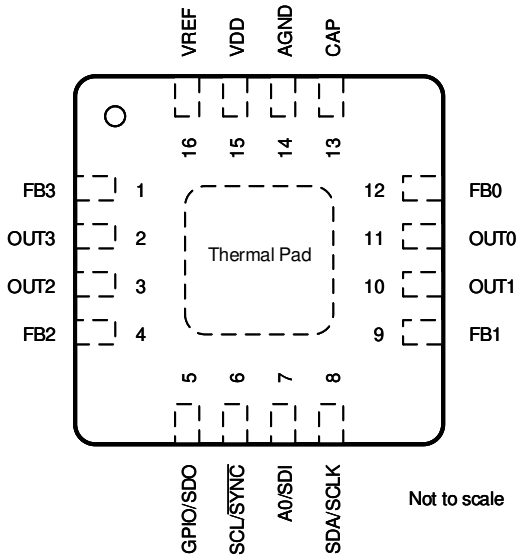

Figure 5-1. RTE Package, 16-pin WQFN, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	FB3	Input	Voltage feedback pin for channel 3. In voltage-output mode, connect to OUT3 for closed-loop amplifier output. In current-output mode, keep the FB3 pin unconnected to minimize leakage current.
2	OUT3	Output	Analog output voltage from DAC channel 3.
3	OUT2	Output	Analog output voltage from DAC channel 2.
4	FB2	Input	Voltage feedback pin for channel 2. In voltage-output mode, connect to OUT2 for closed-loop amplifier output. In current-output mode, keep the FB2 pin unconnected to minimize leakage current.
5	GPIO/SDO	Input/Output	General-purpose input/output configurable as $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, SDO, and $\overline{\text{PROTECT}}$. In $\overline{\text{STATUS}}$ and SDO functions, connect the pin to the IO voltage with an external pullup resistor.
6	SCL/$\overline{\text{SYNC}}$	Output	I^2C serial interface clock or SPI chip select input. This pin must be connected to the IO voltage using an external pullup resistor.
7	A0/SDI	Input	Address configuration pin for I^2C or serial data input for SPI. In A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. In SDI function, this pin need not be pulled up or pulled down.
8	SDA/SCLK	Input/Output	Bidirectional I^2C serial data bus or SPI clock input. This pin must be connected to the IO voltage using an external pullup resistor in the I^2C mode.
9	FB1	Input	Voltage feedback pin for channel 1. In voltage-output mode, connect to OUT1 for closed-loop amplifier output. In current-output mode, keep the FB1 pin unconnected to minimize leakage current.
10	OUT1	Output	Analog output voltage from DAC channel 1.
11	OUT0	Output	Analog output voltage from DAC channel 0.
12	FB0	Input	Voltage feedback pin for channel 0. In voltage-output mode, connect to OUT0 for closed-loop amplifier output. In current-output mode, keep the FB0 pin unconnected to minimize leakage current.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 µF) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V.
16	VREF	Power	External reference input. Connect a capacitor (approximately 0.1 µF) between VREF and AGND. Use a pullup resistor to VDD when the external reference is not used. This pin must not ramp up before VDD. In case an external reference is used, make sure the reference ramps up after VDD.
—	Thermal Pad	Ground	Connect the thermal pad to AGND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage, V_{DD} to A_{GND}	–0.3	6	V
	Digital inputs to A_{GND}	–0.3	V_{DD} + 0.3	V
	CAP to A_{GND}	–0.3	1.65	V
	V_{FBX} to A_{GND}	–0.3	V_{DD} + 0.3	V
	V_{OUTX} to A_{GND}	–0.3	V_{DD} + 0.3	V
	Current into any pin except the OUTx pins	–10	10	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, pins TBD[2]	±750	
		Charged device model (CDM), per JEDEC specification JESD22-C101, pins TBD[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive supply voltage to ground (A_{GND})	1.71		5.5	V
V_{IH}	Digital input high voltage, 1.7 V < V_{DD} ≤ 5.5 V	1.62			V
V_{IL}	Digital input low voltage			0.4	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DACx3004 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics - Voltage Output

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC63004	12			Bits
	Resolution	DAC53004	10			Bits
INL	Relative accuracy[1]	DAC63004	–4		4	LSB
INL	Relative accuracy[1]	DAC53004	–1		1	LSB
DNL	Differential nonlinearity[1]		–1		1	LSB
	Zero-code error[4]	Code 0d into DAC, external reference, V_{DD} = 5.5 V		6	12	mV
		Code 0d into DAC, internal V_{REF}, gain = 4x, V_{DD} = 5.5 V		6	15	
	Zero-code error temperature coefficient[4]			±10		µV/°C
	Offset error[4]	1.8 V ≤ V_{DD} < 2.7 V, V_{FB} pin shorted to V_{OUT}	–0.75	0.3	0.75	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, V_{FB} pin shorted to V_{OUT}	–0.5	0.25	0.5	
	Offset-error temperature coefficient[4]			±0.0003		%FSR/°C
	Gain error[4]		–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient[4]			±0.0008		%FSR/°C
	Full scale error[4]	1.8 V ≤ V_{DD} < 2.7 V, program full code into DAC	-1		1	%FSR
		2.7 V ≤ V_{DD} ≤ 5.5 V, program full code into DAC	–0.5		0.5	
	Full-scale-error temperature coefficient[4]			±0.0008		%FSR/°C
OUTPUT CHARACTERISTICS						
	Output voltage	Reference tied to V_{DD}	0		V_{DD}	V
C_L	Capacitive load[2]	R_L = Infinite, phase margin = 30°			200	pF
		R_L = 5 kΩ, phase margin = 30°			1000	
	Short-circuit current	V_{DD} = 1.8 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		15		mA
		V_{DD} = 2.7 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		50		
		V_{DD} = 5.5 V, full-scale output shorted to A_{GND} or zero-scale output shorted to V_{DD}		60		
	Output-voltage headroom[2]	To V_{DD} (DAC output unloaded, internal reference = 1.21 V), V_{DD} ≥ 1.21 × gain + 0.2 V	0.2			V
		To V_{DD} (DAC output unloaded, reference tied to V_{DD})	0.8			%FSR
		To V_{DD} (I_{LOAD} = 10 mA at V_{DD} = 5.5 V, I_{LOAD} = 3 mA at V_{DD} = 2.7 V, I_{LOAD} = 1 mA at V_{DD} = 1.8 V), DAC code = full scale	10			
Z_O	V_{FB} dc output impedance[3]	DAC output enabled, DAC reference tied to VDD (gain = 1x) or internal reference (gain = 1.5x or 2x)	400	500	600	kΩ
		DAC output enabled, internal V_{REF}, gain = 3x or 4x	325	400	485	
	Power supply rejection ratio (dc)	Internal V_{REF}, gain = 2x, DAC at midscale; V_{DD} = 5 V ±10%		0.25		mV/V

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6.5 Electrical Characteristics - Voltage Output (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		20		µs
		1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V, internal V_{REF}, gain = 4x		25		
	Slew rate	V_{DD} = 5.5 V		0.3		V/µs
	Power on glitch magnitude	At startup (DAC output disabled), R_L = 5 kΩ, C_L = 200 pF		75		mV
		At startup (DAC output disabled), R_L = 100 kΩ		200		
	Output enable glitch magnitude	DAC output disabled to enabled (DAC registers at zero scale, R_L = 100 kΩ		250		mV
V_n	Output noise voltage (peak to peak)	0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		50		$µV_{PP}$
		Internal V_{REF}, gain = 4x, 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		90		
	Output noise density	Measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.35		µV/√Hz
		Internal $V_{REF,}$ gain = 4x, measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.9		
	Power supply rejection ratio (ac)[3]	Internal V_{REF}, gain = 4x, 200-mV 50 Hz or 60 Hz sine wave superimposed on power supply voltage, DAC at midscale		-68		dB
	Code change glitch impulse	±1 LSB change around mid code (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1 LSB change around mid code (including feedthrough)		15		mV
POWER						
I_{DD}	Current flowing into VDD[4]	Normal operation, DACs at full scale, digital pins static		35	50	µA/ch

(1) Measured with DAC output unloaded. For external reference and internal reference V_{DD} ≥ 1.21 x gain + 0.2 V, between end-point codes: 32d to 4032d for 12-bit resolution, 8d to 1016d for 10-bit resolution, 2d to 254d for 8-bit resolution.
(2) Specified by design and characterization, not production tested.
(3) Specified with 200-mV headroom with respect to reference value when internal reference is used.
(4) Measured with DAC output unloaded.

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6.6 Electrical Characteristics - Current Output

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, ±250µA output range, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	All variants	8			Bits
INL	Relative accuracy[1]		–1		1	LSB
DNL	Differential nonlinearity[1]		–1		1	LSB
	Offset error	DAC output ranges: ±25µA, ±50µA, ±125µA, and ±250µA. Measured at mid-scale		±1		%FSR
	Gain error[4]	DAC output ranges: ±25µA, ±50µA, ±125µA, and ±250µA		±1.3		%FSR
OUTPUT CHARACTERISTICS						
	Output compliance voltage[1]	DAC output range: 0µA-25µA, To V_{DD}	200			mV
	Output compliance voltage[1]	DAC output ranges: 0µA-50µA, 0µA-125µA, and 0µA-250µA, To V_{DD}	400			mV
	Output compliance voltage[1]	DAC output ranges: -24µA-0µA, -48µA-0µA, -120µA-0µA, and -200µA-0µA, To V_{DD}	400			mv
	Output compliance voltage[1]	DAC output ranges: ±25µA, ±50µA, ±125µA, and ±250µA, To V_{DD} and to AGND	400			mV
Z_O	I_{OUT} dc output impedance[2]	DAC code = midscale, DAC output kept at V_{DD}/2	100			MΩ
	Power supply rejection ratio (dc)	DAC at midscale, Gain setting: 0µA-25µA, V_{DD} changed from 4.5V to 5.5V		0.28		LSB/V
DYNAMIC PERFORMANCE						
t_{sett}	Output current settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 1 LSB at 8-bit resolution, V_{DD} = 5.5 V, common-mode voltage at OUTx pin is V_{DD}/2		100		µs
V_n	Output noise current (peak to peak)	0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V, ±250µA output range		150		nA_{PP}
	Output noise density	Measured at 1 kHz, DAC at midscale, V_{DD} = 5.5 V, ±250µA output range		1		nA/√Hz
	Power supply rejection ratio (ac)[3]	Measured at ±250µA output range, 200-mV 50 Hz or 60 Hz sine wave superimposed on power supply voltage, DAC at midscale		TBD		LSB/V
POWER						
	Load capacitor - CAP pin[2]		0.5		15	µF
I_{DD}	Current flowing into VDD[3]	Normal operation, DACs at mid scale, 0µA - 25µA output range, digital pins static		18	24	µA/ch
		Normal operation, DACs at mid scale, 0µA - 50µA output range, digital pins static		18	24	
		Normal operation, DACs at mid scale, 0µA - 125µA output range, digital pins static		18	24	
		Normal operation, DACs at mid scale, 0µA - 250µA output range, digital pins static		18	24	
		Normal operation, DACs at mid scale, -24µA - 0µA output range, digital pins static		18	24	
		Normal operation, DACs at mid scale, -48µA - 0µA output range, digital pins static		18	24	
		Normal operation, DACs at mid scale, -120µA - 0µA output range, digital pins static		18	24	
		Normal operation, DACs at mid scale, -240µA - 0µA output range, digital pins static		18	24	

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6.6 Electrical Characteristics - Current Output (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, ±250µA output range, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Current flowing into VDD(3)	Normal operation, DACs at full scale, ±25µA output range, digital pins static		42	50	µA/ch
		Normal operation, DACs at full scale, ±50µA output range, digital pins static		56	70	
		Normal operation, DACs at full scale, ±125µA output range, digital pins static		98	120	
		Normal operation, DACs at full scale, ±250µA output range, digital pins static		167	200	

(1) Measured between end-point codes 0d to 255d.
(2) Specified by design and characterization, not production tested.
(3) The current flowing into VDD doesn't account for the load current sourced or sinked on the OUTx pins. The VREF pin is connected to VDD.
(4) Measured between DAC codes 10d and 255d.

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6.7 Electrical Characteristics - Comparator Mode

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x in voltage output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Offset error[(1)]	1.8 V ≤ V_{DD} ≤ 5.5 V	–5	TBD	5	mV
	Offset error time drift	Measured at VDD = 5.5 V, external reference, 125°C, FB in Hi-Z mode, DAC at full-scale and VFB at 0 V or DAC at zero-scale and VFB at 1.84 V. Drift specified for 10 years of continuous operation		4		mV
OUTPUT CHARACTERISTICS						
	Input signal range	V_{REF} connected to V_{DD}, V_{FB} resistor network connected to ground	0		V_{DD}	V
		V_{REF} connected to V_{DD}, V_{FB} resistor network disconnected from ground	0		V_{DD} (1/3 - 1/100)	
V_{OL}	Logic low output voltage	I_{LOAD} = 100 µA		0.1		V
DYNAMIC PERFORMANCE						
$t_{resp-comp}$	Output response time	Measured with: DAC at mid-scale, FB input at Hi-Z, and transition step at FB node is (V_{DAC} – 2LSB) to (V_{DAC} + 2LSB). Transition time measured between 10% and 90% of output. Output current of 100 µA. Comparator output configured in push-pull mode. Load capacitor at DAC output is 25 pF.		15		µs

(1) Measured at DAC at mid-scale, comparator input at Hi-Z, and DAC operating with external reference.

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6.8 Electrical Characteristics - General

all minimum/maximum specifications at T_A = –40°C to +125°C and typical specifications at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, DAC reference tied to VDD, gain = 1x in voltage output mode or ±250µA output range in current output mode, DAC output pin (OUT) loaded with resistive load (R_L = 5 kΩ to AGND) in voltage-output mode and capacitive load (C_L = 200 pF to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	T_A = 25°C		1.212		V
	Reference output temperature coefficient[(1)]				50	ppm/°C
EXTERNAL REFERENCE						
	External reference input range		1.7		V_{DD}	V
EEPROM						
	Endurance	–40°C ≤ T_A ≤ 85°C		20000		Cycles
		125°C		1000		
	Data retention[(1)]	T_A = 25°C		50		Years
	EEPROM programming write cycle time[(1)]				200	ms
DIGITAL INPUTS						
	Digital feedthrough	Voltage output mode, DAC output static at midscale, fast+ mode, SCL toggling		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER-DOWN MODE						
I_{DD}	Current flowing into VDD	DAC in sleep mode, internal reference powered down			17	µA
I_{DD}	Current flowing into VDD	DAC in deep-sleep mode, internal reference powered down			3	µA
HIGH-IMPEDANCE OUTPUT						
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	DAC in Hi-Z output mode, 1.7V ≤ V_{DD} ≤ 5.5V		10		nA
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	V_{DD} = 0 V, V_{OUT} ≤ 1.5V, Decoupling capacitor between V_{DD} and AGND: 0.1µF		200		nA
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	V_{DD} = 0 V, 1.5V < V_{OUT} ≤ 5.5V, Decoupling capacitor between V_{DD} and AGND: 0.1µF		500		nA
I_{LEAK}	Current flowing into V_{OUTX} and V_{FBX}	100K between V_{DD} and AGND, V_{OUT} ≤ 1.25V, series resistance of 10KΩ at OUT pin		2		µA

(1) Specified by design and characterization, not production tested.

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6.9 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns

6.10 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns

6.11 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, –40°C ≤ T_A ≤ +125°C, and 1.8 V ≤ $V_{pull-up}$ ≤ V_{DD} V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

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6.12 Timing Requirements: SPI Write Operation

all input signals are timed from VIL to 70% of V_{DD}, V_{DD} = 1.8 V to 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency, 1.7 V ≤ V_{DD} ≤ 5.5 V			25	MHz
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ V_{DD} ≤ 5.5 V	18			ns
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ V_{DD} ≤ 5.5 V	18			ns
t_{SDIS}	SDI setup time, 1.7 V ≤ V_{DD} ≤ 5.5 V	8			ns
t_{SDIH}	SDI hold time, 1.7 V ≤ V_{DD} ≤ 5.5 V	8			ns
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time, 1.7 V ≤ V_{DD} ≤ 5.5 V	18			ns
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge, 1.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
t_{CSHIGH}	$\overline{CS}$ hight time, 1.7 V ≤ V_{DD} ≤ 5.5 V	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time for same channel, 1.7 V ≤ V_{DD} ≤ 5.5 V	2			µs
$t_{BCASTWAIT}$	Broadcast DAC update wait time, 1.7 V ≤ V_{DD} ≤ 5.5 V	2			µs

6.13 Timing Requirements: SPI Read and Daisy Chain Operation

all input signals are timed from VIL to 70% of V_{DD}, V_{DD} = 1.8 V to 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency, 1.7 V ≤ V_{DD} ≤ 5.5 V			1	MHz
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ V_{DD} ≤ 5.5 V	400			ns
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ V_{DD} ≤ 5.5 V	400			ns
t_{SDIS}	SDI setup time, 1.7 V ≤ V_{DD} ≤ 5.5 V	8			ns
t_{SDIH}	SDI hold time, 1.7 V ≤ V_{DD} ≤ 5.5 V	8			ns
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time, 1.7 V ≤ V_{DD} ≤ 5.5 V	400			ns
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge, 1.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
t_{CSHIGH}	$\overline{CS}$ hight time, 1.7 V ≤ V_{DD} ≤ 5.5 V	1			µs

6.14 Timing Requirements: GPIO

all input signals are timed from VIL to 70% of V_{DD}, V_{DD} = 1.8 V to 5.5 V, and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$t_{GPIHIGH}$	GPI high time, 1.7 V ≤ V_{DD} ≤ 5.5 V(1)	2			µs
t_{GPILOW}	GPI low time, 1.7 V ≤ V_{DD} ≤ 5.5 V(1)	2			µs
t_{GPAWGD}	$\overline{LDAC}$ falling edge to DAC update delay, 1.7 V ≤ V_{DD} ≤ 5.5 V(2)			2	µs
$t_{CS2LDAC}$	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ V_{DD} ≤ 5.5 V	1			µs
$t_{STP2LDAC}$	I^2C STOP bit rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ V_{DD} ≤ 5.5 V	1			µs
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ V_{DD} ≤ 5.5 V	2			µs

(1) The SCL, SDA, A0, and A1 pins can be configured as GPIOs that can be configured to perform different channel-specific or independent operations.

(2) The GPIOs can be configured as channel-specific or global $\overline{LDAC}$ function. In a channel-specific $\overline{LDAC}$ mode, the $\overline{LDAC}$ pins can be used to trigger DAC code patterns stored in the NVM.

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6.15 Timing Diagrams

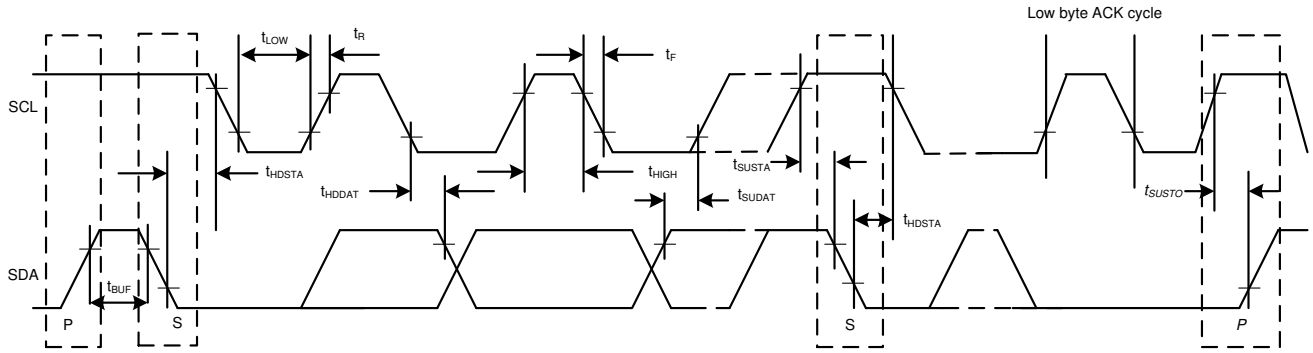

Figure 6-1. I²C Timing Diagram

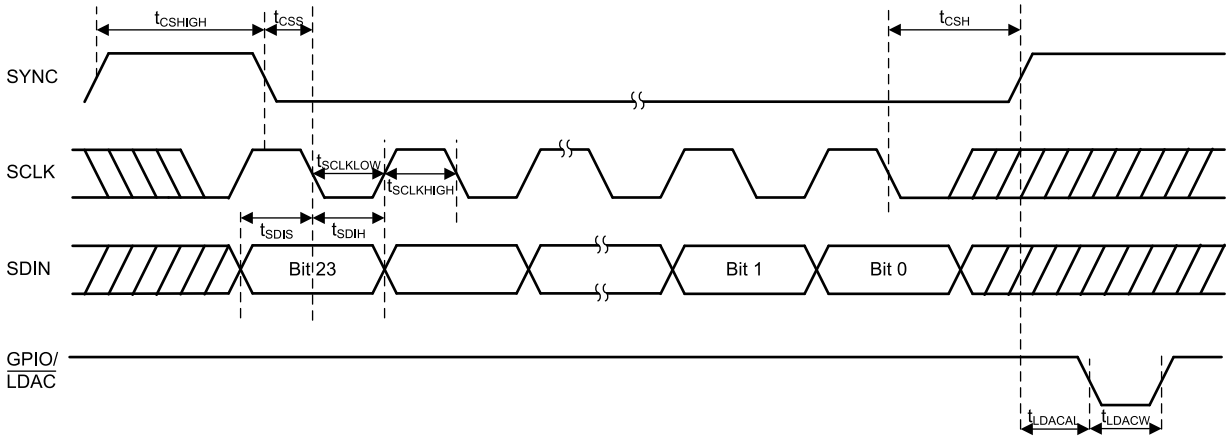

Figure 6-2. SPI Write Timing Diagram

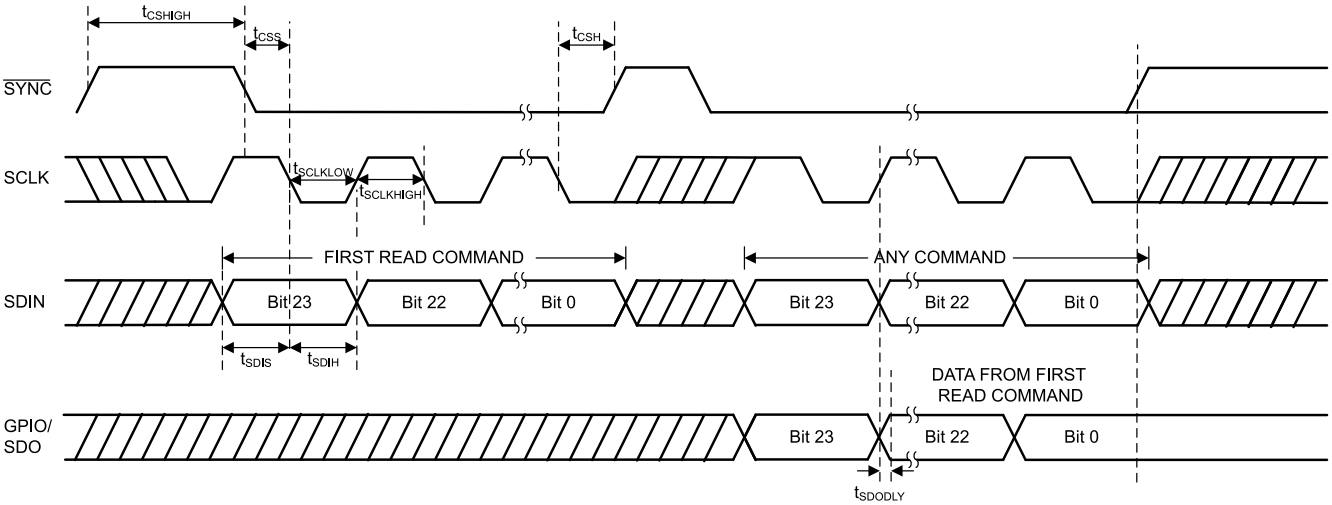

Figure 6-3. SPI Read Timing Diagram

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7 Detailed Description

7.1 Overview

The 12-bit DAC63004 and10-bit DAC53004 (DACx3004) are a pin-compatible family of ultra-low-power, quad-channel, buffered voltage-output and current-output, smart digital-to-analog converters (DACs). The DAC channels are independently configurable as voltage output or current output. The DAC outputs change to Hi-Z when VDD is off; a feature useful in voltage-margining applications. These smart DACs contain nonvolatile memory (NVM), an internal reference, automatically detectable I^2C and SPI interface, PMBus-compatibility in I^2C mode, force-sense output, and a general-purpose input. These devices support Hi-Z power-down modes by default, which can be configured to 10 kΩ-GND or 100 kΩ-GND using the NVM. The DACx3004 have a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The DACx3004 operate with either an internal reference, external reference, or with power supply as the reference and provide a full-scale output of 1.8 V to 5.5 V.

The DACx3004 devices support I^2C standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The I^2C interface can be configured with four slave addresses using the A0 pin. These devices also support specific PMBus commands such as *turn on/off*, *margin high or low*, and more. The SPI mode supports a 3-wire interface by default with up to 25-MHz SCLK input. The GPIO input can be configured as SDO in the NVM for SPI read capability. The GPIO input can alternatively be configurable as $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, $\overline{\text{FAULT-DUMP}}$, $\overline{\text{RESET}}$,and $\overline{\text{PROTECT}}$ functions. This device supports a deep-sleep mode in addition to the sleep (power-down) mode. The deep-sleep mode uses the GPIO pin for power-down and wake up, in which the device draws a very low quiescent current of 3 µA. Together with the ultra-low-power operation, the DACx3004 is designed for battery-operated applications like land mobile radio, medical pulse oximeter, and notebook PCs.

The DACx3004 also include digital slew rate control, and support standard waveform generation such as *sine and cosine*, *triangular*, and *sawtooth* waveforms. These devices can generate pulse-width modulation (PWM) output with the combination of the triangular or sawtooth waveform and the FB pin. The force-sense outputs of the DAC channels can be used as programmable comparators. The comparator mode allows programmable hysteresis, latching comparator, window comparator, and fault-dump to the NVM. These features enable the DACx3004 to go beyond the limitations of a conventional DAC that depends on a processor to function. As a result of processor-less operation and the *smart* feature set, the DACx3004 are called smart DACs.

7.2 Functional Block Diagram

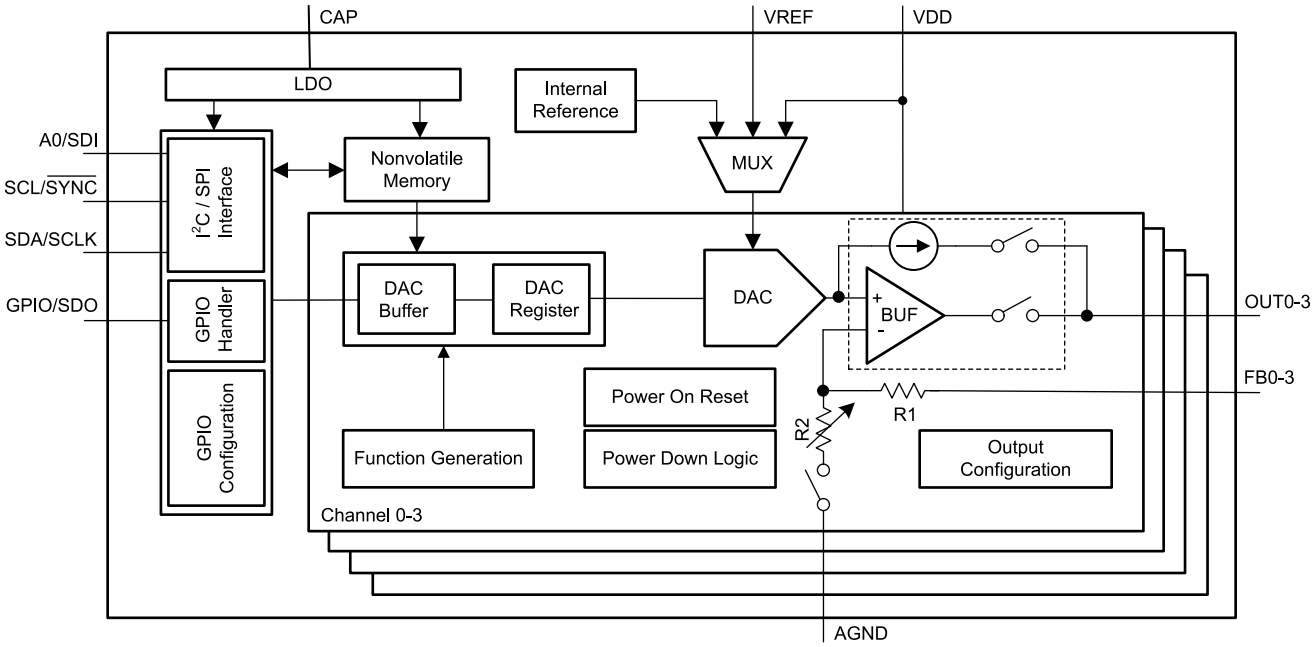

Figure 7-1. Functional Block Diagram

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7.3 Feature Description

7.3.1 Smart Digital-to-Analog Converter (DAC) Architecture

The DACx3004 devices consist of string architecture with a voltage-output amplifier and an external FB pin and voltage-to-current converter for each channel. Section 7.2 shows the DAC architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply. The DAC has an internal voltage reference of 1.21 V. There is an option to select an external reference on the VREF pin or the power supply as a reference. The voltage output mode uses one of these three reference options. The current output mode uses an internal band gap to generate the current outputs. Both the voltage- and current-output modes support multiple programmable output ranges.

The DACx3004 devices support Hi-Z output when VDD is off, maintaining very low leakage current at the output pins with up to 1.25 V of forced voltage. The DAC output pin also starts up in high-impedance mode by default, making these devices an excellent choice for voltage margining and scaling applications. To change the power-up mode to 10 kΩ-GND or 100 kΩ-GND, program the corresponding VOUT-PDN-X field in the COMMON-CONFIG register and load these bits in the device NVM.

The DACx3004 devices support an independent comparator mode for each channel. The respective FBx pins act as the inputs for the comparator. The DAC architecture supports inversion of the comparator output using register settings. The comparator outputs can be push-pull or open-drain. The comparator mode supports programmable hysteresis using *margin-high* and *margin-low* register fields, latching comparator, and window comparator. The comparator outputs are accessible internally by the device.

The DACx3004 devices include a *smart* feature set to enable processor-less operation and high-integration. The NVM enables a predictable start-up. The GPIO triggers the DAC output without the I^2C interface in the absence of a processor or when the processor or software fails. The integrated functions and the FBx pin enable PWM output for control applications. The FBx pin enables this device to be used as a programmable comparator. The digital slew-rate control and the Hi-Z power-down modes enable a hassle-free voltage margining and scaling function.

7.3.2 Digital Input/Output

The DACx3004 have four digital IO pins that include I^2C, SPI, PMBus, and GPIO interfaces. These devices automatically detect I^2C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I^2C interface uses the A0 pin to select from among four address options. The SPI interface is a 3-wire interface by default. No readback capability is available in this mode. The GPIO pin can be configured in the register map and then programmed in to the NVM as the SDO pin. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I^2C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, SDO/GPIO

The GPIO can be configured as multiple functions other than SDO. These are $\overline{\text{LDAC}}$, $\overline{\text{PD}}$, $\overline{\text{STATUS}}$, $\overline{\text{PROTECT}}$, $\overline{\text{FAULT-DUMP}}$, and $\overline{\text{RESET}}$. All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired IO voltage using external registers.

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7.3.3 Nonvolatile Memory (NVM)

The DACx3004 contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in the highlighted gray cells in Table 7-15, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. This is an autoresetting bit. The NVM-BUSY bit in the GENERAL-STATUS register is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all read/write operations to the device. The NVM-BUSY bit is set to 0 after the write or reload operation is complete; at this point, all read/write operations to the device are allowed. The default value for all the registers in the DACx3004 is loaded from NVM as soon as a POR event is issued.

The DACx3004 also implement NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. After completion, the device autoresets this bit to 0. During the NVM-RELOAD operation, the NVM-BUSY bit is set to 1.

7.3.4 Power Consumption

The power consumption of the DACx3004 in sleep mode is 17 µA and in deep-sleep mode 3 µA. In normal operation, the total power consumption of the device depends on the number of channels powered on and the output mode of each channel (voltage or current). In current-output mode, the quiescent current depends on the output range as well. The quiescent current calculation excludes the load current. For example, in the ±250 µA output mode with a DAC setting of +125 µA, the total current drawn through the VDD pin is the total quiescent current plus 125 µA. The total quiescent current in normal operation can be calculated using Equation 1.

$$P_{NORMAL_MODE} = (V_{DD} \times I_{DD_SLEEP}) + \sum_{x=0}^{3} (V_{DD} \times I_{DD_X}) \quad (1)$$

where:

- I_{DD_SLEEP} is the quiescent current in sleep mode (when all the channels are powered down).
- I_{DD_X} is the quiescent current for channel-*X* for every channel that is powered on.

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7.4 Device Functional Modes

7.4.1 Voltage-Output Mode

The voltage-output mode for each DAC channel can be entered by selecting the power-up option in the VOUT-PDN-X fields in the COMMON-CONFIG register and simultaneously powering-down the current output option for the respective channels using the IOUT-PDN-X bits in the same register. Short the OUTx and FBx pins of respective channels externally for closed-loop amplifier output. An open FBx pin saturates the amplifier output. To achive the desired voltage output, select the right reference option, select the amplifier gain for the required output range, and program the DAC code in the DAC-X-DATA register of the respective channels.

7.4.1.1 Voltage Reference and DAC Transfer Function

There are three voltage reference options possible with the DACx3004 devices: internal reference, external reference, and the power supply as reference, as shown in Figure 7-2. The DAC transfer function in the voltage-output and comparator modes changes based on the voltage reference selection.

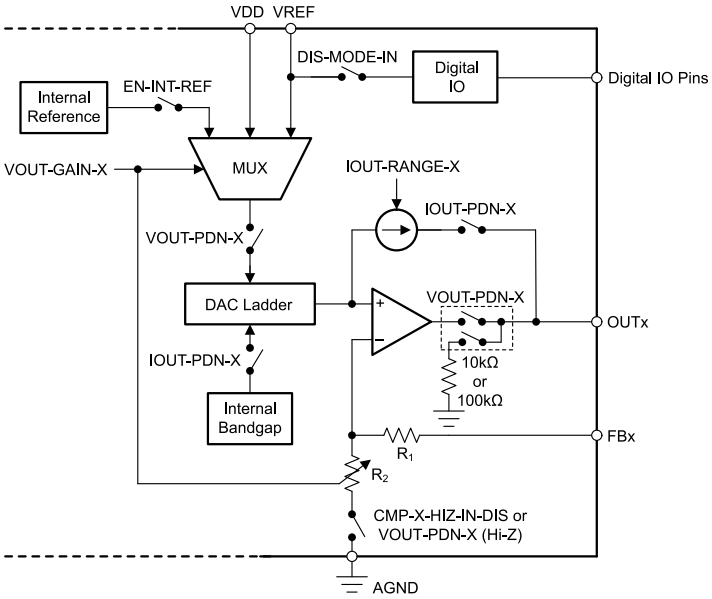

Figure 7-2. Voltage Reference Selection and Power-Down Logic

7.4.1.1.1 Internal Reference

The DACx3004 contain an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register to achieve gains of 1.5x, 2x, 3x, or 4x for the DAC output voltage (V_{OUT}). Equation 2 shows DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC_DATA}{2^N} \times V_{REF} \times GAIN \tag{2}$$

where:

- N is the resolution in bits, 10 (DAC53004), or 12 (DAC63004).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to 2^N – 1.
- V_{REF} is the internal reference voltage = 1.21 V.
- GAIN = 1.5x, 2x, 3x, or 4x, based on VOUT-X-GAIN bits.

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7.4.1.1.2 External Reference

The DACx3004 provide an external reference input. Select the external reference option by configuring the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register appropriately. Write 1 to the DIS-MODE-IN bit in the DEVICE-MODE-CONFIG register to minimize quiescent current. The external reference can be between 1.8 V and VDD. Equation 3 shows DAC transfer function when the external reference is used.

Note

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC_DATA}{2^N} \times V_{REF} \tag{3}$$

where:

- N is the resolution in bits, 10 (DAC53004), or 12 (DAC63004).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to $2^N – 1$.
- V_{REF} is the external reference voltage.

7.4.1.1.3 Power-Supply as Reference

By default, the DACx3004 operate with the power-supply pin (VDD) as a reference. Equation 4 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1x.

$$V_{OUT} = \frac{DAC_DATA}{2^N} \times V_{DD} \tag{4}$$

where:

- N is the resolution in bits, either 10 (DAC53004), or 12 (DAC63004).
- DAC_DATA is the decimal equivalent of the binary code that is loaded to the DAC-X-DATA field in the DAC-X-DATA register.
- DAC_DATA ranges from 0 to $2^N – 1$.
- V_{DD} is used as the DAC reference voltage.

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7.4.2 Current-Output Mode

The current-output mode for each DAC channel can be entered by disabling respective IOUT-PDN-X bits in the COMMON-CONFIG register and putting the respective VOUT-PDN-X fields in the same register in Hi-Z power-down. Select the desired current-output range by writing to the IOUT-RANGE-X field in the DAC-X-IOUT-MISC-CONFIG register. To minimize leakage in current-output mode, disconnect the FBx pin. The internal trimming settings for voltage-output and current-output modes are different; therefore, there can be a momentary dc offset when switching between voltage-output to current-output modes. Program the mode selection into the NVM to avoid this offset. The transfer function of the current-output is shown in Equation 5.

$$I_{OUT} = \frac{DAC_DATA \times (I_{MAX} - I_{MIN})}{2^8} + I_{MIN} \tag{5}$$

where:

- DAC_DATA is the DAC-X-DATA code as specified in Section 7.6.8.
- I_{MAX} is the signed maximum current in the IOUT-RANGE-X setting as specified in Section 7.6.5.
- I_{MIN} is the signed minimum current in the IOUT-RANGE-X setting as specified in Section 7.6.5.

7.4.3 Comparator Mode

All the DAC channels can be configured as programmable comparators. To enter the comparator mode for a channel, write 1 to the CMP-X-EN and the CMP-X-OUT-EN bits in the respective DAC-X-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-X-OD-EN bit. To invert the comparator output, write 1 to the CMP-X-INV-EN bit. The FBx pin has a finite impedance. To enable high-impedance on the FBx pin, write 1 to the CMP-X-HIZ-IN-DIS bit.

Note

In the Hi-Z input mode, the comparator input range is limited to:

- For GAIN = 1x, 1.5x, or 2x: $V_{FB} \leq (V_{REF} \times GAIN) / 3$
- For GAIN = 3x, or 4x: $V_{FB} \leq (V_{REF} \times GAIN) / 6$

Any higher input voltage is clipped.

Individual comparator channels can be configured in no-hysteresis, with-hysteresis, and window-comparator modes using the CMP-X-MODE field in the respective DAC-X-CMP-MODE-CONFIG register.

7.4.4 Application-Specific Modes

This section provides the details of application-specific functional modes available in DACx3004.

7.4.4.1 Voltage Margining and Scaling

Voltage margining or scaling is a primary application for DACx3004. This section provides specific features available for this application such as Hi-Z output, slew-rate control, $\overline{PROTECT}$ input, and PMBus compatibility.

7.4.4.1.1 High-Impedance Output and $\overline{PROTECT}$ Input

All the DAC output channels remain in high-impedance (Hi-Z) when VDD is off. Figure 7-3 shows a simplified schematic of DACx3004 used in a voltage-margining application. The series resistor R_S is needed in voltage-output mode, but is optional in current-output mode. Almost all linear regulators and DC/DC converters have a feedback voltage of ≤ 1.25 V. The low-leakage currents at the outputs are maintained for V_{FB} of ≤ 1.25 V. Thus, for all practical purposes, the DAC outputs appear as Hi-Z when VDD of the DAC is off in voltage margining and scaling applications. This feature allows for seamless integration of the DACx3004 into a system without any need for additional power-supply sequencing for the DAC.

The DAC channels power down to Hi-Z at boot up. The outputs can power up with a preprogrammed code that corresponds to the nominal output of the DC/DC converter or the linear regulator. This feature allows for smooth power up and power down of the DAC without impacting the feedback loop of the DC/DC converter or the linear regulator.

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The GPIO pin of the DACx3004 can be configured as a $\overline{\text{PROTECT}}$ function. $\overline{\text{PROTECT}}$ takes the DAC outputs to a predictable state with a slewed or direct transition. This function is useful in systems where a fault condition (such as a brownout), a subsystem failure, or a software crash requires that the DAC outputs reach a predefined state without the involvement of a processor. The detected event can be fed to the GPIO pin configured as the $\overline{\text{PROTECT}}$ input. The $\overline{\text{PROTECT}}$ function is triggered using the PROTECT bit in the COMMON-TRIGGER register. Configure the behavior of the $\overline{\text{PROTECT}}$ function in the PROTECT-CONFIG field in the DEVICE-MODE-CONFIG register.

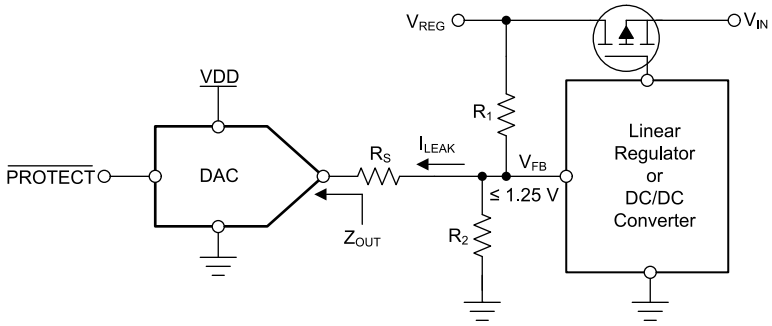

Figure 7-3. High-Impedance (Hi-Z) Output and $\overline{\text{PROTECT}}$ Input

7.4.4.1.2 Programmable Slew-Rate Control

When the DAC data registers are written, the voltage on DAC output (V_{OUT}) immediately transitions to the new code following the slew rate and settling time specified in the *Electrical Characteristics*. The slew rate control feature allows the user to control the rate at which the output voltage (V_{OUT}) changes. When this feature is enabled (using SLEW-RATE-X[3:0] bits), the DAC output changes from the current code to the code in DAC-X-MARGIN-HIGH or DAC-X-MARGIN-LOW registers (when margin high or low commands are issued to the DAC) using the step and rate set in CODE-STEP-X and SLEW-RATE-X bits in the DAC-X-FUNC-CONFIG register. With the default slew rate control setting of no-slew, the output changes smoothly at a rate limited by the output drive circuitry and the attached load. Using the slew-rate control feature, the output steps digitally at a rate defined by bits CODE-STEP-X and SLEW-RATE-X. SLEW-RATE-X defines the rate at which the digital slew updates; CODE-STEP-X defines the amount by which the output value changes at each update, for the corresponding channels. Table 7-1 and Table 7-2 show different settings available for CODE-STEP-X and SLEW-RATE-X.

When the slew rate control feature is used, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output as shown in Figure 7-4. Do not write to CODE-STEP-X, SLEW-RATE-X, or DAC-X-DATA during the output slew operation.

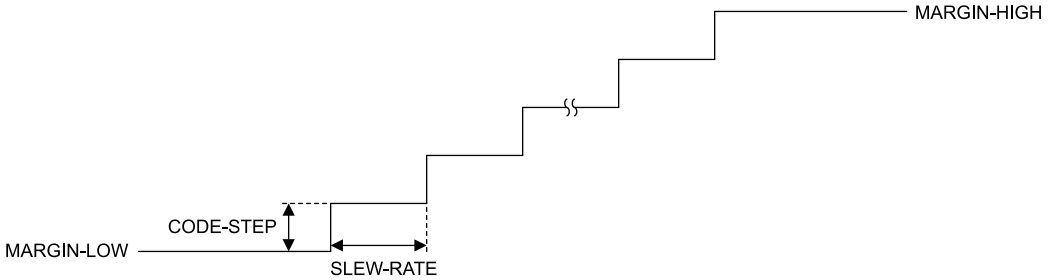

Figure 7-4. Programmable Slew-Rate Control

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Table 7-1. Code Step

REGISTER	CODE-STEP-X[2]	CODE-STEP-X[1]	CODE-STEP-X[0]	CODE STEP SIZE
DAC-X-FUNC-CONFIG	0	0	0	1 LSB (default)
	0	0	1	2 LSB
	0	1	0	3 LSB
	0	1	1	4 LSB
	1	0	0	6 LSB
	1	0	1	8 LSB
	1	1	0	16 LSB
	1	1	1	32 LSB

Table 7-2. Slew Rate

REGISTER	SLEW-RATE-X[3]	SLEW-RATE-X[2]	SLEW-RATE-X[1]	SLEW-RATE-X[0]	TIME PERIOD (PER STEP)
DAC-X-FUNC-CONFIG	0	0	0	0	No slew (default)
	0	0	0	1	4 µs
	0	0	1	0	8 µs
	0	0	1	1	12 µs
	0	1	0	0	18 µs
	0	1	0	1	27 µs
	0	1	1	0	40.5 µs
	0	1	1	1	60.75 µs
	1	0	0	0	91.13 µs
	1	0	0	1	136.69 µs
	1	0	1	0	239.2 µs
	1	0	1	1	418.61 µs
	1	1	0	0	732.56 µs
	1	1	0	1	1281.98 µs
	1	1	1	0	1281.98 µs
	1	1	1	1	5127.92 µs

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7.4.4.1.3 PMBus Compatibility Mode

The PMBus protocol is an I²C-based communication standard for power-supply management. PMBus contains standard command codes tailored to power supply applications. The DACx3004 implement some PMBus commands such as *Turn Off*, *Turn On*, *Margin Low*, *Margin High*, *Communication Failure Alert Bit (CML)*, as well as *PMBUS revision*. Figure 7-5 shows typical PMBus connections. The EN-PMBUS bit in the INTERFACE-CONFIG register must be set to 1 to enable the PMBus protocol.

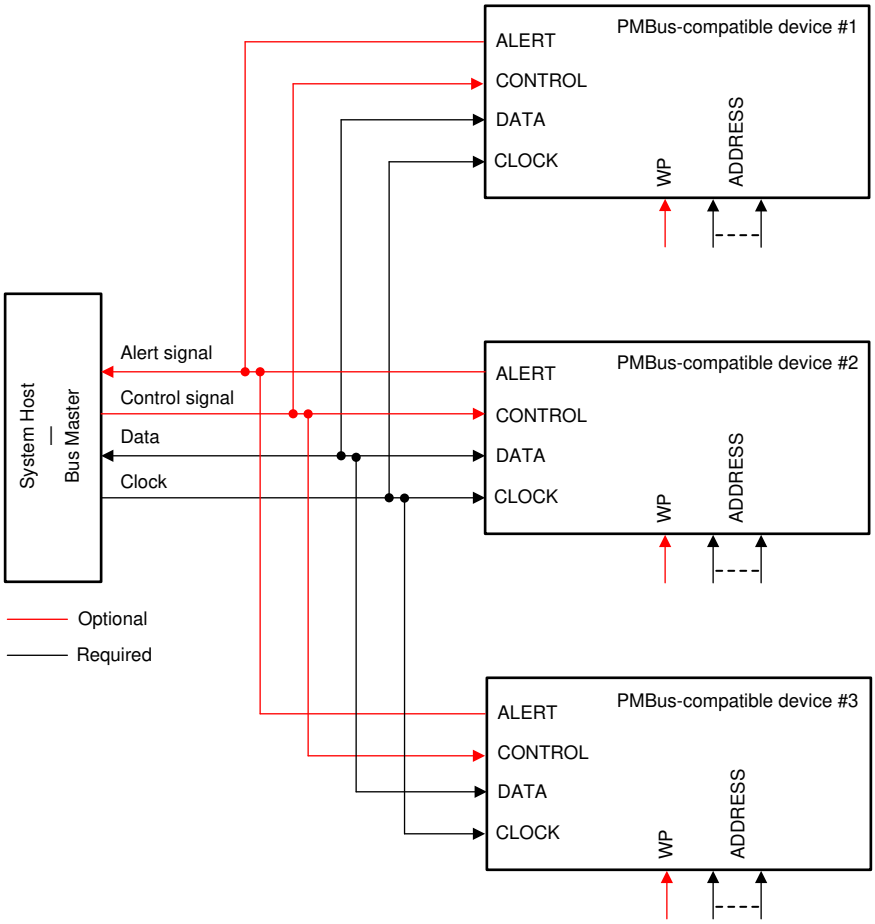

Figure 7-5. PMBus Connections

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Similar to I^{2}C, PMBus is a variable length packet of 8-bit data bytes, each with a receiver acknowledge, wrapped between a start and stop bit. The first byte is always a 7-bit *slave address* followed by a *write* bit, sometimes called the *even address* that identifies the intended receiver of the packet. The second byte is an 8-bit *command* byte, identifying the PMBus command being transmitted using the respective command code. After the command byte, the transmitter either sends data associated with the command to write to the receiver command register (from least significant byte to most significant byte, as shown in Table 7-3), or sends a new start bit indicating the desire to read the data associated with the command register from the receiver. Then the receiver transmits the data following the same least significant byte first format (see Table 7-4).

Table 7-3. PMBus Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 7.5.2.2.1				Command byte Section 7.5.2.2.2				Data byte - LSDB				Data byte - MSDB (Optional)			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

Table 7-4. PMBus Read Sequence

S	MSB	…	R/ $\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/ $\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE Section 7.5.2.2.1				COMMAND BYTE Section 7.5.2.2.2				Sr	ADDRESS BYTE Section 7.5.2.2.1				LSDB				MSDB (Optional)			
From Master				Slave	From Master			Slave	From Master				Slave	From Slave			Master	From Slave			Master

The DACx3004 I^{2}C interface implements some of the PMBus commands. Table 7-5 shows the supported PMBus commands that are implemented in DACx3004.The DAC uses DAC-X-MARGIN-LOW, DAC-X-MARGIN-HIGH bits, SLEW-RATE-X, and CODE-STEP-X bits for PMBUS-OPERATION-CMD-X. To access multiple channels, write to the PMBUS-PAGE register first followed by a write to the channel-specific register.

Table 7-5. PMBus Operation Commands

REGISTER	PMBUS-OPERATION-CMD-X[15:8]	DESCRIPTION
PMBUS-OP-CMD-X	00h	Turn off
	80h	Turn on
	94h	Margin low
	A4h	Margin high

The DACx3004 also implement PMBus features such as group command protocol and communication time-out failure. The CML bit in the PMBUS-CML register indicates a communication fault in the PMBus. This bit is reset by writing 1.

To get the PMBus version, read the PMBUS-VERSION register.

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7.4.4.2 Function Generation

The DACx3004 implement a continuous function or waveform generation feature. These devices can generate a triangular wave, sawtooth wave, and sine wave independently for every channel.

7.4.4.2.1 Triangular Waveform Generation

The triangular waveform uses the DAC-X-MARGIN-LOW and DAC-X-MARGIN-HIGH registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in Equation 6. An external RC load with a time-constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Writing 0b000 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects triangular waveform.

$$f_{TRIANGLE-WAVE} = \frac{1}{2 \times SLEW_RATE \times \left(\frac{MARGIN_HIGH - MARGIN_LOW + 1}{CODE_STEP}\right)} \tag{6}$$

where:

- SLEW_RATE is the SLEW-RATE-X setting as specified in Table 7-2.
- CODE_STEP is the CODE-STEP-X setting as specified in Table 7-1.
- MARGIN_HIGH is the DAC-X-MAGIN-HIGH as specified in Section 7.6.2.
- MARGIN_LOW is the DAC-X-MAGIN-LOW as specified in Section 7.6.3.

7.4.4.2.2 Sawtooth Waveform Generation

The sawtooth and the inverse sawtooth waveforms use the DAC-X-MARGIN-LOW and DAC-X-MARGIN-HIGH registers for minimum and maximum levels, respectively. The frequency of the waveform depends on the min and max levels, CODE-STEP and SLEW-RATE settings as shown in Equation 7. An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The CODE-STEP-X and SLEW-RATE-X settings are available in the DAC-X-FUNC-CONFIG register. Write 0b001 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register to select sawtooth waveform, and write 0b010 to select inverse sawtooth waveform.

$$f_{SAWTOOTH-WAVE} = \frac{1}{SLEW_RATE \times \left(\frac{MARGIN_HIGH - MARGIN_LOW + 1}{CODE_STEP}\right)} \tag{7}$$

where:

- SLEW_RATE is the SLEW-RATE-X setting as specified in Table 7-2.
- CODE_STEP is the CODE-STEP-X setting as specified in Table 7-1.
- MARGIN_HIGH is the DAC-X-MAGIN-HIGH as specified in Section 7.6.2.
- MARGIN_LOW is the DAC-X-MAGIN-LOW as specified in Section 7.6.3.

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7.4.4.2.3 Sine Waveform Generation

The sine wave function uses 24 preprogrammed points per cycle. The frequency of the sine wave depends on the SLEW-RATE settings as shown in Equation 8. An external RC load with a time constant larger than the slew-rate settings can be dominant over the internal frequency calculation. The SLEW-RATE-X setting is available in the DAC-X-FUNC-CONFIG register. Writing 0b100 to the FUNC-CONFIG-X bit field in the DAC-X-FUNC-CONFIG register selects sine wave. The minimum level for the sine wave is always zero-code and the maximum level is always full-code. Use the gain settings at the output amplifier for changing the full-scale output using the internal reference option. The gain settings are accessible through the VOUT-GAIN-X bits in the DAC-X-VOUT-CMP-CONFIG register. There are four phase settings available for the sine wave that are selected using the PHASE-SEL-X bit in the DAC-X-FUNC-CONFIG register.

$$f_{SINE} = \frac{1}{24 \times SLEW_RATE} \tag{8}$$

where:

- SLEW_RATE is the SLEW-RATE-X setting as specified in Table 7-2.

7.4.5 Device Reset and Fault Management

This section provides the details of power-on-reset (POR), software reset, and other diagnostics and fault-management features of DACx3004.

7.4.5.1 Power-on-Reset (POR)

The DACx3004 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the DACx3004 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in Figure 7-6, in order to make sure that the internal capacitors discharge and reset the device on power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

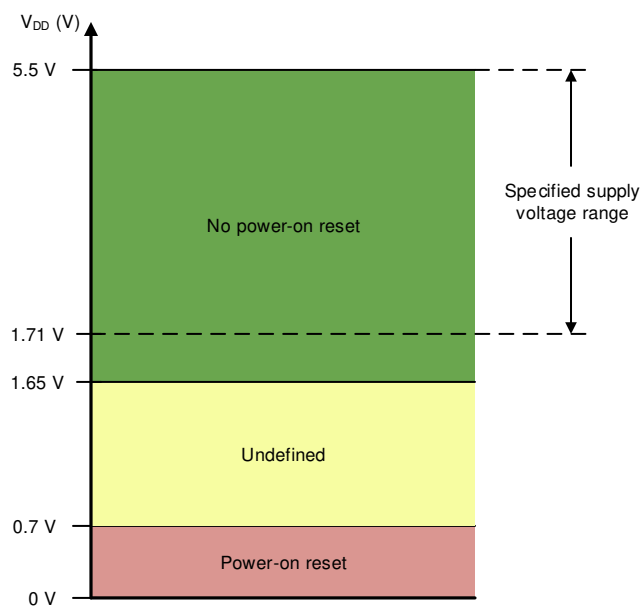

Figure 7-6. Threshold Levels for V_{DD} POR Circuit

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7.4.5.2 External Reset

An external reset to the device can be triggered through the GPIO pin or through the register map. To initiate a device software reset event, write the reserved code 1010 to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event. The GPIO pin can be configured as a $\overline{\text{RESET}}$ pin as shown in Table 7-13. This configuration must be programmed into the NVM so that the setting is not cleared after the device reset. The $\overline{\text{RESET}}$ input must be a low pulse. The device comes out of reset on the rising edge of the $\overline{\text{RESET}}$ input.

7.4.5.3 Register-Map Lock

The DACx3004 implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. To bypass the DEV-LOCK setting, write 0101 to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4.5.4 NVM Cyclic Redundancy Check (CRC)

The DACx3004 implement a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in DACx3004:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits The CRC feature is implemented by storing a 16-Bit CRC (CRC-16-CCITT) along with the NVM data each time NVM program operation (write or reload) is performed and during the device start up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot-up.

7.4.5.4.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see *Section 7.4.5.2*) command, or cycle power to the DAC. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

7.4.5.4.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the DAC are initialized with factory reset values, and any DAC registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see *Section 7.4.5.2*) command or cycle power to the DAC. A permanent failure in the NVM makes the device unusable.

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7.4.6 Power-Down Mode

The DACx3004 output amplifier and internal reference can be independently powered down through the EN-INT-REF, VOUT-PDN-X, and IOUT-PDN-X bits in the COMMON-CONFIG register, as shown in Figure 7-2. At power up, the DAC output and the internal reference are disabled by default. In power-down mode, the DAC outputs (OUTx pins) are in a high-impedance state. To change this state to 10 kΩ-A_{GND} or 100 kΩ-A_{GND} in the voltage-output mode (at power up), use the VOUT-PDN-X bits. The power-down state for current-output mode is always high-impedance.

The DAC power-up state can be programmed to any state (power-down or normal mode) using the NVM. Table 7-6 shows the DAC power-down bits. The individual channel power-down bits can be mapped to the GPIO pin using the GPIO-CONFIG register. This function is called the sleep mode. In this mode, the internal low-dropout regulator (LDO) and the common functional blocks are still powered-on, and the device draws a maximum of 17 µA of current through the power supply.

Table 7-6. DAC Power-Down Bits

REGISTER	VOUT-PDN-X[1]	VOUT-PDN-X[0]	IOUT-PDN-X	DESCRIPTION
COMMON-CONFIG	0	0	1	Power up VOUT-X
	0	1	1	Power down VOUT-X with 10 kΩ to AGND. Power down IOUT-X to Hi-Z
	1	0	1	Power down VOUT-X with 100 kΩ to AGND. Power down IOUT-X to Hi-Z
	1	1	1	Power down VOUT-X to Hi-Z. Power down IOUT-X to Hi-Z (default)
	1	1	0	Power down VOUT-X to Hi-Z. Power up IOUT-X

7.4.6.1 Deep-Sleep Mode

The DACx3004 provides a deep-sleep mode, where the internal LDO and most of the common functional blocks are powered-down. The GPIO pin must be used to enter and exit this mode. The I^2C or SPI interface does not work during the deep-sleep mode. The steps to enter and exit the deep-sleep mode are:

1. Make sure that the GPIO pin is pulled high.
2. Write 1 to the DEEP-SLEEP-EN bit in the GPIO-CONFIG register.
3. Disable GP output and SDO by writing 0 to GPO1-EN and SDO-EN bits.
4. Enable 1 to GPI1-EN and 0b0000 to GPI1-CONFIG bits.
5. To program these settings into the NVM, write 1 to the NVM-PROG bit in the COMMON-TRIGGER register.
6. A negative-edge trigger on the GPIO puts the device into the deep-sleep mode. The LDO takes approximately 550 µs to switch off. The device remains in this mode as long as the signal is low.
7. To bring the device out of the deep-sleep mode, pull the GPIO pin high. The digital circuitry and the LDO takes approximately 550 µs to switch on.

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7.5 Programming

The DACx3004 are programmed through either a 3-wire SPI or 2-wire I^2C interface. A 4-wire SPI mode is enabled by mapping the GPIO pin as SDO. The SPI readback operates at a lower SCLK than the standard SPI write operation. The type of interface is determined based on the first protocol to communicate after device power up. After the interface type is determined, the device ignores any change in the type while the device is on. The interface type can be changed after a power cycle.

7.5.1 SPI Programming Mode

An SPI access cycle for DACx3004 is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for DACx3004 is 24 bits long. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO extends the last bit transmitted.

Note

The SDO pin does not become Hi-Z when $\overline{\text{SYNC}}$ is high. Therefore, when sharing a single SPI bus across multiple receivers, disable the SDO pin of the DAC before reading from other receivers.

Table 7-7 describes the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

Table 7-7. SPI Write/Read Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/$\overline{\text{W}}$ = 0 sets a write operation. R/$\overline{\text{W}}$ = 1 sets a read operation
22 - 16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15 - 0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. The output data format is shown in Table 7-8. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

Table 7-8. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/$\overline{\text{W}}$	Echo R/$\overline{\text{W}}$ from previous access cycle
22 - 16	A[6:0]	Echo register address from previous access cycle
15 - 0	DI[15:0]	Readback data requested on previous access cycle

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7.5.2 I²C Programming Mode

The DACx3004 devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in Section 5. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *master*, and the devices that are controlled by the master are called *slaves*. The master device generates the SCL signal. The master device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the master. The master device on an I²C bus is typically a microcontroller or digital signal processor (DSP). The DACx3004 family operates as a slave device on the I²C bus. A slave device acknowledges master commands, and upon master control, receives or transmits data.

Typically, the DACx3004 family operates as a slave receiver. A master device writes to the DACx3004, a slave receiver. However, if a master device requires the DACx3004 internal register data, the DACx3004 operate as a slave transmitter. In this case, the master device reads from the DACx3004. According to I²C terminology, read and write refer to the master device.

The DACx3004 family is a slave and supports the following data transfer modes:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1.0 Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current would be 3 mA; similar to the case of standard and fast modes. The DACx3004 family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in Figure 7-7.

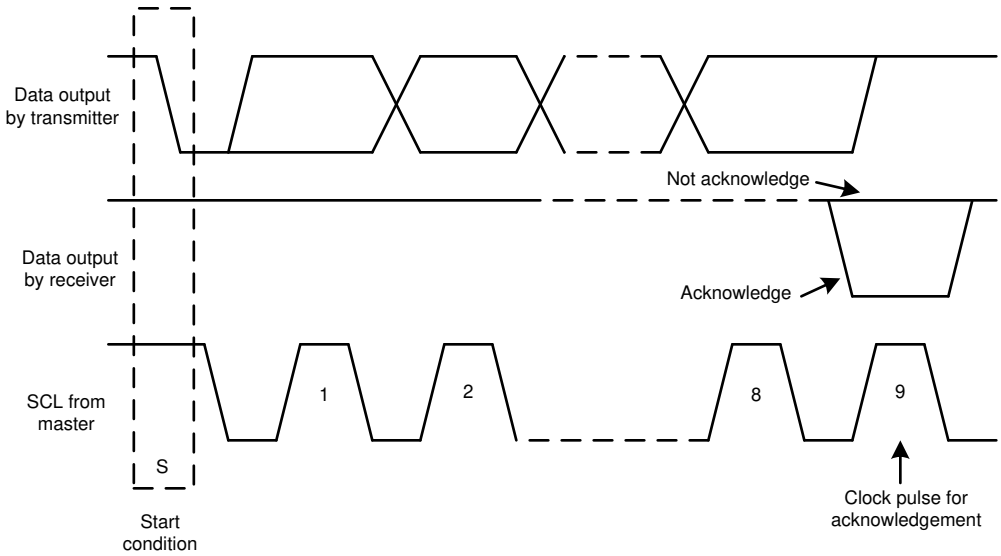

Figure 7-7. Acknowledge and Not Acknowledge on the I²C Bus

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7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-8. All I^2C-compatible devices recognize a start condition.
2. The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the master makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 7-9. All devices recognize the address sent by the master and compare the address to the respective internal fixed address. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in Figure 7-7. When the master detects this acknowledge, the communication link with a slave has been established.
3. The master generates further SCL cycles to transmit (R/$\overline{W}$ bit 0) or receive (R/$\overline{W}$ bit 1) data to the slave. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the master or by the slave, depending on which is the receiver. The 9-bit valid data sequences consists of 8-data bits and 1 acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in Figure 7-8. This action releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

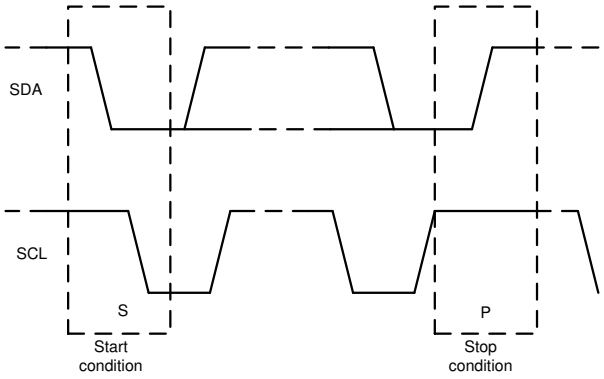

Figure 7-8. Start and Stop Conditions

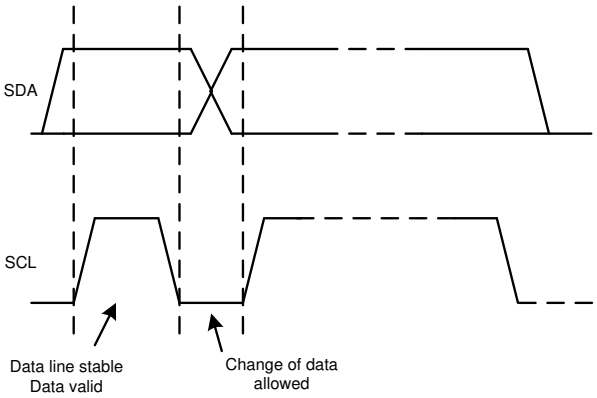

Figure 7-9. Bit Transfer on the I^2C Bus

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7.5.2.2 I²C Update Sequence

For a single update, the DACx3004 require a start condition, a valid I²C address byte, a command byte, and two data bytes, as listed in Table 7-9.

Table 7-9. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte Section 7.5.2.2.1				Command byte Section 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DACx3004 family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 7-10. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the DACx3004 devices.

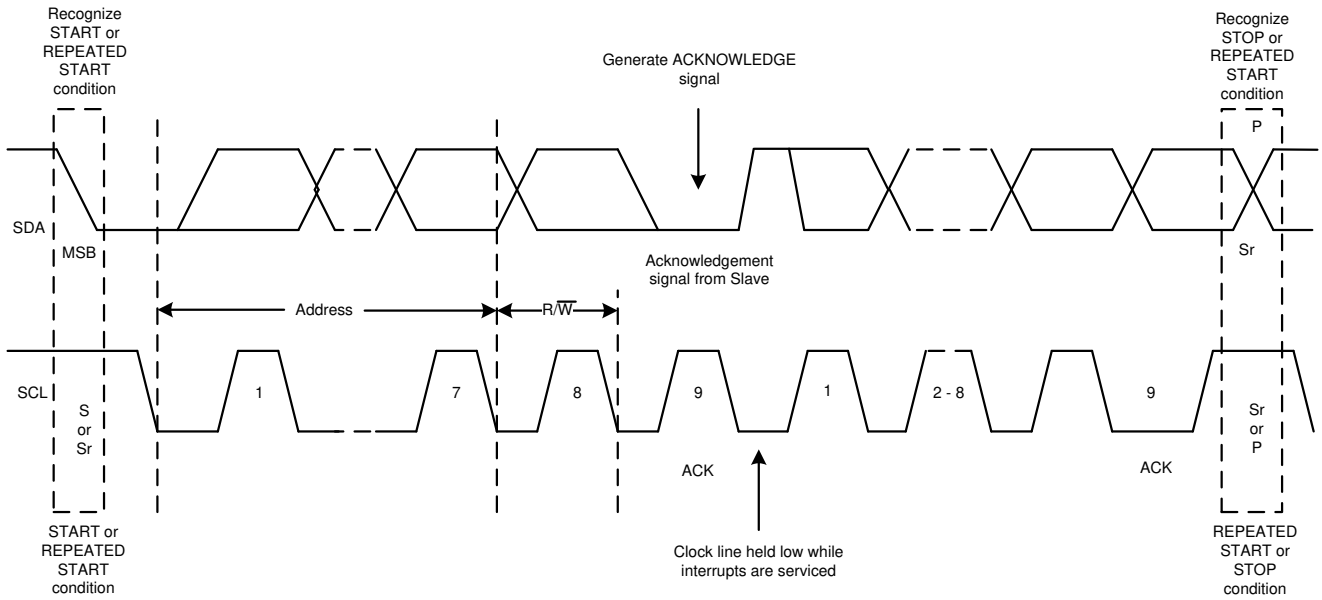

Figure 7-10. I²C Bus Protocol

The command byte sets the operating mode of the selected DACx3004 device. For a data update to occur when the operating mode is selected by this byte, the DACx3004 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DACx3004 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DACx3004 device releases the I²C bus and awaits a new start condition.

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7.5.2.2.1 Address Byte

The address byte, as shown in Table 7-10, is the first byte received from the master device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to Table 7-11.

Table 7-10. Address Byte

COMMENT	MSB							LSB
—	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/ $\overline{W}$
General address	1	0	0	1	See Table 7-11 (slave address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

The DACx3004 supports broadcast addressing, which is used for synchronously updating or powering down multiple DACx3004 devices. When the broadcast address is used, the DACx3004 responds regardless of the address pin state. Broadcast is supported only in write mode.

Table 7-11. Address Format

SLAVE ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

7.5.2.2.2 Command Byte

Table 7-16 lists the command byte in the ADDRESS column.

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7.5.2.3 I²C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a slave address and the R/ $\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the slave address and the R/ $\overline{W}$ bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The master must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

An alternative reading method allows for reading back the value of the last register written. The sequence is a start or repeated start with the slave address and the R/ $\overline{W}$ bit set to 1, and the two bytes of the last register are read out.

The broadcast address cannot be used for reading.

Table 7-12. Read Sequence

S	MSB	…	R/ $\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/ $\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE Section 7.5.2.2.1				COMMAND BYTE Section 7.5.2.2.2				Sr	ADDRESS BYTE Section 7.5.2.2.1				MSDB				LSDB			
From Master				Slave	From Master			Slave	From Master				Slave	From Slave			Master	From Slave			Master

7.5.3 General-Purpose Input/Output (GPIO) Modes

Together with I²C and SPI, the DACx3004 also support a GPIO that can be configured in the NVM for multiple functions. This pin allows for updating the DAC output channels and reading status bits without using the programming interface, thus enabling processor-less operation. In the GPIO-CONFIG register, write 1 to the GPI1-EN bit to set the GPIO pin as an input, or write 1 to the GPO1-EN bit to set the pin as output. There are global and channel-specific functions mapped to the GPIO pin. For channel-specific functions, select the channels using the GPI1-CH-SEL field in the GPIO-CONFIG register. Table 7-13 lists the functional options available for the GPIO as input and Table 7-14 lists the options for the GPIO as output. Some of the GP input operations are edge-triggered after the device boots up. After the power supply ramps up, the device registers the GPI level and executes the associated command. This feature allows the user to configure the initial output state at power-on. By default, the GPIO pin is not mapped to any operation. Pull the GPIO pin to high or low when not used. When the GPIO pin is mapped to a specific input function, the corresponding software bit functionality is disabled to avoid a race condition. When used as a $\overline{RESET}$ input, the GPIO pin must transmit an active-low pulse for triggering a device reset. All other constraints of the functions are applied to the GPIO-based trigger.

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Table 7-13. General-Purpose Input Function Map

REGISTER	BIT FIELD	VALUE	CHANNELS	GPIO EDGE / LEVEL	FUNCTION
GPIO-CONFIG	GPI1-CONFIG	0000	All	Falling-edge	Trigger $\overline{\text{DEEP-SLEEP}}$ mode.
				Rising-edge	Bring the device out of deep-sleep.
		0010	All	Falling-edge	Trigger $\overline{\text{FAULT-DUMP}}$
				Rising-edge	No effect
		0011	As per GPI1-CH-SEL	Low	IOUT power-down
				High	IOUT power-up
		0100	As per GPI1-CH-SEL	Low	VOUT power-down. Pulldown resistor as per the VOUT-PDN-X setting
				High	VOUT power-up
		0101	All	Falling-edge	Trigger $\overline{\text{PROTECT}}$ function
				Rising-edge	No effect
		0111	All	Falling-edge	Trigger $\overline{\text{CLR}}$ function
				Rising-edge	No effect
		1000	As per GPI1-CH-SEL. Both the SYNC-CONFIG-X and the GPI1-CH-SEL must be configured for every channel.	Falling-edge	Trigger $\overline{\text{LDAC}}$ function
				Rising-edge	No effect
		1001	As per GPI1-CH-SEL	Falling-edge	Stop function generation
				Rising-edge	Start function generation
		1010	As per GPI1-CH-SEL	Falling-edge	Trigger margin-low
				Rising-edge	Trigger margin-high
		1011	All	Low pulse	Trigger device $\overline{\text{RESET}}$. The $\overline{\text{RESET}}$ configuration must be programmed into the NVM
				Rising-edge	Brings the device out of reset
		1100	All	Low	NVM programming allowed
				High	NVM programming blocked
		1101	All	Low	Write to the register map allowed
				High	Write to the register map blocked except a write to the DEV-UNLOCK field
		Others	NA	NA	NA

Table 7-14. General-Purpose Output ($\overline{\text{STATUS}}$) Function Map

REGISTER	BIT FIELD	VALUE	FUNCTION
GPIO-CONFIG	GPO1-CONFIG	0001	NVM-BUSY
		0100	DAC-0-BUSY
		0101	DAC-1-BUSY
		0110	DAC-2-BUSY
		0111	DAC-3-BUSY
		1000	WIN-CMP-0
		1001	WIN-CMP-1
		1010	WIN-CMP-2
		1011	WIN-CMP-3
		Others	NA

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7.6 Register Map

Table 7-15. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-X-MARGIN-HIGH	DAC-X-MARGIN-HIGH												X			
DAC-X-MARGIN-LOW	DAC-X-MARGIN-LOW												X			
DAC-X-VOUT-CMP-CONFIG	X			VOUT-X-GAIN			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
DAC-X-IOUT-MISC-CONFIG	X			IOUT-X-RANGE				X								
DAC-X-CMP-MODE-CONFIG	X				CMP-X-MODE		X									
DAC-X-FUNC-CONFIG	CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK-X												
DAC-X-DATA	DAC-X-DATA												X			
COMMON-CONFIG	WIN-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-3		IOUT-PDN-3	VOUT-PDN-2		IOUT-PDN-2	VOUT-PDN-1		IOUT-PDN-1	VOUT-PDN-0		IOUT-PDN-0
COMMON-TRIGGER	DEV-UNLOCK				RESET				LDAC	CLR	X	BIT-FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD
COMMON-DAC-TRIG	RST-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RST-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	RST-CMP-FLAG-2	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	RST-CMP-FLAG-3	TRIG-MAR-LO-3	TRIG-MAR-HI-3	START-FUNC-3
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-BUSY-3	DAC-BUSY-2	DAC-BUSY-1	DAC-BUSY-0	NVM-BUSY	DEVICE-ID							
CMP-STATUS	X							PROTECT-FLAG	WIN-CMP-3	WIN-CMP-2	WIN-CMP-1	WIN-CMP-0	CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
GPIO-CONFIG	GF-EN	DEEP-SLEEP-EN	GPO1-EN	GPO1-CONFIG				GPI-CH-SEL				GPI1-CONFIG				GPI1-EN
DEVICE-MODE-CONFIG	RESERVED		DIS-MODE-IN	RESERVED			PROTECT-CONFIG		RESERVED			X				
INTERFACE-CONFIG	X			TIMEOUT-EN	X			EN-PMBUS	X					FAST-SDO-EN	X	SDO-EN
DAC-X-DATA-8BIT	DAC-X-DATA-8BIT								X							
BRDCAST-DATA	BRDCAST-DATA												X			
PMBUS-PAGE	PMBUS-PAGE								NA							
PMBUS-OP-CMD	PMBUS-OPERATION-CMD-X								NA							
PMBUS-CML	X						CML	X	NA							
PMBUS-VERSION	PMBUS-VERSON								NA							

NOTE: The highlighted gray cells indicate the register bits or fields that are stored in the NVM.

NOTE: X = Don't care.

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Table 7-16. Register Names

I²C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
00h	FFh	D0h	NOP	Section 7.6.1
01h	00h	25h	DAC-0-MARGIN-HIGH	Section 7.6.2
02h	00h	26h	DAC-0-MARGIN-LOW	Section 7.6.3
03h	FFh	D1h	DAC-0-VOUT-CMP-CONFIG	Section 7.6.4
04h	FFh	D2h	DAC-0-IOUT-MISC-CONFIG	Section 7.6.5
05h	FFh	D3h	DAC-0-CMP-MODE-CONFIG	Section 7.6.6
06h	FFh	D4h	DAC-0-FUNC-CONFIG	Section 7.6.7
07h	01h	25h	DAC-1-MARGIN-HIGH	Section 7.6.1
08h	01h	26h	DAC-1-MARGIN-LOW	Section 7.6.2
09h	FFh	D5h	DAC-1-VOUT-CMP-CONFIG	Section 7.6.3
0Ah	FFh	D6h	DAC-1-IOUT-MISC-CONFIG	Section 7.6.4
0Bh	FFh	D7h	DAC-1-CMP-MODE-CONFIG	Section 7.6.5
0Ch	FFh	D8h	DAC-1-FUNC-CONFIG	Section 7.6.6
0Dh	02h	25h	DAC-2-MARGIN-HIGH	Section 7.6.1
0Eh	02h	26h	DAC-2-MARGIN-LOW	Section 7.6.2
0Fh	FFh	D9h	DAC-2-VOUT-CMP-CONFIG	Section 7.6.3
10h	FFh	DAh	DAC-2-IOUT-MISC-CONFIG	Section 7.6.4
11h	FFh	DBh	DAC-2-CMP-MODE-CONFIG	Section 7.6.5
12h	FFh	DCh	DAC-2-FUNC-CONFIG	Section 7.6.6
13h	03h	25h	DAC-3-MARGIN-HIGH	Section 7.6.1
14h	03h	26h	DAC-3-MARGIN-LOW	Section 7.6.2
15h	FFh	DDh	DAC-3-VOUT-CMP-CONFIG	Section 7.6.3
16h	FFh	DEh	DAC-3-IOUT-MISC-CONFIG	Section 7.6.4
17h	FFh	DFh	DAC-3-CMP-MODE-CONFIG	Section 7.6.5
18h	FFh	E0h	DAC-3-FUNC-CONFIG	Section 7.6.6
19h	00h	21h	DAC-0-DATA	Section 7.6.8
1Ah	01h	21h	DAC-1-DATA	Section 7.6.8
1Bh	02h	21h	DAC-2-DATA	Section 7.6.8
1Ch	03h	21h	DAC-3-DATA	Section 7.6.8
1Fh	FFh	E3h	COMMON-CONFIG	Section 7.6.9
20h	FFh	E4h	COMMON-TRIGGER	Section 7.6.10
21h	FFh	E5h	COMMON-DAC-TRIG	Section 7.6.11

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Table 7-16. Register Names (continued)

I²C/SPI ADDRESS	PMBUS PAGE ADDR	PMBUS REGISTER ADDR	REGISTER NAME	SECTION
22h	FFh	E6h	GENERAL-STATUS	Section 7.6.12
23h	FFh	E7h	CMP-STATUS	Section 7.6.13
24h	FFh	E8h	GPIO-CONFIG	Section 7.6.14
25h	FFh	E9h	DEVICE-MODE-CONFIG	Section 7.6.15
26h	FFh	EAh	INTERFACE-CONFIG	Section 7.6.16
40h	NA	NA	DAC-0-DATA-8BIT	Section 7.6.17
41h	NA	NA	DAC-1-DATA-8BIT	Section 7.6.17
42h	NA	NA	DAC-2-DATA-8BIT	Section 7.6.17
43h	NA	NA	DAC-3-DATA-8BIT	Section 7.6.17
50h	FFh	F1h	BRDCAST-DATA	Section 7.6.18
51h	All pages	00h	PMBUS-PAGE	Section 7.6.19
52h	00h	01h	PMBIS-OP-CMD-0	Section 7.6.20
53h	01h	01h	PMBUS-OP-CMD-1	Section 7.6.20
54h	02h	01h	PMBUS-OP-CMD-2	Section 7.6.20
55h	03h	01h	PMBUS-OP-CMD-3	Section 7.6.20
56h	All pages	78h	PMBUS-CML	Section 7.6.21
57h	All pages	98h	PMBUS-VERSION	Section 7.6.22

Table 7-17. Access Type Codes

Access Type	Code	Description
X	X	Don't care
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.6.1 NOP Register (address = 00h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D0h

Figure 7-11. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/ $\overline{W}$-0h															

Table 7-18. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	NOP	R/$\overline{W}$	0000h	No operation

7.6.2 DAC-X-MARGIN-HIGH Register (address = 01h, 07h, 0Dh, 13h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 25h

Figure 7-12. DAC-X-MARGIN-HIGH Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-MARGIN-HIGH[11:0] DAC-X-MARGIN-HIGH[9:0]												X			
R/ $\overline{W}$-0h												X-0h			

Table 7-19. DAC-X-MARGIN-HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	DAC-X-MARGIN-HIGH[11:0] DAC-X-MARGIN-HIGH[9:0]	R/$\overline{W}$	000h	Margin-high code for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004: {DAC-X-MARGIN-HIGH[11:0]} DAC53004: {DAC-X-MARGIN-HIGH[9:0], X, X} X = Don't care bits.
3 - 0	X	X	0	Don't care

7.6.3 DAC-X-MARGIN-LOW Register (address = 02h, 08h, 0Eh, 14h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 26h

Figure 7-13. DAC-X-MARGIN-LOW Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-MARGIN-LOW[11:0] DAC-X-MARGIN-LOW[9:0]												X			
R/ $\overline{W}$-0h												X-0h			

Table 7-20. DAC-X-MARGIN-LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	DAC-X-MARGIN-LOW[11:0] DAC-X-MARGIN-LOW[9:0]	R/$\overline{W}$	000h	Margin-low code for DAC output Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004: {DAC-X-MARGIN-LOW[11:0]} DAC53004: {DAC-X-MARGIN-LOW[9:0], X, X} X = Don't care bits.
3 - 0	X	X	0	Don't care

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7.6.4 DAC-X-VOUT-CMP-CONFIG Register (address = 03h, 09h, 0Fh, 15h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D1h, D5h, D9h, DDh

Figure 7-14. DAC-X-VOUT-CMP-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			VOUT-GAIN-X			X					CMP-X-OD-EN	CMP-X-OUT-EN	CMP-X-HIZ-IN-DIS	CMP-X-INV-EN	CMP-X-EN
X-0h			R/$\overline{W}$-0h			X-0h					R/$\overline{W}$-0h	R/$\overline{W}$-0h	R/$\overline{W}$-0h	R/$\overline{W}$-0h	R/$\overline{W}$-0h

Table 7-21. DAC-X-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	X	X	0h	Don't care
12 - 10	VOUT-GAIN-X	R/$\overline{W}$	0h	000: Gain = 1x, external reference on VREF pin. 001: Gain = 1x, VDD as reference. 010: Gain = 1.5x, internal reference. 011: Gain = 2x, internal reference. 100: Gain = 3x, internal reference. 101: Gain = 4x, internal reference. Others: NA.
9 - 5	X	X	0h	Don't care
4	CMP-X-OD-EN	R/$\overline{W}$	0	1: Set OUTx pin as open-drain in comparator mode (CMP-X-EN = 1 and CMP-X-OUT-EN = 1). 0: Set OUTx pin as push-pull.
3	CMP-X-OUT-EN	R/$\overline{W}$	0	1: Bring comparator output to the respective OUTx pin. 0: Generate comparator output but consume internally.
2	CMP-X-HIZ-IN-DIS	R/$\overline{W}$	0	1: FBx input has high-impedance. Input voltage range is limited. 0: FBx input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-X-INV-EN	R/$\overline{W}$	0	1: Invert the comparator output. 0: Don't invert the comparator output.
0	CMP-X-EN	R/$\overline{W}$	0	1: Enable comparator mode. Current-output must be in power-down. 0: Disable comparator mode.

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7.6.5 DAC-X-IOUT-MISC-CONFIG Register (address = 04h, 0Ah, 10h, 16h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D2h, D6h, DAh, DEh

Figure 7-15. DAC-X-IOUT-MISC-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			IOUT-RANGE-X				X								
X-0h			R/ $\overline{W}$-0h				X-0h								

Table 7-22. DAC-X-IOUT-MISC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	X	X	0h	Don't care.
12 - 9	IOUT-RANGE-X	R/$\overline{W}$	0000	0000: 0 µA to 25 µA 0001: 0 µA to 50 µA 0010: 0 µA to 125 µA 0011: 0 µA to 250 µA 0100: -24 µA to 0 µA 0101: -48 µA to 0 µA 0110: -120 µA to 0 µA 0111: -240 µA to 0 µA 1000: -25 µA to +25 µA 1001: -50 µA to +50 µA 1010: -125 µA to +125 µA 1011: -250 µA to +250 µA Others: NA.
8 - 0	X	X	000h	Don't care.

7.6.6 DAC-X-CMP-MODE-CONFIG Register (address = 05h, 0Bh, 11h, 17h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D3h, D7h, DBh, DFh

Figure 7-16. DAC-X-CMP-MODE-CONFIG Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				CMP-X-MODE		X									
X-0h				R/$\overline{W}$-0h		X-0h									

Table 7-23. DAC-X-CMP-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	X	X	00h	Don't care.
11 - 10	CMP-X-MODE	R/$\overline{W}$	00	00: No hysteresis or window function. 01: Hysteresis provided using DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers. 10: Window comparator mode with DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers setting window bounds. 11: Invalid setting.
9 - 0	X	X	000h	Don't care.

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7.6.7 DAC-X-FUNC-CONFIG Register (address = 06h, 0Ch, 12h, 18h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = D4h, D8h, DCh, E0h

Figure 7-17. DAC-X-FUNC-CONFIG Register (X = 0, 1, 2, 3) for Linear Slew-Rate Setting

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR-SEL-X	SYNC-CONFIG-X	BRD-CONFIG-X	FUNC-GEN-CONFIG-BLOCK												
R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h												

Table 7-24. DAC-X-FUNC-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR-SEL-X	R/$\overline{W}$	0	0: Clear DAC-X to zero-scale. 1: Clear DAC-X to mid-scale.
14	SYNC-CONFIG-X	R/$\overline{W}$	0	0: DAC-X output updates immediately after a write command. 1: DAC-X output updates with $\overline{LDAC}$ pin falling-edge or when the LDAC bit in the COMMON-TRIGGER register is set to 1.
13	BRD-CONFIG-X	R/$\overline{W}$	0	0: Don't update DAC-X with broadcast command. 1: Update DAC-X with broadcast command.

Table 7-25. Linear-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12 - 11	PHASE-SEL-X	R/$\overline{W}$	0	00: 0 degree. 01: 120 degree. 10: 240 degree. 11: 90 degree.
10 - 8	FUNC-CONFIG-X	R/$\overline{W}$	0	000: Triangular wave. 001: Sawtooth wave. 010: Inverse sawtooth wave. 100: Sine wave. 111: Disable function generation. Others: Invalid.
7	LOG-SLEW-EN-X	R/$\overline{W}$	0	0: Enable linear slew.
6 - 4	CODE-STEP-X	R/$\overline{W}$	0	CODE-STEP for linear-slew mode: 000: 1-LSB. 001: 2-LSB. 010: 3-LSB. 011: 4-LSB. 100: 6-LSB. 101: 8-LSB. 110: 16-LSB. 111: 32-LSB.
3 - 0	SLEW-RATE-X	R/$\overline{W}$	0	SLEW-RATE for logarithmic-slew mode: 0000: No slew for margin-high and margin-low. Invalid for waveform generation. 0001: 4 µs/step. 0010: 8 µs/step. 0011: 12 µs/step. 0100: 18 µs/step. 0101: 27.04 µs/step. 0110: 40.48 µs/step. 0111: 60.72 µs/step. 1000: 91.12 µs/step. 1001: 136.72 µs/step. 1010: 239.2 µs/step. 1011: 418.64 µs/step. 1100: 732.56 µs/step. 1101: 1282 µs/step. 1110: 2563.92 µs/step. 1111: 5127.92 µs/step.

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Table 7-26. Logarithmic-Slew Mode: FUNC-GEN-CONFIG-BLOCK Field Descriptions

Bit	Field	Type	Reset	Description
12 - 11	PHASE-SEL-X	R/$\overline{W}$	0	00: 0 degree. 01: 120 degree. 10: 240 degree. 11: 90 degree.
10 - 8	FUNC-CONFIG-X	R/$\overline{W}$	0	000: Triangular wave. 001: Sawtooth wave. 010: Inverse sawtooth wave. 100: Sine wave. 111: Disable function generation. Others: Invalid.
7	LOG-SLEW-EN-X	R/$\overline{W}$	0	1: Enable logarithmic slew.
6 - 4	RISE-SLEW-X	R/$\overline{W}$	0	SLEW-RATE for log-slew mode: 000: 4 µs/step. 001: 12 µs/step. 010: 27.04 µs/step. 011: 60.72 µs/step. 100: 136.72 µs/step. 101: 418.64 µs/step. 110: 1282 µs/step. 111: 5127.92 µs/step.
3 - 1	FALL-SLEW-X	R/$\overline{W}$	0	SLEW-RATE for log-slew mode: 000: 4 µs/step. 001: 12 µs/step. 010: 27.04 µs/step. 011: 60.72 µs/step. 100: 136.72 µs/step. 101: 418.64 µs/step. 110: 1282 µs/step. 111: 5127.92 µs/step.
0	X	X	0	Don't care.

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7.6.8 DAC-X-DATA Register (address = 19h, 1Ah, 1Bh, 1Ch) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 21h

Figure 7-18. DAC-X-DATA Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-DATA[11:0] DAC-X-DATA[9:0]												X			
R/ $\overline{W}$-0h												X-0h			

Table 7-27. DAC-X-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	DAC-X-DATA[11:0] DAC-X-DATA[9:0]	R/$\overline{W}$	000h	Data for DAC output Data are in straight-binary format. MSB left-aligned. MSB left-aligned. Use the following bit-alignment: DAC63004: {DAC-X-DATA[11:0]} DAC53004: {DAC-X-DATA[9:0], X, X} X = Don't care bits.
3 - 0	X	X	0h	Don't care.

7.6.9 COMMON-CONFIG Register (address = 1Fh) [reset = 0FFFh]

PMBus page address = FFh, PMBus register address = E3h

Figure 7-19. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WINDOW-LATCH-EN	DEV-LOCK	EE-READ-ADDR	EN-INT-REF	VOUT-PDN-3		IOUT-PDN-3	VOUT-PDN-2		IOUT-PDN-2	VOUT-PDN-1		IOUT-PDN-1	VOUT-PDN-0		IOUT-PDN-0
R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h		R/ $\overline{W}$-0h	R/ $\overline{W}$-0h		R/ $\overline{W}$-0h	R/ $\overline{W}$-0h		R/ $\overline{W}$-0h	R/ $\overline{W}$-0h		R/ $\overline{W}$-0h

Table 7-28. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	WINDOW-LATCH-EN	R/$\overline{W}$	0	0: Non-latching window-comparator output. 1: Latching window-comparator output
14	DEV-LOCK	R/$\overline{W}$	0	0 : Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	EE-READ-ADDR	R/$\overline{W}$	0	0: Fault-dump read enable at address 0x00. 1: Fault-dump read enable at address 0x01.
12	EN-INT-REF	R/$\overline{W}$	000	0: Disable internal reference 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11 - 10, 8 - 7, 5 - 4, 2 - 1	VOUT-PDN-X	R/$\overline{W}$	11	00: Power-up VOUT-X. 01: Power-down VOUT-X with 10 KΩ to AGND. 10: Power-down VOUT-X with 100 KΩ to AGND. 11: Power-down VOUT-X with Hi-Z to AGND.
9, 6, 3, 0	IOUT-PDN-X	R/$\overline{W}$	1	0: Power-up IOUT-X. 1: Power-down IOUT-X

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7.6.10 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E4h

Figure 7-20. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				LDAC	CLR	X	FAULT-DUMP	PROTECT	READ-ONE-TRIG	NVM-PROG	NVM-RELOAD
R/ $\overline{W}$-0h				R/ $\overline{W}$-0h				R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	X-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h

Table 7-29. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	DEV-UNLOCK	R/$\overline{W}$	0000	0101: Device unlocking password. Others: Don't care.
11 - 8	RESET	$\overline{W}$	0000	1010 : POR reset triggered. This field is self-resetting. Others: Don't care.
7	LDAC	R/$\overline{W}$	0	0: LDAC operation not triggered. 1: LDAC operation triggered if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1. This bit is self-resetting.
6	CLR	R/$\overline{W}$	0	0: DAC registers and outputs unaffected. 1: DAC registers and outputs set to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register. This bit is self-resetting.
5	X	X	0	Don't care.
4	FAULT-DUMP	R/$\overline{W}$	0	0: Fault-dump is not triggered. 1: Triggers fault-dump sequence. This bit is self-resetting.
3	PROTECT	R/$\overline{W}$	0	0: PROTECT function not triggered. 1: Trigger PROTECT function. This bit is self-resetting.
2	READ-ONE-TRIG	R/$\overline{W}$	0	0: Fault-dump read not triggered. 1: Read one row of NVM for fault-dump. This bit is self-resetting.
1	NVM-PROG	R/$\overline{W}$	0	0: NVM write not triggered. 1: NVM write triggered. This bit is self-resetting.
0	NVM-RELOAD	R/$\overline{W}$	0	0: NVM reload not triggered. 1: Reload data from NVM to register map. This bit is self-resetting.

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7.6.11 COMMON-DAC-TRIG Register (address = 21h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E5h

Figure 7-21. COMMON-DAC-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET-CMP-FLAG-0	TRIG-MAR-LO-0	TRIG-MAR-HI-0	START-FUNC-0	RESET-CMP-FLAG-1	TRIG-MAR-LO-1	TRIG-MAR-HI-1	START-FUNC-1	RESET-CMP-FLAG-2	TRIG-MAR-LO-2	TRIG-MAR-HI-2	START-FUNC-2	RESET-CMP-FLAG-2	TRIG-MAR-LO-3	TRIG-MAR-HI-3	START-FUNC-3
$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	R/$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	R/$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	R/$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	$\overline{W}$-0h	R/$\overline{W}$-0h

Table 7-30. COMMON-DAC-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 , 11, 7, 3	RESET-CMP-FLAG-X	$\overline{W}$	0	0: Latching-comparator output unaffected. 1: Reset latching-comparator output. This bit is self-resetting.
14, 10, 6, 2	TRIG-MAR-LO-X	$\overline{W}$	0	0: Don't care. 1: Trigger margin-low command. This bit is self-resetting.
13, 9, 5, 1	TRIG-MAR-HI-X	$\overline{W}$	0	0: Don't care. 1: Trigger margin-high command. This bit is self-resetting.
12, 8, 4, 0	START-FUNC-X	R/$\overline{W}$	0	0: Stop function generation. 1: Start function generation as per FUNC-GEN-CONFIG-X in the DAC-X-FUNC-CONFIG register.

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7.6.12 GENERAL-STATUS Register (address = 22h) [reset = TBD]

PMBus page address = FFh, PMBus register address = E6h

Figure 7-22. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X	DAC-3-BUSY	DAC-2-BUSY	DAC-1-BUSY	DAC-0-BUSY	X	DEVICE-ID							
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	X-0h	R-0h							

Table 7-31. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP. 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading. 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this temporary error condition.
13	X	R	0	Don't care.
12	DAC-3-BUSY	R	0	0: DAC-3 channel can accept commands. 1: DAC-3 channel doesn't accept commands.
11	DAC-2-BUSY	R	0	0: DAC-2 channel can accept commands. 1: DAC-2 channel doesn't accept commands.
10	DAC-1-BUSY	R	0	0: DAC-1 channel can accept commands. 1: DAC-1 channel doesn't accept commands.
9	DAC-0-BUSY	R	0	0: DAC-0 channel can accept commands. 1: DAC-0 channel doesn't accept commands.
8	X	R	0	Don't care
7 - 0	DEVICE-ID	R		Device identifier: DAC53004: 24h DAC63004: 34h

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7.6.13 CMP-STATUS Register (address = 23h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E7h

Figure 7-23. CMP-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X							PROTECT-FLAG	WIN-CMP-3	WIN-CMP-2	WIN-CMP-1	WIN-CMP-0	CMP-FLAG-3	CMP-FLAG-2	CMP-FLAG-1	CMP-FLAG-0
X-0h							R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-32. CMP-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	X	X	0	Don't care.
8	PROTECT-FLAG	R	0	0 : PROTECT operation not triggred or in progress. 1: PROTECT function is completed. This bit resets to 0 when read.
7, 6, 5, 4	WIN-CMP-X	R	0	Window comparator output from respective channels. The output is latched or unlatched based on the WINDOW-LATCH-EN setting in the COMMON-CONFIG register.
3, 2, 1, 0	CMP-FLAG-X	R	0	Synchronized comparator output from respective channels.

7.6.14 GPIO-CONFIG Register (address = 24h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E8h

Figure 7-24. GPIO-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GF-EN	DEEP-SLEEP-EN	GPO1-EN	GPO1-CONFIG				GPI1-CH-SEL				GPI1-CONFIG				GPI1-EN
R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h	R/ $\overline{W}$-0h				R/ $\overline{W}$-0h				R/ $\overline{W}$-0h				R/ $\overline{W}$-0h

Table 7-33. GPIO-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GF-EN	R/$\overline{W}$	0	0: Glitch filter disabled for GP input. This setting provides faster response. 1: Glitch filter enabled for GP input. This setting introduces additional propagation delay but provides robustness.
14	DEEP-SLEEP-EN	R/$\overline{W}$	0	0: Deep-sleep mode disabled. 1: Deep-sleep mode enabled for GP input.
13	GPO1-EN	R/$\overline{W}$	0	0: Disable output mode for GPIO pin. 1: Enable output mode for GPIO pin.
12 - 9	GPO1-CONFIG	R/$\overline{W}$	0000	$\overline{\text{STATUS}}$ function setting. The GPIO pin is mapped to the following register bits as output: 0001: NVM-BUSY 0100: DAC-0-BUSY 0101: DAC-1-BUSY 0110: DAC-2-BUSY 0111: DAC-3-BUSY 1000: WIN-CMP-0 1001: WIN-CMP-1 1010: WIN-CMP-2 1011:WIN-CMP-3 Others: NA

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Table 7-33. GPIO-CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8 - 5	GPI1-CH-SEL	R/$\overline{W}$	0000	Each bit corresponds to a DAC channel. 0b is *disabled* and 1b is *enabled*. GPI1-CH-SEL[0]: Channel 0 GPI1-CH-SEL[1]: Channel 1 GPI1-CH-SEL[2]: Channel 2 GPI1-CH-SEL[3]: Channel 3 Example: when GPI1-CH-SEL is 0101, both channel-0 and channel-2 are enabled and both channel-1 and channel-3 are disabled.
4 - 1	GPI1-CONFIG	R/$\overline{W}$	0000	GPIO pin input configuration. Global settings act on the entire device. Channel-specific settings are dependent on the channel selection by the GPI1-CH-SEL bits: 0000: $\overline{\text{DEEP-SLEEP}}$ (global). GPIO falling-edge triggers deep-sleep mode, GPIO rising-edge takes the device out of deep-sleep mode. 0010: $\overline{\text{FAULT-DUMP}}$ (global). GPIO falling-edge triggers fault-dump, GPIO = 1 has no effect. 0011: IOUT power-up, down (channel-specific). GPIO = 0 is power-down, GPIO = 1 is power-up. 0100: VOUT power-up/down (channel-specific). The output load is as per the VOUT-PDN-X setting. GPIO = 0 is power-down, GPIO = 1 is power-up. 0101: $\overline{\text{PROTECT}}$ input (global). GPIO falling-edge asserts $\overline{\text{PROTECT}}$ function, GPIO = 1 has no effect. 0111: $\overline{\text{CLR}}$ input (global). GPIO = 0 asserts $\overline{\text{CLR}}$ function, GPIO = 1has no effect. 1000: $\overline{\text{LDAC}}$ input (channel-specific). GPIO falling-edge asserts $\overline{\text{LDAC}}$ function, GPIO = 1 has no effect. Both the SYNC-CONFIG-X and the GPI1-CH-SEL must be configured for every channel. 1001: Start, stop function generation (channel-specific). GPIO falling-edge stops function generation. GPIO rising-edge starts function generation. 1010: Trigger margin-high, low (channel-specific). GPIO falling-edge triggers margin-low. GPIO rising-edge triggers margin-high. 1011:$\overline{\text{RESET}}$ input (global). The falling-edge of the GPIO pin asserts the $\overline{\text{RESET}}$ function. The $\overline{\text{RESET}}$ input must be a pulse. The GPIO rising-edge brings the device out of reset. The $\overline{\text{RESET}}$ configuration must be programmed into the NVM. Otherwise the setting will be cleared after the device reset. 1100: NVM write-protection (global). GPIO falling-edge allows NVM programming. GPIO = 1 blocks NVM programming. 1101: Register-map lock (global). GPIO = 0 allows update to the register map. GPIO = 1 blocks any register map update except a write to the DEV-UNLOCK field. Others: NA
0	GPI1-EN	R/$\overline{W}$	0	0: Disable input mode for GPIO pin. 1: Enable input mode for GPIO pin.

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7.6.15 DEVICE-MODE-CONFIG Register (address = 25h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = E9h

Figure 7-25. DEVICE-MODE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DIS-MODE-IN	RESERVED			PROTECT-CONFIG		RESERVED			X				
R/ $\overline{W}$-0h		R/ $\overline{W}$-0h	R/ $\overline{W}$-0h			R/ $\overline{W}$-0h		R/ $\overline{W}$-0h			X-0h				

Table 7-34. DEVICE-MODE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R/$\overline{W}$	00	Always write 0b00.
13	DIS-MODE-IN	R/$\overline{W}$	0	Always write 1.
12 - 10	RESERVED	R/$\overline{W}$	0	Always write 0b000.
9 - 8	PROTECT-CONFIG	R/$\overline{W}$	00	00: Switch to power-down (no slew). 01: Switch to DAC code stored in NVM (no slew) and then switch to power-down. 10: Slew to margin-low code and then switch to power-down. 11: Slew to margin-high code and then switch to power-down.
7 - 5	RESERVED	R/$\overline{W}$	0	Always write 0b000.
4 - 0	X	R/$\overline{W}$	00h	Don't care.

7.6.16 INTERFACE-CONFIG Register (address = D1h) [reset = 0000h]

Figure 7-26. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X			TIMEOUT-EN	X			EN-PMBUS	X					FSDO-EN	X	SDO-EN
X-0h			R/ $\overline{W}$-0h	X-0h			R/ $\overline{W}$-0h	X-0h					R/ $\overline{W}$-0h	X-0h	R/ $\overline{W}$-0h

Table 7-35. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	X	X	0h	Don't care.
12	TIMEOUT-EN	R/$\overline{W}$	0	0: I^2C timeout disabled. 1: I^2C timeout enabled.
11 - 9	X	X	0h	Don't care.
8	EN-PMBUS	R/$\overline{W}$	0	0: PMBus disabled. 1: Enable PMBus.
7 - 3	X	X	00h	Don't care.
2	FSDO-EN	R/$\overline{W}$	0	0: Fast SDO disabled. 1: Fast SDO enabled.
1	X	X	0	Don't care.
0	SDO-EN	R/$\overline{W}$	0	0: SDO disabled. 1: SDO enabled on GPIO pin.

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7.6.17 DAC-X-DATA-8BIT Register (address = 40h, 41h, 42h, 43h) [reset = 0000h]

PMBus page address = Not applicable, PMBus register address = Not applicable

Figure 7-27. DAC-X-DATA-8BIT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-X-DATA-8BIT[7:0]								X							
R/ $\overline{W}$-0h								X-0h							

Table 7-36. DAC-X-DATA-8BIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	DAC-X-DATA-8BIT[7:0]	R/$\overline{W}$	00h	8-bit data for current output. This register provides faster update rate. Data are in straight-binary format.
7 - 0	X	X	00h	Don't care.

7.6.18 BRDCAST-DATA Register (address = 50h) [reset = 0000h]

PMBus page address = FFh, PMBus register address = F1h

Figure 7-28. BRDCAST-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[11:0] BRDCAST-DATA[9:0]												X			
R/ $\overline{W}$-0h												X-0h			

Table 7-37. BRDCAST-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	BRDCAST-DATA[11:0] BRDCAST-DATA[9:0]	R/$\overline{W}$	000h	Broadcast code for all DAC channels Data are in straight-binary format. MSB left-aligned. Use the following bit-alignment: DAC63004: {BRDCAST-DATA[11:0]} DAC53004: {BRDCAST-DATA[9:0], X, X} X = Don't care bits. The BRD-CONFIG-X bit in the DAC-X-FUNC-CONFIG register must be enabled for the respective channels.
3 - 0	X	X	0h	Don't care.

7.6.19 PMBUS-PAGE Register (address = 51h) [reset = 0000h]

PMBus page address = X, PMBus register address = 00h

Figure 7-29. PMBUS-PAGE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-PAGE								X							
R/ $\overline{W}$-00h								X-00h							

Table 7-38. PMBUS_OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	PMBUS-PAGE	R/$\overline{W}$	00h	8-bit PMBus page address.
7 - 0	X	X	00h	Not applicable.

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7.6.20 PMBUS-OP-CMD-X Register (address = 52h, 53h, 54h, 55h) [reset = 0000h]

PMBus page address = 00h, 01h, 02h, 03h, PMBus register address = 01h

Figure 7-30. PMBUS-OP-CMD-X Register (X = 0, 1, 2, 3)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-OPERATION-CMD-X								X							
R/ $\overline{W}$-00h								X-00h							

Table 7-39. PMBUS-OP-CMD-X Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	PMBUS-OPERATION-CMD-X	R/$\overline{W}$	00h	PMBus operation commands: 00h: Turn off . 80h: Turn on. A4h: Margin high, DAC output margins high to DAC-X-MARGIN-HIGH code. 94h: Margin low, DAC output margins low to DAC-X-MARGIN-LOW code.
7 - 0	X	X	00h	Not applicable.

7.6.21 PMBUS-CML Register (address = 56h) [reset = 0000h]

PMBus page address = X, PMBus register address = 78h

Figure 7-31. PMBUS-CML Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X						CML	X	N/A							
X-00h						R/$\overline{W}$-0h	X-0h	X-00h							

Table 7-40. PMBUS-CML Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	X	X	00h	Don't care.
9	CML	R/$\overline{W}$	0	0: No communication fault. 1: PMBus communication fault for write with incorrect number of clocks, read before write command, invalid command address, and invalid or unsupported data value; reset this bit by writing 1.
8	X	X	0h	Don't care.
7 - 0	X	X	00h	Not applicable

7.6.22 PMBUS-VERSION Register (address = 57h) [reset = 2200h]

PMBus page address = X, PMBus register address =98h

Figure 7-32. PMBUS-VERSION Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMBUS-VERSION								X							
R-22h								X-00h							

Table 7-41. PMBUS-VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	PMBUS-VERSION	R	22h	PMBus version.
7 - 0	X	X	00h	Not applicable.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DACx3004 are quad-channel buffered, force-sense output, voltage-output and current-output smart DACs that include an NVM and internal reference, and available in a tiny 3-mm × 3-mm package. In voltage-output mode, short the OUTx and FBx pins for each channel. In current-output mode, leave the FBx pins unconnected. The FBx pins function as inputs in comparator mode. The external reference must not exceed VDD, either during transient or steady-state conditions. For the best Hi-Z output performance, use a pullup resistor on the VREF pin to VDD. In case the VDD remains floating during the off condition, place a 100-kΩ resistor to AGND for proper detection of the VDD off condition. All the digital outputs are open drain; use external pullup resistors on these pins. The interface protocol is detected at power-on, and the device locks to the protocol as long as VDD is on. In I^2C mode, when allocating the I^2C addresses in the system, consider the broadcast address as well. I^2C timeout can be enabled for robustness. SPI mode is 3-wire by default. Configure the GPIO pin as SDO in the NVM for SPI readback capability. The SPI clock speed in readback mode is slower than that in write mode. Power-down mode sets the DAC outputs in Hi-Z by default. Change the configuration appropriately for different power-down settings. The DAC channels can also power-up with a programmed DAC code in the NVM.

8.2 Typical Application

A power-supply margining and scaling circuit is used to trim, scale, or test the output of a power converter. This example circuit is used to test a system by margining the power supplies for adaptive voltage scaling or to program a desired value at the output. Adjustable power supplies, such as low dropout regulators (LDOs) and DC/DC converters, provide a feedback or adjust the input that is used to set the desired output. A precision voltage-output DAC is the best choice for controlling the power-supply output linearly. Figure 8-1 shows a control circuit for a switch-mode power supply (SMPS) using the DACx3004. Typical applications of power-supply margining are communications equipment, enterprise servers, test and measurement, and general-purpose power-supply modules.

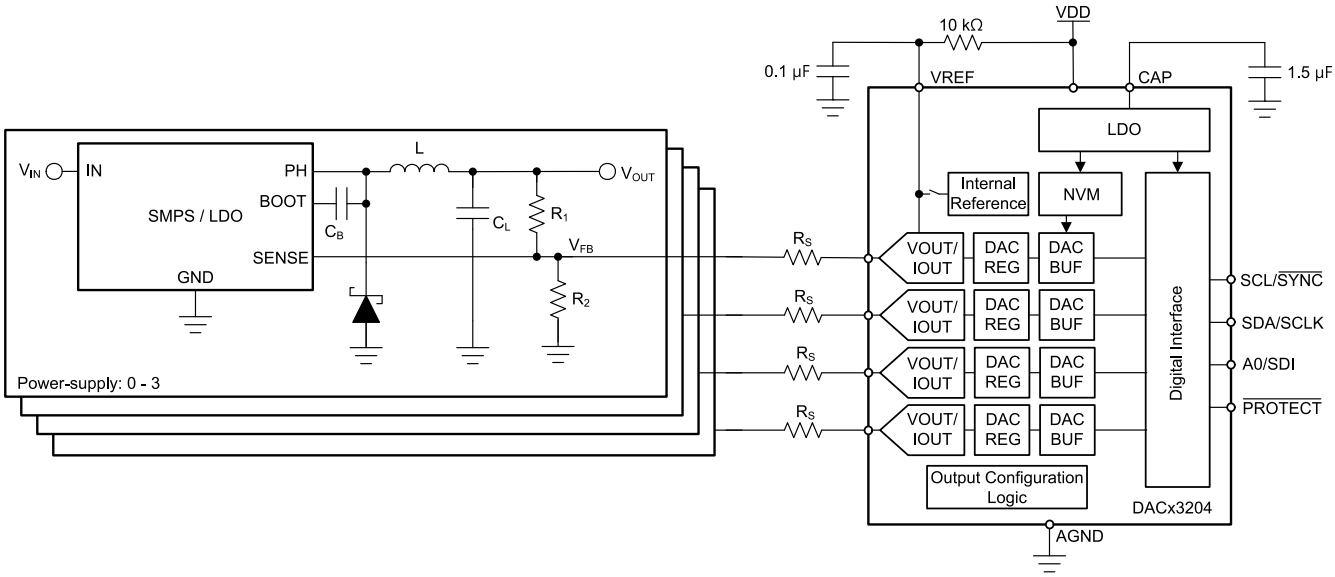

Figure 8-1. Voltage Margining and Scaling

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8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Power-supply nominal output	3.3 V
Reference voltage of the converter (V_{FB})	0.6 V
Margin	±10% (that is, 2.97 V to 3.63 V)
DAC output range	1.8 V
Nominal current through R_1 and R_2	100 µA

8.2.2 Detailed Design Procedure

The DACx3004 features a Hi-Z power-down mode that is set by default at power-up, unless the device is programmed otherwise using the NVM. When the DAC output is at Hi-Z, the current through R_3 is zero and the SMPS is set at the nominal output voltage of 3.3 V. To have the same nominal condition when the DAC powers up, bring up the device at the same output as V_{FB} (that is 0.6 V). This configuration makes sure there is no current through R_3 even at power-up. Calculate R_1 as ($V_{OUT} – V_{FB}$) / 100 µA = 27 kΩ.

To achieve ±10% margin-high and margin-low conditions, the DAC must sink or source additional current through R_1. Calculate the current from the DAC (I_{MARGIN}) using Equation 9 as 12 µA.

$$I_{MARGIN} = \left(\frac{V_{OUT} \times (1 + MARGIN) - V_{FB}}{R_1} \right) - I_{NOMINAL} \tag{9}$$

where

- I_{MARGIN} is the margin current sourced or sinked from the DAC.
- MARGIN is the percentage margin value divided by 100.
- $I_{NOMINAL}$ is the nominal current through R_1 and R_2.

To calculate the value of R_3, first decide the DAC output range, and make sure to avoid the codes near zero-scale and full-scale for safe operation in the linear region. A DAC output of 20 mV is a safe consideration as the minimum output, and (1.8 V – 0.6 V – 20 mV = 1.18 V) as the maximum output. When the DAC output is at 20 mV, the power supply goes to margin high, and when the DAC output is at 1.18 V, the power supply goes to margin low. Calculate the value of R_3 using Equation 10 as 48.3 kΩ. Choose a standard resistor value and adjust the DAC outputs. Choosing R_3 = 47 kΩ makes the DAC margin high code as 1.164 V and the DAC margin low code as 36 mV.

$$R_3 = \frac{|V_{DAC} - V_{FB}|}{I_{MARGIN}} \tag{10}$$

When the DACx3004 are set in the current-output mode, the series resistor R_3 is not required. Set the DAC output at the current-output range of –25 µA to +25 µA, and set the DAC code appropriately to achieve a margin current of ±12 µA.

The DACx3004 have a slew-rate feature that is used to toggle between margin high, margin low, and nominal outputs with a defined slew rate. See Section 7.6.7 for the slew-rate setting details.

Note

The DAC-X-MARGIN-HIGH register value in DACx3004 results in the *margin-low* value at the power supply output. Similarly, the DAC-X-MARGIN-LOW register value in DACx3004 results in the *margin-high* value at the power-supply output.

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9 Power Supply Recommendations

The DACx3004 family of devices does not require specific power-supply sequencing. These devices require a single power supply, V_{DD}. However, make sure the external voltage reference is applied after VDD. Use a 0.1-µF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 µF for the CAP pin.

10 Layout

10.1 Layout Guidelines

The DACx3004 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

10.2 Layout Example

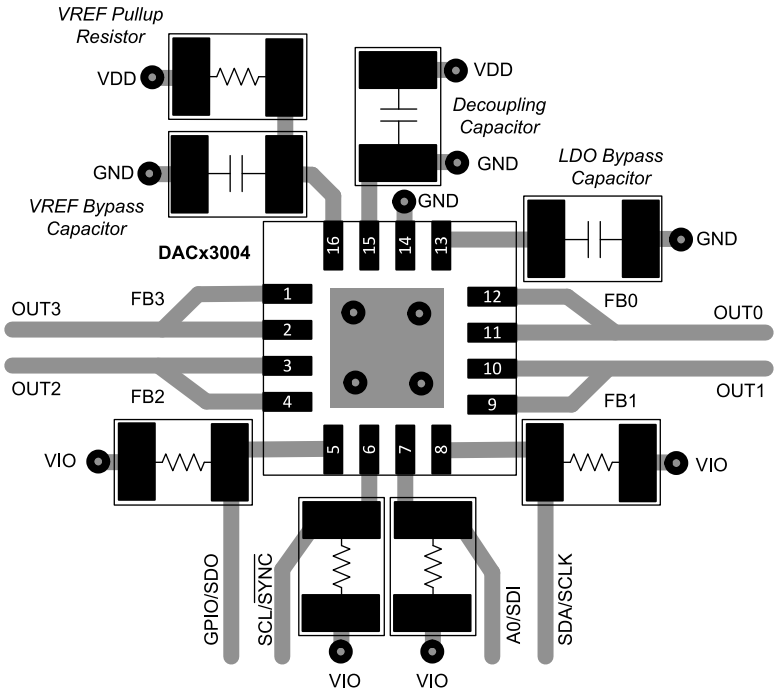

Figure 10-1. Layout Example

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

PMBus™ is a trademark of SMIF, Inc..
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

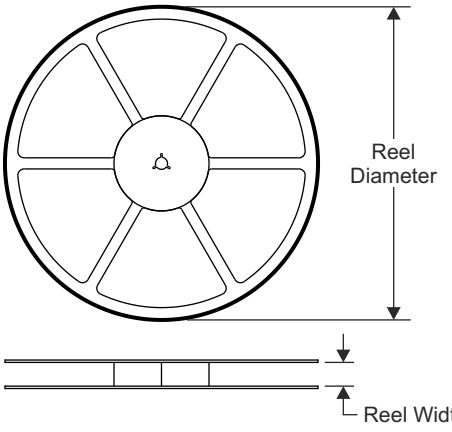
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

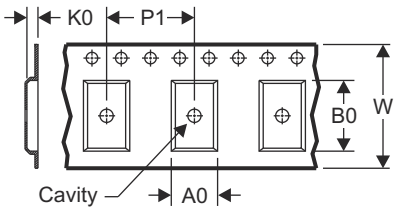
ADVANCE INFORMATION

Tape and Reel Information

REEL DIMENSIONS

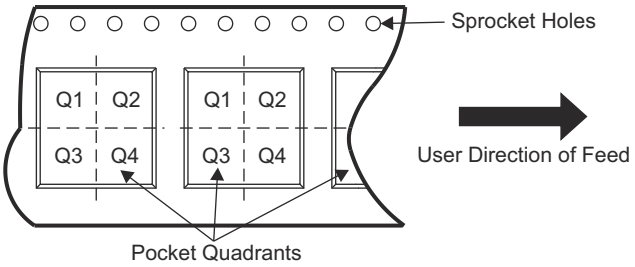


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC53004RTER	WQFN	RTE	16	3000	330	12.4	3.3	3.3	1.1	8	12	Q2
DAC63004RTER	WQFN	RTE	16	3000	330	12.4	3.3	3.3	1.1	8	12	Q2

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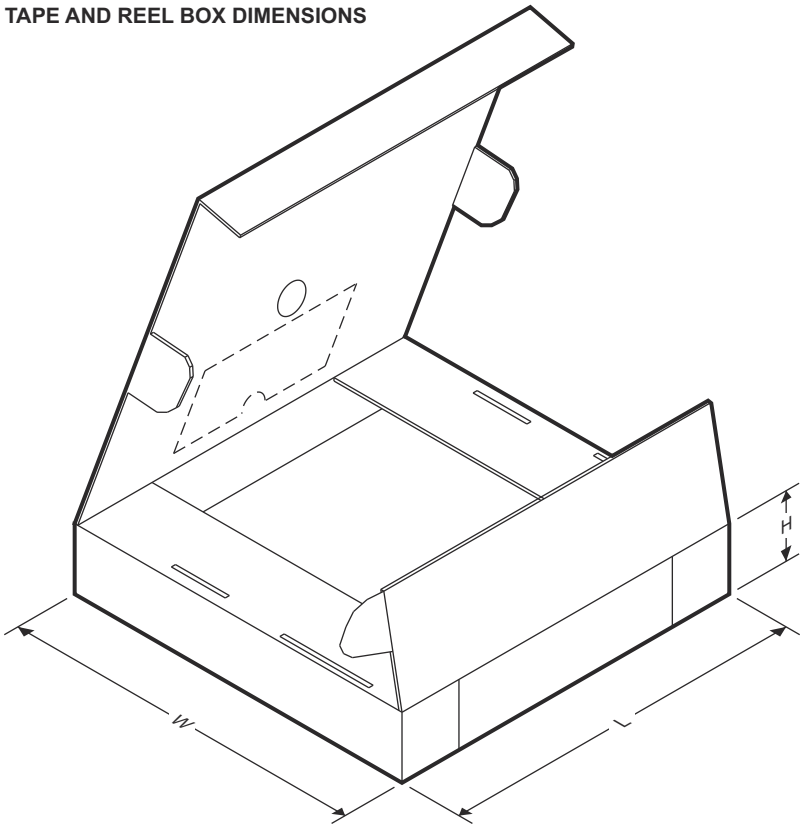
TAPE AND REEL BOX DIMENSIONS

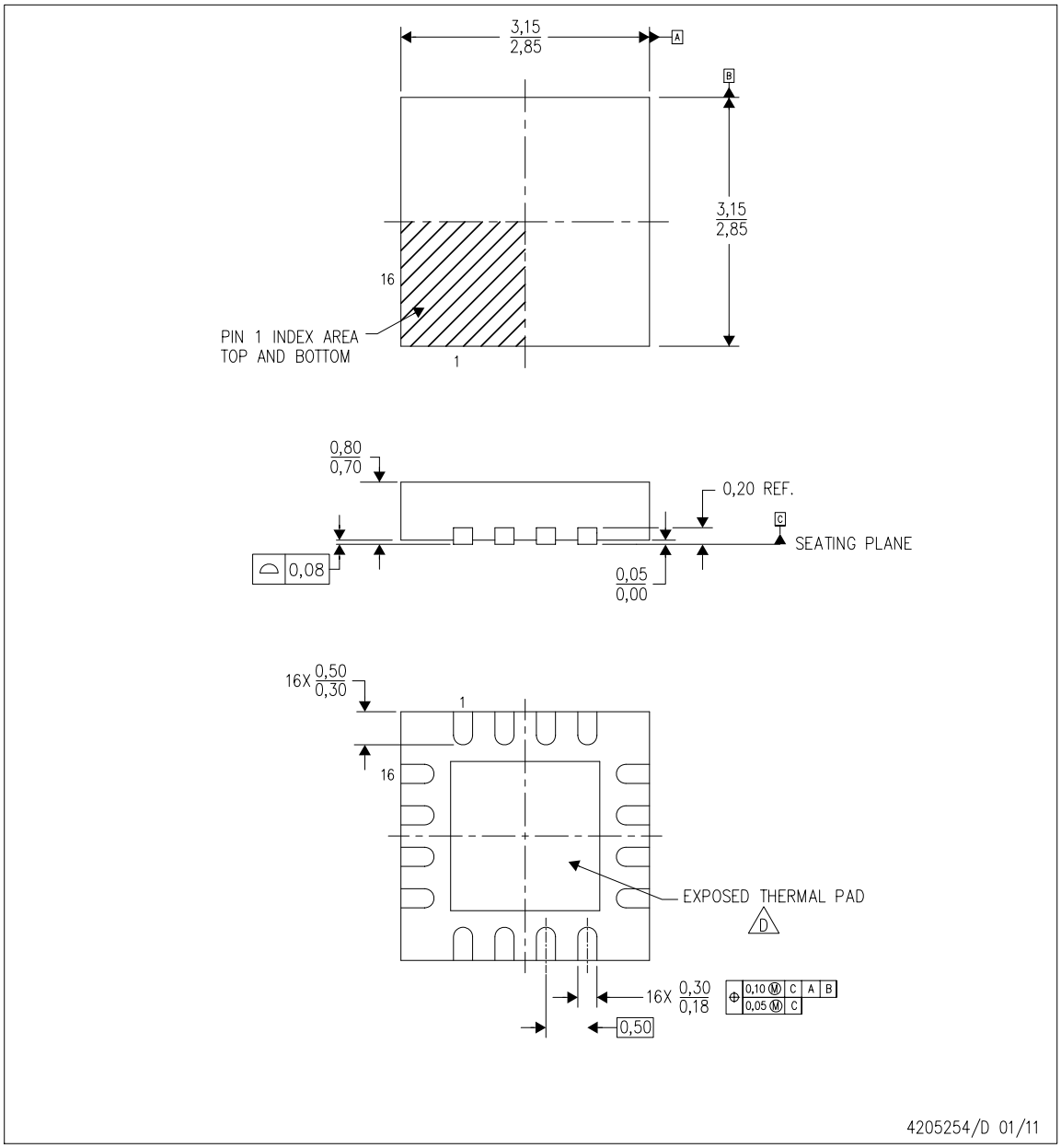


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC53004RTER	WQFN	RTE	16	3000	367	367	35
DAC63004RTER	WQFN	RTE	16	3000	367	367	35

ADVANCE INFORMATION

MECHANICAL DATA

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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THERMAL PAD MECHANICAL DATA

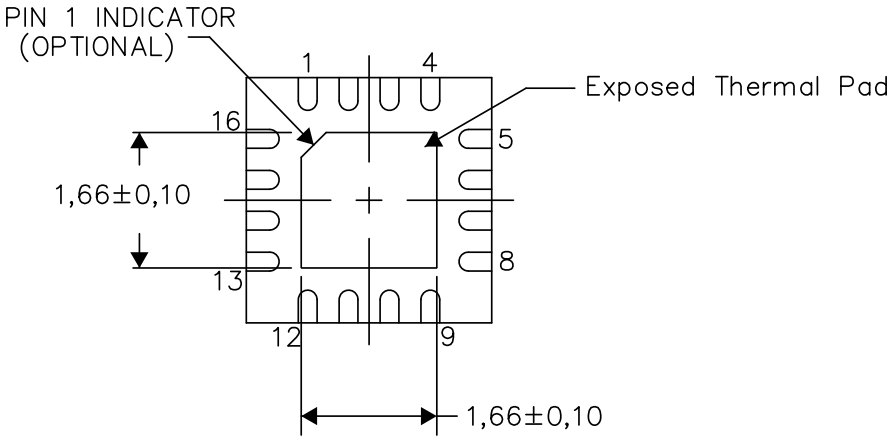
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

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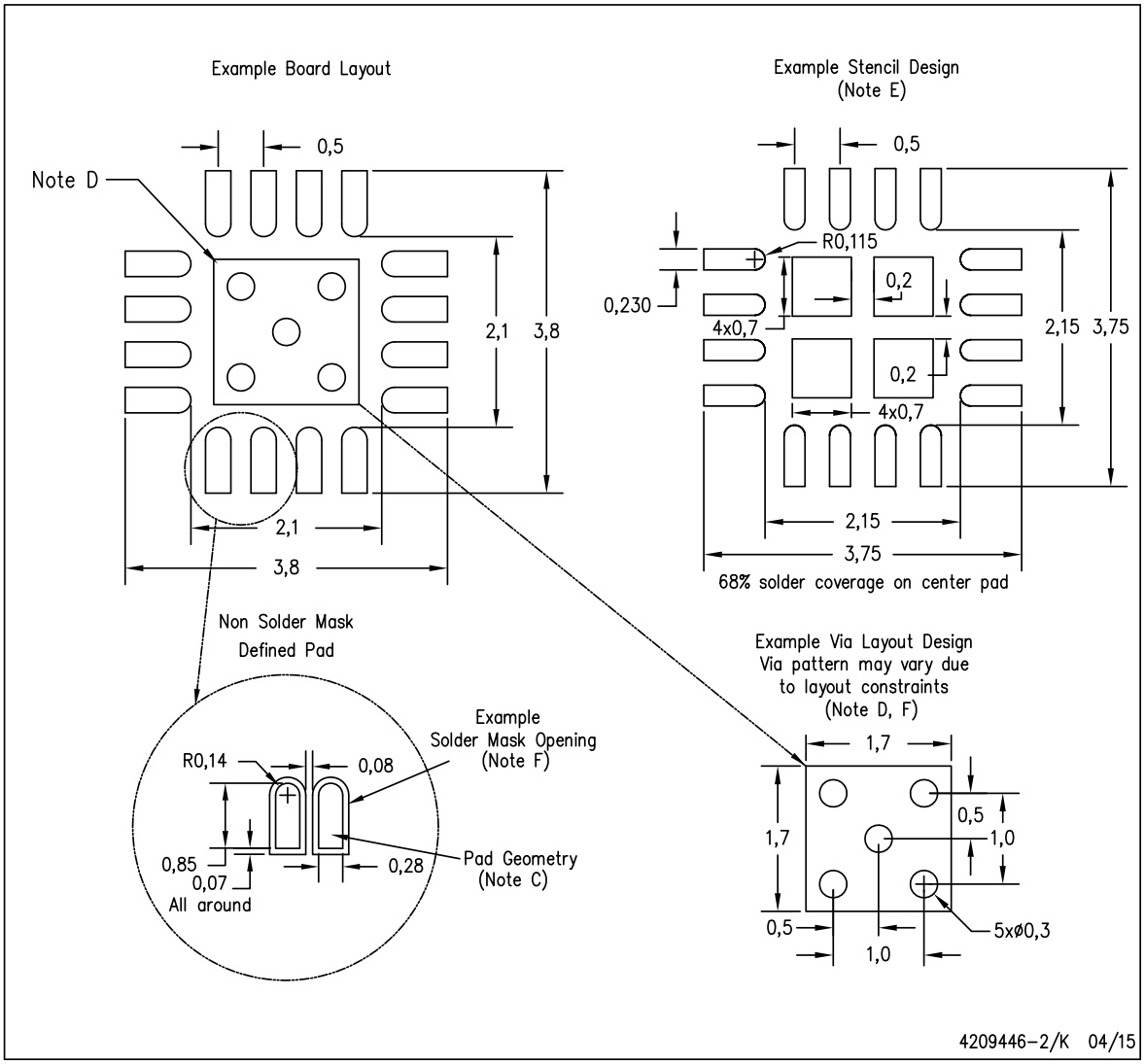
LAND PATTERN DATA

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC53004RTET	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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