Nonvolatile Memory, Dual 1024-Position Digital Potentiometer

AD5235-EP

FEATURES

Dual-channel, 1024-position resolution
25 kΩ nominal resistance
Low temperature coefficient: 35 ppm/°C
Nonvolatile memory stores wiper settings
Permanent memory write protection
Wiper setting readback
Resistance tolerance stored in EEMEM
Predefined linear increment/decrement instructions
Predefined ±6 dB/step log taper increment/decrement instructions
SPI-compatible serial interface
3 V to 5 V single supply or ±2.5 V dual supply
26 bytes extra nonvolatile memory for user-defined information
100-year typical data retention, T_A = 55°C
Power-on refreshed with EEMEM settings
Enhanced Features
- **Supports defense and aerospace applications (AQEC)**
- **Temperature range: −40°C to +125°C**
- **Controlled manufacturing baseline**
- **1 assembly/test site**
- **1 fabrication site**
- **Enhanced product change notification**
- **Qualification data available on request**

APPLICATIONS

DWDM laser diode driver, optical supervisory systems
Mechanical potentiometer replacement
Instrumentation: gain, offset adjustment
Programmable voltage-to-current conversion
Programmable filters, delays, time constants
Programmable power supply
Low resolution DAC replacement
Sensor calibration

GENERAL DESCRIPTION

The AD5235-EP is a dual-channel, nonvolatile memory,[1] digitally controlled potentiometer[2] with 1024-step resolution. The device performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. The AD5235-EP's versatile programming via an SPI®-compatible serial interface allows 16 modes of operation and adjustment including scratchpad programming, memory storing and restoring, increment/decrement, ±6 dB/step log taper adjustment, wiper setting readback, and extra EEMEM[1] for user-defined information such as memory data for other components, look-up tables, or system identification information.

FUNCTIONAL BLOCK DIAGRAM

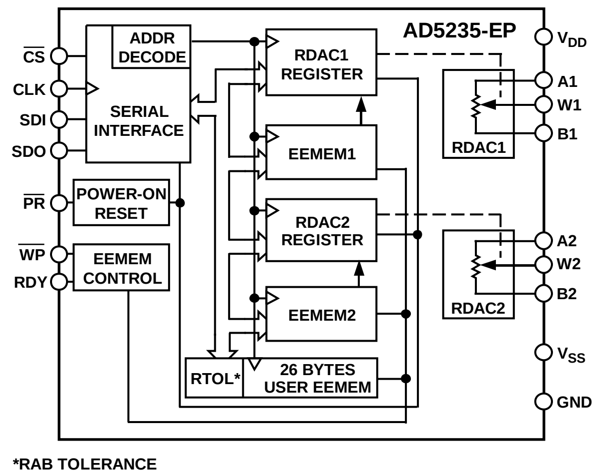

Figure 1.

In scratchpad programming mode, a specific setting can be programmed directly to the RDAC[2] register that sets the resistance between Terminal W and Terminal A, and Terminal W and Terminal B. This setting can be stored into the EEMEM and is restored automatically to the RDAC register during system power-on.

The EEMEM content can be restored dynamically or through external $\overline{PR}$ strobing, and a $\overline{WP}$ function protects EEMEM contents. To simplify the programming, the independent or simultaneous linear-step increment or decrement commands can be used to move the RDAC wiper up or down, one step at a time. For logarithmic ±6 dB changes in the wiper setting, the left or right bit shift command can be used to double or halve the RDAC wiper setting.

The AD5235-EP patterned resistance tolerance is stored in the EEMEM. Therefore, in readback mode, the host processor can know the actual end-to-end resistance. The host can execute the appropriate resistance step through a software routine that simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5235-EP is available in a thin, 16-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Full details about this enhanced product, including theory of operation, register details, and applications information, are available in the AD5235 data sheet, which should be consulted in conjunction with this data sheet.

[1] The terms nonvolatile memory and EEMEM are used interchangeably.
[2] The terms digital potentiometer and RDAC are used interchangeably.

Rev. 0

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REVISION HISTORY

7/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 3 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V, V_{SS} = −2.5 V, V_A = V_{DD}, V_B = V_{SS}, −40°C < T_A < +125°C, unless otherwise noted. The part can be operated at 2.7 V single supply, except from 0°C to −40°C, where a minimum of 3 V is needed.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (All RDACs)						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−2		+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}	−4		+4	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	Code = full scale	−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R_{WB}, V_{DD} = 5 V, code = half scale		50	100	Ω
		I_W = 1 V/R_{WB}, V_{DD} = 3 V, code = half scale		200		Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = full scale, T_A = 25°C		±0.1		%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (All RDACs)						
Resolution	N				10	Bits
Differential Nonlinearity[3]	DNL		−2		+2	LSB
Integral Nonlinearity[3]	INL		−4		+4	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−9		0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		5	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance Ax, Bx[5]	C_A, C_B	f = 1 MHz, measured to GND, code = half-scale		11		pF
Capacitance Wx[5]	C_W	f = 1 MHz, measured to GND, code = half-scale		80		pF
Common-Mode Leakage Current[5, 6]	I_{CM}	V_W = V_{DD}/2		0.01	±2	μA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V	2.0			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±2.25	μA
Input Capacitance[5]	C_{IL}			5		pF

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	3.0		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		3.5	8	μA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V		3.5	7	μA
EEMEM Store Mode Current	I_{DD} (store)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$		35		mA
	I_{SS} (store)	V_{DD} = +2.5 V, V_{SS} = −2.5 V		−35		mA
EEMEM Restore Mode Current[7]	I_{DD} (restore)	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$	0.3	3	9	mA
	I_{SS} (restore)	V_{DD} = +2.5 V, V_{SS} = −2.5 V	−0.3	−3	−9	mA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		18	50	μW
Power Supply Sensitivity[5]	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[5, 9]						
Bandwidth	BW	−3 dB, V_{DD}/V_{SS} = ±2.5 V		125		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, V_W = 0.50% error band, Code 0x000 to Code 0x200		4		μs
Resistor Noise Density	e_{N_WB}	T_A = 25°C		20		nV/√Hz
Crosstalk (C_{W1}/C_{W2})	C_T	$V_A = V_{DD}$, V_B = 0 V, measured V_{W1} with V_{W2} making full-scale change		90		nV-s
Analog Crosstalk	C_{TA}	$V_{DD} = V_{A1}$ = +2.5 V, $V_{SS} = V_{B1}$ = −2.5 V, measured V_{W1} with V_{W2} = 5 V p-p @ f = 1 kHz, Code 1 = 0x200, Code 2 = 0x3FF		−81		dB

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W ~ 50 μA for V_{DD} = 2.7 V and I_W ~ 400 μA for V_{DD} = 5 V (see Figure 23).
[3] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B = V_{SS}$. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions (see Figure 24).
[4] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[5] Guaranteed by design and not subject to production test.
[6] Common-mode leakage current is a measure of the dc leakage from any Terminal A, Terminal B, or Terminal W to a common-mode bias level of $V_{DD}/2$.
[7] EEMEM restore mode current is not continuous. Current is consumed while EEMEM locations are read and transferred to the RDAC register (see Figure 20). To minimize power dissipation, a NOP, Instruction 0 (0x0) should be issued immediately after Instruction 1 (0x1).
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[9] All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = −2.5 V.

INTERFACE TIMING AND EEMEM RELIABILITY CHARACTERISTICS

Guaranteed by design and not subject to production test. See the Timing Diagrams section for the location of measured values. All input control voltages are specified with $t_R = t_F = 2.5$ ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD} = 3$ V and $V_{DD} = 5$ V.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulse Width	t_4, t_5	Clock level high or low	10			ns
Data Setup Time	t_6	From positive CLK transition	5			ns
Data Hold Time	t_7	From positive CLK transition	5			ns
$\overline{CS}$-to-SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$-to-SDO-SPI Line Release	t_9				50	ns
CLK-to-SDO Propagation Delay[2]	t_{10}	$R_P = 2.2$ kΩ, $C_L < 20$ pF			50	ns
CLK-to-SDO Data Hold Time	t_{11}	$R_P = 2.2$ kΩ, $C_L < 20$ pF	0			ns
$\overline{CS}$ High Pulse Width[3]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[3]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.15	0.3	ms
Store/Read EEMEM Time[4]	t_{16}	Applies to instructions 0x2, 0x3, and 0x9		30		ms
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		15			ns
Preset Pulse Width (Asynchronous)[5]	t_{PRW}		50			ns
Preset Response Time to Wiper Setting[5]	t_{PRESP}	$\overline{PR}$ pulsed low to refresh wiper positions		140		μs
Power-On EEMEM Restore Time[5]	t_{EEMEM}			140		μs
FLASH/EE MEMORY RELIABILITY						
Endurance[6]			100			kCycles
Data Retention[7]				100		Years

[1] Typicals represent average readings at 25°C and $V_{DD} = 5$ V.
[2] Propagation delay depends on the value of V_{DD}, $R_{PULL-UP}$, and C_L.
[3] Valid for commands that do not activate the RDY pin.
[4] RDY pin low only for Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and the $\overline{PR}$ hardware pulse: CMD_8 ~ 1 ms; CMD_9, CMD_10 ~ 0.1 ms; CMD_2, CMD_3 ~ 20 ms. Device operation at $T_A = -40$°C and $V_{DD} < 3$ V extends the save time to 35 ms.
[5] Not shown in Figure 2 and Figure 3.
[6] Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, and +85°C; typical endurance at +25°C is 700,000 cycles.
[7] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature in the Flash/EE memory.

Timing Diagrams

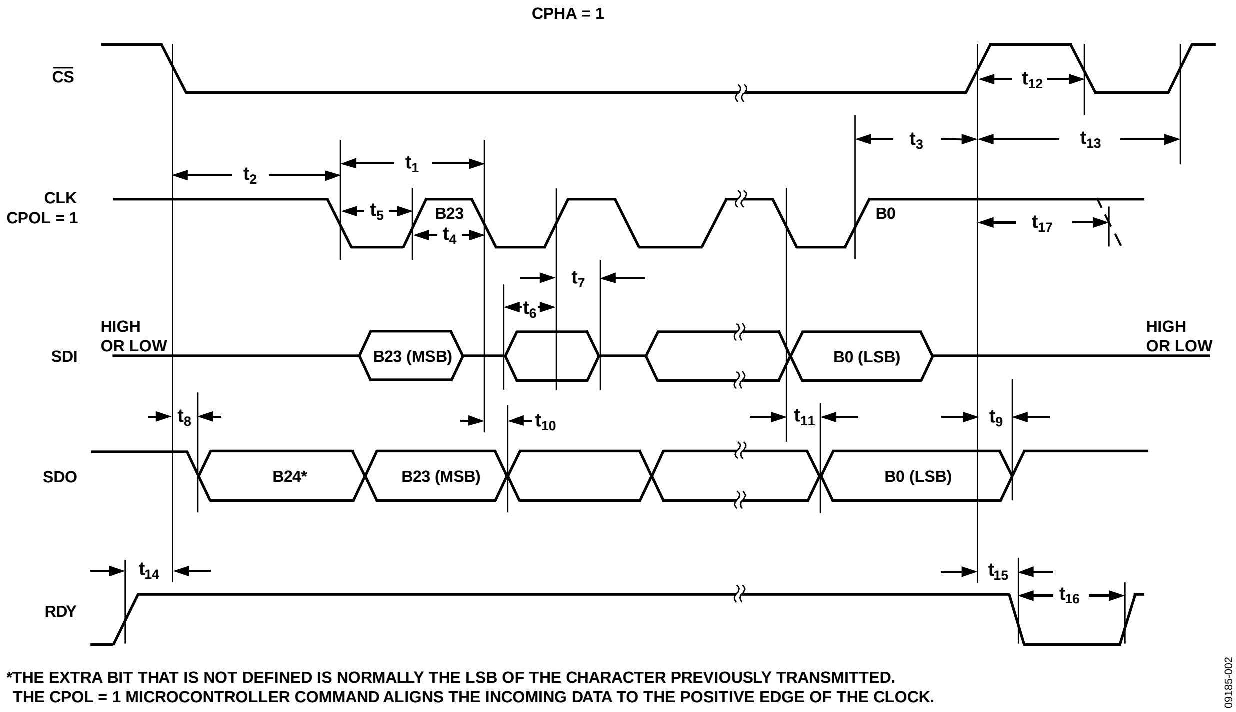

Figure 2. CPHA = 1 Timing Diagram

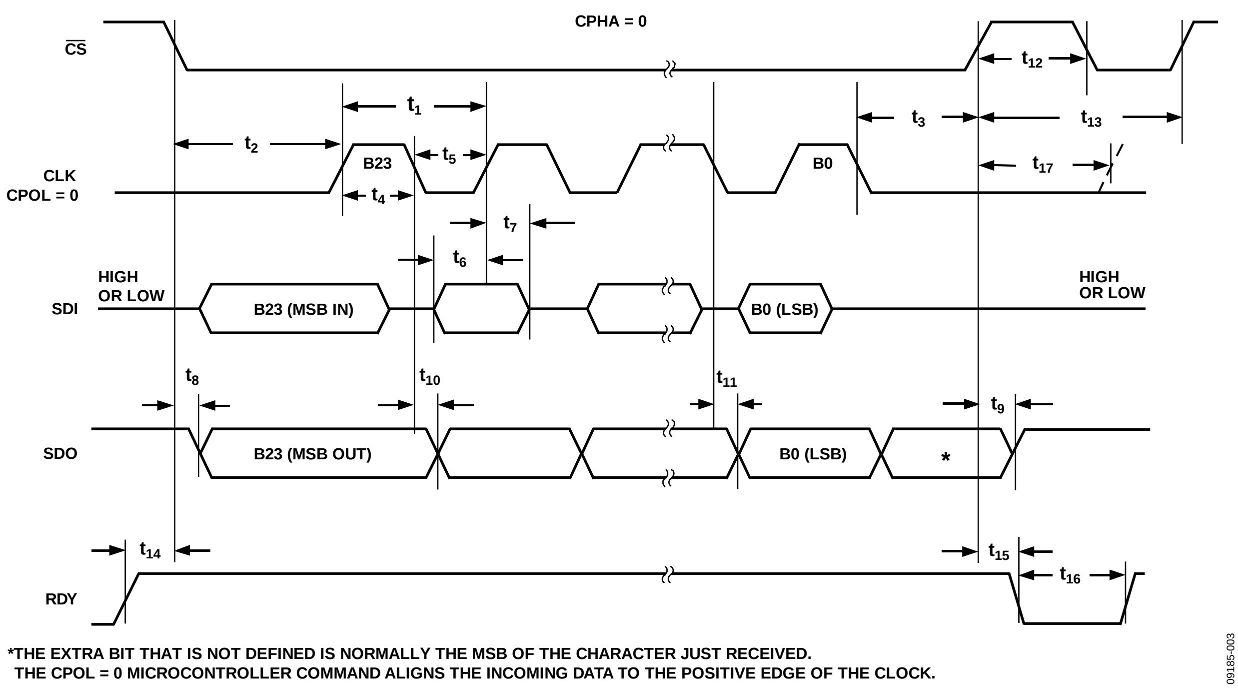

Figure 3. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	+0.3 V to −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
I_A, I_B, I_W	
Pulsed[1]	±2.5 mA
Continuous	±1.1 mA
Digital Input and Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range[2]	−40°C to +125°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance	
Junction-to-Ambient, θ_{JA}	150°C/W
Junction-to-Case, θ_{JC}	28°C/W
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Includes programming of nonvolatile memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

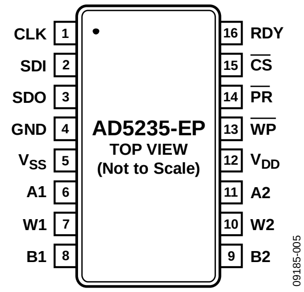

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
3	SDO	Serial Data Output. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 2 and Figure 3). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 2 and Figure 3). This previously shifted out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
4	GND	Ground Pin, Logic Ground Reference.
5	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. If V_{SS} is used in dual supply, it must be able to sink 35 mA for 30 ms when storing data to EEMEM.
6	A1	Terminal A of RDAC1.
7	W1	Wiper terminal of RDAC1. ADDR (RDAC1) = 0x0.
8	B1	Terminal B of RDAC1.
9	B2	Terminal B of RDAC2.
10	W2	Wiper terminal of RDAC2. ADDR (RDAC2) = 0x1.
11	A2	Terminal A of RDAC2.
12	V_{DD}	Positive Power Supply.
13	$\overline{WP}$	Optional Write Protect. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe. CMD_1 and COMD_8 refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high. Tie $\overline{WP}$ to V_{DD}, if not used.
14	$\overline{PR}$	Optional Hardware Override Preset. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the logic high transition. Tie $\overline{PR}$ to V_{DD}, if not used.
15	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active high open-drain output. Identifies completion of Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and $\overline{PR}$.

TYPICAL PERFORMANCE CHARACTERISTICS

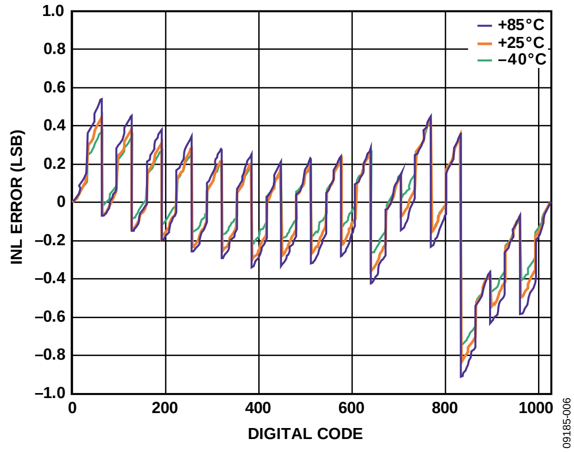

Figure 5. INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay

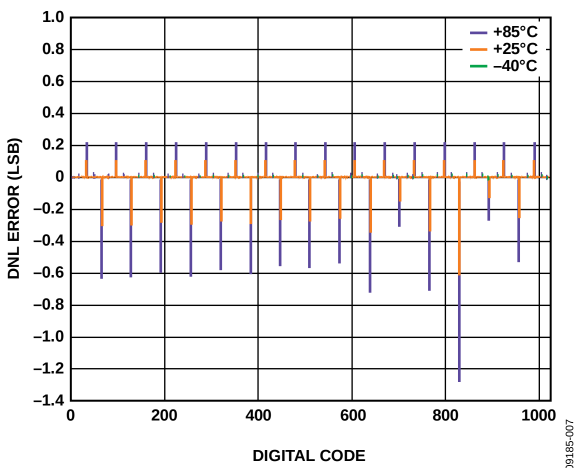

Figure 6. DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay

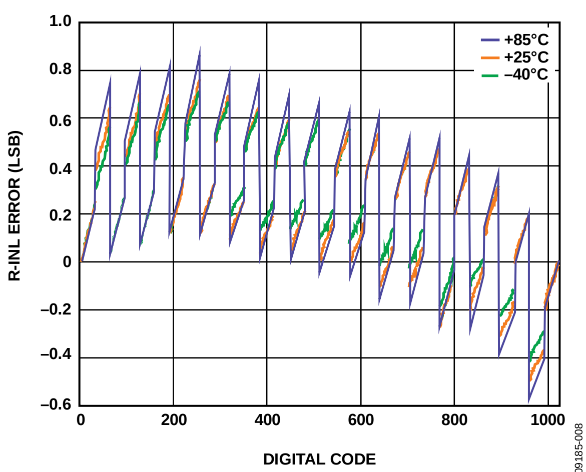

Figure 7. R-INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay

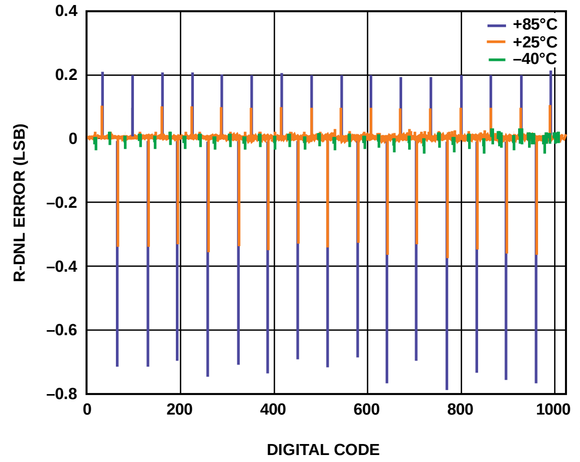

Figure 8. R-DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay

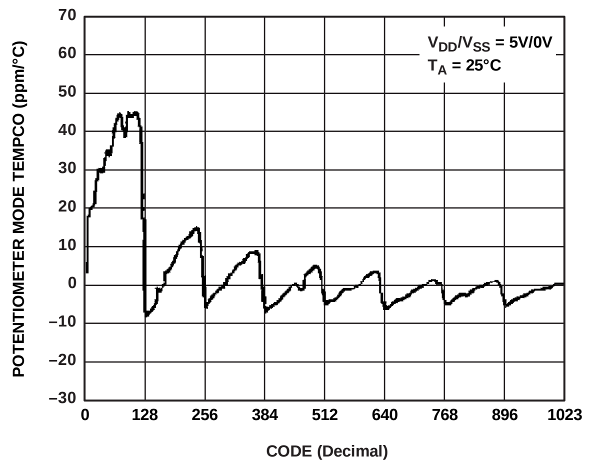

Figure 9. $(\Delta V_W/V_W)/\Delta T \times 10^6$ Potentiometer Mode Tempco

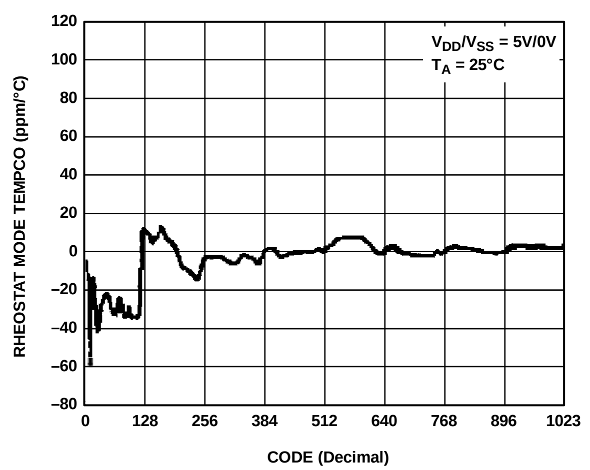

Figure 10. $(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$ Rheostat Mode Tempco

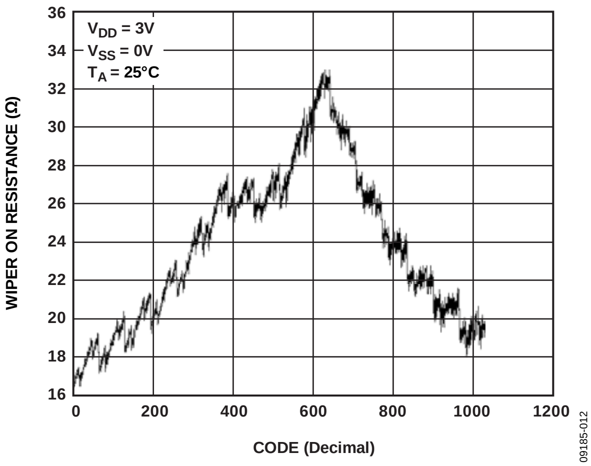

Figure 11. Wiper On Resistance vs. Code

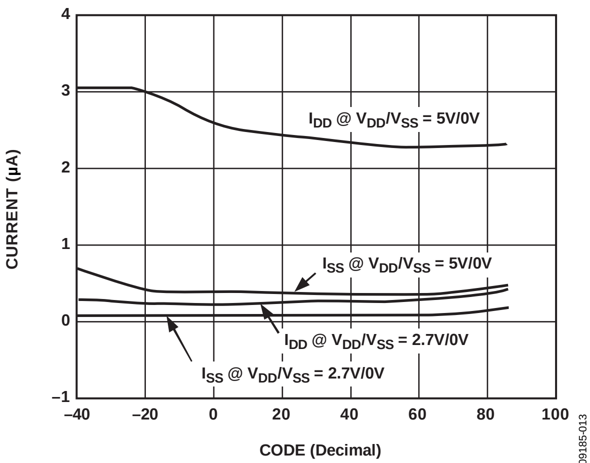

Figure 12. I_{DD} vs. Temperature

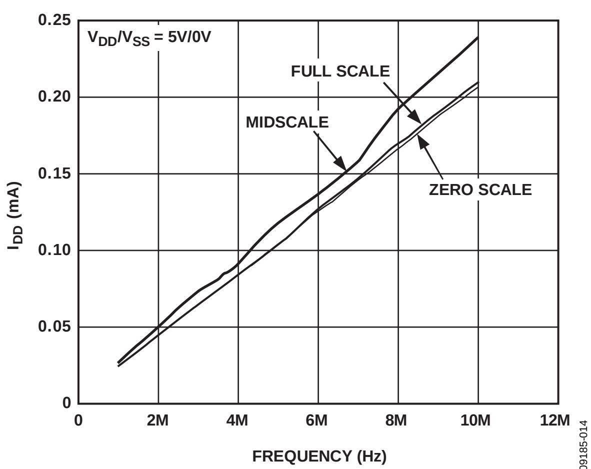

Figure 13. I_{DD} vs. Clock Frequency

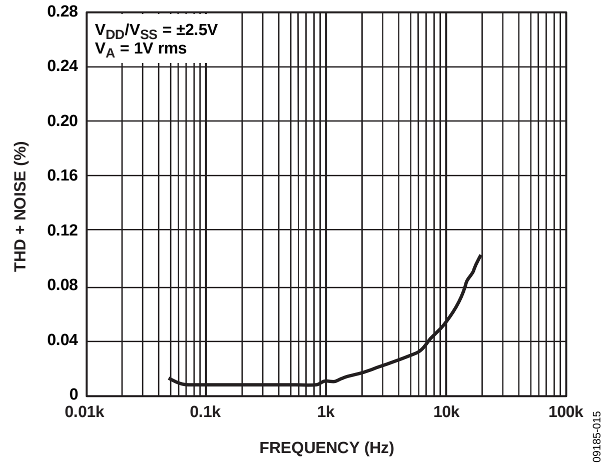

Figure 14. THD + Noise vs. Frequency

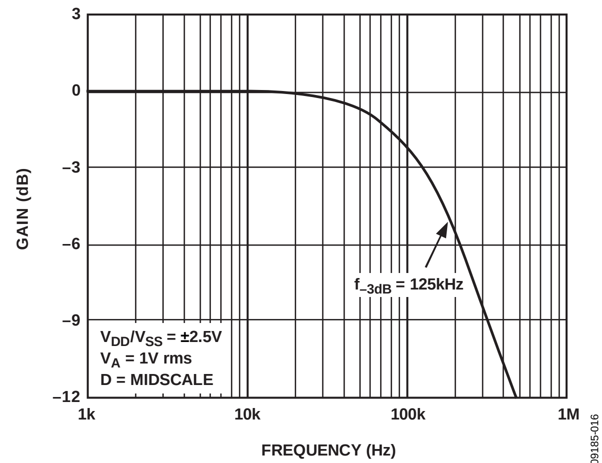

Figure 15. −3 dB Bandwidth vs. Resistance (See Figure 29)

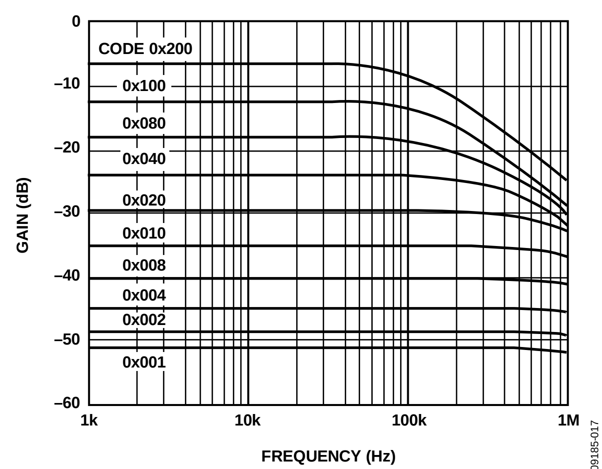

Figure 16. Gain vs. Frequency vs. Code (See Figure 29)

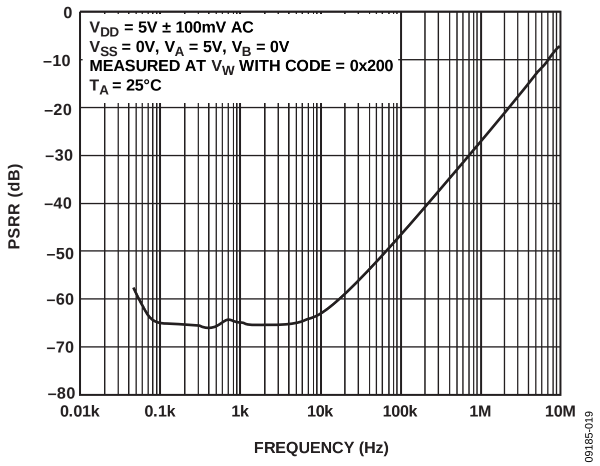

Figure 17. PSRR vs. Frequency

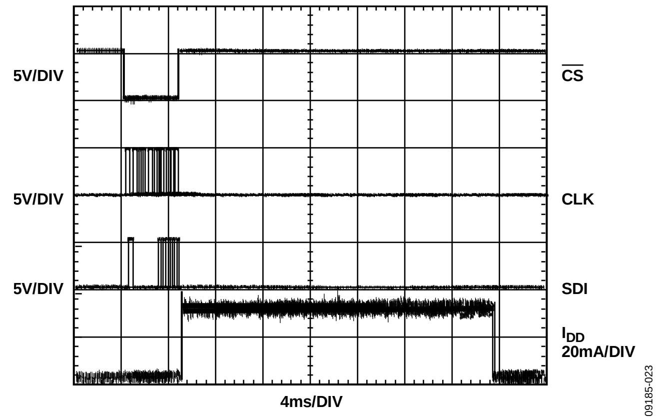

Figure 20. I_{DD} vs. Time when Storing Data to EEMEM

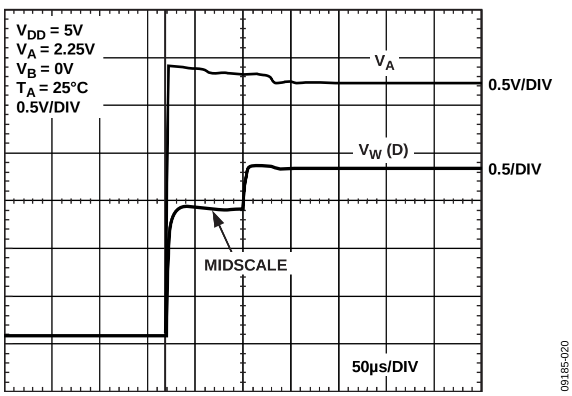

Figure 18. Power-On Reset, V_{DD} = 2.25 V, Previously Stored Code = 0x2AA

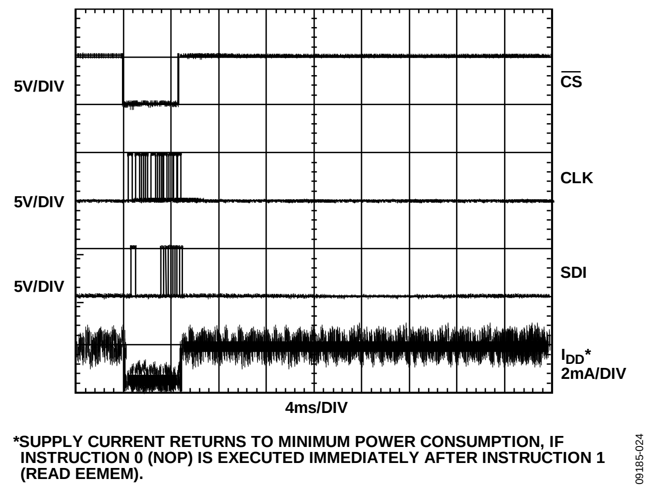

Figure 21. I_{DD} vs. Time when Restoring Data from EEMEM

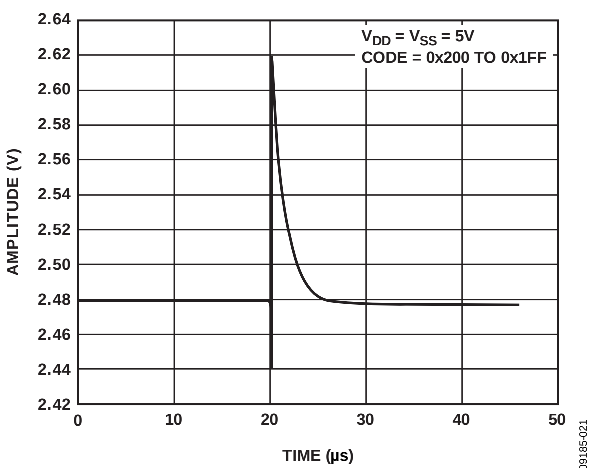

Figure 19. Midscale Glitch Energy, Code 0x200 to Code 0x1FF

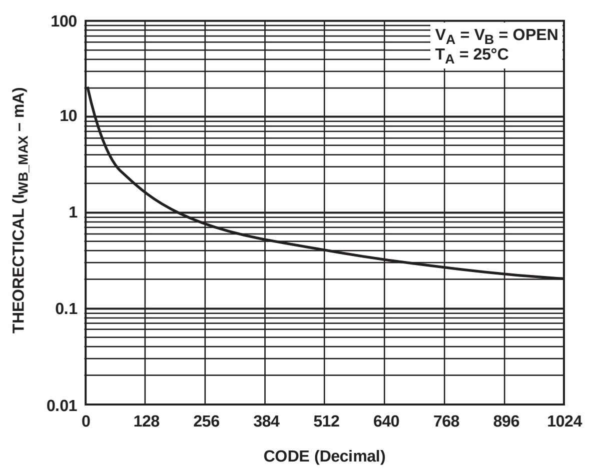

Figure 22. I_{WB_MAX} vs. Code.

TEST CIRCUITS

Figure 23 to Figure 33 define the test conditions used in the Specifications section.

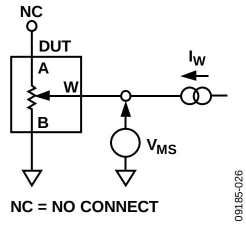

Figure 23. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

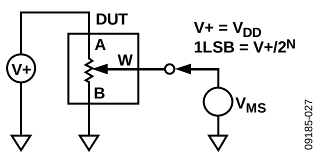

Figure 24. Potentiometer Divider Nonlinearity Error (INL, DNL)

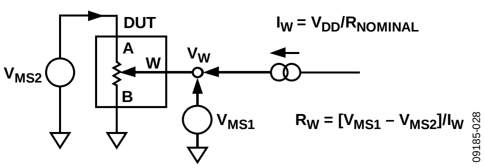

Figure 25. Wiper Resistance

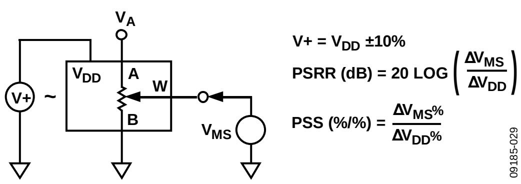

Figure 26. Power Supply Sensitivity (PSS, PSRR)

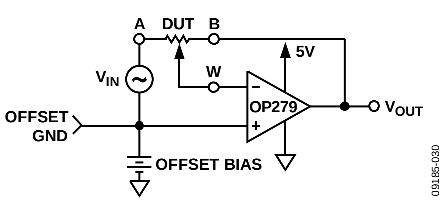

Figure 27. Inverting Gain

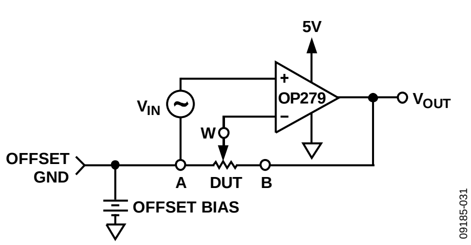

Figure 28. Noninverting Gain

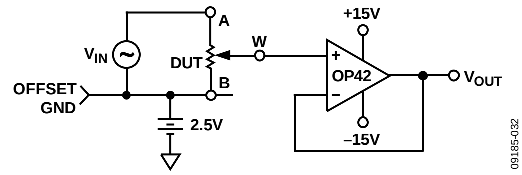

Figure 29. Gain vs. Frequency

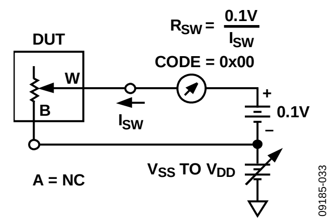

Figure 30. Incremental On Resistance

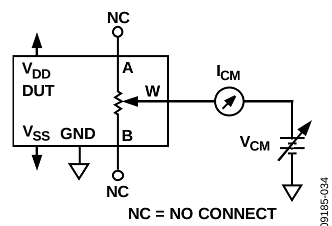

Figure 31. Common-Mode Leakage Current

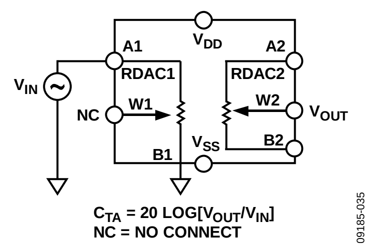

Figure 32. Analog Crosstalk

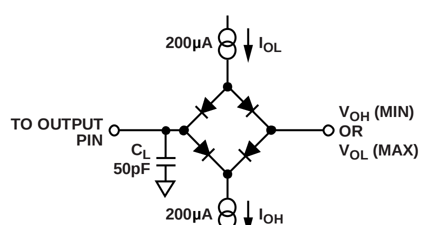

Figure 33. Load Circuit for Measuring V_{OH} and V_{OL} (The diode bridge test circuit is equivalent to the application circuit with $R_{PULL\text{-}UP}$ of 2.2 kΩ.)

OUTLINE DIMENSIONS

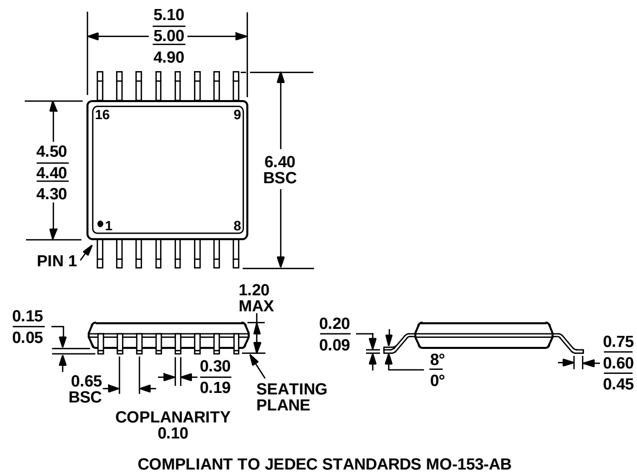

Figure 34. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option
AD5235BRU25-EP-RL7	25	–40°C to +125°C	16-Lead TSSOP	RU-16

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