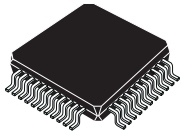
STLC3085

Integrated Pots Interface for Home Access Gateway and WLL

Preliminary Data

Features

- Monochip SLIC optimised for WLL & VoIP applications
- Implement all key features of the borsht function
- Single supply (4.5 to 12V)
- Built in DC/DC Converter controller
- Soft battery reversal with programmable transition time
- On-hook transmission
- Programmable off-hook detector threshold
- Integrated ringing
- Integrated ring trip
- Parallel control interface (3.3V logic level)
- Programmable constant current feed
- Surface mount package
- Integrated thermal protection
- Dual gain value option
- Automatic recognition flyback and buckboost configuration
- BCDIIIS 90V technology
- -40 to +85°C operating range



TQFP44

Description

The STLC3085 is a SLIC device specifically designed for WLL (Wireless Local Loop), and ISDN Terminal Adaptors and VoIP applications. One of the distinctive characteristic of this device is the ability to operate with a single supply voltage (from +4.5V to +12V) and self generate the negative battery by means of an on chip DC/DC converter controller that drives an external MOS switch.

The battery level is properly adjusted depending on the operating mode. A useful characteristic for these applications is the integrated ringing generator.

The control interface is a parallel type with open drain output and 3.3V logic levels. Constant current feed can be set from 20mA to 25mA.

Off-hook detection threshold is programmable from 5mA to 9mA.

The device, developed in BCDIIIS technology (90V process), operates in the extended temperature range and integrates a thermal protection that sets the device in power down when Tj exceeds 140°C..

Order codes

Part number	Temp range, °C	Package	Packing
E-STLC3085 (*)	-40 to 85	TQFP44	Tube

(*) ECOPACK® (see *Section 5*)

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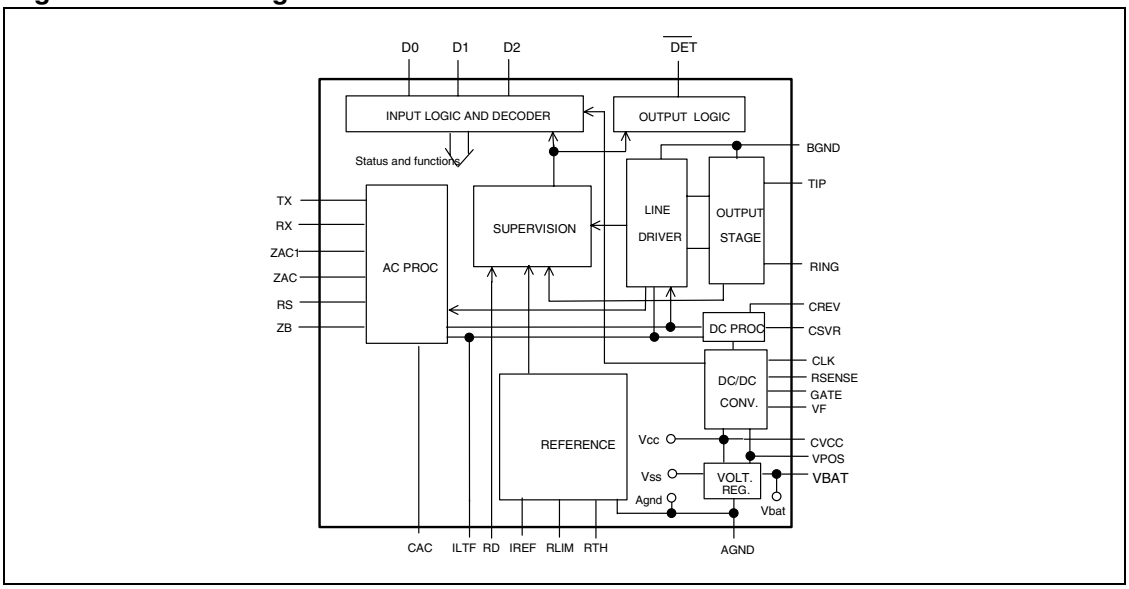
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1 Block diagram and pin description

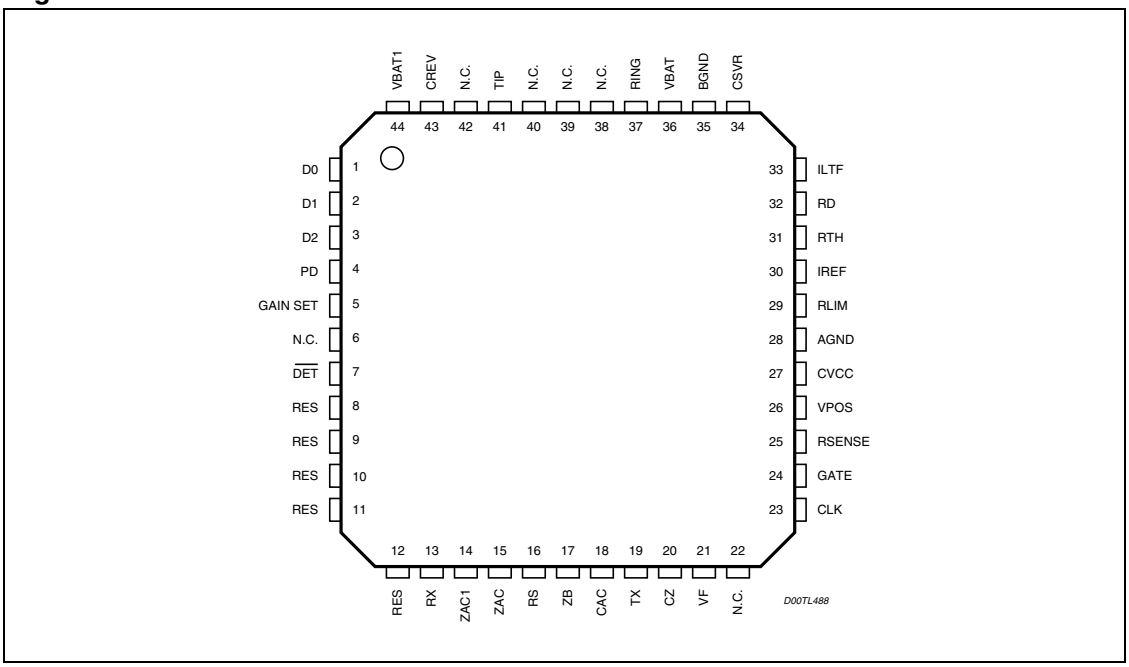
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin connection

Figure 2. Pin connection



1.3 Pin description

Table 1. Pin description

N°	Pin	Function
1	D0	Control Interface: input bit 0.
2	D1	Control Interface: input bit 1.
3	D2	Control interface: input bit 2.
4	PD	Power Down input. Normally connected to CVCC (or to logic level high).
5	Gain SET	Control gain interface: 0 Level R_{xgain} = 0dB T_{xgain} = -6dB 1 Level R_{xgain} = +6dB T_{xgain} = -12dB
6,22,38, 39,40,42	NC	Not connected.
7	$\overline{DET}$	Logic interface output of the supervision detector (active low).
8	RESERVED	Connected to GND
9	RESERVED	Connected to GND
10	RESERVED	Connected to GND
11	RESERVED	Left open.
12	RESERVED	Connected to GND
13	RX	4 wire input port (RX input); 300KΩ input impedance. This signal is referred to AGND. If connected to single supply CODEC output it must be DC decoupled with proper capacitor.
14	ZAC1	RX buffer output (the AC impedance is connected from this node to ZAC).
15	ZAC	AC impedance synthesis.
16	RS	Protection resistors image (the image resistor is connected from this node to ZAC).
17	ZB	Balance Network for 2 to 4 wire conversion (the balance impedance ZB is connected from this node to AGND. ZA impedance is connected from this node to ZAC1).
18	CAC	AC feedback input, AC/DC split capacitor (CAC).
19	TX	4 wire output port (TX output). The signal is referred to AGND. If connected to single supply CODEC input it must be DC decoupled with proper capacitor.
20	CZ	Fly-Back compensation
21	VF	Feedback input for DC/DC converter controller.
23	CLK	Power Switch Controller Clock (typ. 125KHz). This pin can also be connected to CVCC or AGND. When the CLK pin is connected to CVCC an internal auto-oscillation is internally generated and it is used instead of the external clock. When the CLK pin is connected to AGND, the GATE output is disabled.
24	GATE	Driver for external Power MOS transistor (P-chanell in Buck-boost configuration, N-channel in Fly-back configuration).
25	RSENSE	Voltage input for current sensing. RSENSE resistor should be connected close to this pin and VPOS pin (Buck-boost) or GND (Fly-back). The PCB layout should minimize the extra resistance introduced by the copper tracks.

Table 1. Pin description (continued)

N°	Pin	Function
26	VPOS	Positive supply input.
27	CVCC	Internal positive voltage supply filter.
28	AGND	Analog Ground, must be shorted with BGND.
29	RLIM	Constant current feed programming pin (via RLIM). RLIM should be connected close to this pin and AGND pin to avoid noise injection.
30	IREF	Internal bias current setting pin. RREF should be connected close to this pin and AGND pin to avoid noise injection.
31	RTH	Off-hook threshold programming pin (via RTH). RTH should be connected close to this pin and AGND pin to avoid noise injection.
32	RD	DC feedback and ring trip input. RD should be connected close to this pin and AGND pin to avoid noise injection.
33	ILTF	Transversal line current image output.
34	CSVR	Battery supply filter capacitor.
35	BGND	Battery Ground, must be shorted with AGND.
36	VBAT	Regulated battery voltage self generated by the device via DC/DC converter. Must be shorted to VBAT1.
37	RING	2 wire port; RING wire (Ib is the current sunk into this pin).
41	TIP	2 wire port; TIP wire (Ia is the current sourced from this pin).
43	CREV	Reverse polarity transition time control. A proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. This is the same transition time used to shape the "trapezoidal ringing" during ringing injection.
44	VBAT1	Frame connection. Must be shorted to VBAT.

1.4 Thermal data

Table 2. Thermal data

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Typ.	60	°C/W

2 Electrical specification

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{pos}	Positive Supply Voltage	-0.4 to +13	V
A/BGND	AGND to BGND	-1 to +1	V
V_{dig}	Pin D0, D1, D2, $\overline{DET}$	-0.4 to 5.5	V
T_j	Max. junction Temperature	150	°C
V_{btot}	Vbtot=|Vpos|+|Vbat|. (Total voltage applied to the device supply pins).	85	V
ESD RATING	Human Body Model	±1750	V
	Charged Device Model	±500	V

2.2 Operating range

Table 4. Operating range

Symbol	Parameter	Value	Unit
V_{pos}	Positive Supply Voltage	4.5 to +12	V
A/BGND	AGND to BGND	-100 to +100	mV
V_{dig}	Pin D0, D1, D2, $\overline{DET}$, PD	-0.25 to 5.25	V
T_{op}	Ambient Operating Temperature Range	-40 to +85	°C
V_{bat} (1)	Self Generated Battery Voltage	-64 max.	V

(1) Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 shall be selected in order to fulfil the a.m limits (see *Table 10*)

2.3 Electrical characteristics

Table 5. Electrical characteristics

Test conditions: V_{pos} = 6.0V, AGND = BGND, Normal Polarity, T_{amb} = 25°C.

External components as listed in the "Typical Values" column of EXTERNAL COMPONENTS Table.

Note: Testing of all parameter is performed at 25°C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_{lohi}	Line voltage	Il = 0, HI-Z (High impedance feeding) T_{amb} = 0 to 85°C	40	46		V
V_{lohi}	Line voltage	Il = 0, HI-Z (High impedance feeding) T_{amb} = -40 to 85°C	38	44		V
V_{loa}	Line voltage	Il = 0, ACTIVE T_{amb} = 0 to 85°C	31	38		V
V_{loa}	Line voltage	Il = 0, ACTIVE T_{amb} = -40 to 85°C	29	35		V
Ilim	Lim. current programming range	ACTIVE mode	20		25	mA
Ilima	Lim. current accuracy	ACTIVE mode. Rel. to programmed value 20mA to 25mA	-10		10	%
Rfeed HI	Feeding resistance	HI-Z (High Impedance feeding)	2.4		3.6	kΩ
AC CHARACTERISTICS						
L/T	Long. to transv. (see Appendix for test circuit)	Rp = 50Ω, 1% tol., ACTIVE N. P., R_L = 600Ω (1) f = 300 to 3400Hz	50	58		dB
T/L	Transv. to long. (see Appendix for test circuit)	Rp = 50Ω, 1% tol., ACTIVE N. P., R_L = 600Ω (1) f = 300 to 3400Hz	40	45		dB
T/L	Transv. to long. (see Appendix for test circuit)	Rp = 50Ω, 1% tol., ACTIVE N. P., R_L = 600Ω (1) f = 1kHz	48	53		dB
2WRL	2W return loss	300 to 3400Hz, ACTIVE N. P., R_L = 600Ω (1)	22	26		dB
THL	Trans-hybrid loss	300 to 3400Hz, 20Log|VRX/VTX|, ACTIVE N. P., R_L = 600Ω (1)	30			dB

Table 5. Electrical characteristics (continued)

Test conditions: V_{pos} = 6.0V, AGND = BGND, Normal Polarity, T_{amb} = 25°C.

External components as listed in the "Typical Values" column of EXTERNAL COMPONENTS Table.

Note: Testing of all parameter is performed at 25°C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Ovl	2W overload level	at line terminals on ref. imped. ACTIVE N. P., R_L = 600Ω (1)	3.2			dBm
TXoff	TX output offset	ACTIVE N. P., R_L = 600Ω (1)	-250		250	mV
G24	Transmit gain abs.	0dBm @ 1020Hz, ACTIVE N. P., R_L = 600Ω (1)	-6.4		-5.6	dB
G42	Receive gain abs.	0dBm @ 1020Hz, ACTIVE N. P., R_L = 600Ω (1)	-0.4		0.4	dB
G24f	TX gain variation vs. freq.	rel. 1020Hz; 0dBm, 300 to 3400Hz, ACTIVE N. P., R_L = 600Ω (1)	-0.12		0.12	dB
G24f	RX gain variation vs. freq.	rel. 1020Hz; 0dBm, 300 to 3400Hz, ACTIVE N. P., R_L = 600Ω (1)	-0.12		0.12	dB
V2Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600Ω (1) T_{amb} = 0 to +85°C		-73	-68	dBmp
V2Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600Ω (1) T_{amb} = -40 to +85°C		-68		dBmp
V4Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600Ω (1) T_{amb} = 0 to +85°C		-75	-70	dBmp
V4Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600Ω (1) T_{amb} = -40 to +85°C		-75		dBmp
Thd	Total Harmonic Distortion	ACTIVE N. P., R_L = 600Ω (1)			-44	dB
CLKfreq	CLK operating range		-10%	125	10%	kHz
RING						
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 2REN; Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = 0 to +85°C	41	45		Vrms

Table 5. Electrical characteristics (continued)

Test conditions: V_{pos} = 6.0V, AGND = BGND, Normal Polarity, T_{amb} = 25°C.

External components as listed in the "Typical Values" column of EXTERNAL COMPONENTS Table.

Note: Testing of all parameter is performed at 25°C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 2REN; Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = -40 to +85°C	40	44		Vrms
DETECTORS						
IOFFTHA	Off/hook current threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFTHA	Off/hook loop resistance threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			3.4	kΩ
IONTHA	On/hook current threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHA	On/hook loop resistance threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	8			kΩ
IOFFTHI	Off/hook current threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFFTHI	Off/hook loop resistance threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			800	W
IONTHI	On/hook current threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHI	On/hook loop resistance threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	8			kΩ
Irt	Ring Trip detector threshold range	RING	20		50	mA
Irta	Ring Trip detector threshold accuracy	RING	-15		15	%
Trtd	Ring trip detection time	RING		TBD		ms
Td	Dialling distortion	ACTIVE	-1		1	ms
Rlrt (2)	Loop resistance				500	W
ThAl	Tj for th. alarm activation			160		°C
DIGITAL INTERFACE INPUTS: D0, D1, D2, PD, CLK OUTPUTS: $\overline{DET}$						
Vih	In put high voltage		2			V
Vil	Input low voltage				0.8	V

Table 5. Electrical characteristics (continued)

Test conditions: V_{pos} = 6.0V, AGND = BGND, Normal Polarity, T_{amb} = 25°C.

External components as listed in the "Typical Values" column of EXTERNAL COMPONENTS Table.

Note: Testing of all parameter is performed at 25°C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Iih	Input high current		-10		10	µA
Iil	Input low current		-10		10	µA
Vol	Output low voltage	Iol = 1mA			0.45	V
PSRR AND POWER CONSUMPTION						
PSERRC	Power supply rejection Vpos to 2W port	Vripple = 100mVrms 50 to 4000Hz	26	36		dB
Ivpos	Vpos supply current @ ii = 0	HI-Z On-Hook ACTIVE On-Hook, RING (line open)		13 50 55	25 80 90	mA mA mA
Ipk (3)	Peak current limiting accuracy	RING Off-Hook RSENSE = 130mΩ	-20%	770	+20%	mApk

(1) R_L: Line Resistance

(2) R_{lrt} = Maximum loop resistance (incl. telephone) for correct ring trip detection.

(3) Buck Boost configuration.

3 Functional description

The STLC3085 is a device specifically developed for WLL VoIP and ISDN-TA applications.

It is based on a SLIC core, on purpose optimised for these applications, with the addition of a DC/DC converter controller to fulfil the WLL and ISDN-TA design requirements.

The SLIC performs the standard feeding, signalling and transmission functions.

It can be set in three different operating modes via the D0, D1, D2 pins of the control logic interface (0 to 3.3V logic levels). The loop status is carried out on the $\overline{DET}$ pin (active low).

The $\overline{DET}$ pin is an open drain output to allow easy interfacing with both 3.3V and 5V logic levels.

The four possible SLIC's operating modes are:

- Power Down
- High Impedance Feeding (HI-Z)
- Active
- Ringing

Table 6 shows how to set the different SLIC operating modes.

Table 6. SLIC operating modes.

PD	D0	D1	D2	Operating Mode
0	0	0	X	Power Down
1	0	0	X	H.I. Feeding (HI-Z)
1	0	1	0	Active Normal Polarity
1	0	1	1	Active Reverse Polarity
				Not used
				Not used
1	1	0	0/1	Ring (D2 bit toggles @ fring)

3.1 DC/DC converter

The DC/DC converter controller is driving an external power MOS transistor N-Ch plus transformer (Flyback configuration) or P-Ch plus inductor (BuckBoost configuration), in order to generate the negative battery voltage needed for device operation.

The DC/DC converter controller is synchronised with an external CLK (125KHz typ.) or with an internal clock generated when the pin CLK is connected to CVCC. One R_{sense} in series to PGND supply (FlyBack) or to VPOS supply (BuckBoost) allows to fix the maximum allowed input peak current.

This feature is implemented in order to avoid overload on Vpos supply in case of line transient (ex. ring trip detection). Typ. value of 130mΩ guarantees an average current consumption from Vpos < 600mA for BuckBoost configuration and < 1.25A for Fly- Back configuration.

Typ. value of 220mΩ guarantees an average current consumption from Vpos < 800mA for Fly-Back configuration

The self generated battery voltage is set to a predefined value in on-hook state.

This value can be adjusted via one external resistor (RF1) and it is typical -46V. When RING mode is selected this value is increased to -64V typ.

Once the line goes in off-hook condition, the DC/DC converter automatically adjusts the generated battery voltage in order to feed the line with a fixed DC current (programmable via RLIM) optimising the power dissipation.

3.2 Operating modes

3.2.1 Power down

When this mode is selected the SLIC is switched off and the TIP and RING pins are in high impedance. Also the line detectors are disabled therefore the off-hook condition cannot be detected. This mode can be selected in emergency condition when it is necessary to cut any current delivered to the line. This mode is also forced by STLC3085 in case of thermal overload (T_j > 140°C).

In this case the device goes back to the previous status as soon as the junction temperature decrease under the hysteresis threshold.

No AC transmission is possible

3.2.2 High impedance feeding (HI-Z)

This operating mode is normally selected when the telephone is in on-hook in order to monitor the line status keeping the power consumption at the minimum.

The output voltage in on-hook condition is equal to the self generated battery voltage (-46V typ).

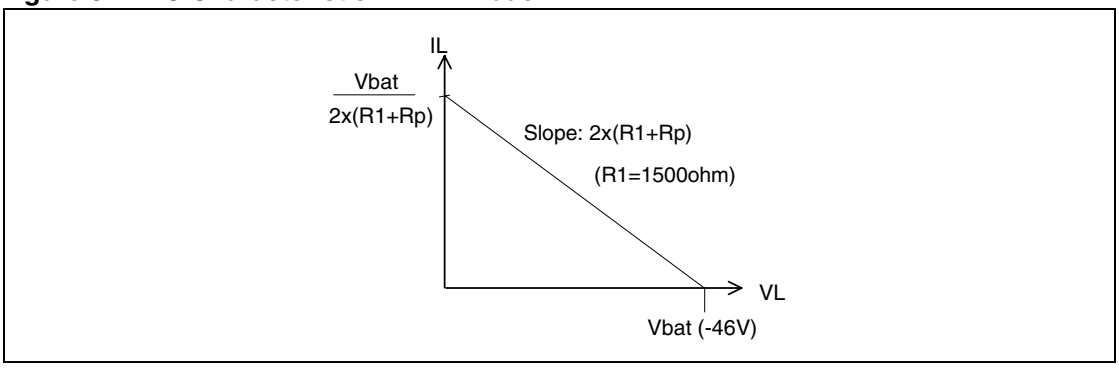
When off-hook occurs the $\overline{DET}$ becomes active (low logic level).

The off-hook threshold in HI-Z mode is the same value as programmed in ACTIVE mode.

The DC characteristic in HI-Z mode is just equal to the self generated battery with 2x(1600Ω+Rp) in series (see *Figure 3*), where Rp is the external protection resistance.

No AC transmission is possibile.

Figure 3. DC Characteristic in HI-Z Mode.



3.2.3 Active

3.2.3.1 DC characteristics & supervision

When this mode is selected the STLC3085 provides both DC feeding and AC transmission.

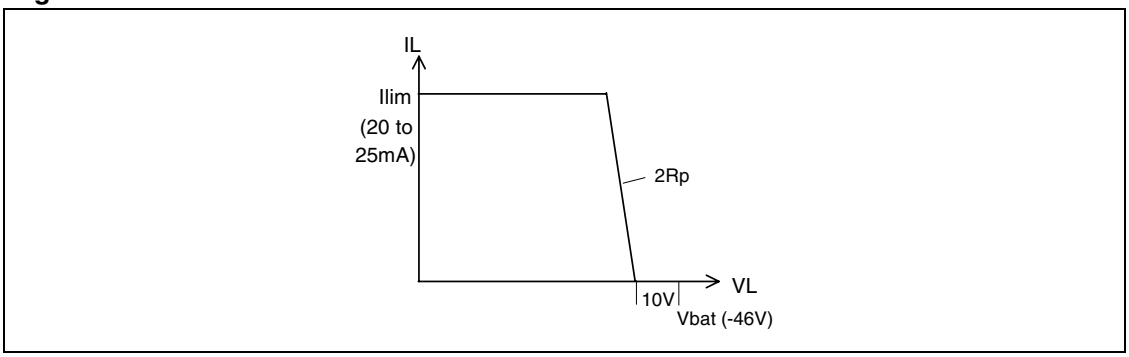
The STLC3085 feeds the line with a constant current fixed by RLIM (20mA to 25mA range). The on-hook voltage is typically 38V allowing on-hook transmission; the self generated Vbat is -46V typ.

If the loop resistance is very high and the line current cannot reach the programmed constant current feed value, the STLC3085 behaves like a 38V voltage source with a series impedance equal to the protection resistors 2xRp (typ. 2x50Ω). *Figure 4* shows the typical DC characteristic in ACTIVE mode.

The line status (on/off hook) is monitored by the SLIC'S supervision circuit. The off-hook threshold can be programmed via the external resistor RTH in the range from 5mA to 9mA.

Independently on the programmed constant current value, the TIP and RING buffers have a current source capability limited to 65mA typ.

Figure 4. DC characteristic in ACTIVE mode



Moreover the power available at Vbat is controlled by the DC/DC converter that limits the peak current drawn from the Vpos supply. The maximum allowed current peak is set by R_{SENSE} resistor.

3.2.3.2 AC characteristics

The SLIC provides the standard SLIC transmission functions:

Once in active mode the SLIC can operate with two different Tx, Rx Gain. Setting properly by the Gain set control bit (see *Table 7*).

Table 7. Gain Set in Active Mode

Gain set	4 to 2 wire Gain	2 to 4 wire Gain	Impedance Synthesis Scale Factor
0	0dB	-6dB	x 50
1	+6dB	-12dB	x 25

- **Input impedance synthesis:** can be real or complex and is set by a scaled (x50 or x25) external ZAC impedance.

- **Transmit and receive:** The AC signal present on the 2W port (TIP/RING) is transferred to the TX output with a -6dB or -12dB gain and from the RX input to the 2W port with a 0dB or +6dB gain.
- **2 to 4 wire conversion:** The balance impedance can be real or complex, the proper cancellation is obtained by means of two external impedance ZA and ZB

Once in Active mode (D1=1) the SLIC can operate in different states setting properly D0 and D2 control bits (see also *Table 8*).

Table 8. SLIC states in ACTIVE mode

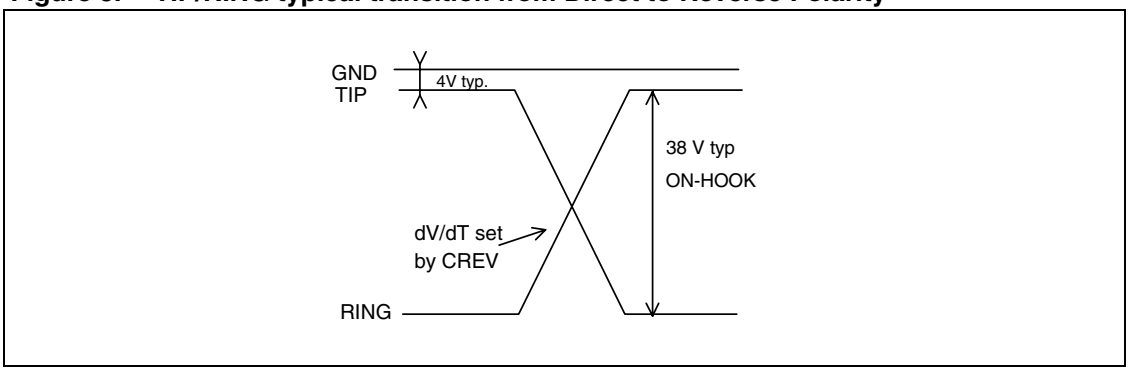
D0	D1	D2	Operating Mode
0	1	0	Active Normal Polarity
0	1	1	Active Reverse Polarity

3.2.3.3 Polarity reversal

The D2 bit controls the line polarity, the transition between the two polarities is performed in a "soft" way. This means that the TIP and RING wire exchange their polarities following a ramp transition (see *Figure 5*).

The transition time is controlled by an external capacitor CREV. This capacitor is also setting the shape of the ringing trapezoidal waveform. When the control pins set battery reversal the line polarity is reversed with a proper transition time set via an external capacitor (CREV).

Figure 5. TIP/RING typical transition from Direct to Reverse Polarity



3.2.4 Ringing

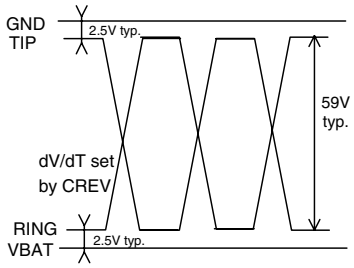
When this mode is selected STLC3085 self generate an higher negative battery (-64V typ.) in order to allow a balanced ringing signal of typically 59Vpeak.

In this condition both the DC and AC feedback loop are disabled and the SLIC line drivers operate as voltage buffers. The ring waveform is obtained toggling the D2 control bit at the desired ring frequency. This bit in fact controls the line polarity (0=direct; 1= reverse).

As in the ACTIVE mode the line voltage transition is performed with a ramp transition, obtaining in this way a trapezoidal balanced ring waveform (see *Figure 6*).

The shaping is defined by the CREV external capacitor.

Figure 6. TIP/RING typical ringing waveform



Selecting the proper capacitor value it is possible to get different crest factor values.

The following table shows the crest factor values obtained with a 20Hz and 25Hz ring frequency and with 1REN. These value are valid either with European or USA specification:

Table 9.

CREV	CREST FACTOR @20Hz	CREST FACTOR @25Hz
22nF	1.2	1.26
27nF	1.25	1.32
33nF	1.33	Not significant (1)

(1) Distorsion already less than 10%.

The ring trip detection is performed sensing the variation of the AC line impedance from on hook (relatively high) to off-hook (low). This particular ring trip method allows to operate without DC offset superimposed on the ring signal and therefore obtaining the maximum possible ring level on the load starting from a given negative battery.

It should be noted that such a method is optimised for operation on short loop applications and may not operate properly in presence of long loop applications (> 500Ω).

Once ring trip is detected, the $\overline{DET}$ output is activated (logic level low), at this point the card controller or a simple logic circuit should stop the D2 toggling in order to effectively disconnect the ring signal and then set the STLC3085 in the proper operating mode (normally ACTIVE).

3.2.4.1 Ring level in presence of more telephone in parallel

As already mentioned above the maximum current that can be drawn from the Vpos supply is controlled and limited via the external RSENSE.

This will limit also the power available at the self generated negative battery.

If for any reason the ringer load is too low the self generated battery will drop in order to keep the power consumption to the fixed limit and therefore also the ring voltage level will be reduced.

In the typical Buck Boost configuration with R_{SENSE} = 130mΩ the peak current from Vpos is limited to about 770mA, which correspond to an average current of 600mA max. In this condition the STLC3085 can drive up to 2REN with a ring frequency fr=25Hz (1REN = 1800Ω + 1.0μF, European standard).

In Fly-Back configuration the value of R_{SENSE} = 220mΩ guarantees match both European and USA standards.

3.2.5 Layout recommendation

A properly designed PCB layout is a basic issue to guarantee a correct behaviour and good noise performances.

Particular care must be taken on the ground connection and in this case the star configuration allows surely to avoid possible problems (see Application Diagram *Figure 7* and *Figure 8*).

The ground of the power supply (VPOS) has to be connected to the center of the star, let's call this point SYSTEM-GND. This point should show a resistance as low as possible, that means it should be a ground plane.

In particular to avoid noise problems the layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (ex: RD, IREF, RTH, RLIM, VF). As a first reccomendation the components CV, L, T1, D1, CVPOS, RSENSE should be kept as close as possible to each other and isolated from the other components.

Additional improvements can be obtained:

- decoupling the center of the star from the analog ground of STLC3085 using small chokes.
- adding a capacitor in the range of 100nF between VPOS and AGND in order to filter the switch frequency on VPOS.

3.2.6 External components list

In order to properly define the external components value the following system parameters have to be defined:

- The AC input impedance shown by the SLIC at the line terminals "Zs" to which the return loss measurement is referred. It can be real (typ. 600Ω) or complex.
- The AC balance impedance, it is the equivalent impedance of the line "Zl" used for evaluation of the trans-hybrid loss performances (2/4 wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The slope of the ringing waveform "$\Delta V_{TR}/\Delta_T$ ".
- The value of the constant current limit current "Ilim".
- The value of the off-hook current threshold "I_{TH}".
- The value of the ring trip rectified average threshold current "I_{RTH}".
- The value of the required self generated negative battery "V_{BATR}" in ring mode (max value is 64V). This value can be obtained from the desired ring peak level + 5V.
- The value of the maximum current peak drawn from Vpos "IPK".

Table 10. External Components

Name	Function	Formula	Typ. Value
BUCKBOOST CONFIGURATION			
RREF	Bias setting current	RREF = 1.3/Ibias Ibias = 50μA	26kΩ 1%
CSVR	Negative Battery Filter	CSVR = 1/(2π · fp · 1.8MΩ) fp = 50Hz	1.5nF 10% 100V

Table 10. External Components (continued)

Name	Function	Formula	Typ. Value
RD	Ring Trip threshold setting resistor	RD = 100/I_{RTH} 2KΩ < RD < 5KΩ	4.12kΩ 1% @ IRTH = 24mA
CAC	AC/DC split capacitance		22µF 20% 15V @ RD = 4.12kΩ
RP	Line protection resistor	Rp > 30Ω	50Ω 1%
RLIM	Current limiting programming	RLIM = 1300/Ilim 32.5kΩ < RLIM < 65kΩ	52.3kΩ 1% @ Ilim = 25mA
RTH	Off-hook threshold programming (ACTIVE mode)	RTH = 290/I_{TH} 27kΩ < RTH < 52kΩ	32.4kΩ 1% @I_{TH} = 9mA
CREV	Reverse polarity transition time programming	CREV = ((1/3750) · $\Delta T/\Delta V_{TR}$)	22nF 10% 10V @ 12V/ms
RDD	Pull up resistors		100kΩ
CVCC	Internally supply filter capacitor		100nF 20% 10V
CVpos(1)	Positive supply filter capacitor with low impedance for switch mode power supply		100µF
CV(2)	Battery supply filter capacitor with low impedance for switch mode power supply		100µF 20% 100V
CVB	High frequency noise filter		470nF 20% 100V
CRD(3)	High frequency noise filter		100nF 10% 15V
Q1	DC/DC converter switch P ch. MOS transistor	RDS(ON)≤1.2Ω,VDS = -100V Total gate charge=20nC max. with VGS=4.5V and VDS=1V ID>500mA	Possible choiches: IRF9510 or IRF9520 or IRF9120 or equivalent
D1	DC/DC converter series diode	V_r > 100V, t_{RR} ≤ 50ns	SMBYW01-200 or equivalent
RSENSE	DC/DC converter peak current limiting	R_{SENSE} = 100mV/I_{PK}	130mΩ @I_{PK} = 770mA
RF1	Negative battery programming level	250KΩ<RF1<270KΩ	270kΩ 1% @ V_{BATR} = -64V
RF2	Negative battery programming level		9.1kΩ 1%
L(4)	DC/DC converter inductor	DC resistance ≤ 0.1Ω	L=100µH SUMIDA CDRH125 or equivalent

FLY-BACK CONFIGURATION

RREF	Bias setting current	RREF = 1.3/Ibias; Ibias = 50µA	26kΩ 1%

Table 10. External Components (continued)

Name	Function	Formula	Typ. Value
CSVR	Negative Battery Filter	CSVR = 1/(2π · fp · 1.8MΩ) fp = 50Hz	1.5nF 10% 100V
RD	Ring Trip threshold setting resistor	RD = 100/I_{RTH} 2KΩ < RD < 5KΩ	4.12kΩ 1% @ IRTH = 24mA
CAC	AC/DC split capacitance		22µF 20% 15V @ RD = 4.12kΩ
RP	Line protection resistor	Rp > 30Ω	50Ω 1%
RLIM	Current limiting programming	RLIM = 1300/Ilim 52.3kΩ < RLIM < 65kΩ	52.3kΩ 1% @ Ilim = 25mA
RTH	Off-hook threshold programming (ACTIVE mode)	RTH = 290/I_{TH} 27kΩ < RTH < 52kΩ	32.4kΩ 1% @I_{TH} = 9mA
CREV	Reverse polarity transition time programming	CREV = ((1/3750) · $\Delta T/\Delta V_{TR}$)	22nF 10% 10V @ 12V/ms
RDD	Pull up resistors		100kΩ
CVCC	Internally supply filter capacitor		100nF 20% 10V
CVpos(1)	Positive supply filter capacitor with low impedance for switch mode power supply		100µF
CV(2)	Battery supply filter capacitor with low impedance for switch mode power supply		100µF 20% 100V
CVB	High frequency noise filter		470nF 20% 100V
CRD(3)	High frequency noise filter		100nF 10% 15V
CZ	Fly-Back compensation capacitor		2.2nF, 20%
CSF	Sense Filter capacitor		120pF, 20%
RSF	Sense Filter resistor		1kΩ
RSENSE	DC/DC converter peak current limiting	R_{SENSE} = 375mV/I_{PK}	220mΩ @I_{PK} = 1.7A
Q1	DC/DC converter switch Nchan MOS transistor	RDS(ON)≤0.05Ω,VDSS = 30V VDG=30V, ID = 6.5A Low threshold drive	STN4NF03L or equivalent
D1	DC/DC converter series diode	V_r > 350V, t_{RR} ≤ 80ns	SMBYTW01-400 or equivalent
T1	DC/DC Converter transformer	Fly-Back transformer 4W, Turns Ratio 1:16 fro VPOS range from 4.5V to 8.5V	Tyco COEV MAGNETICS MGPWG-00007
Name	**Function**	**Formula**	**Typ. Value**

Table 10. External Components (continued)

T1	DC/DC Converter transformer	Fly-Back transformer 4W, Turns Ratio 1:8 fro VPOS range from 8.5V to 12V	Tyco COEV MAGNETICS MGPWG-00008
RF1	Negative battery programming level	250KΩ<RF1<270KΩ	270kΩ 1% @ V_{BATR} = -64V
RF2	Negative battery programming level		9.1kΩ 1%

@Gain Set = 0

RS	Protection resistance image	RS = 50 · (2Rp)	5kΩ @ Rp = 50Ω
ZAC	Two wire AC impedance	ZAC = 50 · (Zs - 2Rp)	25kΩ 1% @ Zs = 600Ω
ZA(5)	SLIC impedance balancing network	ZA = 50 · Zs	30kΩ 1% @ Zs = 600Ω
ZB(5)	Line impedance balancing network	ZB = 50 · Zl	30kΩ 1% @ Zl = 600Ω
CCOMP	AC feedback loop compensation	fo = 250kHz CCOMP = 1/(2π·fo·100·(RP))	120pF 10% 10V @ Rp = 50Ω
CH	Trans-Hybrid Loss frequency compensation	CH = CCOMP	120pF 10% 10V

@Gain Set = 1

RS	Protection resistance image	RS = 25 · (2Rp)	2.55kΩ @ Rp = 50Ω
ZAC	Two wire AC impedance	ZAC = 25 · (Zs - 2Rp)	12.5kΩ 1% @ Zs = 600Ω
ZA(5)	SLIC impedance balancing network	ZA = 25 · Zs	15kΩ 1% @ Zs = 600Ω
ZB(5)	Line impedance balancing network	ZB = 25 · Zl	15kΩ 1% @ Zl = 600Ω
CCOMP	AC feedback loop compensation	fo = 250kHz CCOMP = 2/(2π·fo·100·(RP))	220pF 10% 10VL @ Rp = 50Ω
CH	Trans-Hybrid Loss frequency compensation	CH = CCOMP	220pF 10% 10V

(1) CVpos should be defined depending on the power supply current capability and maximum allowable ripple.

(2) For low ripple application use 2x47 µF in parallel.

(3) Can be saved if proper PCB layout avoid noise coupling on RD pin (high impedance input).

(4) For high efficiency in HI-Z mode coil resistance @125kHz must be < 3Ω.

(5) In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.

4 Applications diagram

Figure 7. Application Diagram with N-Channel

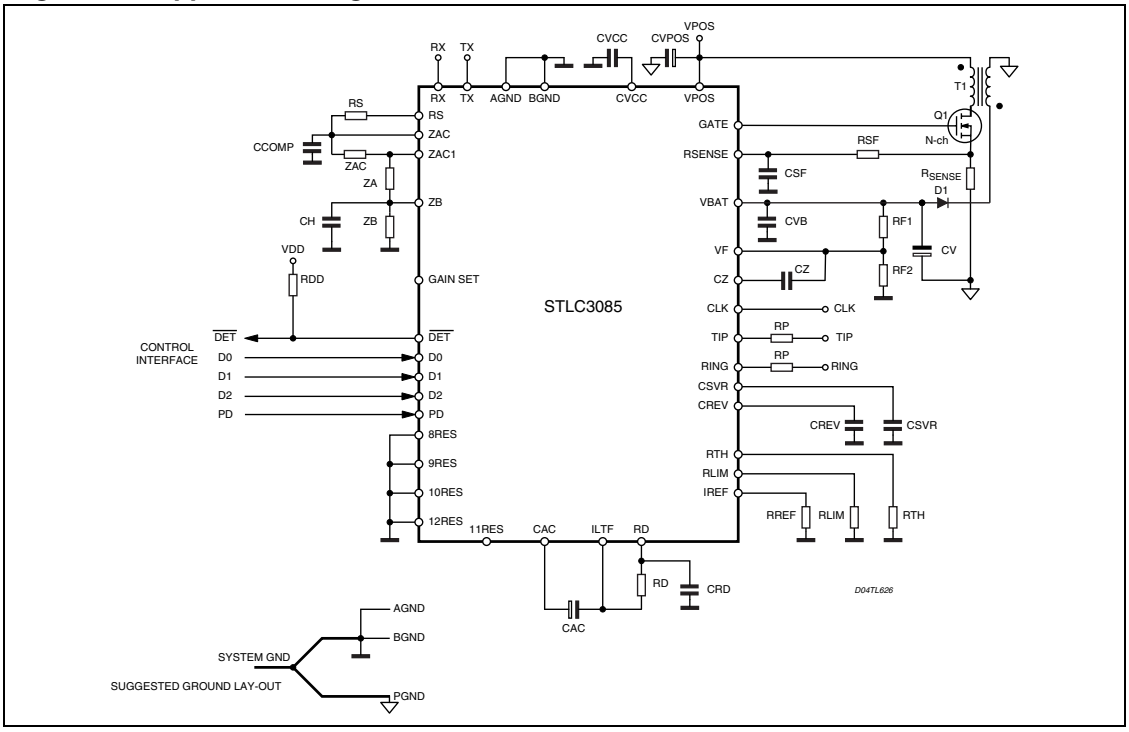
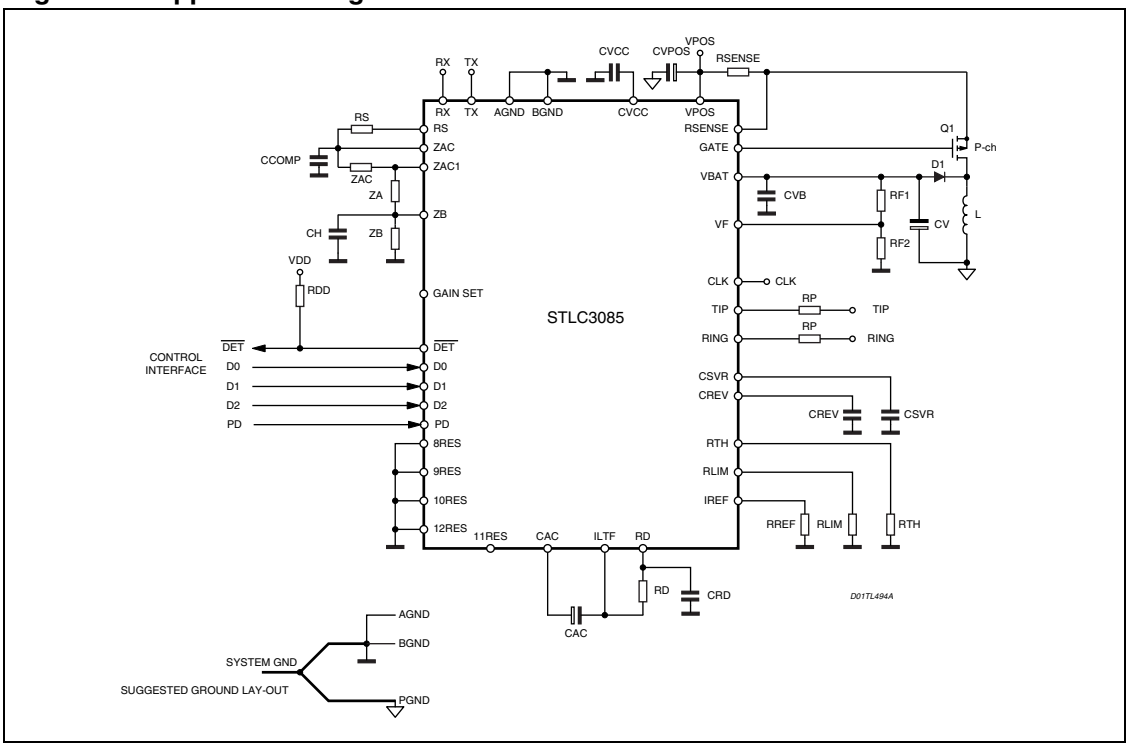


Figure 8. Application Diagram with P-Channel



Appendix A STLC3085 test circuits

Referring to the application diagram shown in *Figure 11* and using as external components the Typ. Values specified in the "External Components" *Table 10* find below the proper configuration for each measurement.

All measurements requiring DC current termination should be performed using "Wandel & Goltermann DC Loop Holding Circuit GH-1" or equivalent.

Figure 9. 2W Return Loss
2WRL = 20Log(\|Zref + Zs\|/\|Zref-Zs\|) = 20Log(E/2Vs)

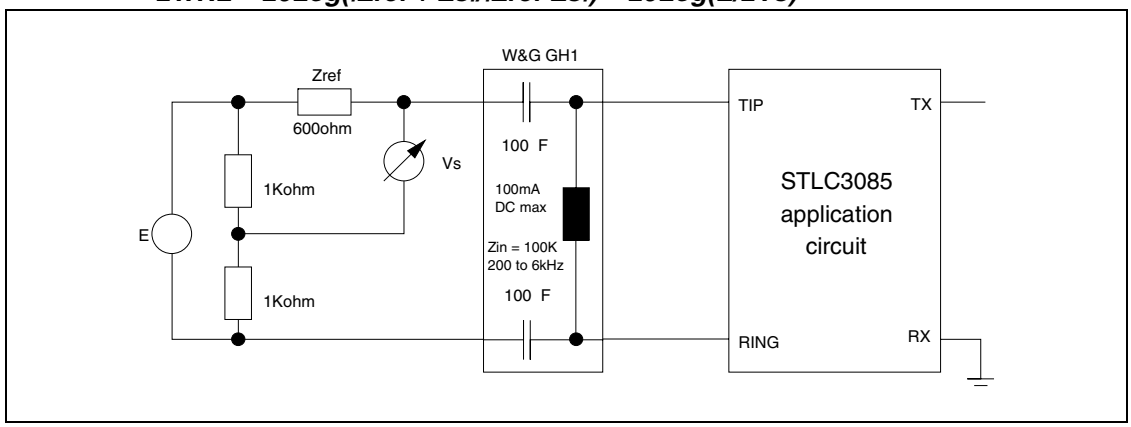


Figure 10. THL Trans Hybrid Loss
THL = 20Log\|Vrx/Vtx\|

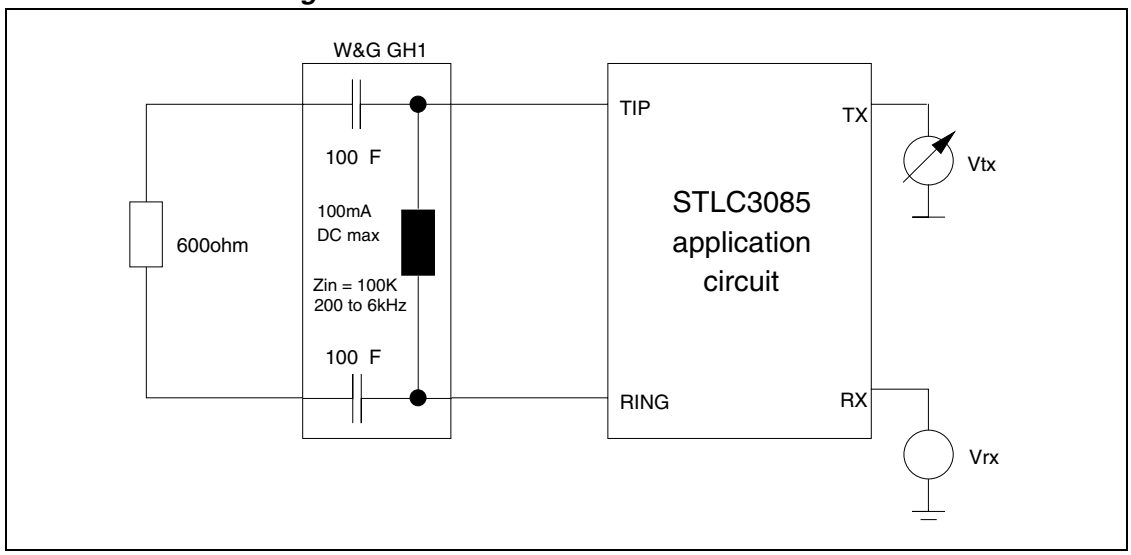


Figure 11. G24 Transmit Gain
G24 = 20Log\|2Vtx/E\|

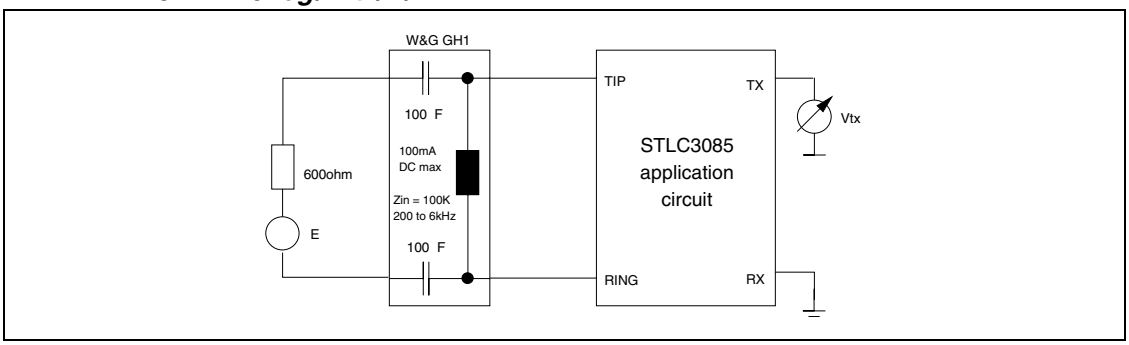


Figure 12. G42 Receive Gain
G42 = 20Log\|VI/Vrx\|

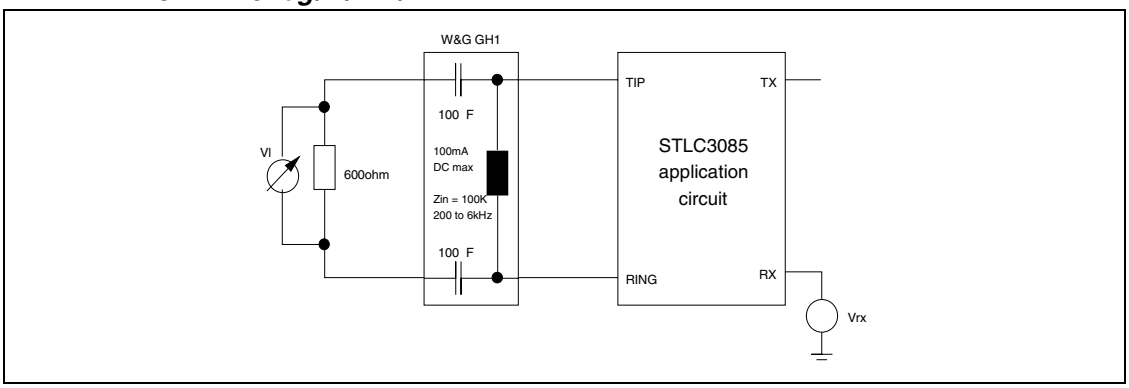


Figure 13. PSRRC Power supply rejection Vpos to 2W port
PSSRC = 20Log\|Vn/VI\|

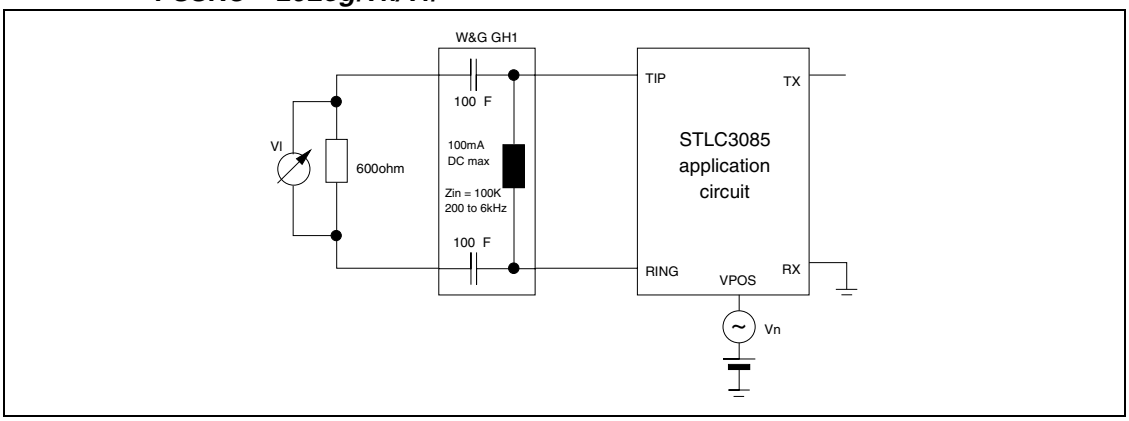


Figure 14. L/T Longitudinal to Transversal Conversion
L/T = 20Log|Vcm/VI|

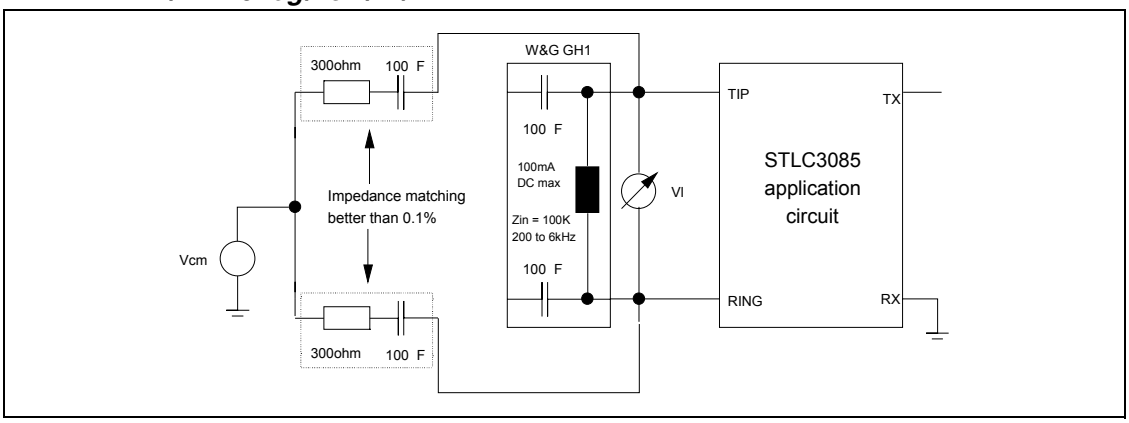


Figure 15. T/L Transversal to Longitudinal Conversion
T/L = 20Log|Vrx/Vcm|

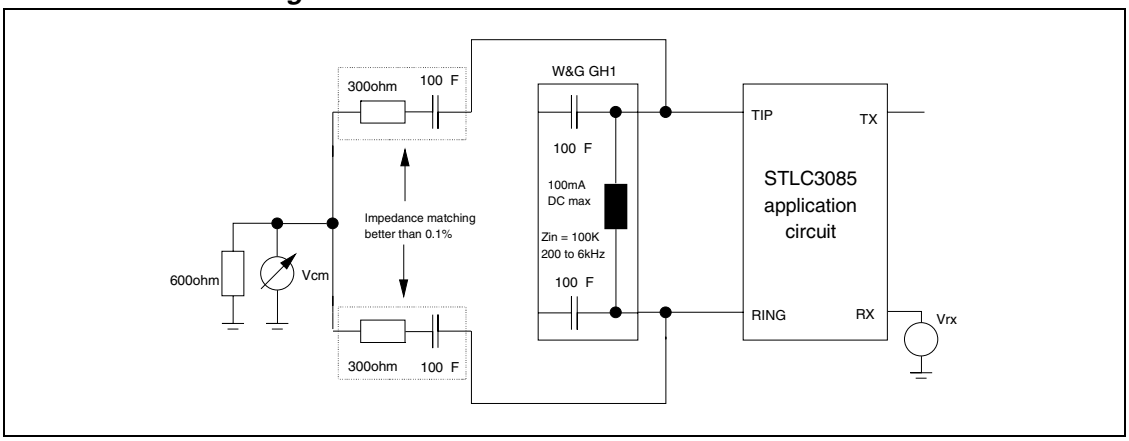
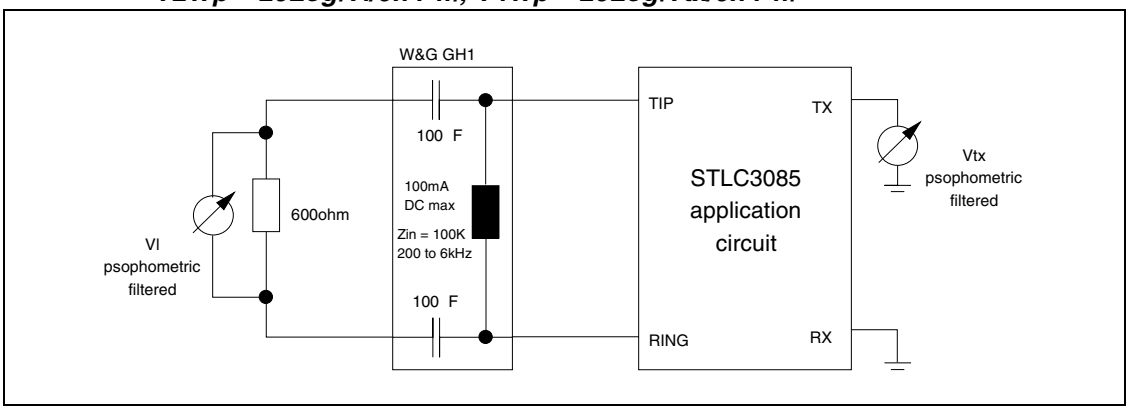


Figure 16. V2Wp and W4Wp: Idle channel psophometric noise at line and TX.
V2Wp = 20Log|VI/0.774I|; V4Wp = 20Log|Vtx/0.774I|



Appendix B STLC3085 overvoltage protection

Figure 17. Simplified configuration for indoor overvoltage protection

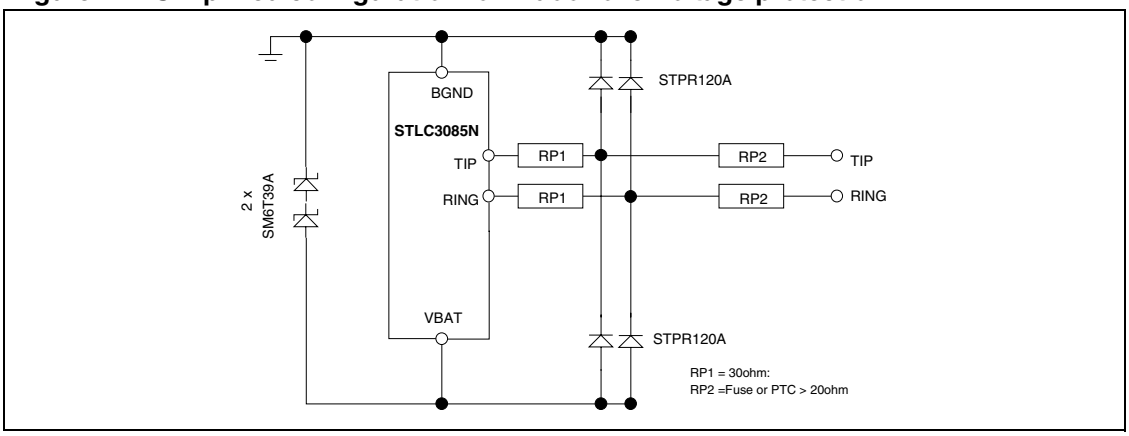
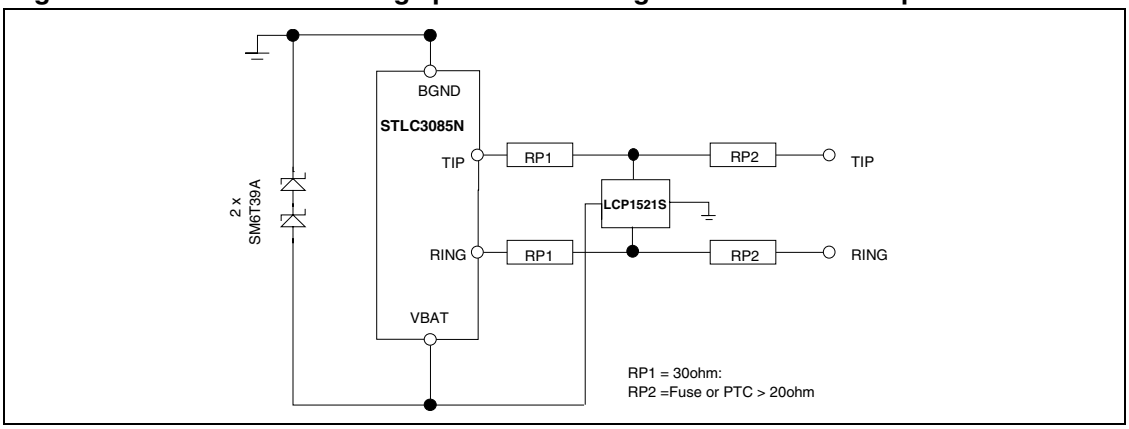
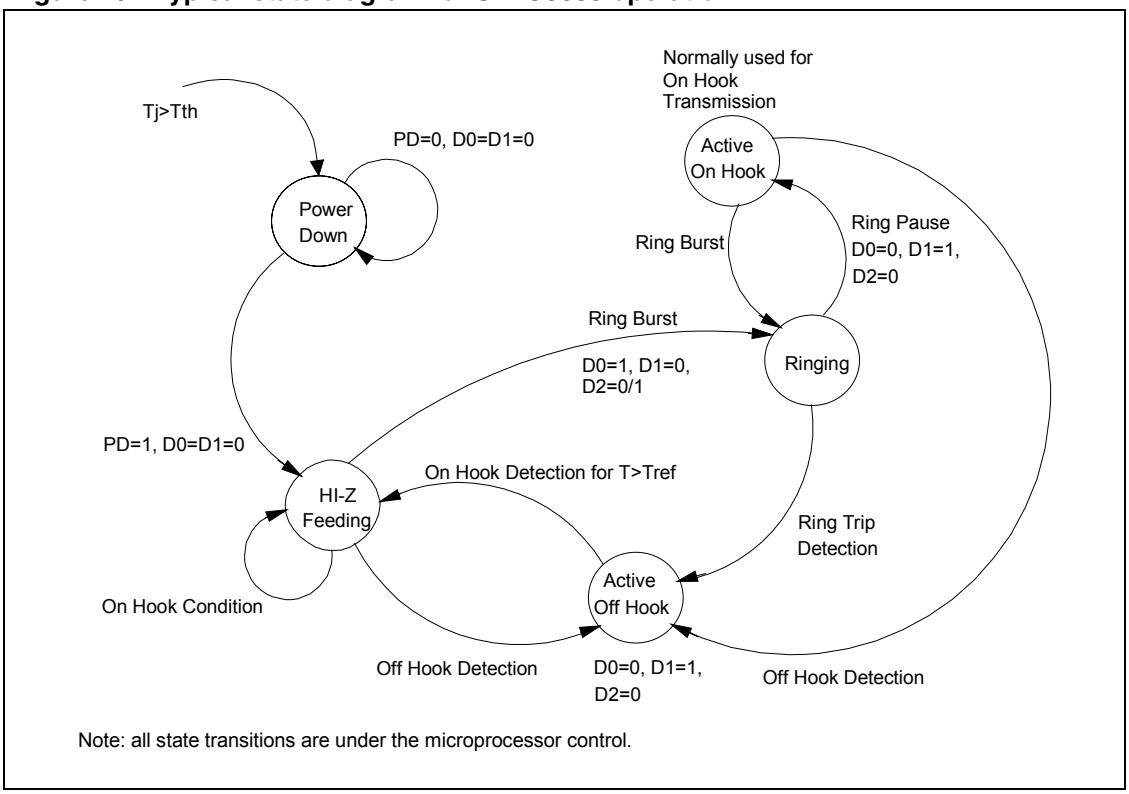


Figure 18. Standard overvoltage protection configuration for K20 compliance



Appendix C Typical state diagram for STLC3085 operation

Figure 19. Typical state diagram for STLC3085 operation



Note: all state transitions are under the microprocessor control.

5 Package information

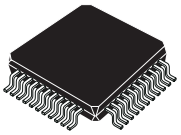
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

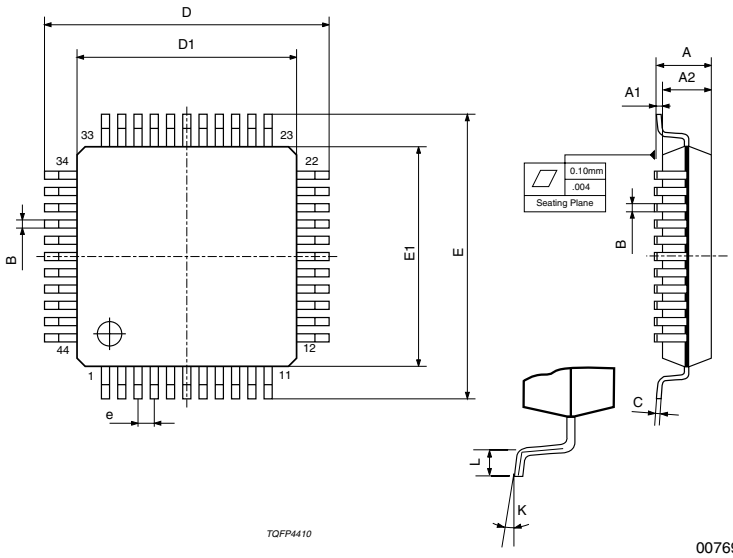
Figure 20. TQFP44 (10x10x1.4mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)



6 Revision history

Table 11.Document revision history

Date	Revision	Changes
15-Feb-2006	1	Initial release.

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