

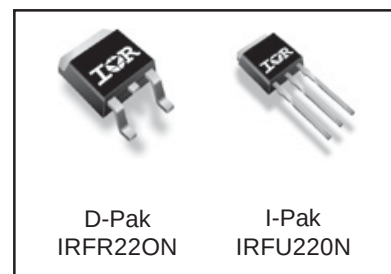
#### Applications

- High frequency DC-DC converters
- Lead-Free

| $V_{DSS}$ | $R_{DS(on)}$ max (m $\Omega$ ) | $I_D$ |
|-----------|--------------------------------|-------|
| 200V      | 600                            | 5.0A  |

#### Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



#### Absolute Maximum Ratings

|                                   | Parameter                                | Max.                   | Units               |
|-----------------------------------|------------------------------------------|------------------------|---------------------|
| $I_D$ @ $T_C = 25^\circ\text{C}$  | Continuous Drain Current, $V_{GS}$ @ 10V | 5.0                    | A                   |
| $I_D$ @ $T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS}$ @ 10V | 3.5                    |                     |
| $I_{DM}$                          | Pulsed Drain Current ①                   | 20                     |                     |
| $P_D$ @ $T_C = 25^\circ\text{C}$  | Power Dissipation                        | 43                     | W                   |
|                                   | Linear Derating Factor                   | 0.71                   | W/ $^\circ\text{C}$ |
| $V_{GS}$                          | Gate-to-Source Voltage                   | $\pm 20$               | V                   |
| $dv/dt$                           | Peak Diode Recovery $dv/dt$ ②            | 7.5                    | V/ns                |
| $T_J$                             | Operating Junction and                   | -55 to + 175           | $^\circ\text{C}$    |
| $T_{STG}$                         | Storage Temperature Range                |                        |                     |
|                                   | Soldering Temperature, for 10 seconds    | 300 (1.6mm from case ) |                     |

#### Typical SMPS Topologies

- Telecom 48V input Forward Converters

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Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

|                                 | Parameter                            | Min. | Typ. | Max. | Units | Conditions                                            |
|---------------------------------|--------------------------------------|------|------|------|-------|-------------------------------------------------------|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | 200  | —    | —    | V     | $V_{GS} = 0V, I_D = 250\mu A$                         |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.23 | —    | V/°C  | Reference to $25^\circ\text{C}, I_D = 1mA$ ④          |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | —    | 600  | mΩ    | $V_{GS} = 10V, I_D = 2.9A$ ④                          |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | 2.0  | —    | 4.0  | V     | $V_{DS} = V_{GS}, I_D = 250\mu A$                     |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —    | 25   | μA    | $V_{DS} = 200V, V_{GS} = 0V$                          |
|                                 |                                      | —    | —    | 250  |       | $V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA    | $V_{GS} = 20V$                                        |
|                                 | Gate-to-Source Reverse Leakage       | —    | —    | -100 |       | $V_{GS} = -20V$                                       |

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

|                        | Parameter                       | Min. | Typ. | Max. | Units | Conditions                                    |
|------------------------|---------------------------------|------|------|------|-------|-----------------------------------------------|
| $g_{fs}$               | Forward Transconductance        | 2.6  | —    | —    | S     | $V_{DS} = 50V, I_D = 2.9A$                    |
| $Q_g$                  | Total Gate Charge               | —    | 15   | 23   | nC    | $I_D = 2.9A$                                  |
| $Q_{gs}$               | Gate-to-Source Charge           | —    | 2.4  | 3.6  |       | $V_{DS} = 160V$                               |
| $Q_{gd}$               | Gate-to-Drain ("Miller") Charge | —    | 6.1  | 9.2  |       | $V_{GS} = 10V,$                               |
| $t_{d(on)}$            | Turn-On Delay Time              | —    | 6.4  | —    | ns    | $V_{DD} = 100V$                               |
| $t_r$                  | Rise Time                       | —    | 11   | —    |       | $I_D = 2.9A$                                  |
| $t_{d(off)}$           | Turn-Off Delay Time             | —    | 20   | —    |       | $R_G = 24\Omega$                              |
| $t_f$                  | Fall Time                       | —    | 12   | —    |       | $V_{GS} = 10V$ ④                              |
| $C_{iss}$              | Input Capacitance               | —    | 300  | —    | pF    | $V_{GS} = 0V$                                 |
| $C_{oss}$              | Output Capacitance              | —    | 53   | —    |       | $V_{DS} = 25V$                                |
| $C_{rss}$              | Reverse Transfer Capacitance    | —    | 15   | —    |       | $f = 1.0MHz$                                  |
| $C_{oss}$              | Output Capacitance              | —    | 300  | —    |       | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$      |
| $C_{oss}$              | Output Capacitance              | —    | 23   | —    |       | $V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz$      |
| $C_{oss \text{ eff.}}$ | Effective Output Capacitance    | —    | 46   | —    |       | $V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$ ⑤ |

## Avalanche Characteristics

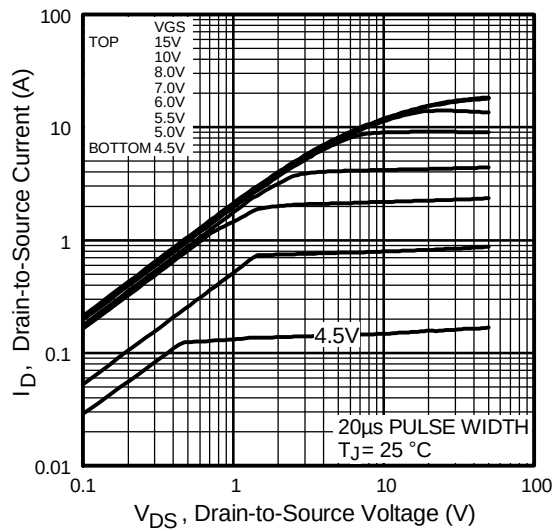
|          | Parameter                      | Typ. | Max. | Units |
|----------|--------------------------------|------|------|-------|
| $E_{AS}$ | Single Pulse Avalanche Energy② | —    | 46   | mJ    |
| $I_{AR}$ | Avalanche Current①             | —    | 2.9  | A     |
| $E_{AR}$ | Repetitive Avalanche Energy①   | —    | 4.3  | mJ    |

## Thermal Resistance

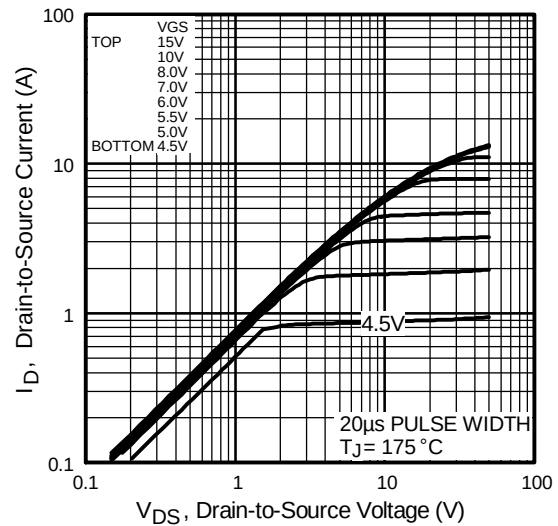
|                 | Parameter                        | Typ. | Max. | Units |
|-----------------|----------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case                 | —    | 3.5  | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount)* | —    | 50   |       |
| $R_{\theta JA}$ | Junction-to-Ambient              | —    | 110  |       |

## Diode Characteristics

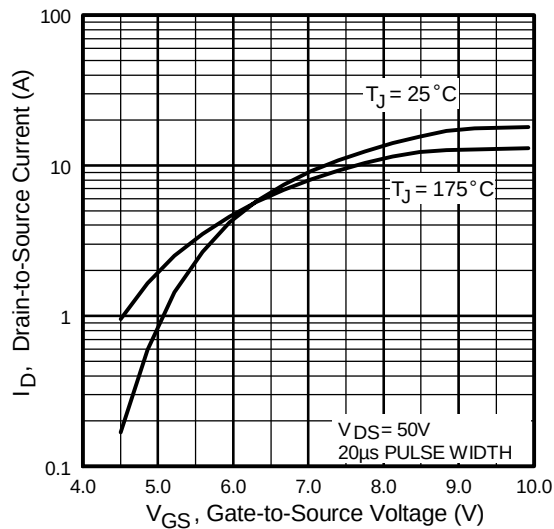
|          | Parameter                              | Min.                                                                        | Typ. | Max. | Units | Conditions                                                     |
|----------|----------------------------------------|-----------------------------------------------------------------------------|------|------|-------|----------------------------------------------------------------|
| $I_S$    | Continuous Source Current (Body Diode) | —                                                                           | —    | 5.0  | A     | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ①   | —                                                                           | —    | 20   |       |                                                                |
| $V_{SD}$ | Diode Forward Voltage                  | —                                                                           | —    | 1.3  | V     | $T_J = 25^\circ\text{C}, I_S = 2.9A, V_{GS} = 0V$ ④            |
| $t_{rr}$ | Reverse Recovery Time                  | —                                                                           | 90   | 140  | ns    | $T_J = 25^\circ\text{C}, I_F = 2.9A$                           |
| $Q_{rr}$ | Reverse Recovery Charge                | —                                                                           | 320  | 480  | nC    | $di/dt = 100A/\mu s$ ④                                         |
| $t_{on}$ | Forward Turn-On Time                   | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ ) |      |      |       |                                                                |



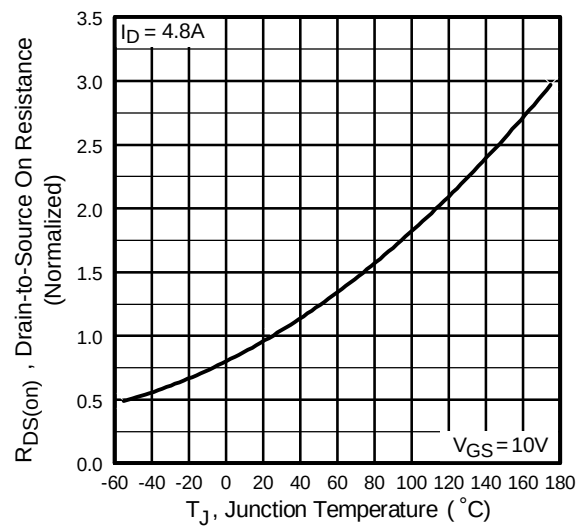
**Fig 1.** Typical Output Characteristics



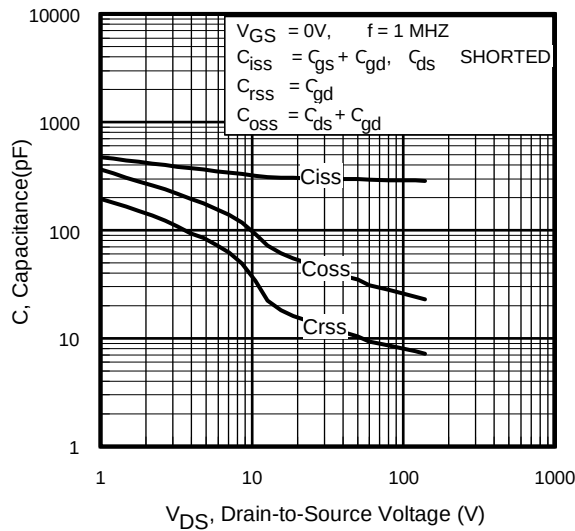
**Fig 2.** Typical Output Characteristics



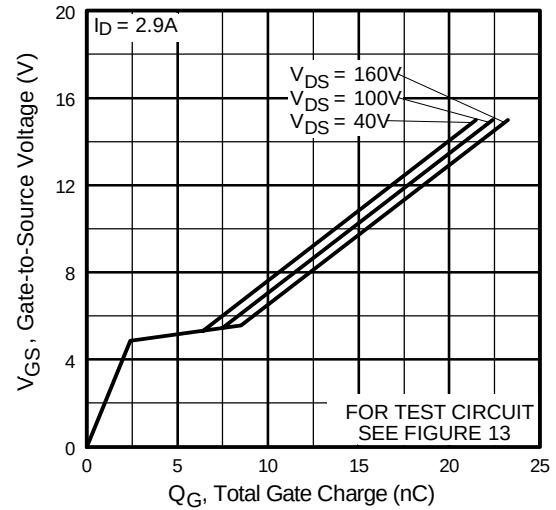
**Fig 3.** Typical Transfer Characteristics



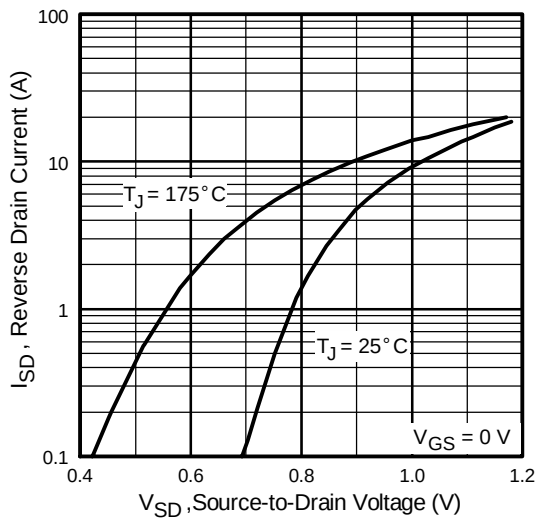
**Fig 4.** Normalized On-Resistance Vs. Temperature



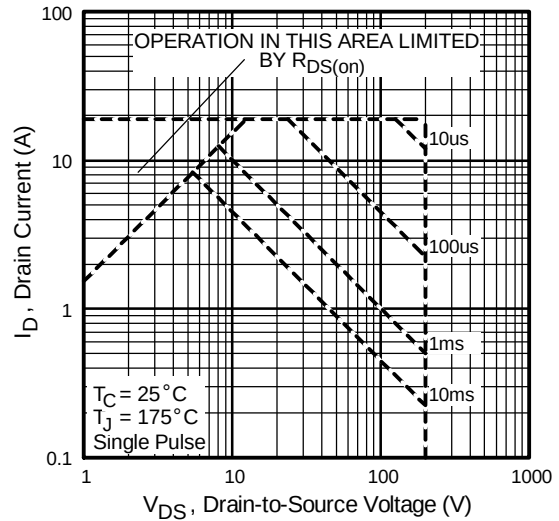
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



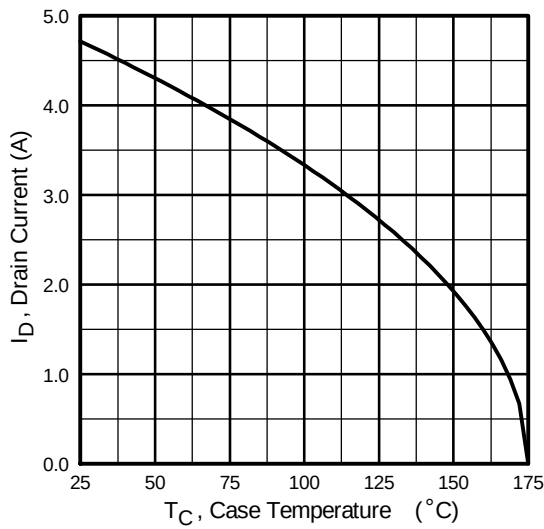
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



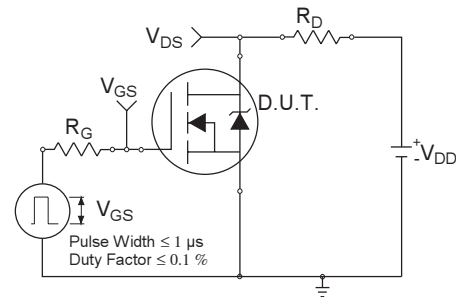
**Fig 7.** Typical Source-Drain Diode Forward Voltage



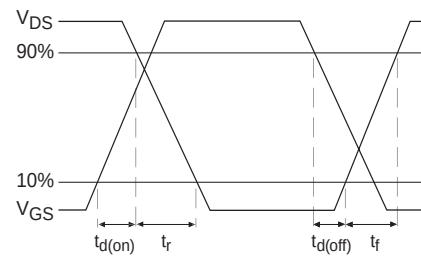
**Fig 8.** Maximum Safe Operating Area



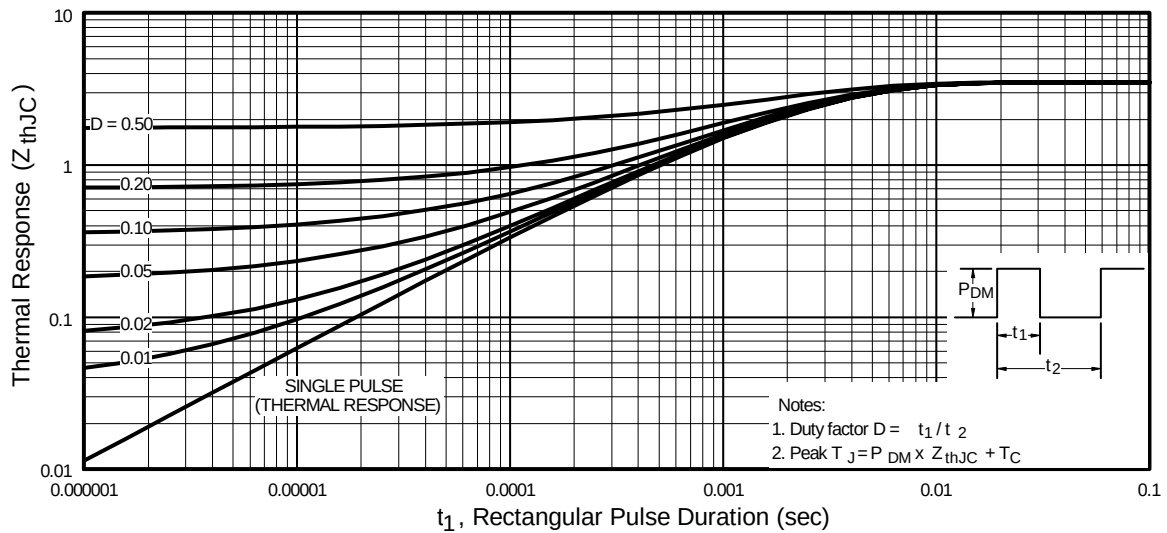
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



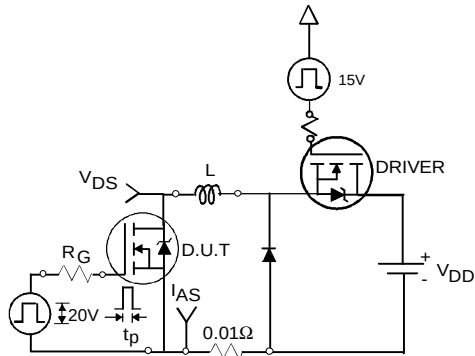
**Fig 10b.** Switching Time Waveforms



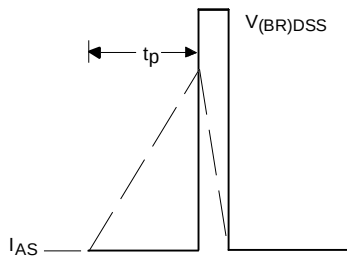
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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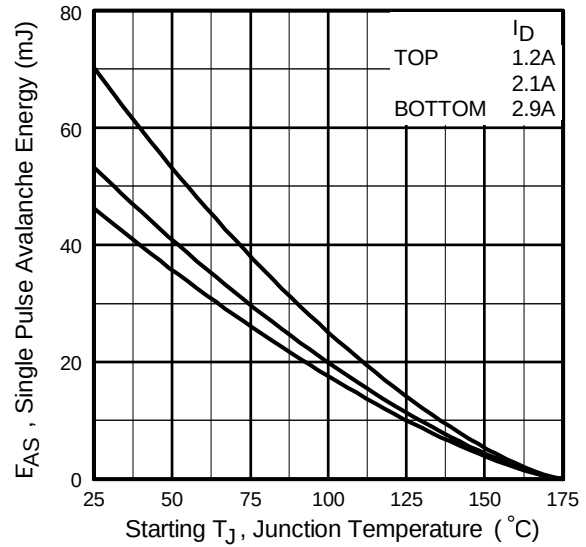
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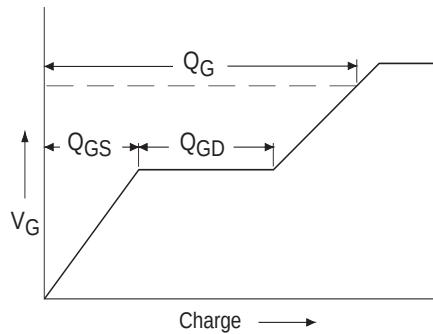
**Fig 12a.** Unclamped Inductive Test Circuit



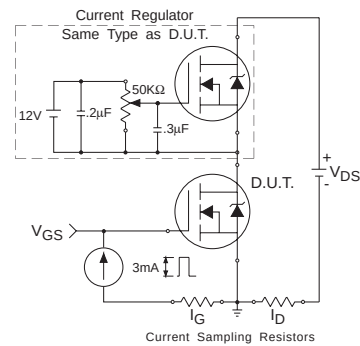
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

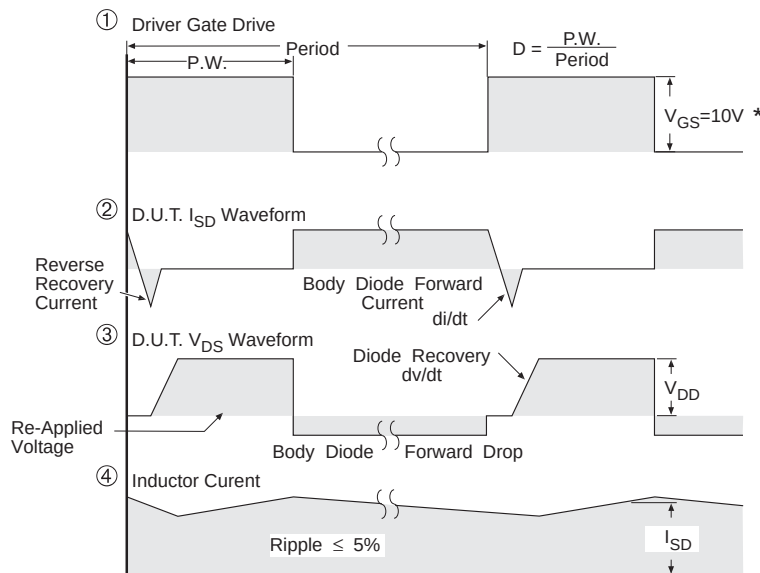
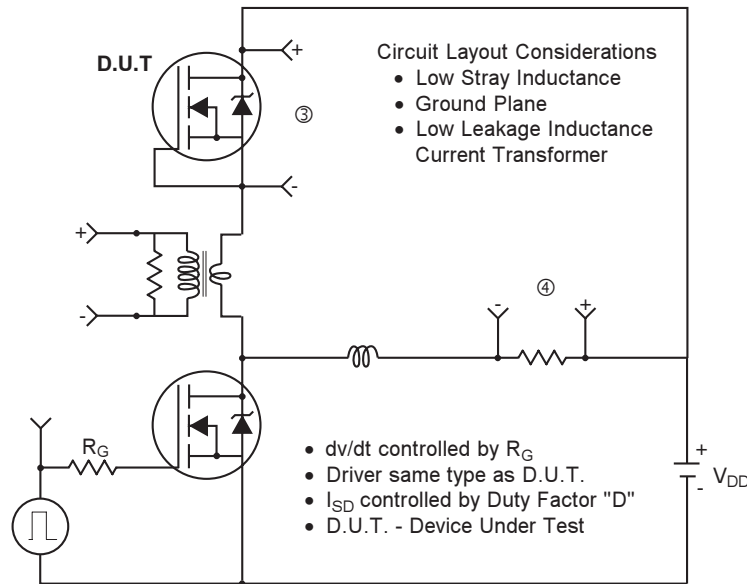


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

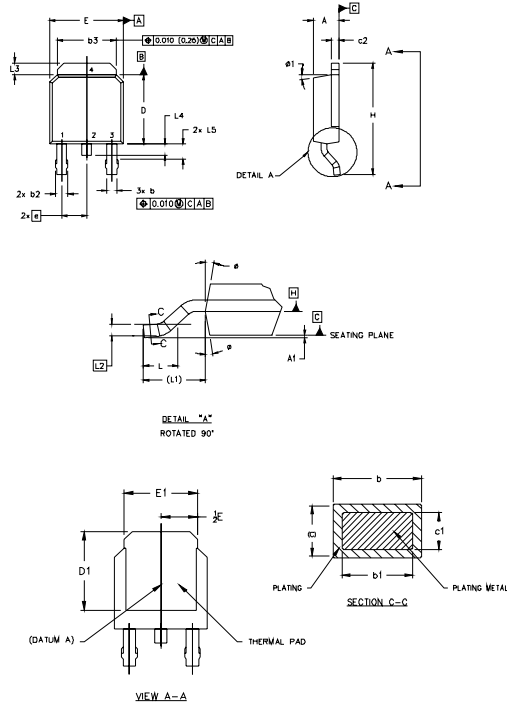
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
  - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
  - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS  |       |           |       | NOTES |                                                           |
|--------|-------------|-------|-----------|-------|-------|-----------------------------------------------------------|
|        | MILLIMETERS |       | INCHES    |       |       |                                                           |
|        | MIN.        | MAX.  | MIN.      | MAX.  |       |                                                           |
| A      | 2.18        | 2.39  | .086      | .094  | 5     | LEAD ASSIGNMENTS                                          |
| A1     |             | 0.13  |           | .005  |       |                                                           |
| b      | 0.64        | 0.89  | .025      | .035  |       |                                                           |
| b1     | 0.64        | 0.79  | .025      | 0.031 |       |                                                           |
| b2     | 0.76        | 1.14  | .030      | .045  |       |                                                           |
| b3     | 4.95        | 5.46  | .195      | .215  | 5     | HEXFET                                                    |
| c      | 0.46        | 0.61  | .018      | .024  |       |                                                           |
| c1     | 0.41        | 0.56  | .016      | .022  |       |                                                           |
| c2     | .046        | 0.89  | .018      | .035  |       |                                                           |
| D      | 5.97        | 6.22  | .235      | .245  |       |                                                           |
| D1     | 5.21        | -     | .205      | -     | 4     | 1 - GATE<br>2 - DRAIN<br>3 - SOURCE<br>4 - DRAIN          |
| E      | 6.35        | 6.73  | .250      | .265  | 6     |                                                           |
| E1     | 4.32        | -     | .170      | -     | 4     |                                                           |
| e      | 2.29        |       | .090 BSC  |       |       | 1 - GATE<br>2 - COLLECTOR<br>3 - EMITTER<br>4 - COLLECTOR |
| H      | 9.40        | 10.41 | .370      | .410  |       |                                                           |
| L      | 1.40        | 1.78  | .055      | .070  |       |                                                           |
| L1     | 2.74 REF.   |       | .108 REF. |       |       |                                                           |
| L2     | .0051 BSC   |       | .020 BSC  |       |       |                                                           |
| L3     | 0.89        | 1.27  | .035      | .050  |       |                                                           |
| L4     |             | 1.02  |           | .040  |       |                                                           |
| L5     | 1.14        | 1.52  | .045      | .060  | 3     |                                                           |
| ø      | 0"          | 10"   | 0"        | 10"   |       |                                                           |
| ø1     | 0"          | 15"   | 0"        | 15"   |       |                                                           |

### LEAD ASSIGNMENTS

#### HEXFET

1. - GATE
2. - DRAIN
3. - SOURCE
4. - DRAIN

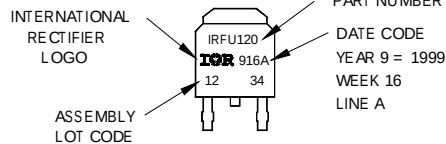
#### IGBTs, CoPACK

1. - GATE
2. - COLLECTOR
3. - EMITTER
4. - COLLECTOR

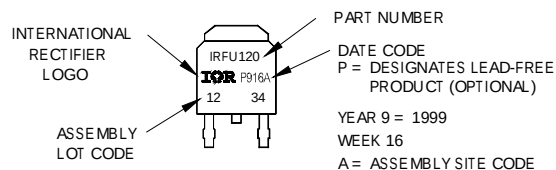
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"



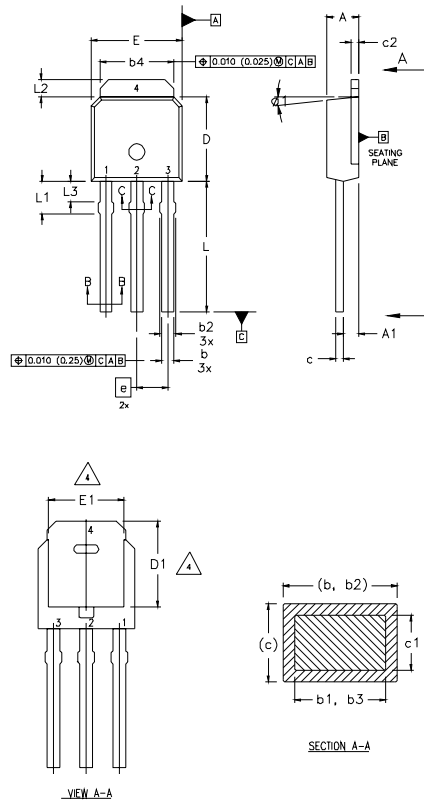
OR





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

### LEAD ASSIGNMENTS

#### HEXFET

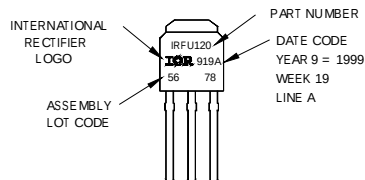
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

| SYMBOL | DIMENSIONS  |      |           |       | NOTES |
|--------|-------------|------|-----------|-------|-------|
|        | MILLIMETERS |      | INCHES    |       |       |
|        | MIN.        | MAX. | MIN.      | MAX.  |       |
| A      | 2.18        | 2.39 | 0.086     | .094  |       |
| A1     | 0.89        | 1.14 | 0.035     | 0.045 |       |
| b      | 0.64        | 0.89 | 0.025     | 0.035 |       |
| b1     | 0.64        | 0.79 | 0.025     | 0.031 | 4     |
| b2     | 0.76        | 1.14 | 0.030     | 0.045 |       |
| b3     | 0.76        | 1.04 | 0.030     | 0.041 |       |
| b4     | 5.00        | 5.46 | 0.195     | 0.215 | 4     |
| c      | 0.46        | 0.61 | 0.018     | 0.024 |       |
| c1     | 0.41        | 0.56 | 0.016     | 0.022 |       |
| c2     | .046        | 0.86 | 0.018     | 0.035 |       |
| D      | 5.97        | 6.22 | 0.235     | 0.245 | 3, 4  |
| D1     | 5.21        | —    | 0.205     | —     | 4     |
| E      | 6.35        | 6.73 | 0.250     | 0.265 | 3, 4  |
| E1     | 4.32        | —    | 0.170     | —     | 4     |
| e      | 2.29        |      | 0.090 BSC |       |       |
| L      | 8.89        | 9.60 | 0.350     | 0.380 |       |
| L1     | 1.91        | 2.29 | 0.075     | 0.090 |       |
| L2     | 0.89        | 1.27 | 0.035     | 0.050 | 4     |
| L3     | 1.14        | 1.52 | 0.045     | 0.060 | 5     |
| ø1     | 0"          | 15"  | 0"        | 15"   |       |

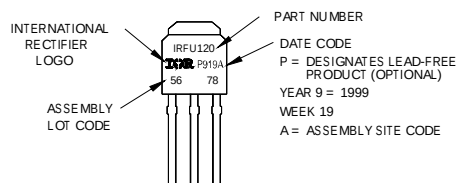
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW19, 1999  
IN THE ASSEMBLY LINE "A"

**Note:** "P" in assembly line  
position indicates "Lead-Free"



OR

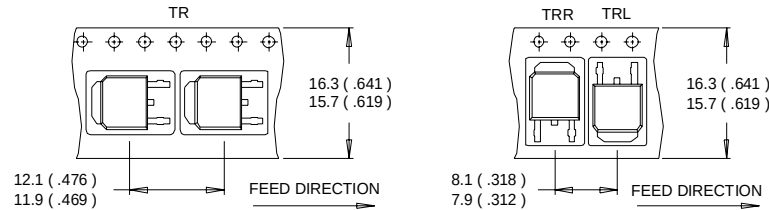


# IRFR/U220NPbF

## D-Pak (TO-252AA) Tape & Reel Information

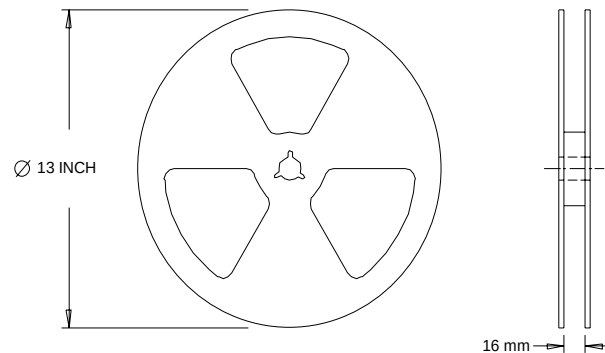
Dimensions are shown in millimeters (inches)

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**IR** Rectifier



### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



### NOTES :

1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
  - ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 11\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 2.9\text{A}$ .
  - ③  $I_{SD} \leq 2.9\text{A}$ ,  $di/dt \leq 320\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
  - ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
  - ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- \* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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Data and specifications subject to change without notice. 12/04

[www.irf.com](http://www.irf.com)

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>