AMIC

AP160

8-BIT MICROCONTROLLER WITH 8KB OTP

DATA SHEET

October 2001

GENERAL DESCRIPTION

The AP160 is a wide operating voltage, Low power consumption and high performance with AMIC high-density CMOS technology. All instruction set of AP160 are fully compatible with the standard 8051. The AP160 contains 8K bytes OTP EPROM, 256 bytes RAM, four 8-bit bi-directional and bit addressable I/O ports, three 16-bit timer/counter and eight interrupt sources. To reduce power consumption, idle mode and power down mode are provided to implementation. For data protection, program lock bits can be performed through programming LB1, LB2 and LB3. The AMIC AP160 is a useful and powerful microcontroller in many control system application.

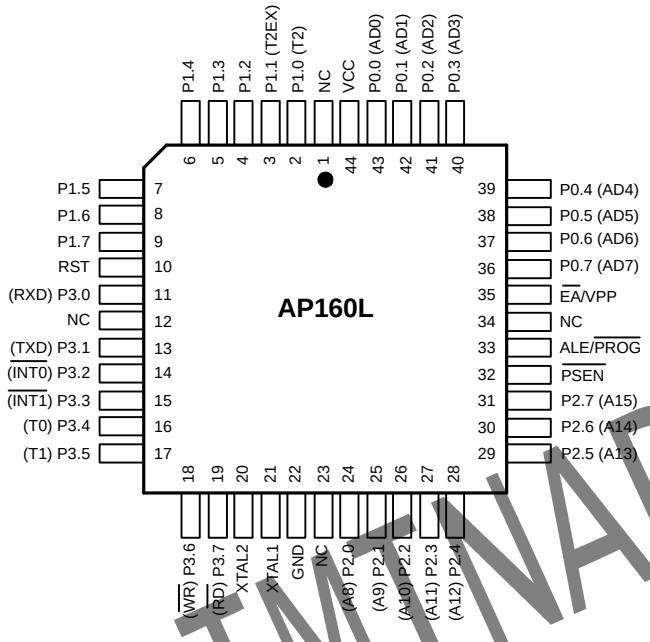
FEATURES

- Compatible with MCS-51 Products
- 256 X 8 bit internal Data RAM.
- 8KB On-Chip OTP EPROM.
- 2.7V~5.5V Operating Range.
- Fully Static Operation : 0Hz to 16 MHz
- 0~33MHZ speed range at VCC=5V.
- 32 Programmable I/O pins
- Three 16-Bit Timers/Counters.
- Programmable clock out.
- Full-duplex UART
- Eight interrupt sources.
- 2 level priority-interrupt.
- Power reduction control modes
  - Idle mode
  - Power-down mode
- 3 security bits.
- Low EMI (Inhibit ALE)
- Wake-up from Power Down by an external interrupt.
- Available in PLCC and QFP44 packages.

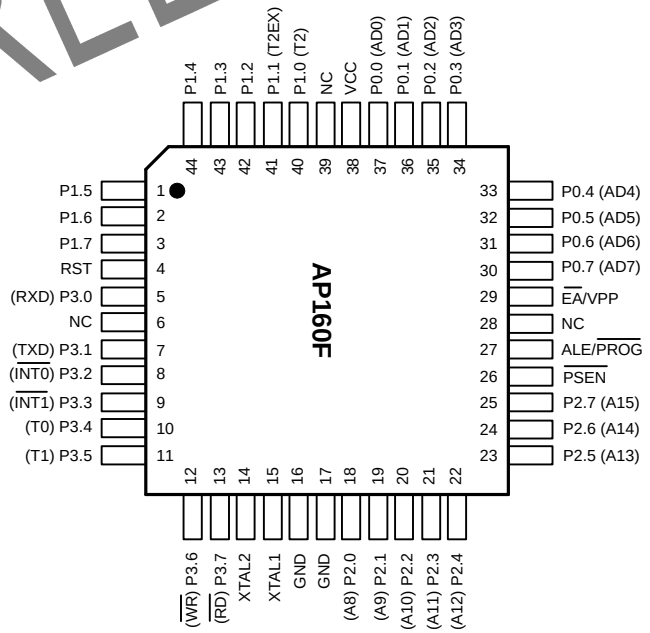
PRELIMINARY

PIN CONFIGURATIONS

■ PLCC

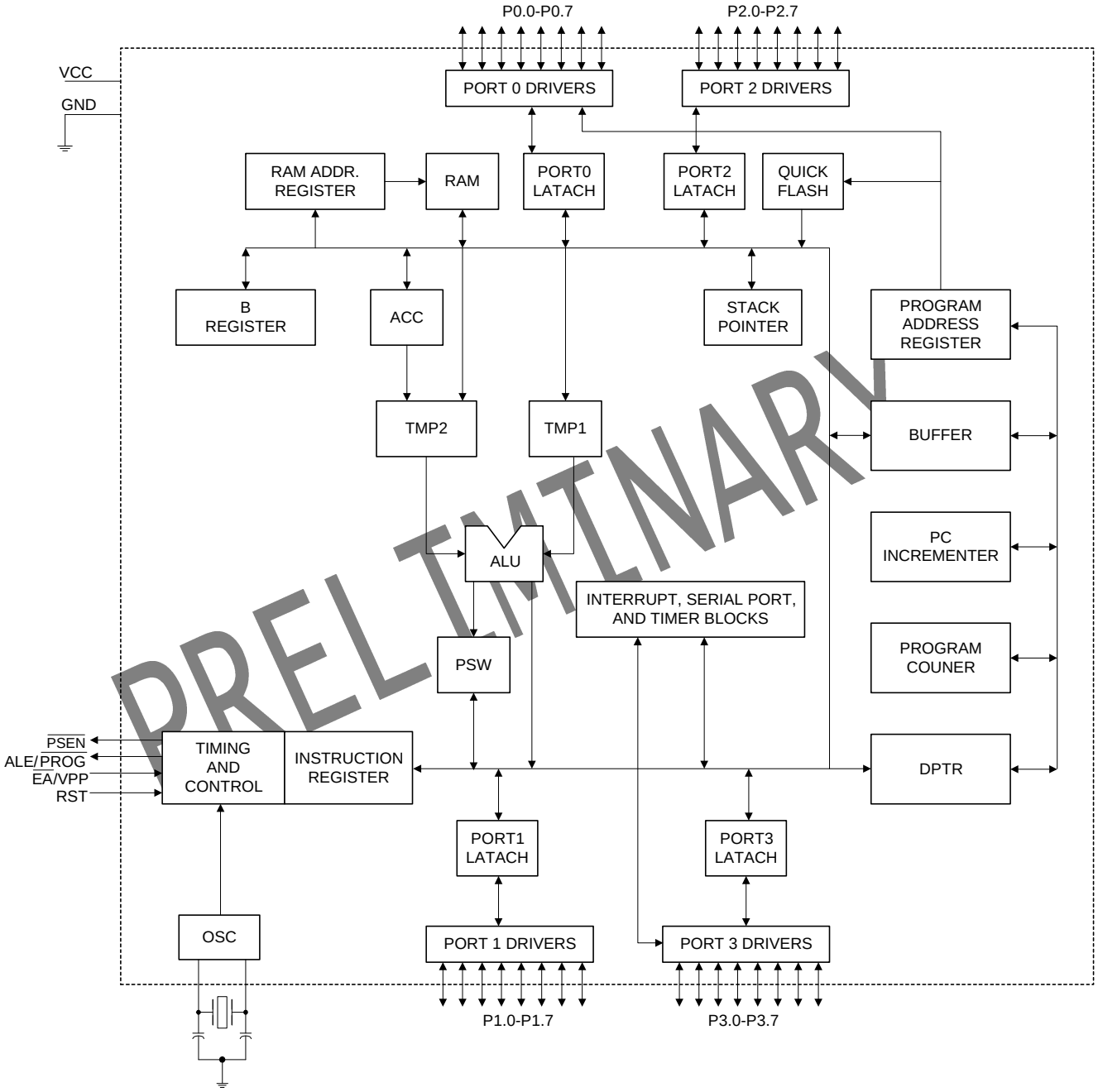


■ QFP



PRELIMINARY

BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTIONS
VSS	I	Ground.
VCC	I	Supply voltage.
P0.0-P0.7	I/O	Port 0 is an 8-bit open drain, bidirectional I/O port. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups. Port 0 also receives the code bytes during programming on-chip OTP EPROM and outputs the code bytes during program verification. External pullups are required during program verification.
P1.0-P1.7	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following: **T2** (P1.0): Timer/Counter 2 external count input/clockout (see Programmable Clock-Out) **T2EX** (P1.1): Timer/Counter 2 Reload/Capture/Direction control. Port 1 also receives the low-order address bytes during programming on-chip OTP EPROM and verification.
P2.0-P2.7	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during programming on-chip OTP EPROM and verification.
P3.0-P3.7	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs.When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups. Port 3 also serves the functions of various special features of the AP160, as shown below: **RXD** (P3.0): Serial input port **TXD** (P3.1): Serial output port **INT0** (P3.2): External interrupt **INT1** (P3.3): External interrupt **T0** (P3.4): Timer 0 external input **T1** (P3.5): Timer 1 external input **WR** (P3.6): External data memory write strobe **RD** (P3.7): External data memory read strobe Port 3 also receives some control signals for programming and verification.
RST	I	Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

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SYMBOL	TYPE	DESCRIPTIONS
ALE/PROG	O/I	Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Programming on-chip OPT EPROM. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.
PSEN	O	Program Store Enable is the read strobe to external program memory. When the AP160 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.
EA/Vpp	I	External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during programming OTP EPROM.
XTAL1	I	Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
XTAL2	O	Output from the inverting oscillator amplifier.

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SPECIAL FUNCTION REGISTERS

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Table 1. AP160 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	TL2 00000000	TH2 00000000				0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111								0A7H
098H	SCON 00000000	SBUF XXXXXXXX							09FH
090H	P1 11111111								097H
088H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			08FH
080H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 0XXX0000	087H

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Note that not all of the addresses are occupied. Unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write 1s to these unlisted locations, since they may be used in future AMIC products to invoke new features. In that case the reset or inactive values of the new bits will always be 0.

TIMER2

Timer2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/T2 in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3.

Table 2. T2CON – Timer/Counter 2 Control Register
T2CON Address = 0C8H

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Reset Value = 00000000
Bit Addressable

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN=1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/T2	Timer or counter select for Timer 2. C/T2 = 0 for timer function. C/T2 = 1 for external event counter (falling edge triggered0.
CP/RL2	Capture/Reload select. CP/RL2 = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/Rl2 = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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Table 3. Timer 2 Operating Modes

RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	16-Bit Auto-Reload
0	1	1	16-Bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Timer2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2.

In this function, the external input is samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2=0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2=1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

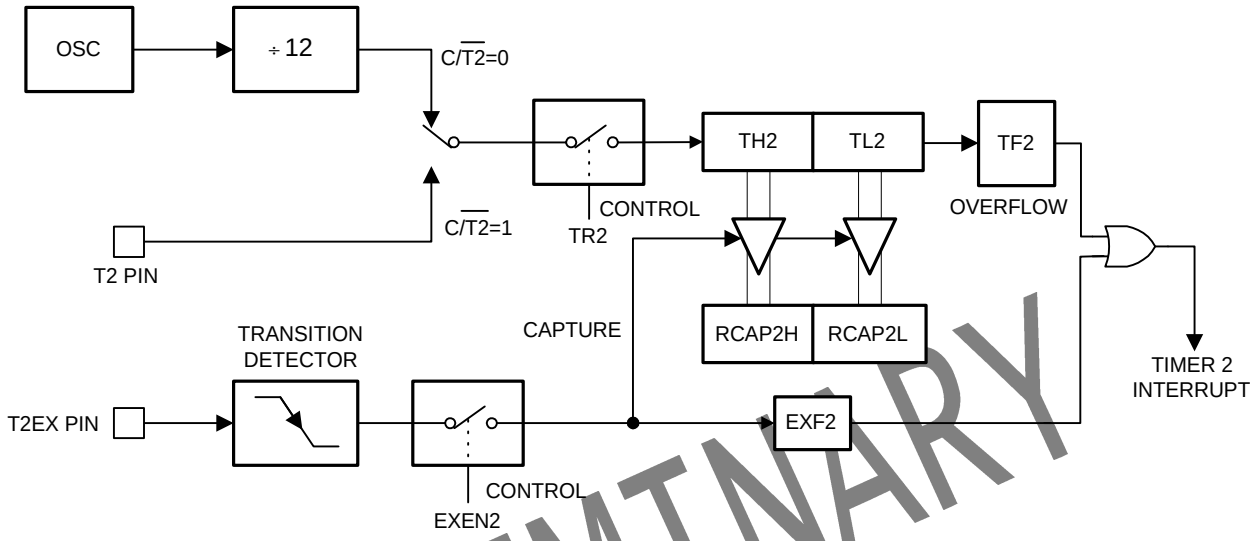


Figure 1. Timer in Capture Mode

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Auto-Reload (UP or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 3). Upon reset, the DCEN bit is set to 0 so that Timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin. Figure 2 shows Timer 2 automatically counting up when DCEN=0.

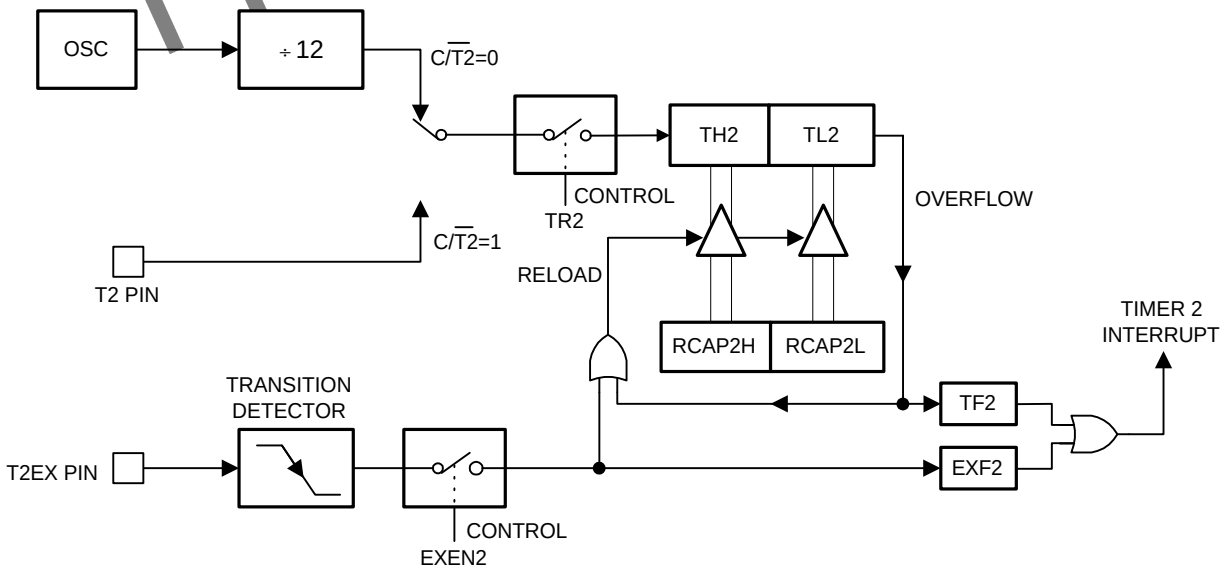


Figure 2. Timer 2 Auto Reload Mode (DCEN=0)

In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2=0, Timer2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture Mode RCAP2H and RCAP2L are preset by software.

If EXEN2=1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled. Setting the DCEN bit enables Timer2 to count up or down, as shown in Figure 3. In the mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. The overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively. A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and Tl2 equal the values stored in RCAP2H and RACP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers. The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Table 3. T2MOD (Timer 2 Mode Control Register)
T2Mod Address = 0C9H Reset Value = XXXX XX00B

Not bit addressable

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Symbol	Function
-	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

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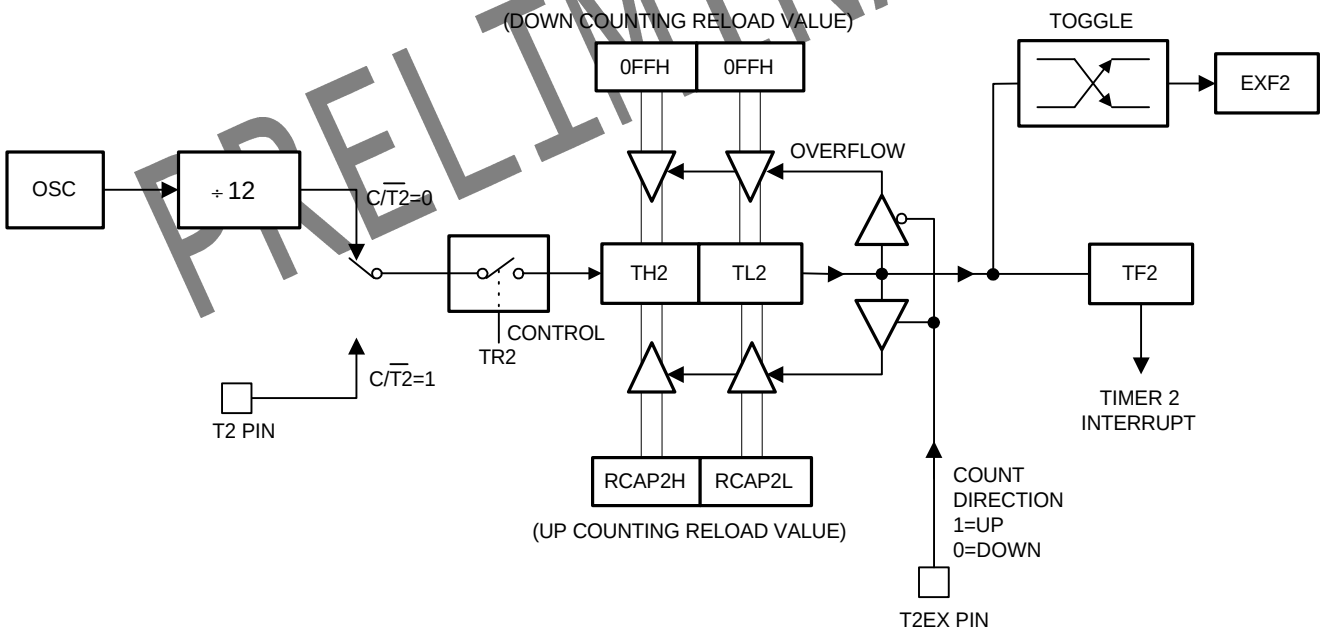


Figure 3. Timer 2 Auto Reload Mode (DCEN=1)

Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4. The baud rate generator mode is similar to the auto-reload mode, in that a rollover in Th2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software. The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Mode 1 and 3 Baud Rates} = \frac{Timer\ 2\ Overflow\ Rate}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/T2=0). The Timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{Modes\ 1\ and\ 3}{Baud\ Rate} = \frac{Oscillator\ Frequency}{32 \times [65536 - (RCAP2H, RCAP2L)]}$$

where (RCAP2H,RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK=1 in T2CON. Note that a rollover in TH2 does not ser TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Thus when timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt. Note that when Timer 2 is running (TR2=1) as a timer in the baud rate generator mode. TH2 or TL2 should not be read from or written to. Under there conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the timer 2 or RCAP2 register.

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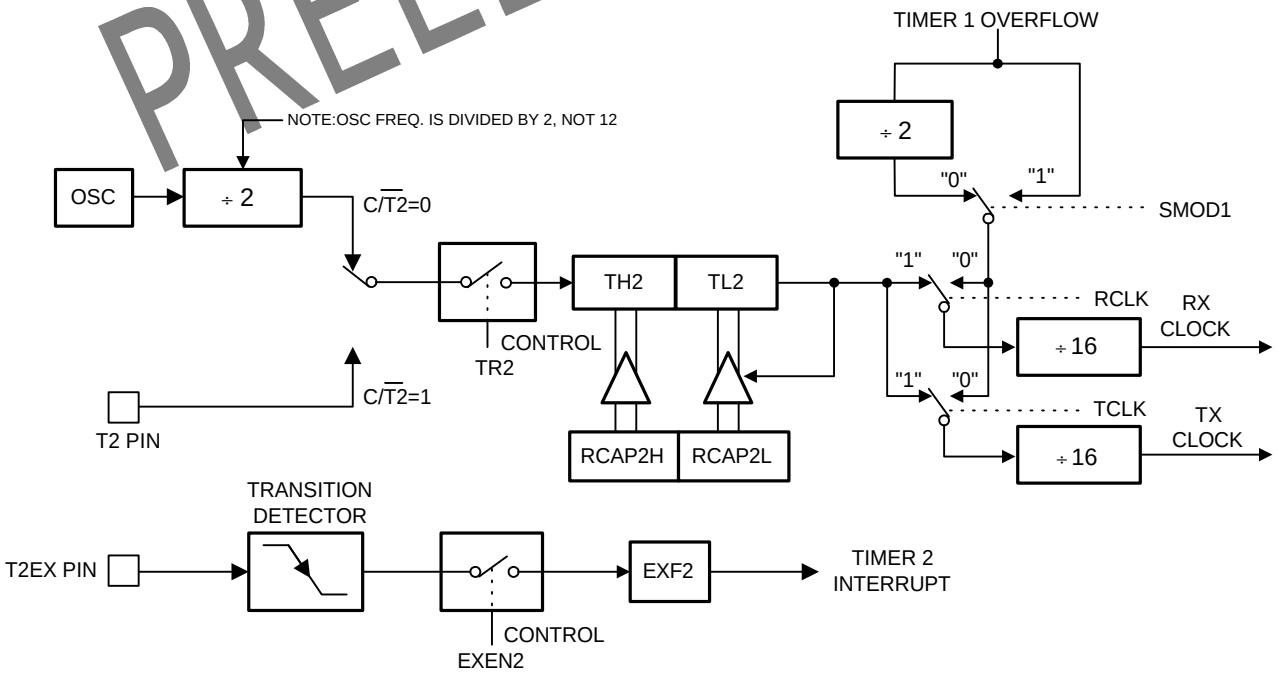


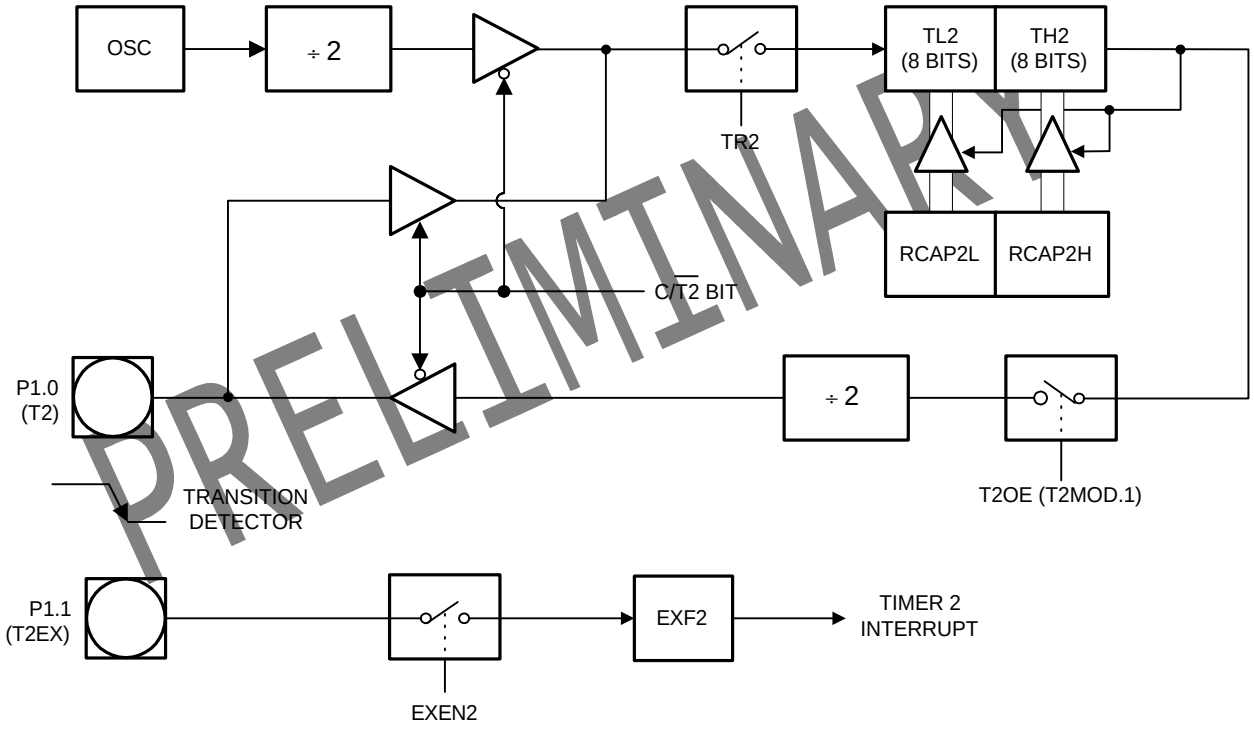
Figure 4. Timer 2 in Baud Rate Generator Mode

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 HZ to 4MHZ at a 16MHZ operating frequency. To configure the Timer/Counter 2 as a clock generator, bit C/T2 (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit Tr2 (T2CON.2) starts and stops the timer. The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$Clock-Out\ Frequency = \frac{Oscillator\ Frequency}{4\times[65535-(RCAP2H, RCAP2L)]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.



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Figure 5. Timer 2 in Clock-Out Mode

INTERRUPTS

The AP160 has a total of six interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once. Note that Table 4 shows that bit position IE.6 is unimplemented. User software should not write 1s to the bit position, since they may be used in future AMIC products. Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software. The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 4: Interrupt Enable (IE) Register

(MSB)							(LSB)
EA	--	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
--	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AMIC products		

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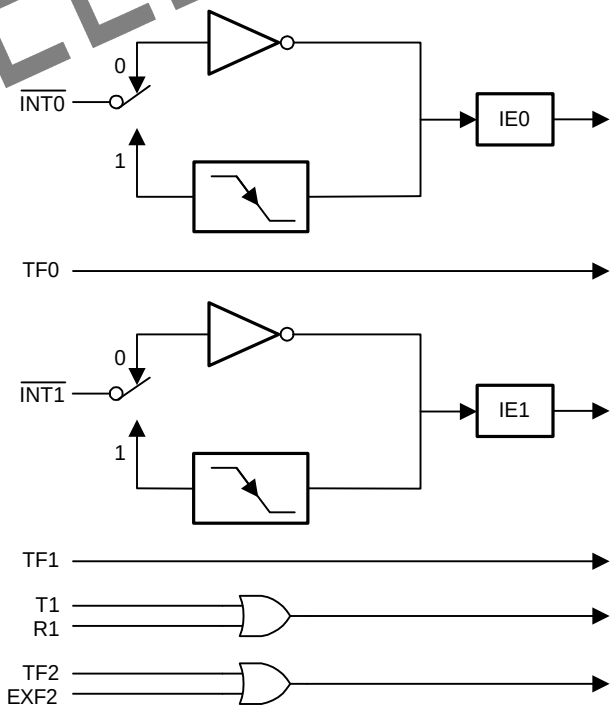


Figure 6. Interrupt Sources

DATA MEMORY

The AP160 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space. For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

MOV 0A0H, #data

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

MOV @R0, #data

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are avail-able as stack space.

POWER MANAGEMENT

IDLE MODE

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset. Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

POWER DOWN MODE

In the power down mode, the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The way to exit from power down mode is either hardware reset or external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V CC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

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Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

REDUCED EMI

All port pins of the AP160 have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

AUXR Address = 8EH

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	AO

NOTE: The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

EPROM PROGRAMMING MODE

The setup for programming and verification on-chip OPT EPROM of AP160 is shown in Figure 7 and Figure 8, independently. The address of the EPROM location to be programmed is applied to ports 1 and 2. The code byte to be programmed into that location and read verified data are applied to port 0. The programming, verifying, Write Lock bits and read signature byte mode are selectable by the pins of RST, PSEN, ALE/PROG, P2.6, P2.7, P3.6 and P3.7, as shown in table 8. The programming and verification waveform is shown in Figure 9. VCC must be rising to VCC1 during programming.

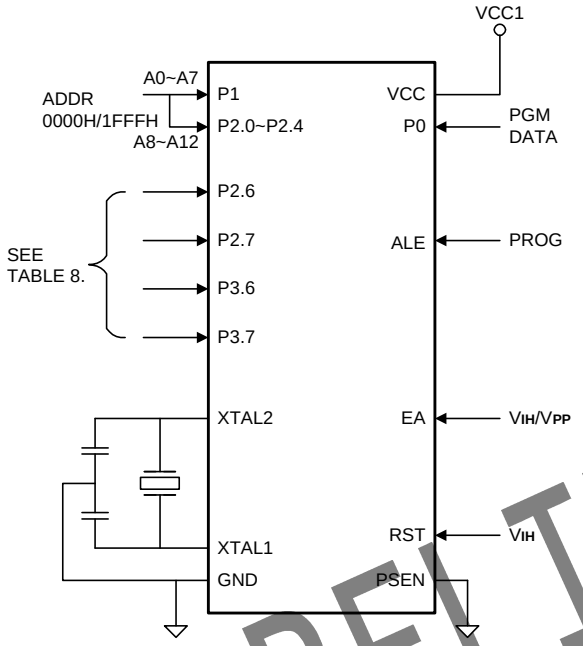


Figure 7. Programming the EPROM MEMORY

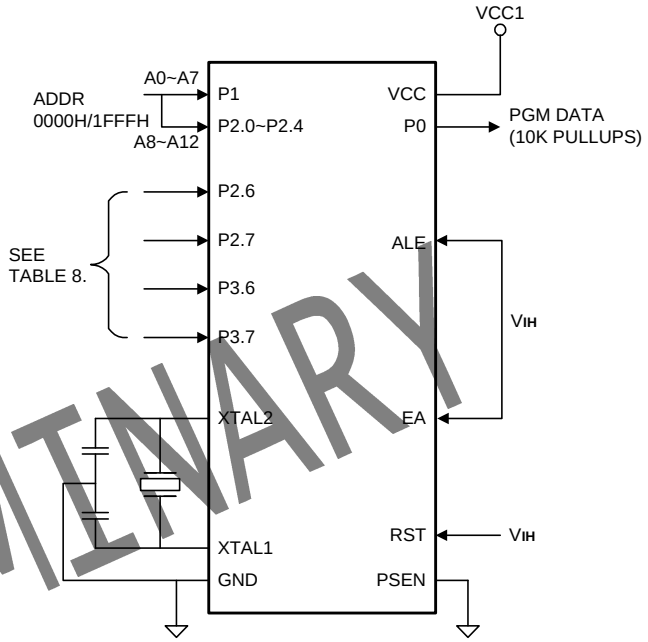


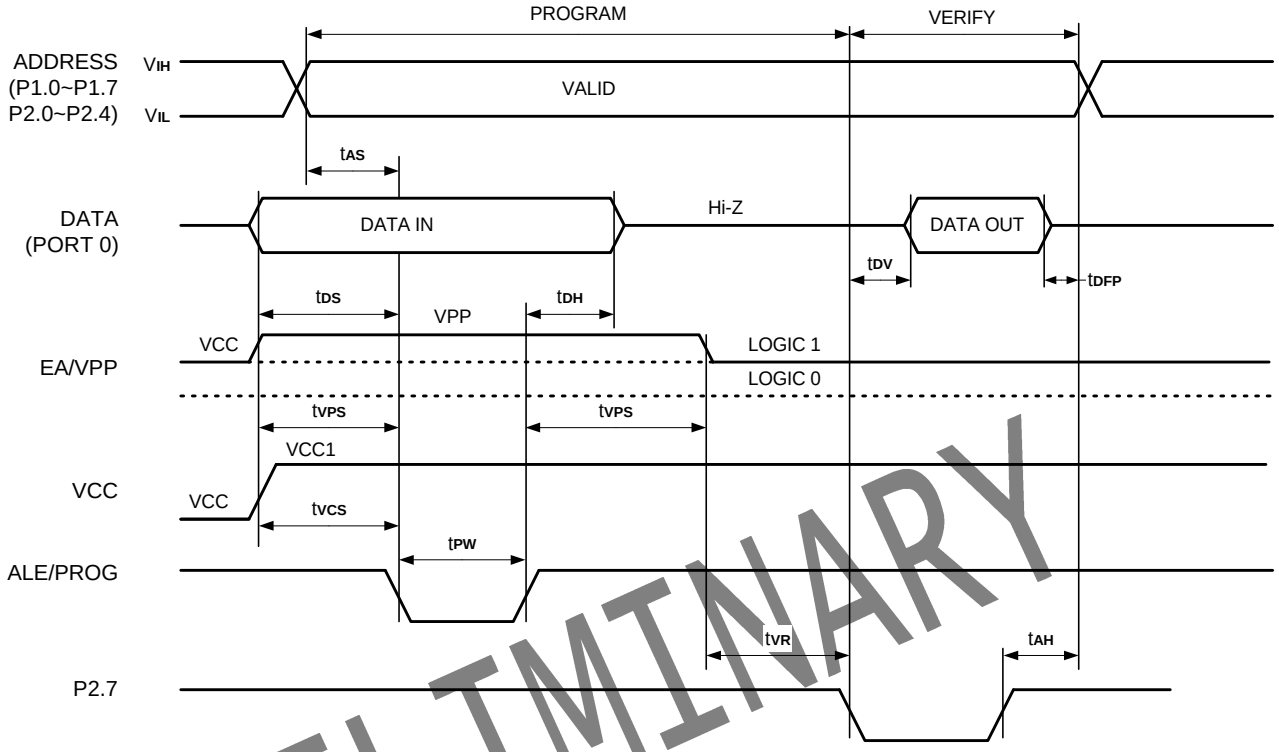
Figure 8. Verifying the EPROM MEMORY.

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
VPP	Programming Voltage	11.5	12.5	V	
VCC1	Programming Supply Voltage	6.0	6.5	V	
I_{PP}	VPP Current During Program		1.0	mA	ALE/PROG = V_{IL}
t_{AS}	Address Valid to Program Low	2		us	
t_{DS}	Input Valid to Program Low	2		us	
t_{VPS}	VPP Setup Time	2		us	
t_{VCS}	VCC Setup Time	2		us	
t_{PW}	Program Pulse Width	95	105	us	
t_{DH}	Data Hold Time	2		us	
t_{VR}	EA/VPP Recovery Time	2		us	
t_{DV}	Data Valid from P2.7		100	ns	
t_{DFP}	Chip Enable to Output Float Delay		130	ns	
t_{AH}	Address Hold Time	0		ns	

PRGRAMMING AND VERIFY MODE AC WAVEFORMS



PRELIMINARY

Table 8. EPROM PROGRAMMING MODE

Mode		RST	PSEN	ALE/PROG	EA/VPP	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L	⌥	12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit -1	H	L	⌥	12V	H	H	H	H
	Bit -2	H	L	⌥	12V	H	H	L	L
	Bit -3	H	L	⌥	12V	H	L	H	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: The signature bytes are read by the same procedure as a normal verification of locations 30H, 31H and 32H. The values returns are as follows:

(30H) = 37H indicates manufactured by AMIC.
(31H) = 6EH indicates embedded OTP device.
(32H) = 7FH indicates JEDEC continuation code.

PROGRAM MEMORY LOCK BITS

The AP160 has three lock bits that can be left unprogrammed(U) or can be programmed (P) to obtain the additional features listed in the following table.

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the OPT EPROM is disabled.
3	P	P	U	Same as mode 2, but verify is also disabled.
4	P	P	P	Same as mode 3, bur external execution is also disabled.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating temperature under bias	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Voltage on EA/V PP pin to V SS	0 to +12.5	V
Voltage on any other pin to V SS	-0.1 to +7.0	V
Maximum Operating Voltage	6.0	V
Maximum I OL per I/O pin	15.0	mA

NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERICSTICS

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 2.7V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except EA)	-0.5	0.2 VCC-0.1	V
V_{IL1}	Input Low Voltage (EA)		-0.5	0.2 VCC-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 VCC+0.9	VCC+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 VCC	VCC+0.5	V
V_{OL}	Output Low Voltage (Ports 1,2,3)	I_{OL} = 1.6mA		0.45	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN)	I_{OL} = 3.2mA		0.45	V
V_{OH}	Output High Voltage (Port 1,2,3, ALE, PSEN)	I_{OH} =-60uA, VCC=5V±10%	2.4		V
		I_{OH} =-25uA	0.75 VCC		V
		I_{OH} =-10uA	0.9 VCC		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} =-800uA, VCC=5V±10%	2.4		V
		I_{OH} =-300uA	0.75 VCC		V
		I_{OH} =-80uA	0.9 VCC		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} =0.45V		-50	uA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} =2V, VCC=5V±10%		-650	uA
I_{LI}	Input Leakage Current (Port 0, EA)	0.45< V_{IN} < VCC		±10	uA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. =1 MHZ, T_A =25°C		10	PF
I_{CC}	Power Supply Current	Active Mode, 12 MHZ		25	mA
		Idle Mode, 12MHZ		6.5	mA
	Power Down Mode	VCC = 5.5V		100	uA
		VCC = 3V		40	uA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10mA

Maximum I_{OL} per 8-biit port: Port 0: 26mA, Ports 1,2,3: 15mA

Maximum total I_{OL} for all output pins: 71mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink currenr greater than the listed test condition.

2. Minimum VCC for Power Down is 2V.

PRELIMINARY

AC CHARACTERISTICS

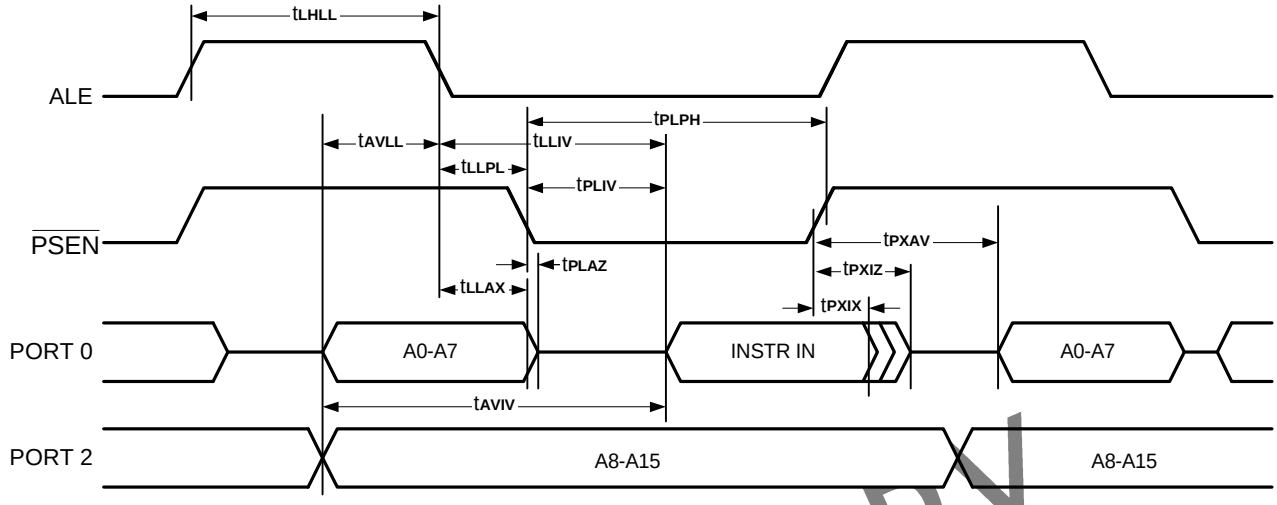
Under operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other outputs = 80 pF.

EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

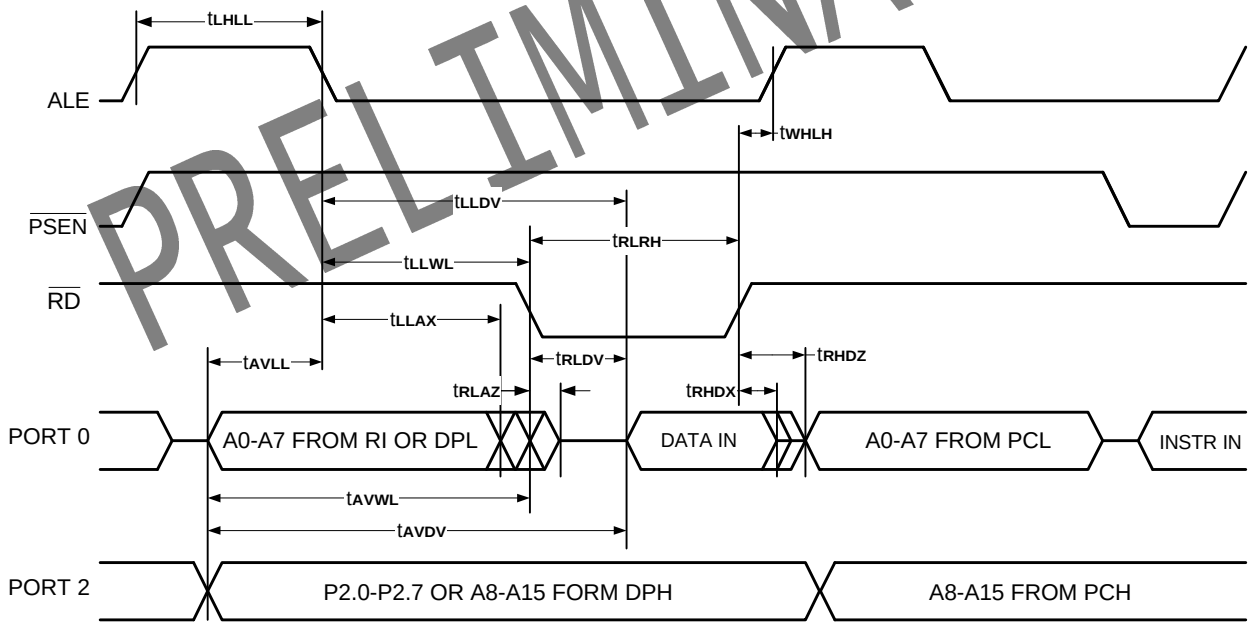
Symbol	Parameter	12MHZ Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	16	MHZ
t_{LHLL}	ALE Pulse Width	127		$2\,t_{CLCL}$ -40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL} -40		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL} -35		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4\,t_{CLCL}$ -100	ns
t_{LLPL}	ALE Low to PSEN Low	43		t_{CLCL} -40		ns
t_{PLPH}	PSEN Pulse Width	205		$3\,t_{CLCL}$ -45		ns
t_{PLIV}	PSEN Low to Valid Instruction In		145		$3\,t_{CLCL}$ -105	ns
t_{PXIX}	Input Instruction Hold After PSEN	0		0		ns
t_{PXIZ}	Input Instruction Float After PSEN		59		t_{CLCL} -25	ns
t_{PXAV}	PSEN to Address Valid	75		t_{CLCL} -8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5\,t_{CLCL}$ -105	ns
t_{PLAZ}	PSEN Low to Address Float		10		10	ns
t_{RLRH}	RD Pulse Width	400		$6\,t_{CLCL}$ -100		ns
t_{WLWH}	WR Pulse Width	400		$6\,t_{CLCL}$ -100		ns
t_{RLDV}	RD Low to Valid Data In		252		$5\,t_{CLCL}$ -165	ns
t_{RHDX}	Data Hold After RD	0		0		ns
t_{RHDZ}	Data Float After RD		97		$2\,t_{CLCL}$ -70	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8\,t_{CLCL}$ -150	ns
t_{AVDV}	Address to Valid Data In		585		$9\,t_{CLCL}$ -165	ns
t_{LLWL}	ALE Low to RD or WR Low	200	300	$3\,t_{CLCL}$ -50	$3\,t_{CLCL}$ +50	ns
t_{AVWL}	Address to RD or WR Low	203		$4\,t_{CLCL}$ -130		ns
t_{QVWX}	Data Valid to WR Transition	33		t_{CLCL} -50		ns
t_{QVWH}	Data Valid to WR High	433		$7\,t_{CLCL}$ -150		ns
t_{WHQX}	Data Hold After WR	33		t_{CLCL} -50		ns
t_{RLAZ}	RD low to Address Float		0		0	ns
t_{WHLH}	RD or WR High to ALE High	43	123	t_{CLCL} -40	t_{CLCL} +40	ns

PRELIMINARY

External Program Memory Read Cycle

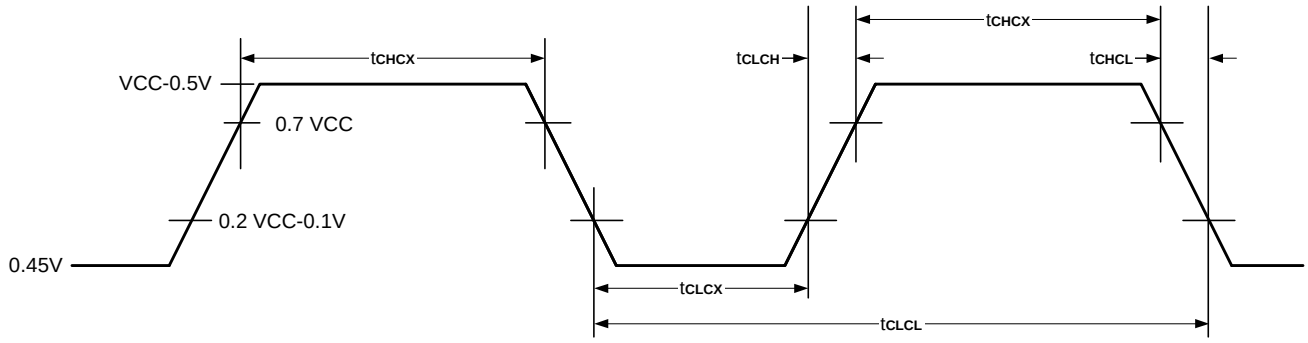


External Data Memory Read Cycle



PRELIMINARY

EXTERNAL CLOCK DRIVE WAVEFORMS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	16	MHZ
t_{CLCL}	Clock Period	62.5		ns
t_{CHCX}	High Time	20		ns
t_{CLCX}	Low Time	20		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall time		20	ns

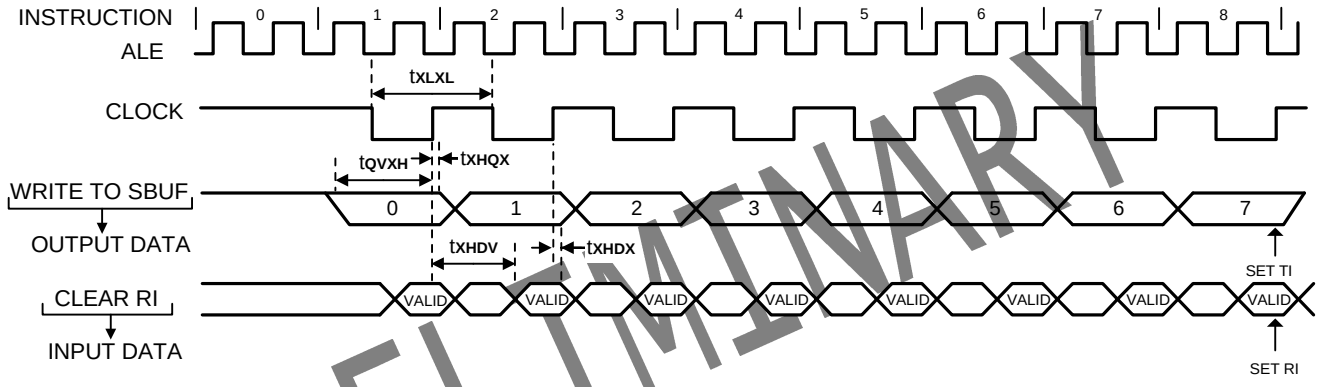
PRELIMINARY

SERIAL PORT TIMING: SHIFT REGISTER MODE TEST CONDITIONS

The values in this table are valid for VCC = 2.7V to 5.5V and Load Capacitance = 80pF

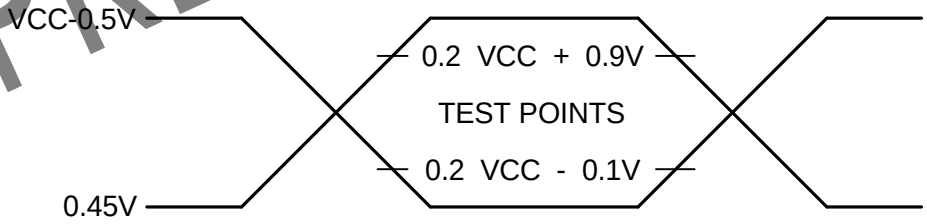
Symbol	Parameter	12MHZ Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		ns
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL} -133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL} -117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL} -133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



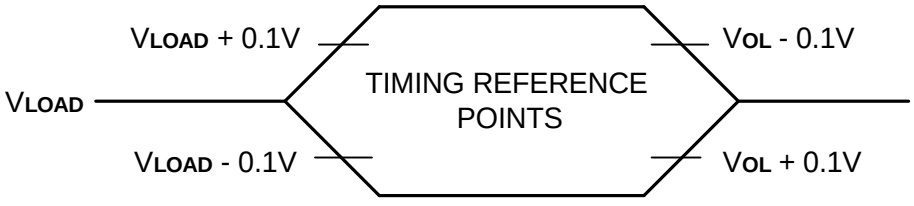
PRELIMINARY

AC TESTING INPUT/OUTPUT WAVEFORMS



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

FLOAT WAVEFORMS



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH} /V_{OL} level occurs.

ORDERING INFORMATION

Part Number	Package Type	Operation Temperature Range
AP160L	PLCC	-40°C ~ +85°C
AP160F	QFP	-40°C ~ +85°C

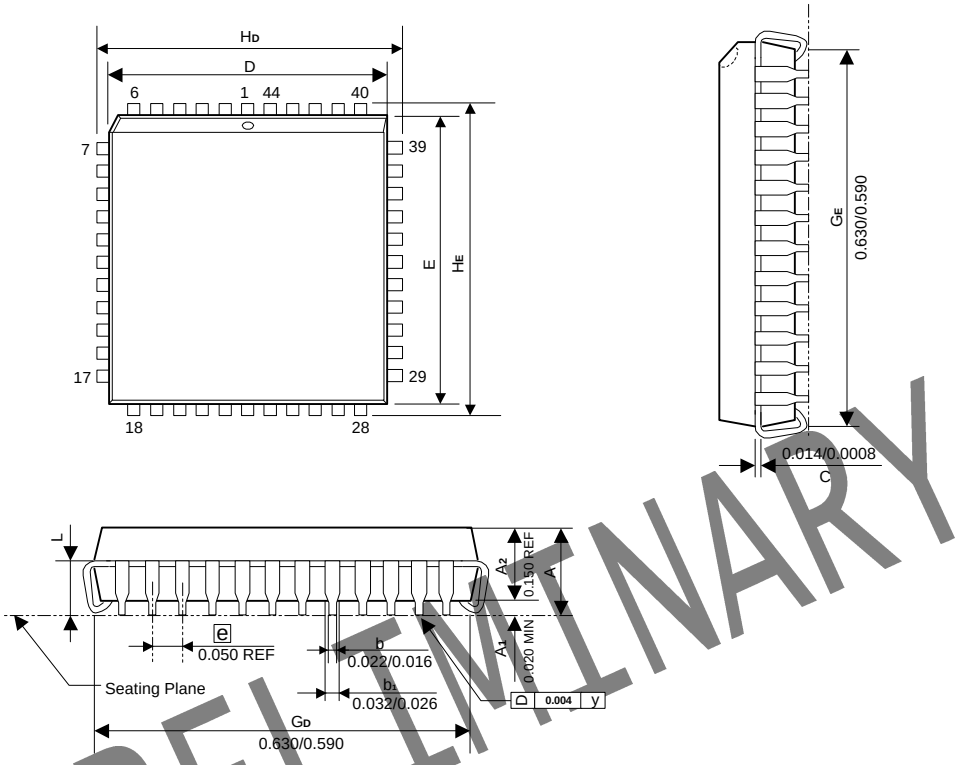
NOTE : AMIC Technology, Inc. reserves the right to make changes without prior notice.

PRELIMINARY

Package Information

PLCC 44L Outline Dimension

unit: inches/mm



PRELIMINARY

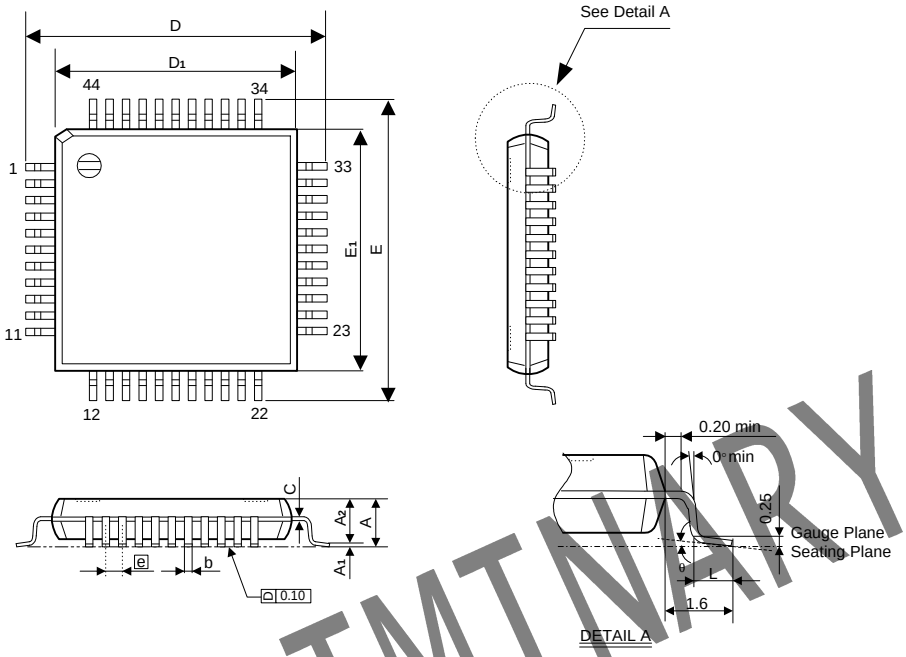
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.185	-	-	4.70
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Package Information

QFP 44L Outline Dimensions

unit: inches/mm



PRELIMINARY

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.106	-	-	2.7
A_1	0.010	0.012	0.014	0.25	0.30	0.35
A_2	0.0748	0.0787	0.0866	1.9	2.0	2.2
b	0.012 TYP			0.3 TYP		
D	0.5118	0.5196	0.5274	13.00	13.20	13.40
D_1	0.3897	0.3937	0.3977	9.9	10.00	10.10
E	0.5118	0.5196	0.5275	13.00	13.20	13.40
E_1	0.3897	0.3937	0.3977	9.9	10.00	10.10
L	0.0287	0.0346	0.0366	0.73	0.88	0.93
e	0.0315 TYP			0.80 TYP		
C	0.0021	0.0060	0.0099	0.1	0.15	0.2
θ	0°	-	7°	0°	-	7°

Notes:
1. Dimensions D_1 and E_1 do not include mold protrusion.
2. Dimension b does not include dambar protrusion.

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