Features

- Integrated PLL Loop Filter
- ESD Protection (4 kV HBM/200V MM; Except Pin 2: 4 kV HBM/100V MM) also at ANT1/ANT2
- High Output Power (8.0 dBm) with Low Supply Current (9.0 mA)
- Modulation Scheme ASK/FSK
  - FSK Modulation is Achieved by Connecting an Additional Capacitor Between the XTAL Load Capacitor and the Open Drain Output of the Modulating Microcontroller
- Easy to Design-in Due to Excellent Isolation of the PLL from the PA and Power Supply
- Single Li-cell for Power Supply
- Supply Voltage 2.0V to 4.0V in the Temperature Range of –40°C to +85°C
- Package TSSOP8L
- Single-ended Antenna Output with High Efficient Power Amplifier
- CLK Output for Clocking the Microcontroller
- One-chip Solution with Minimum External Circuitry

Applications

- Industrial/Aftermarket Remote Keyless Entry Systems
- Alarm, Telemetering, and Energy Metering Systems
- Remote Control Systems for Consumer and Industrial Markets
- Access Control Systems
- Home Automation
- Home Entertainment
- Toys

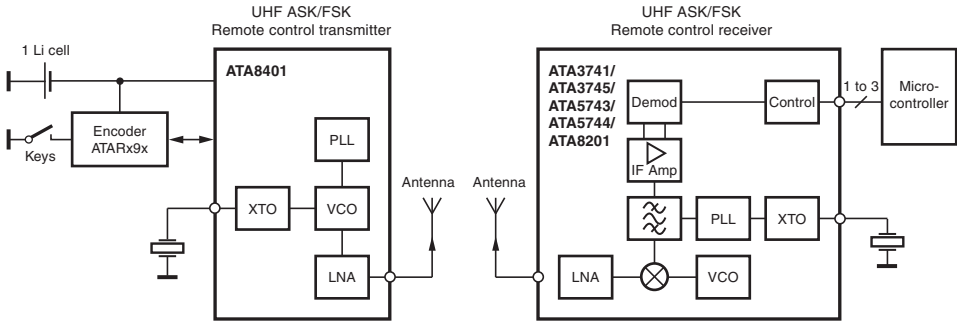
UHF ASK/FSK Industrial Transmitter

ATA8401

1. Description

The ATA8401 is a PLL transmitter IC, which has been developed for the demands of RF low-cost transmission systems for industrial applications at data rates up to 50 kBaud ASK and 32 kBaud FSK modulation scheme. The transmitting frequency range is 310 MHz to 350 MHz. It can be used in both FSK and ASK systems.

Figure 1-1. System Block Diagram



4984B–INDCO–11/08

2. Pin Configuration

Figure 2-1. Pinning TSSOP8L

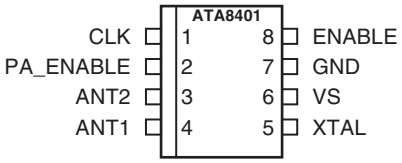


Table 2-1. Pin Description

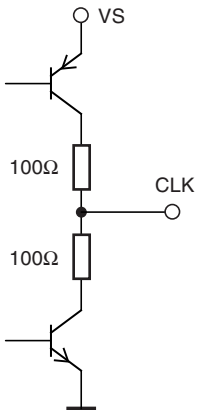
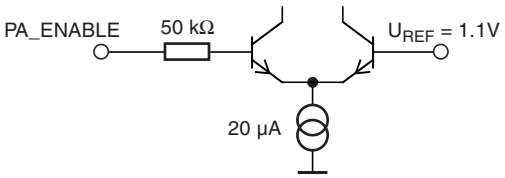
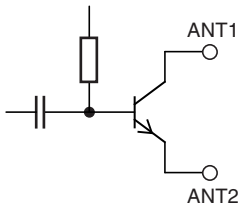
Pin	Symbol	Function	Configuration
1	CLK	Clock output signal for microcontroller The clock output frequency is set by the crystal to $f_{XTAL}/4$	
2	PA_ENABLE	Switches on power amplifier used for ASK modulation	
3 4	ANT2 ANT1	Emitter of antenna output stage Open collector antenna output	

Table 2-1. Pin Description (Continued)

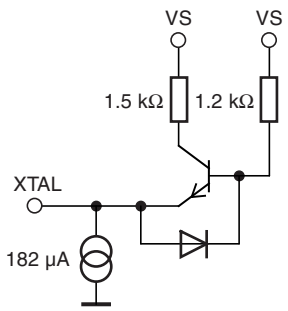
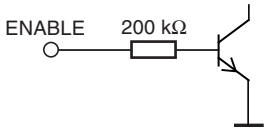
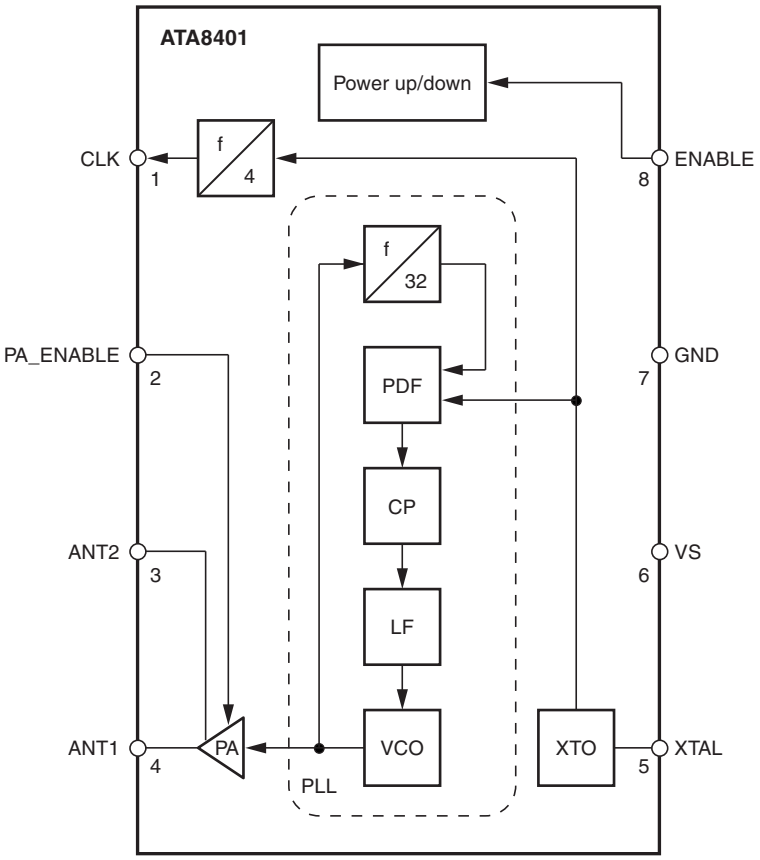
Pin	Symbol	Function	Configuration
5	XTAL	Connection for crystal	
6	VS	Supply voltage	See ESD protection circuitry (see Figure 4-5 on page 9)
7	GND	Ground	See ESD protection circuitry (see Figure 4-5 on page 9)
8	ENABLE	Enable input	

Figure 2-2. Block Diagram



3. General Description

This fully integrated PLL transmitter allows particularly simple, low-cost RF miniature transmitters to be assembled. The VCO is locked to 32 f_{XTAL}, and therefore a 9.8438 MHz crystal is needed for a 315 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL typically needs < 3 ms until the PLL is locked and the CLK output is stable. There is a wait time of ≥ 3 ms until the CLK is used for the microcontroller and the PA is switched on.

The power amplifier is an open-collector output delivering a current pulse, which is nearly independent from the load impedance. The delivered output power is therefore controllable via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50 Ω. A high power efficiency of $\eta = P_{out}/(I_{S,PA} \ V_S)$ of 40% for the power amplifier results when an optimized load impedance of Z_{Load} = (255 + j192) Ω is used at 3V supply voltage.

4. Functional Description

If ENABLE = L and the PA_ENABLE = L, the circuit is in standby mode, consuming only a very small amount of current, so that a lithium cell used as power supply can work for several years.

With ENABLE = H the XTO, PLL, and the CLK driver are switched on. If PA_ENABLE remains L, only the PLL and the XTO are running, and the CLK signal is delivered to the microcontroller. The VCO locks to 32 times the XTO frequency.

With ENABLE = H and PA_ENABLE = H the PLL, XTO, CLK driver, and the power amplifier are on. The power amplifier can be switched on and off with PA_ENABLE. This is used to perform the ASK modulation.

4.1 ASK Transmission

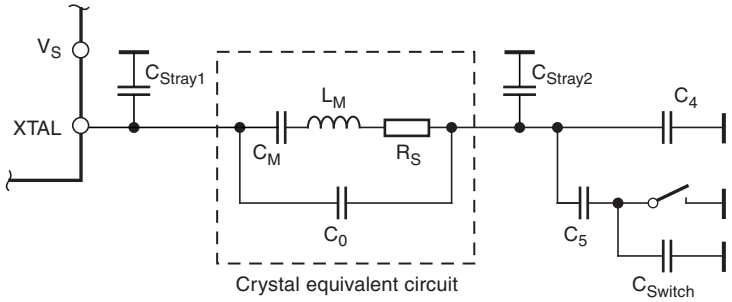
The ATA8401 is activated by ENABLE = H. PA_ENABLE must remain L for typically ≥ 3 ms, then the CLK signal can be taken to clock the microcontroller and the output power can be modulated by means of the PA_ENABLE pin. After transmission, PA_ENABLE is switched to L and the microcontroller switches back to internal clocking. The ATA8401 is switched back to standby mode with ENABLE = L.

4.2 FSK Transmission

The ATA8401 is activated by ENABLE = H. PA_ENABLE must remain L for typically ≥ 3 ms, then the CLK signal can be taken to clock the microcontroller, and the power amplifier is switched on with PA_ENABLE = H. The chip is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. If the switch is closed, the output frequency is lower than if the switch is open. After transmission, PA_ENABLE is switched to L, and the microcontroller switches back to internal clocking. The ATA8401 is switched back to standby mode with ENABLE = L.

The accuracy of the frequency deviation with XTAL pulling method is about ±25% when the following tolerances are considered.

Figure 4-1. Tolerances of Frequency Modulation



Using C_4 = 8.2 pF ±5%, C_5 = 10 pF ±5%, a switch port with C_{Switch} = 3 pF ±10%, stray capacitances on each side of the crystal of $C_{Stray1} = C_{Stray2}$ = 1 pF ±10%, a parallel capacitance of the crystal of C_0 = 3.2 pF ±10%, and a crystal with C_M = 13 fF ±10%, typically results in an FSK deviation of ±21.5 kHz with worst case tolerances of ±16.25 kHz to ±28.01 kHz.

4.3 CLK Output

An output CLK signal is provided for a connected microcontroller. The delivered signal is CMOS compatible if the load capacitance is lower than 10 pF.

4.3.1 Clock Pulse Take-over

The clock of the crystal oscillator can be used for clocking the microcontroller. A special feature of Atmel®'s ATARx9x is that it starts with an integrated RC-oscillator to switch on the ATA8401 with ENABLE = H, and after 3 ms assumes the clock signal of the transmission IC, so that the message can be sent with crystal accuracy.

4.3.2 Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of $Z_{Load,opt}$ = (255 + j192)Ω. There must be a low resistive path to V_S to deliver the DC current.

The delivered current pulse of the power amplifier is 9 mA. The maximum output power is delivered to a resistive load of 400Ω if the 1.0 pF output capacitance of the power amplifier is compensated by the load impedance.

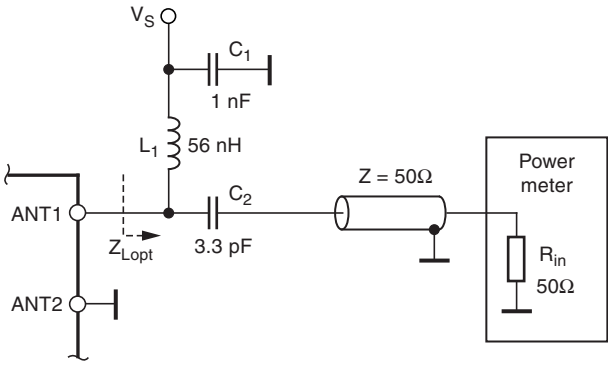
An optimum load impedance of:
Z_{Load} = 400Ω || j/(2 × π 1.0 pF) = (255 + j192)Ω thus results for the maximum output power of 8 dBm.

The load impedance is defined as the impedance seen from the ATA8401's ANT1, ANT2 into the matching network. Do not confuse this large signal load impedance with a small signal input impedance delivered as input characteristic of RF amplifiers and measured from the application into the IC instead of from the IC into the application for a power amplifier.

Less output power is achieved by lowering the real parallel part of 400Ω where the parallel imaginary part should be kept constant.

Output power measurement can be done with the circuit shown in Figure 4-2. Note that the component values must be changed to compensate for the individual board parasitics until the ATA8401 has the right load impedance $Z_{Load,opt}$ = (255 + j192)Ω. Also the damping of the cable used to measure the output power must be calibrated out.

Figure 4-2. Output Power Measurement at f = 315 MHz



Note: For 345 MHz C_2 has to be changed to 2.7 pF

4.4 Application Circuit

A value of C_3 = 68 nF/X7R is recommended for the supply-voltage blocking capacitor C_3 (see Figure 4-3 on page 7 and Figure 4-4 on page 8). C_1 and C_2 are used to match the loop antenna to the power amplifier where C_1 typically is 22 pF/NP0 and C_2 is 10.8 pF/NP0 (18 pF + 27 pF in series). For C_2, two capacitors in series should be used to achieve a better tolerance value and to have the possibility of realizing the $Z_{Load,opt}$ using standard valued capacitors.

C_1, together with the pins of ATA8401 and the PCB board wires, forms a series resonance loop that suppresses the 1st harmonic. Therefore, the position of C_1 on the PCB is important. Normally the best suppression is achieved when C_1 is placed as close as possible to the pins ANT1 and ANT2.

The loop antenna should not exceed a width of 1.5 mm, otherwise the Q-factor of the loop antenna is too high.

L_1 ([50 nH to 100 nH) can be printed on PCB. C_4 should be selected so that the XTO runs on the load resonance frequency of the crystal. Normally, a 15 pF load-capacitance crystal results in a value of 12 pF.

Figure 4-3. ASK Application Circuit

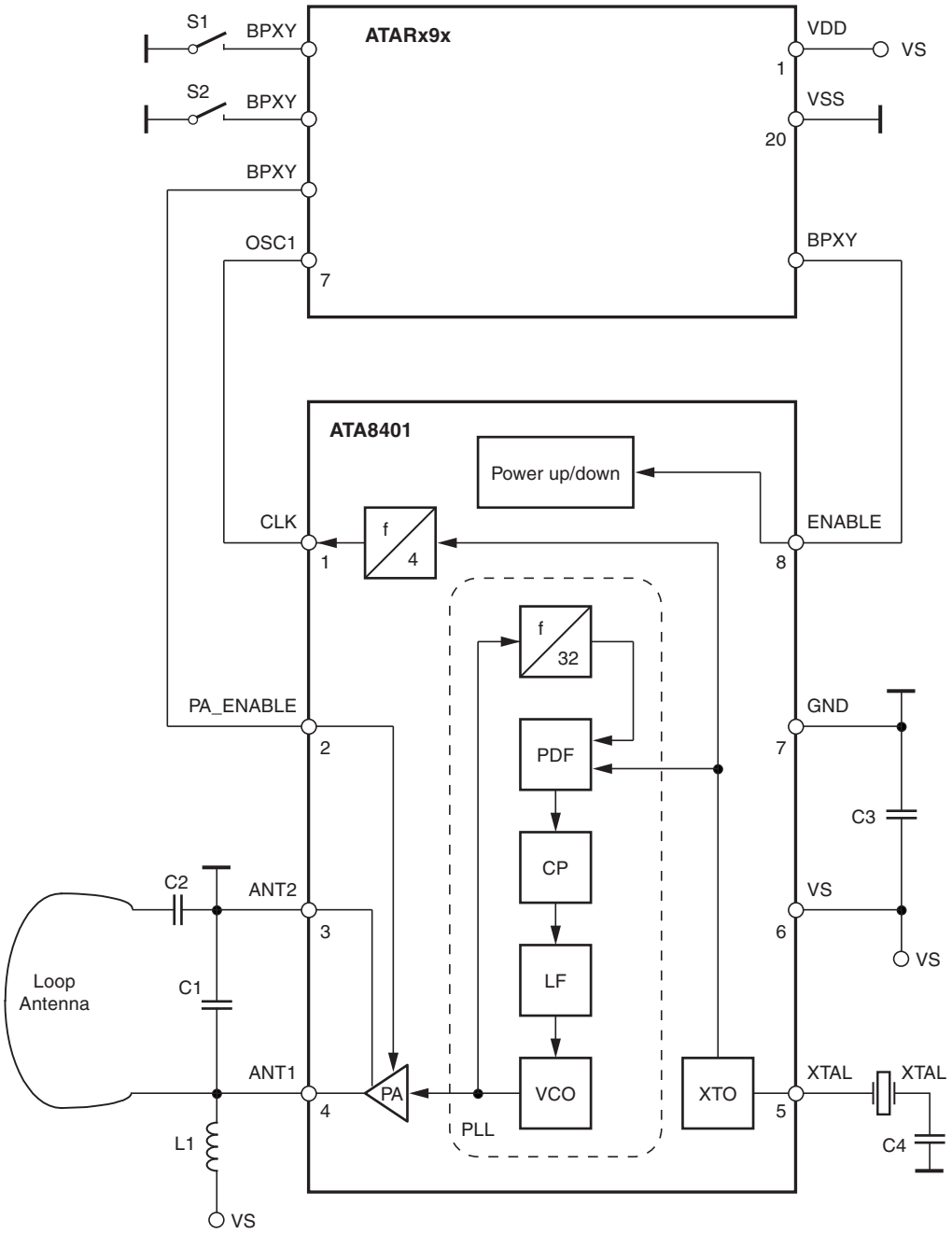


Figure 4-4. FSK Application Circuit

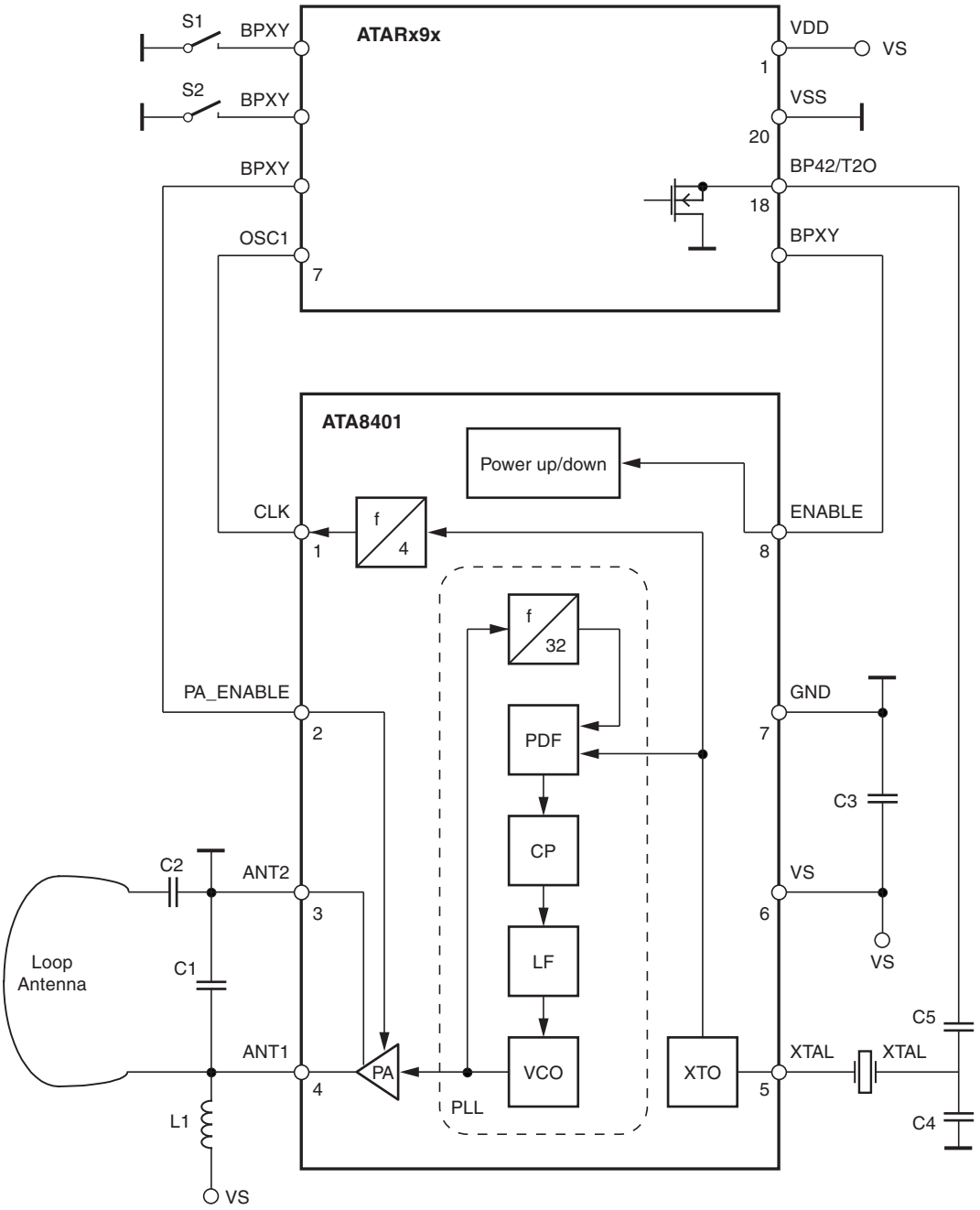
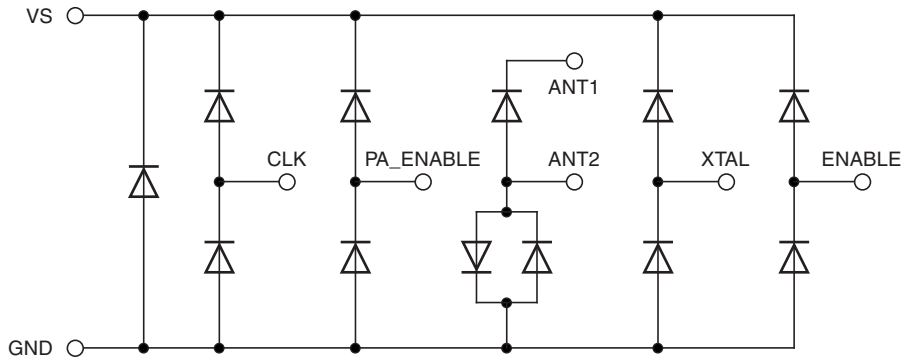


Figure 4-5. ESD Protection Circuit



5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Minimum	Maximum	Unit
Supply voltage	V_S		5	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	+85	°C
Ambient temperature	T_{amb}	–55	+85	°C
Input voltage	V_{maxPA_ENABLE}	–0.3	$(V_S + 0.3)^{(1)}$	V

Note: 1. If V_S + 0.3 is higher than 3.7V, the maximum voltage will be reduced to 3.7V.

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	170	K/W

7. Electrical Characteristics

V_S = 2.0V to 4.0V, T_{amb} = 25°C unless otherwise specified.
Typical values are given at V_S = 3.0V and T_{amb} = 25°C. All parameters are referred to GND (pin 7).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply current	Power down, V_{ENABLE} < 0.25V, –40°C to 85°C $V_{PA\text{-}ENABLE}$ < 0.25V, 25°C (100% correlation tested)	I_{S_Off}		< 10	350	nA nA
Supply current	Power up, PA off, V_S = 3V, V_{ENABLE} > 1.7V, $V_{PA\text{-}ENABLE}$ < 0.25V	I_S		3.7	4.8	mA
Supply current	Power up, V_S = 3.0V, V_{ENABLE} > 1.7V, $V_{PA\text{-}ENABLE}$ > 1.7V	$I_{S_Transmit}$		9	11.6	mA

Note: 1. If V_S is higher than 3.6V, the maximum voltage will be reduced to 3.6V.

7. Electrical Characteristics (Continued)

V_S = 2.0V to 4.0V, T_{amb} = 25°C unless otherwise specified.
Typical values are given at V_S = 3.0V and T_{amb} = 25°C. All parameters are referred to GND (pin 7).

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Output power	V_S = 3.0V, T_{amb} = 25°C, f = 315 MHz, Z_{Load} = (255 + j192)W	P_{Ref}	6.0	8.0	10.5	dBm
Output power variation for the full temperature range	T_{amb} = 25°C, V_S = 3.0V V_S = 2.0V	 ΔP_{Ref} ΔP_{Ref}			 –1.5 –4.0	 dB dB
Output power variation for the full temperature range	T_{amb} = 25°C, V_S = 3.0V V_S = 2.0V, $P_{Out} = P_{Ref} + \Delta P_{Ref}$	 ΔP_{Ref} ΔP_{Ref}			 –2.0 –4.5	 dB dB
Achievable output-power range	Selectable by load impedance	P_{Out_typ}	0		8.0	dBm
Spurious emission	$f_{CLK} = f_0/128$ Load capacitance at pin CLK = 10 pF $f_O \pm 1 \times f_{CLK}$ $f_O \pm 4 \times f_{CLK}$ Other spurious are lower			 –55 –52		 dBc dBc
Oscillator frequency XTO (= phase comparator frequency)	$f_{XTO} = f_0/32$ f_{XTAL} = resonant frequency of the XTAL, $C_M \leq 10$ fF, load capacitance selected accordingly T_{amb} = 25°C	f_{XTO}		f_{XTAL}		ppm
PLL loop bandwidth				250		kHz
Phase noise of phase comparator	Referred to $f_{PC} = f_{XT0}$, 25 kHz distance to carrier			–116	–110	dBc/Hz
In-loop phase noise PLL	25 kHz distance to carrier			–86	–80	dBc/Hz
Phase noise VCO	At 1 MHz At 36 MHz			–94 –125	–90 –121	dBc/Hz dBc/Hz
Frequency range of VCO		f_{VCO}	310		350	MHz
Clock output frequency (CMOS microcontroller compatible)				$f_0/128$		MHz
Voltage swing at pin CLK	$C_{Load} \leq 10$ pF	V_{0h} V_{0l}	$V_S \times 0.8$		$V_S \times 0.2$	V V
Series resonance R of the crystal		Rs			110	Ω
Capacitive load at pin XT0					7	pF
FSK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ASK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		50	kHz
ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	 1.7		0.25 20	V V µA
PA_ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	 1.7		0.25 V_S (1) 5	V V µA

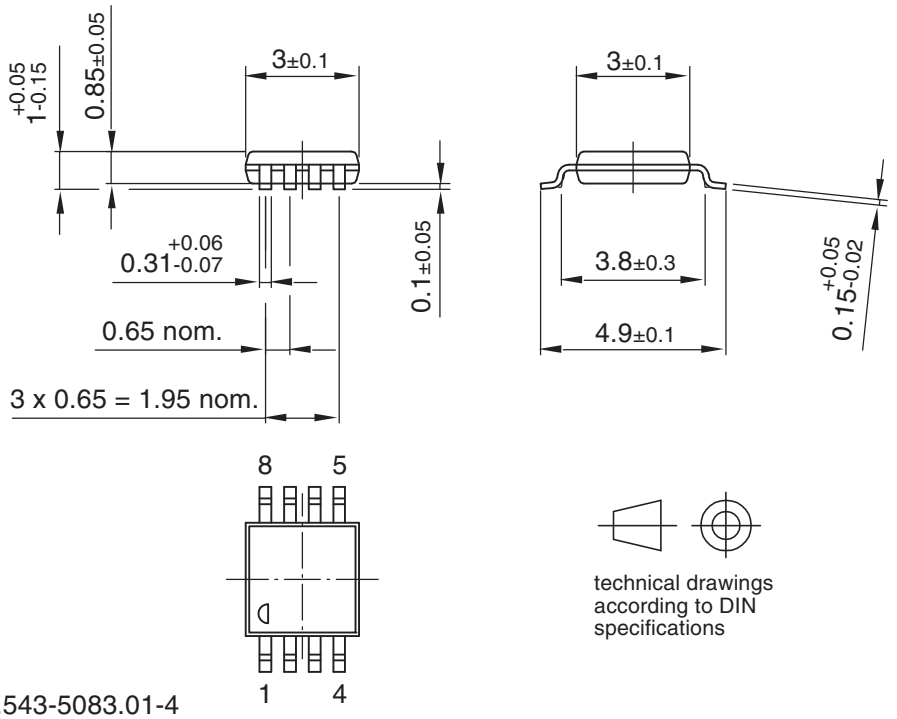
Note: 1. If V_S is higher than 3.6V, the maximum voltage will be reduced to 3.6V.

8. Ordering Information

Extended Type Number	Package	MOQ	Remarks
ATA8401-6AQY	TSSOP8L	5000 pcs	Taped and reeled, Pb-free

9. Package Information

Package: TSSOP 8L
Dimensions in mm



Drawing-No.: 6.543-5083.01-4
Issue: 2; 15.03.04

10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4984B-INDCO-11/08	• Put datasheet in the newest template • Section 4.3.1 “Clock Pulse Take-over” on page 5 changed

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