

HD74HC680

12-bit Address Comparator

REJ03D0641-0200
(Previous ADE-205-527)
Rev.2.00
Mar 30, 2006

Description

The HD74HC680 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A₁ through A₇ must be low and that inputs A₈ through A₁₂ must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The HD74HC680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

Features

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max (T_a = 25°C)
- Ordering Information

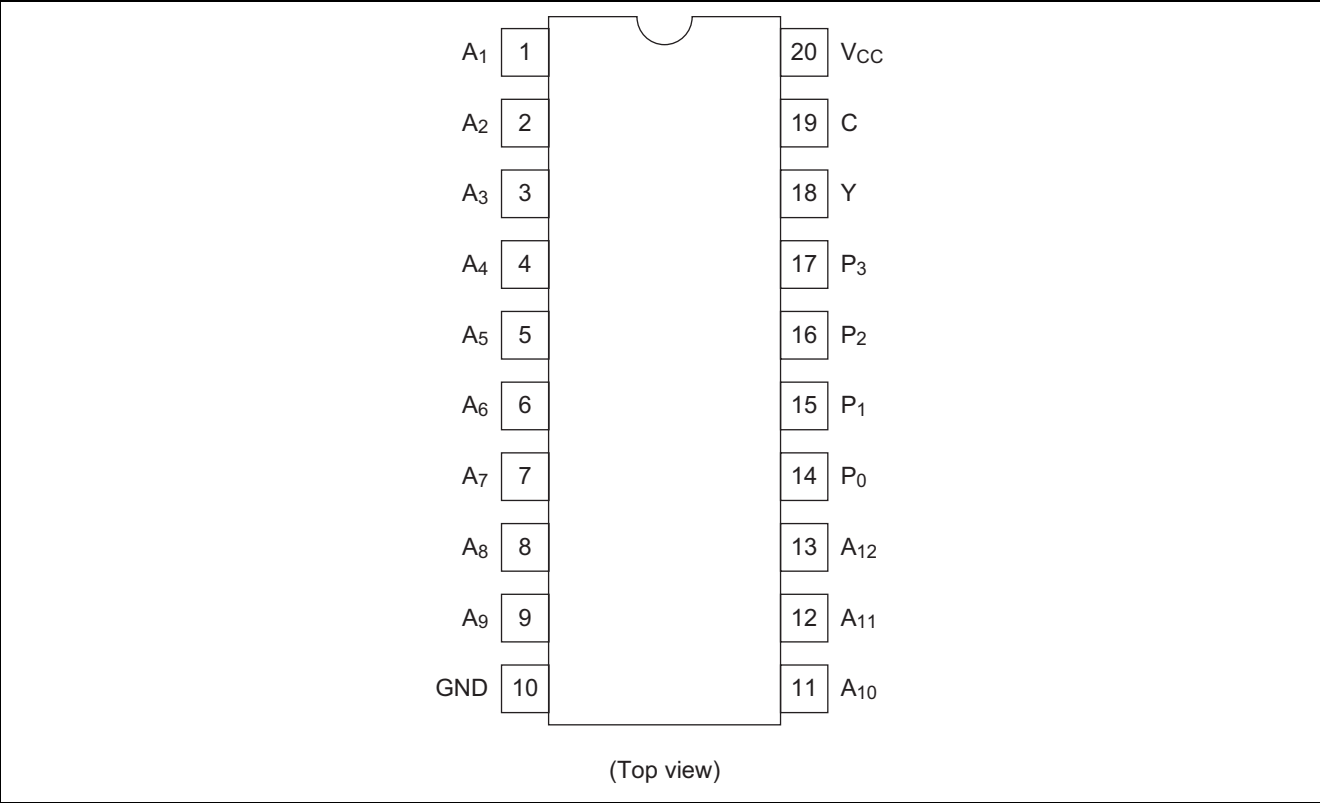
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC680RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Function Table

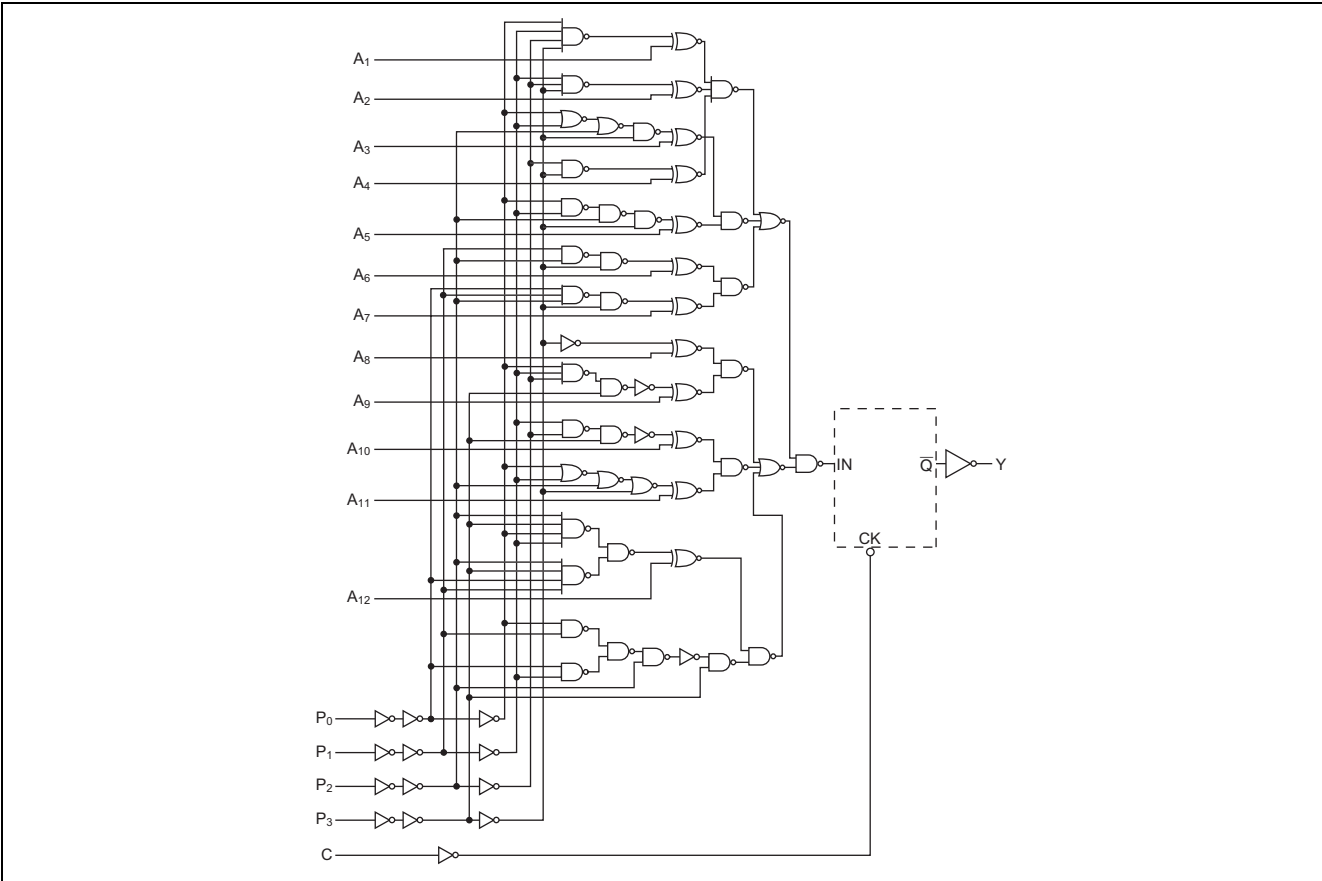
C	Inputs																Output Y
	P ₃	P ₂	P ₁	P ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	A ₈	A ₉	A ₁₀	A ₁₁	A ₁₂	
H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
H	All other combinations																H
L	Any combination																Latched

H : high level
L : low level
X : irrelevant

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0 \text{ V}$
		0 to 500		$V_{CC} = 4.5 \text{ V}$
		0 to 400		$V_{CC} = 6.0 \text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

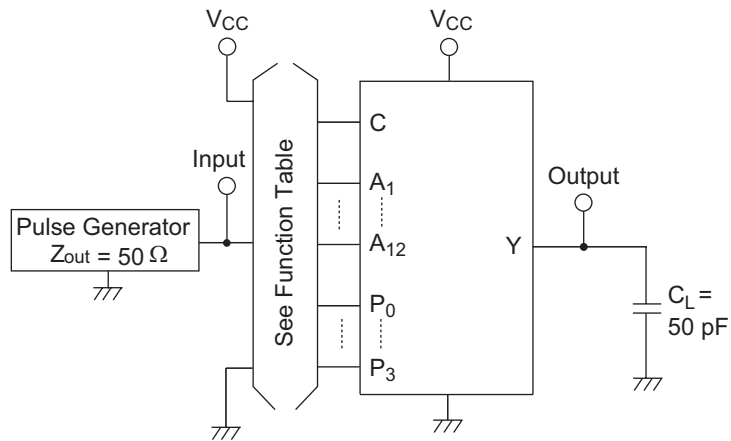
Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA
		4.5	4.4	4.5	—	4.4	—			I _{OH} = -4 mA
		6.0	5.9	6.0	—	5.9	—			I _{OH} = -5.2 mA
		4.5	4.18	—	—	4.13	—			I _{OL} = 20 μA
		6.0	5.68	—	—	5.63	—			
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			I _{OL} = 4 mA
		4.5	—	—	0.26	—	0.33			
		6.0	—	—	0.26	—	0.33			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

Switching Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Propagation delay time	t _{PLH}	2.0	—	—	330	—	410	ns	P to Y	
		t _{PHL}	4.5	—	26	66	—			82
			6.0	—	—	56	—			70
	t _{PLH}	2.0	—	—	210	—	265	ns	A to Y	
		t _{PHL}	4.5	—	19	42	—			53
			6.0	—	—	36	—			45
	t _{PLH}	2.0	—	—	150	—	190	ns	C to Y	
		t _{PHL}	4.5	—	18	30	—			38
			6.0	—	—	26	—			33
Setup time	t _{SU}	2.0	100	—	—	125	—	ns	A to C	
		4.5	20	12	—	25	—			
		6.0	17	—	—	21	—			
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns		
		t _{THL}	4.5	—	6	15	—			19
			6.0	—	—	13	—			16
Input capacitance	C _{in}	—	—	5	10	—	10	pF		

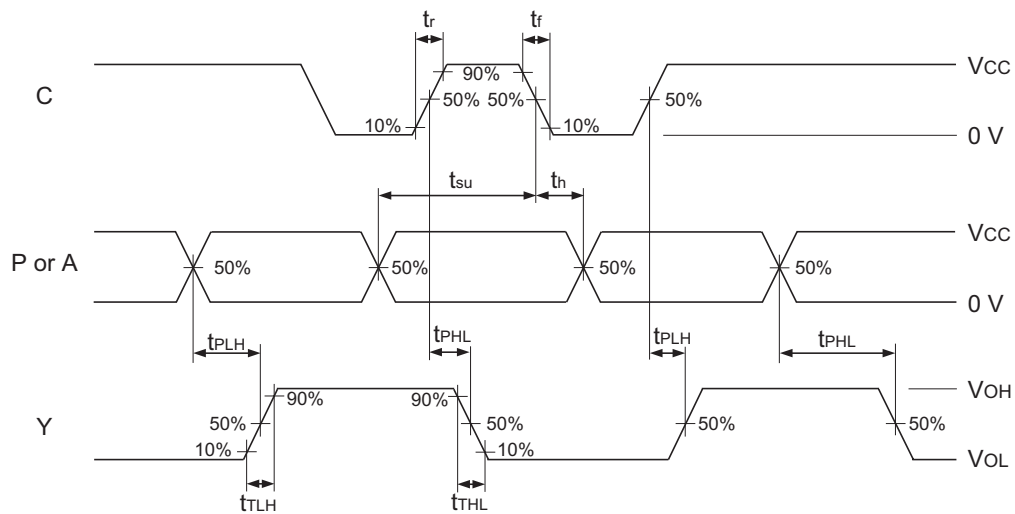
Test Circuit



Note : 1. C_L includes probe and jig capacitance.

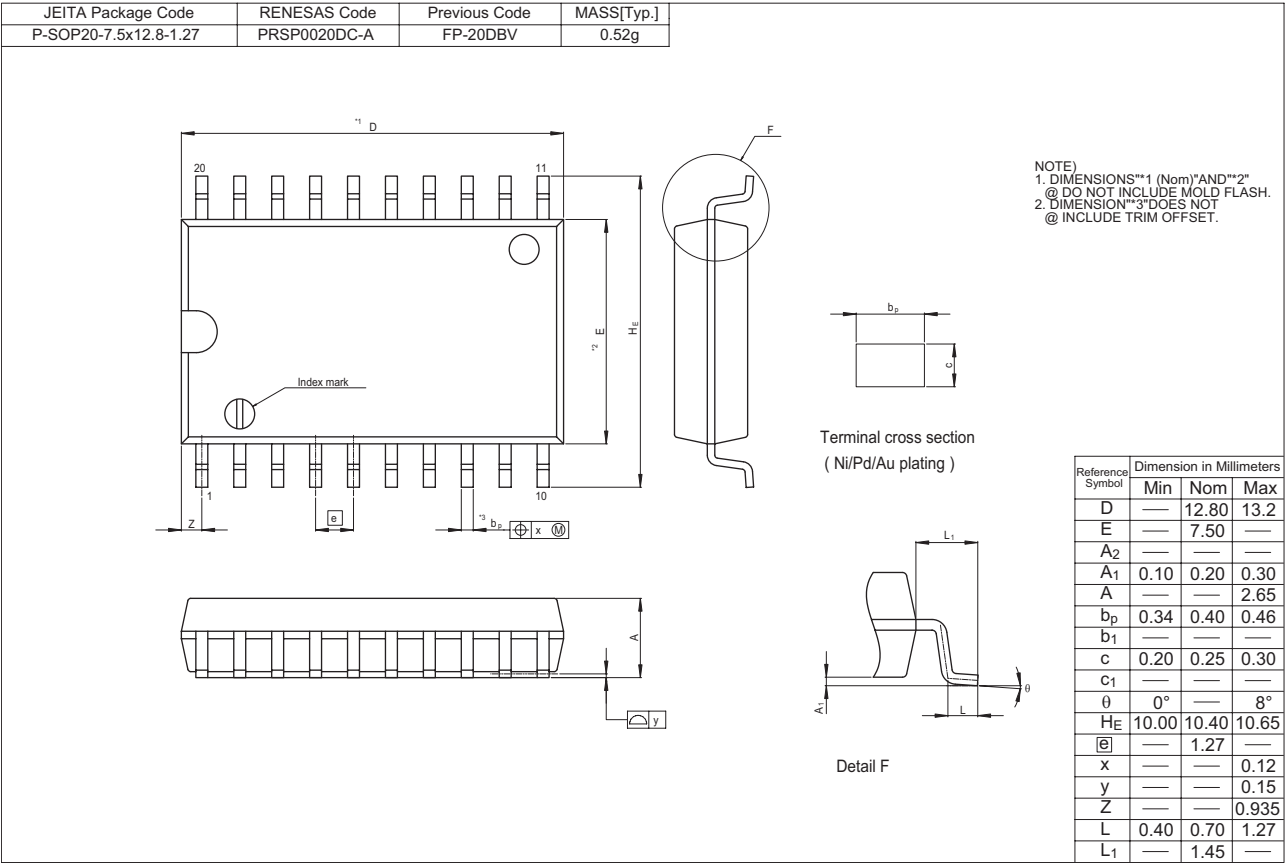
Waveforms

• Waveform



Note : 1. Input waveform : PRR $\leq$ 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

Package Dimensions



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