# HD74HC680

## 12-bit Address Comparator

REJ03D0641-0200
(Previous ADE-205-527)
Rev.2.00
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## Description

The HD74HC680 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs $A_1$ through $A_7$ must be low and that inputs $A_8$ through $A_{12}$ must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The HD74HC680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

## Features

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC}$ = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: $I_{CC}$ (static) = 4 µA max (Ta = 25°C)
- Ordering Information

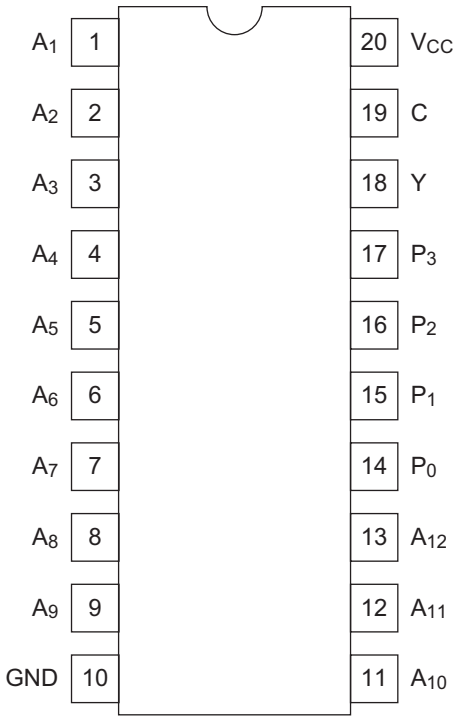
| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74HC680RPEL | SOP-20 pin (JEDEC) | PRSP0020DC-A (FP-20DBV) | RP | EL (1,000 pcs/reel) |

## Function Table

| C | Inputs | | | | | | | | | | | | | | | | Output Y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $P_3$ | $P_2$ | $P_1$ | $P_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | |
| H | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| H | L | L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | L |
| H | L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | L |
| H | L | L | H | H | L | L | L | H | H | H | H | H | H | H | H | H | L |
| H | L | H | L | L | L | L | L | L | H | H | H | H | H | H | H | H | L |
| H | L | H | L | H | L | L | L | L | L | H | H | H | H | H | H | H | L |
| H | L | H | H | L | L | L | L | L | L | L | H | H | H | H | H | H | L |
| H | L | H | H | H | L | L | L | L | L | L | L | H | H | H | H | H | L |
| H | H | L | L | L | L | L | L | L | L | L | L | L | H | H | H | H | L |
| H | H | L | L | H | L | L | L | L | L | L | L | L | L | H | H | H | L |
| H | H | L | H | L | L | L | L | L | L | L | L | L | L | L | H | H | L |
| H | H | L | H | H | L | L | L | L | L | L | L | L | L | L | L | H | L |
| H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L |
| H | H | H | L | H | X | X | X | X | X | X | X | X | X | X | X | X | H |
| H | H | H | H | L | X | X | X | X | X | X | X | X | X | X | X | X | H |
| H | H | H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L |
| H | All other combinations | | | | | | | | | | | | | | | | H |
| L | Any combination | | | | | | | | | | | | | | | | Latched |

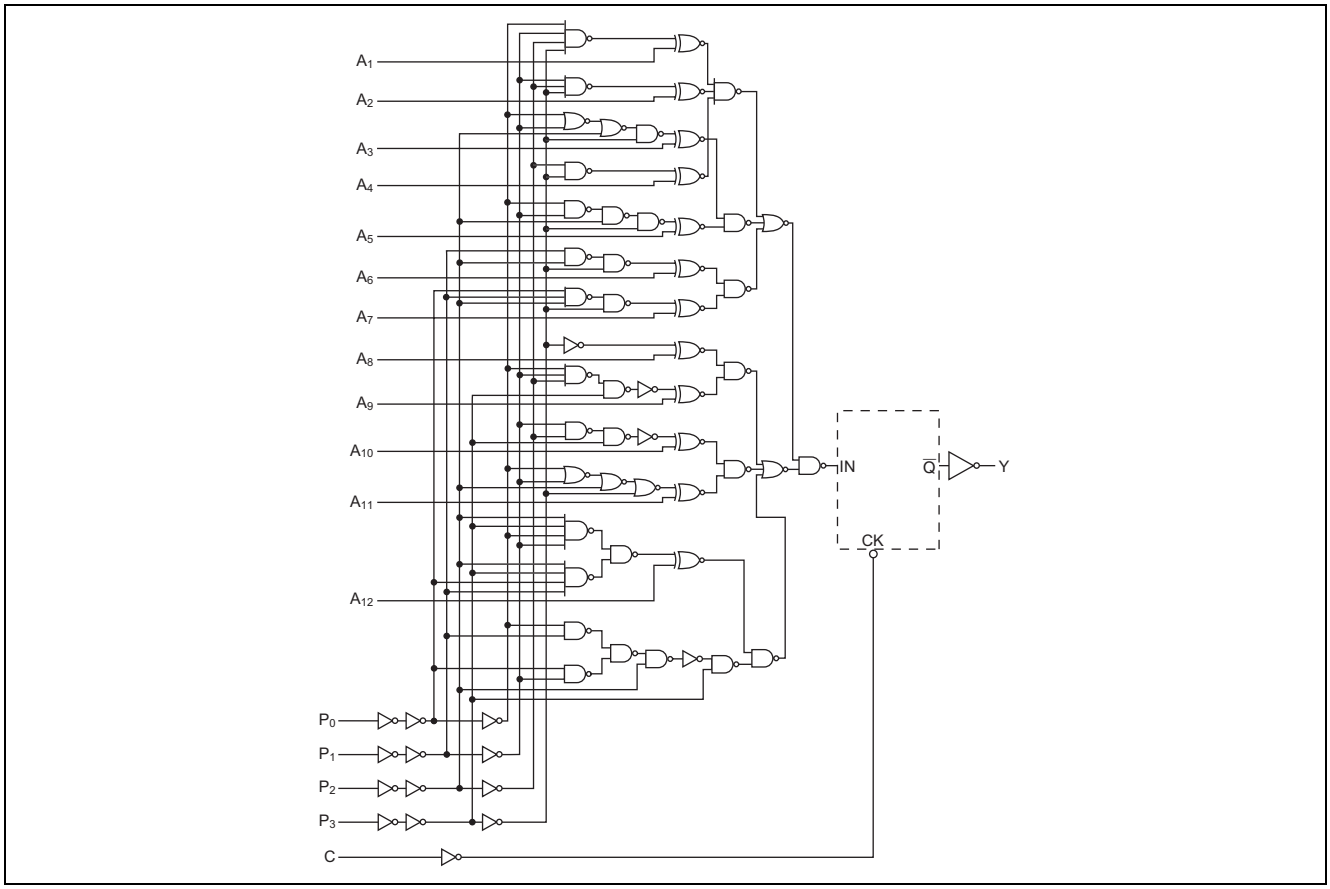
H : high level
L : low level
X : irrelevant

## Pin Arrangement




(Top view)

## Logic Diagram




## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | –0.5 to 7.0 | V |
| Input / Output voltage | $V_{IN}$, $V_{OUT}$ | –0.5 to $V_{CC}$ +0.5 | V |
| Input / Output diode current | $I_{IK}$, $I_{OK}$ | ±20 | mA |
| Output current | $I_{OUT}$ | ±25 | mA |
| $V_{CC}$, GND current | $I_{CC}$ or $I_{GND}$ | ±50 | mA |
| Power dissipation | $P_T$ | 500 | mW |
| Storage temperature | Tstg | –65 to +150 | °C |

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2 to 6 | V | |
| Input / Output voltage | $V_{IN}$, $V_{OUT}$ | 0 to $V_{CC}$ | V | |
| Operating temperature | Ta | –40 to 85 | °C | |
| Input rise / fall time[*1] | $t_r$, $t_f$ | 0 to 1000 | ns | $V_{CC}$ = 2.0 V |
| | | 0 to 500 | | $V_{CC}$ = 4.5 V |
| | | 0 to 400 | | $V_{CC}$ = 6.0 V |

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

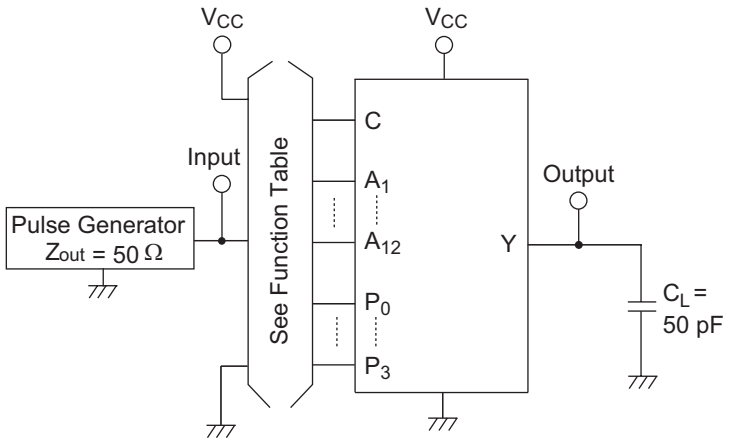
## Electrical Characteristics

| Item | Symbol | $V_{CC}$ (V) | Ta = 25°C | | | Ta = –40 to+85°C | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| Input voltage | $V_{IH}$ | 2.0 | 1.5 | — | — | 1.5 | — | V | | |
| | | 4.5 | 3.15 | — | — | 3.15 | — | | | |
| | | 6.0 | 4.2 | — | — | 4.2 | — | | | |
| | $V_{IL}$ | 2.0 | — | — | 0.5 | — | 0.5 | V | | |
| | | 4.5 | — | — | 1.35 | — | 1.35 | | | |
| | | 6.0 | — | — | 1.8 | — | 1.8 | | | |
| Output voltage | $V_{OH}$ | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V | Vin = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA |
| | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | | | |
| | | 6.0 | 5.9 | 6.0 | — | 5.9 | — | | | |
| | | 4.5 | 4.18 | — | — | 4.13 | — | | | $I_{OH}$ = –4 mA |
| | | 6.0 | 5.68 | — | — | 5.63 | — | | | $I_{OH}$ = –5.2 mA |
| | $V_{OL}$ | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V | Vin = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA |
| | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 6.0 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 4.5 | — | — | 0.26 | — | 0.33 | | | $I_{OL}$ = 4 mA |
| | | 6.0 | — | — | 0.26 | — | 0.33 | | | $I_{OL}$ = 5.2 mA |
| Input current | Iin | 6.0 | — | — | ±0.1 | — | ±1.0 | µA | Vin = $V_{CC}$ or GND | |
| Quiescent supply current | $I_{CC}$ | 6.0 | — | — | 4.0 | — | 40 | µA | Vin = $V_{CC}$ or GND, Iout = 0 µA | |

## Switching Characteristics ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)

| Item | Symbol | $V_{CC}$ (V) | Ta = 25°C | | | Ta = –40 to +85°C | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| Propagation delay time | $t_{PLH}$ $t_{PHL}$ | 2.0 | — | — | 330 | — | 410 | ns | P to Y |
| | | 4.5 | — | 26 | 66 | — | 82 | | |
| | | 6.0 | — | — | 56 | — | 70 | | |
| | $t_{PLH}$ $t_{PHL}$ | 2.0 | — | — | 210 | — | 265 | ns | A to Y |
| | | 4.5 | — | 19 | 42 | — | 53 | | |
| | | 6.0 | — | — | 36 | — | 45 | | |
| | $t_{PLH}$ $t_{PHL}$ | 2.0 | — | — | 150 | — | 190 | ns | C to Y |
| | | 4.5 | — | 18 | 30 | — | 38 | | |
| | | 6.0 | — | — | 26 | — | 33 | | |
| Setup time | $t_{SU}$ | 2.0 | 100 | — | — | 125 | — | ns | A to C |
| | | 4.5 | 20 | 12 | — | 25 | — | | |
| | | 6.0 | 17 | — | — | 21 | — | | |
| Output rise/fall time | $t_{TLH}$ $t_{THL}$ | 2.0 | — | — | 75 | — | 95 | ns | |
| | | 4.5 | — | 6 | 15 | — | 19 | | |
| | | 6.0 | — | — | 13 | — | 16 | | |
| Input capacitance | Cin | — | — | 5 | 10 | — | 10 | pF | |

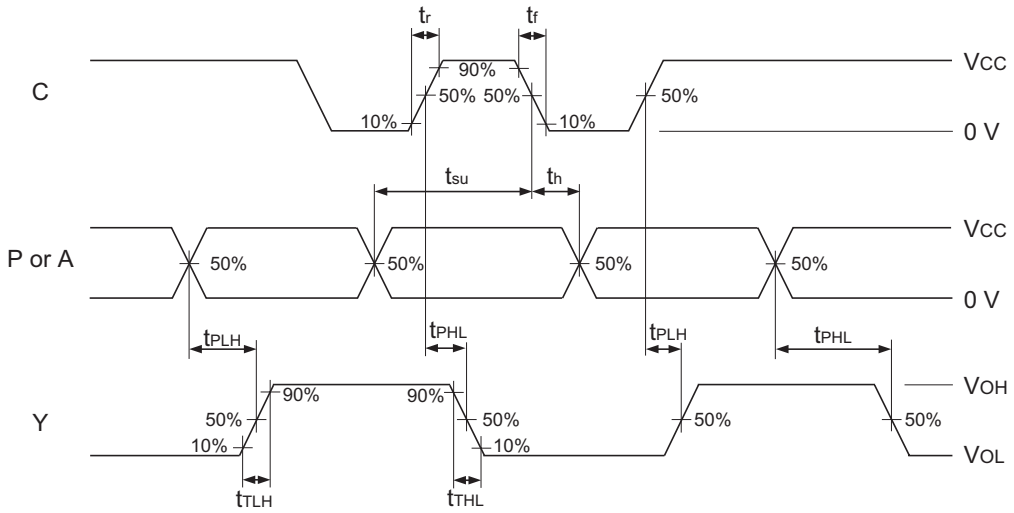
## Test Circuit




Note : 1. $C_L$ includes probe and jig capacitance.

## Waveforms

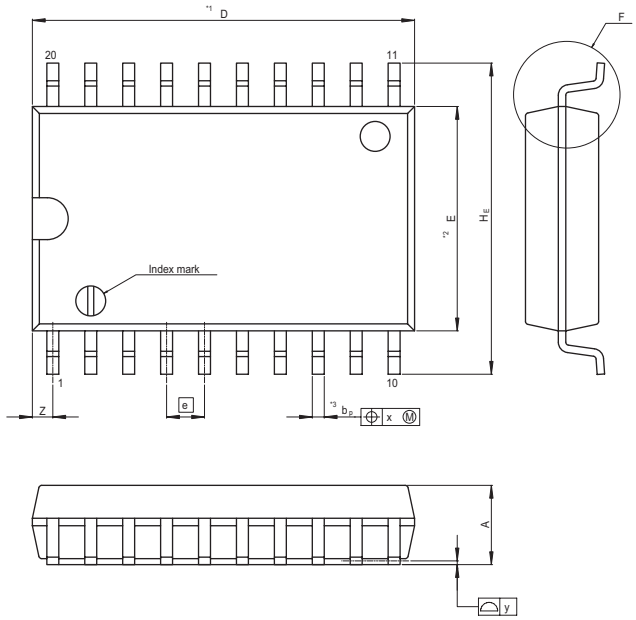
• Waveform

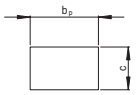



Note : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

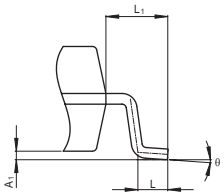
# Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP20-7.5x12.8-1.27 | PRSP0020DC-A | FP-20DBV | 0.52g |




Terminal cross section
( Ni/Pd/Au plating )




Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   @ DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   @ INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 12.80 | 13.2 |
| E | — | 7.50 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.10 | 0.20 | 0.30 |
| A | — | — | 2.65 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.20 | 0.25 | 0.30 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 10.00 | 10.40 | 10.65 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.935 |
| L | 0.40 | 0.70 | 1.27 |
| $L_1$ | — | 1.45 | — |

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan



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**Renesas Technology America, Inc.**
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510



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