



3.3V CMOS 18-BIT BUS-INTERFACE FLIP- FLOP WITH 3-STATE OUT- PUTS AND BUS-HOLD

IDT74ALVCH16823

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 18-bit bus-interface flip-flop is built using advanced dual metal CMOS technology. The ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

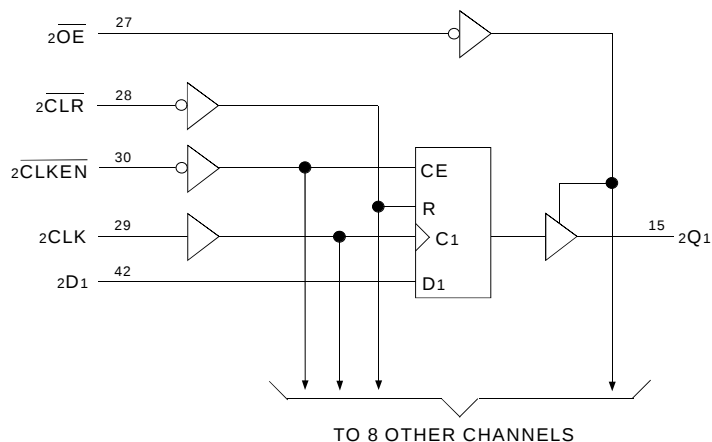
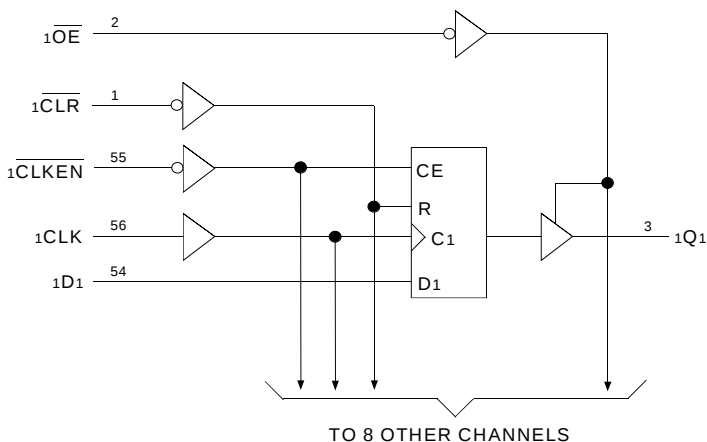
The ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The $\overline{OE}$ input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The ALVCH16823 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16823 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

FUNCTIONAL BLOCK DIAGRAM

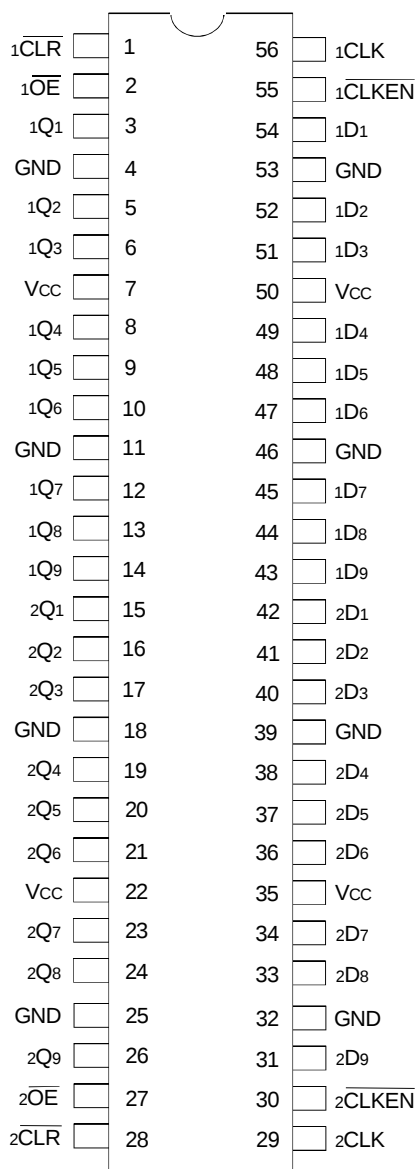


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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2004

PIN CONFIGURATION



TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
x Dx	Data Inputs ⁽¹⁾
x CLK	Clock Input
$\overline{x}$ CLKEN	Clock Enable Inputs
x Qx	3-State Outputs
$\overline{x}$ OE	3-State Output Enable Inputs
x CLR	Clear Inputs

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, Vi < 0 or Vi > Vcc	±50	mA
IOK	Continuous Clamp Current, Vo < 0	-50	mA
ICC ISS	Continuous Current through each Vcc or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COU	Output Capacitance	VOU = 0V	7	9	pF
COUT	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

- As applicable to the device type.

FUNCTION TABLE (EACH 9-BIT FLIP-FLOP)⁽¹⁾

Inputs					Output
$\overline{x}$ OE	$\overline{x}$ CLR	$\overline{x}$ CLKEN	x CLK	x Dx	x Qx
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q ₀ ⁽²⁾
L	H	H	X	X	Q ₀ ⁽²⁾
H	X	X	X	X	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	μA
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	LOL = 0.1mA	—	0.2	V
		VCC = 2.3V	LOL = 6mA	—	0.4	
			LOL = 12mA	—	0.7	
		VCC = 2.7V	LOL = 12mA	—	0.4	
		VCC = 3V	LOL = 24mA	—	0.55	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.
TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	27	30	pF
CPD	Power Dissipation Capacitance Outputs disabled		16	18	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay xCLK to xQx	1	5.8	—	5.2	1	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay x $\overline{\text{CLR}}$ to xQx	1	5.4	—	5.2	1.2	4.6	ns
t _{PZH} t _{PZL}	Output Enable Time x $\overline{\text{OE}}$ to xQx	1	6	—	5.7	1	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time x $\overline{\text{OE}}$ to xQx	1.1	5.4	—	4.7	1.3	4.5	ns
t _w	Pulse Duration, x $\overline{\text{CLR}}$ LOW	3.3	—	3.3	—	3.3	—	ns
t _w	Pulse Duration, xCLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{SU}	Set-up Time, x $\overline{\text{CLR}}$ inactive	0.7	—	0.7	—	0.8	—	ns
t _{SU}	Set-up Time, data LOW before xCLK↑	1.4	—	1.6	—	1.3	—	ns
t _{SU}	Set-up Time, data HIGH before xCLK↑	1.1	—	1.1	—	1	—	ns
t _{SU}	Set-up Time, x $\overline{\text{CLKEN}}$ LOW before xCLK↑	1.8	—	1.9	—	1.5	—	ns
t _H	Hold Time, data LOW after xCLK↑	0.4	—	0.5	—	0.5	—	ns
t _H	Hold Time, data HIGH after xCLK↑	0.7	—	0.1	—	0.8	—	ns
t _H	Hold Time, x $\overline{\text{CLKEN}}$ LOW after CLK↑	0.2	—	0.3	—	0.4	—	ns
t _{SK(O)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

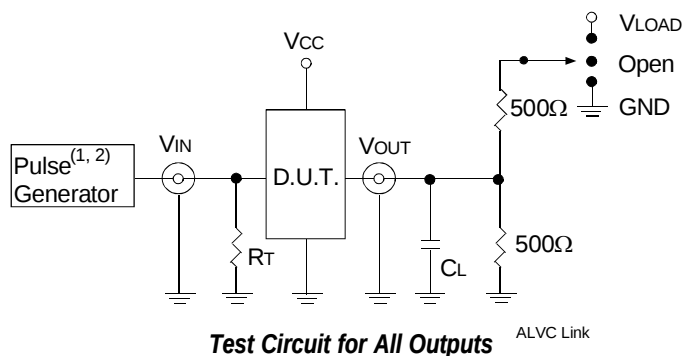
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

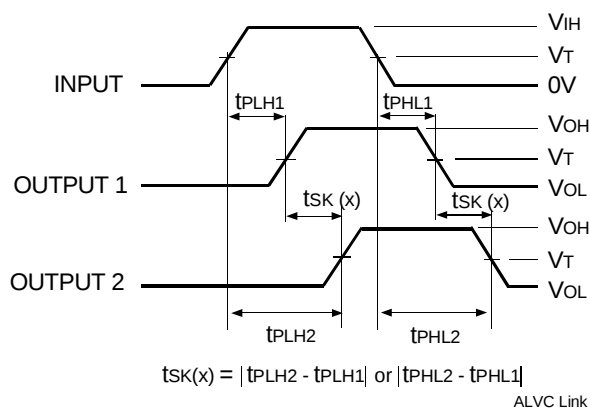
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

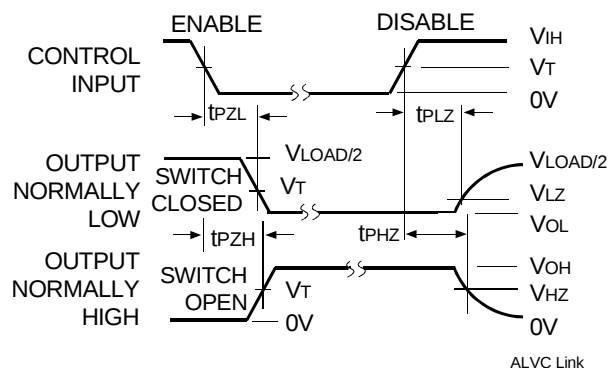
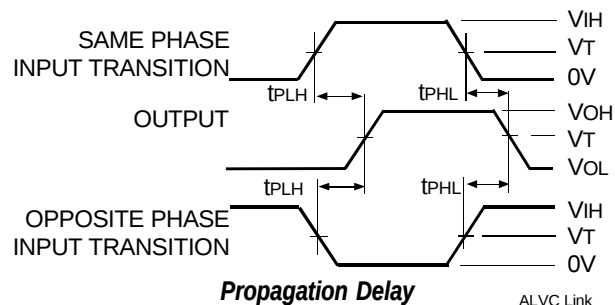
Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



Output Skew - t_{sk}(x)

NOTES:

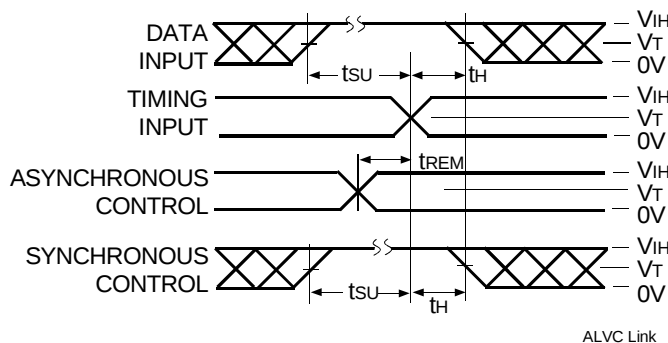
1. For t_{sk}(0) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{sk}(b) OUTPUT1 and OUTPUT2 are in the same bank.



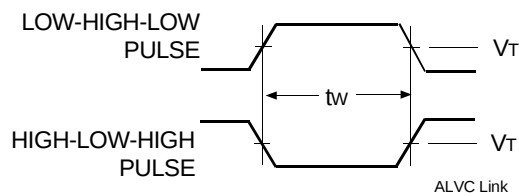
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
Temp. Range			Bus-Hold	Family	Device Type	Package	
						PA	Thin Shrink Small Outline Package
					823		18-Bit Bus-Interface Flip-Flop with 3-State Outputs
				16			Double-Density, $\pm 24\text{mA}$
			H				Bus-Hold
74							-40°C to $+85^{\circ}\text{C}$



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