

74F543

Octal latched transceiver with dual enable; 3-state

Rev. 04 — 26 January 2010

Product data sheet

1. General description

The 74F543 octal latched transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and output enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. The A outputs are guaranteed to sink 24 mA while the B outputs are rated for 64 mA.

2. Features

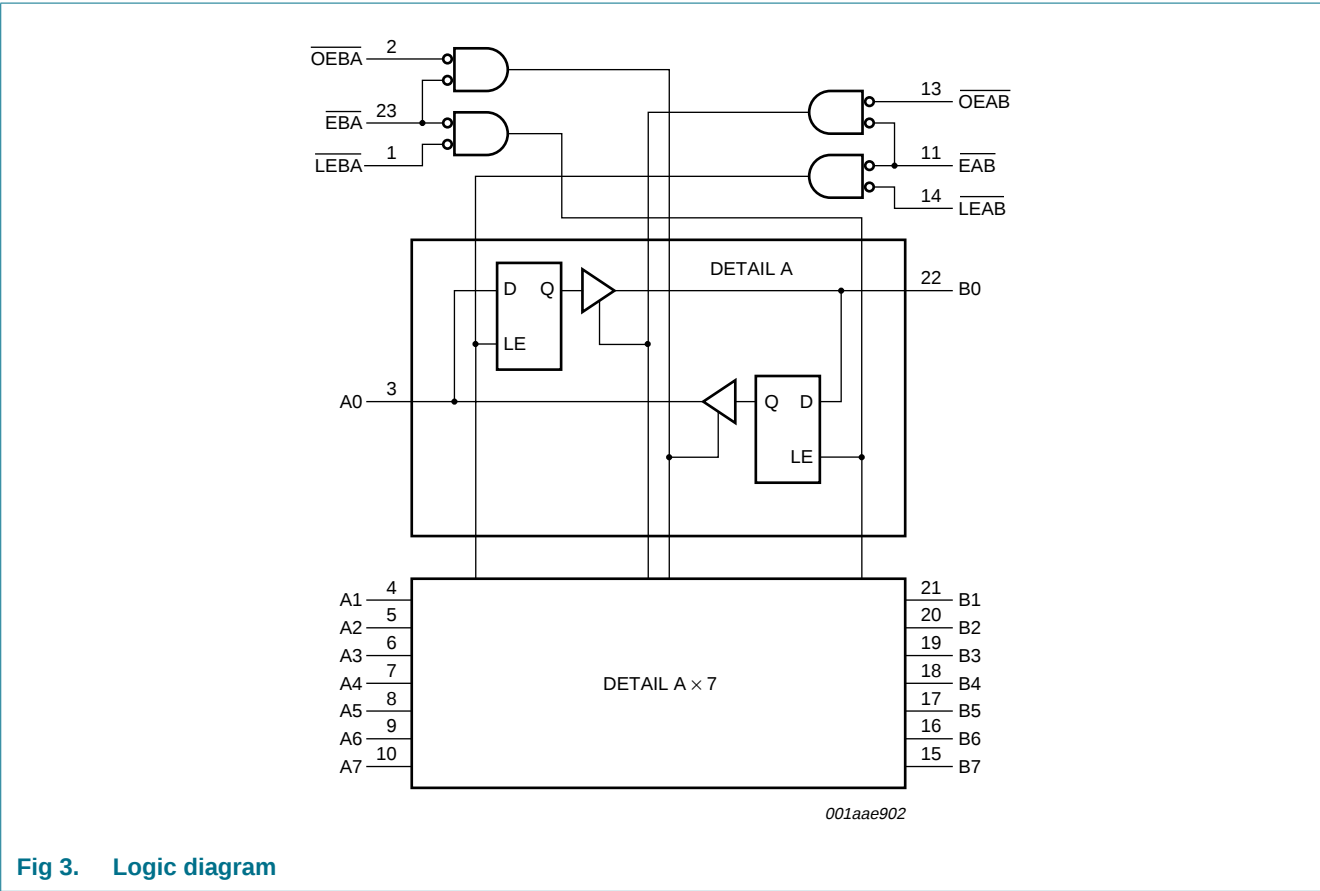
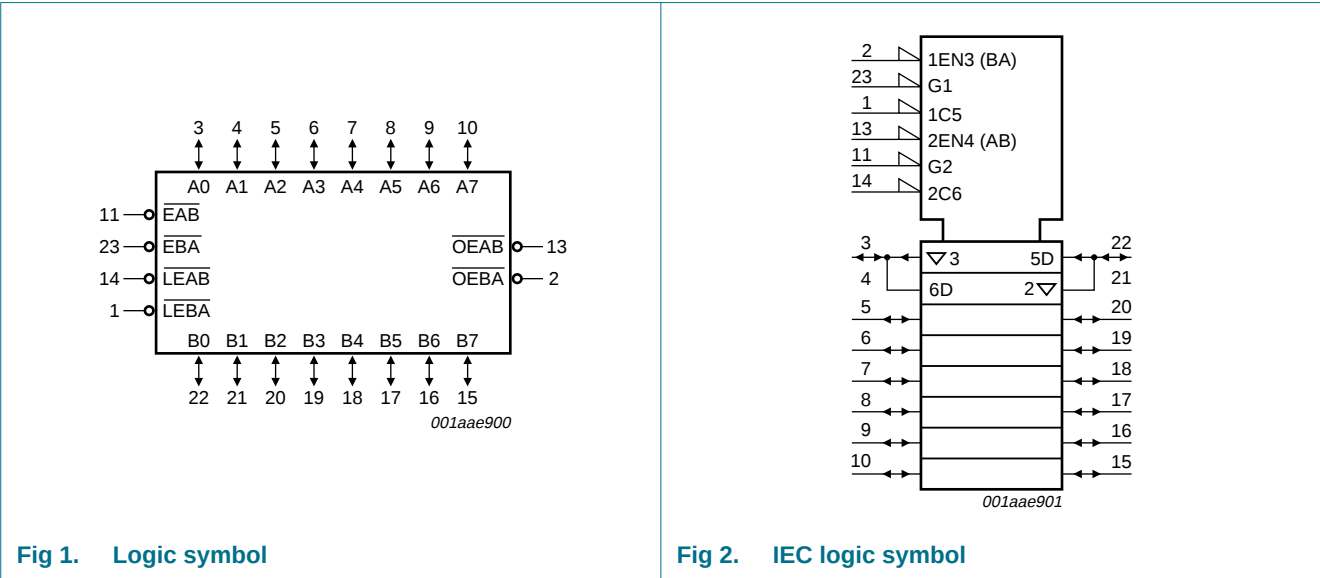
- Combines 74F245 and 74F373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A output capability: +20 mA to –3 mA
- B output capability: +64 mA to –15 mA
- 3-state outputs for bus-oriented applications

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
N74F543D	0 °C to +70 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F543DB	0 °C to +70 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

4. Functional diagram



5. Pinning information

5.1 Pinning

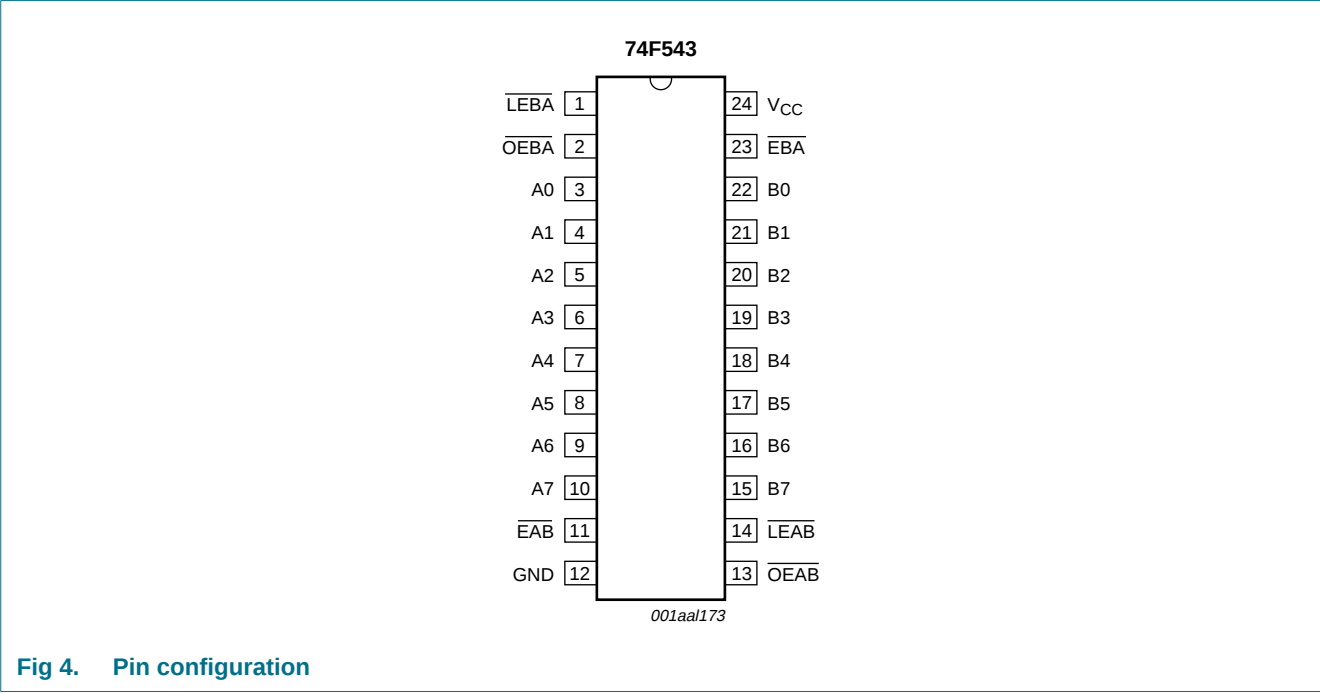


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value ^[1] HIGH/LOW
LEBA	1	B-to-A latch enable input (active LOW)	1.0/1.0	20 µA/0.6 mA
OEBA	2	B-to-A output enable input (active LOW)	1.0/1.0	20 µA/0.6 mA
A0 to A7	3, 4, 5, 6, 7, 8, 9, 10	data input or output	inputs 3.5/1.0; outputs 150/40	inputs 70 µA/0.6 mA; outputs 3.0 mA/24 mA
EAB	11	A-to-B enable input (active LOW)	1.0/2.0	20 µA/1.2 mA
GND	12	ground (0 V)		
OEAB	13	A-to-B output enable input (active LOW)	1.0/1.0	20 µA/0.6 mA
LEAB	14	A-to-B latch enable input (active LOW)	1.0/1.0	20 µA/0.6 mA
B0 to B7	22, 21, 20, 19, 18, 17, 16, 15	data input or output	inputs 3.5/1.0; outputs 750/106.7	inputs 70 µA/0.6 mA; outputs 15 mA/64 mA
EBA	23	B-to-A enable input (active LOW)	1.0/2.0	20 µA/1.2 mA
V _{CC}	24	positive supply voltage		

[1] One FAST Unit Load (UL) is defined as 20 µA in HIGH state, 0.6 µA in LOW state.

6. Functional description

6.1 Function table

Table 3. Function selection^[1]

Input				Output	Status
$\overline{\text{OEXX}}$	$\overline{\text{EXX}}$	$\overline{\text{LEXX}}$	An or Bn	Bn or An	
H	X	X	X	Z	disabled
X	H	X	X	Z	
L	↑	L	h	Z	disabled + latch
			l	Z	
L	L	↑	h	H	latch + display
			l	L	
L	L	L	H	H	transparent
			L	L	
L	L	H	X	NC	hold

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
↑ = LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
NC = no change;
X = don't care;
Z = high-impedance OFF-state.

6.2 Description

The 74F543 contains two sets of eight D-type latches, with separate control pins for each set.

Using data flow from A-to-B as an example, when the A-to-B enable ($\overline{\text{EAB}}$) input, the A-to-B latch enable ($\overline{\text{LEAB}}$) input and the A-to-B output latch enable ($\overline{\text{OEAB}}$) are all LOW, the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B-to-A is similar, but using the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
V _I	input voltage		^[1] −0.5	+7.0	V
V _O	output voltage	output in HIGH-state	^[1] −0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	−30	+5	mA
I _O	output current	output in LOW-state			
		pins A0 to A7	−	48	mA
		pins B0 to B7	−	128	mA
T _{amb}	ambient temperature	in free air	^[2] 0	70	°C
T _{stg}	storage temperature		−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _{IH}	HIGH-level input voltage		2.0	−	−	V
V _{IL}	LOW-level input voltage		−	−	0.8	V
I _{IK}	input clamping current		−	−	−18	mA
I _{OH}	HIGH-level output current	pins A0 to A7	−3	−	−	mA
		pins B0 to B7	−15	−	−	mA
I _{OL}	LOW-level output current	pins A0 to A7	−	−	24	mA
		pins B0 to B7	−	−	64	mA

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			0 °C to 70 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_{IK} = -18\text{ mA}$	-1.2	-0.73	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 4.5\text{ V}$; $V_{IL} = 0.8\text{ V}$; $V_{IH} = 2.0\text{ V}$ pins A0 to A7; $I_{OH} = -3\text{ mA}$						
		$V_{CC} = \pm 10\%$	-	-	-	2.4	-	V
		$V_{CC} = \pm 5\%$	-	3.4	-	2.7	-	V
		pins B0 to B7; $I_{OH} = -15\text{ mA}$						
		$V_{CC} = \pm 10\%$	-	-	-	2.0	-	V
		$V_{CC} = \pm 5\%$	-	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5\text{ V}$; $V_{IL} = 0.8\text{ V}$; $V_{IH} = 2.0\text{ V}$ pins A0 to A7; $I_{OL} = 24\text{ mA}$						
		$V_{CC} = \pm 10\%$	-	0.35	-	-	0.5	V
		$V_{CC} = \pm 5\%$	-	0.35	-	-	0.5	V
		pins B0 to B7; $I_{OL} = 64\text{ mA}$						
		$V_{CC} = \pm 10\%$	-	-	-	-	0.55	V
		$V_{CC} = \pm 5\%$	-	0.42	-	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5\text{ V}$ pins $\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$; $V_I = 7.0\text{ V}$	-	-	-	-	100	μA
		other pins; $V_I = 5.5\text{ V}$	-	-	-	-	1	mA
			-	-	-	-	20	μA
I_{IH}	HIGH-level input current	$V_{CC} = 5.5\text{ V}$; $V_I = 2.7\text{ V}$	-	-	-	-	20	μA
I_{IL}	LOW-level input current	$V_{CC} = 5.5\text{ V}$; $V_I = 0.5\text{ V}$ pins $\overline{EAB}$, $\overline{EBA}$	-	-	-	-	-1.2	mA
		other pins	-	-	-	-	-0.6	mA
			-	-	-	-	-0.6	mA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5\text{ V}$ $V_O = 2.7\text{ V}$; $V_I = 2.0\text{ V}$	-	-	-	-	70	μA
		$V_O = 0.5\text{ V}$; $V_I = 0.8\text{ V}$	-	-	-	-	-600	μA
			-	-	-	-	-600	μA
I_O	output current	$V_{CC} = 5.5\text{ V}$ ^[2] pins A0 to A7	-	-60	-	-	-150	mA
		pins B0 to B7	-	-100	-	-	-225	mA
			-	-	-	-	-225	mA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}$ outputs HIGH-state	-	70	-	-	105	mA
		outputs LOW-state	-	95	-	-	135	mA
		outputs OFF-state	-	95	-	-	135	mA
			-	95	-	-	135	mA

[1] All typical values are measured at $V_{CC} = 5\text{ V}$.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

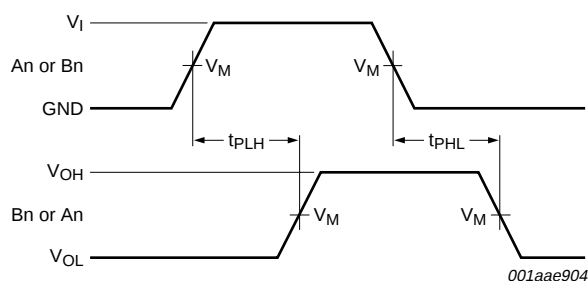
10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			0 °C to 70 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Figure 5	3.5	5.5	8.5	3.0	9.0	ns
		Bn to An; see Figure 5	2.5	4.0	7.0	2.5	7.5	ns
		$\overline{LEBA}$ to An; see Figure 6	5.0	7.0	10.0	4.5	11.0	ns
		$\overline{LEAB}$ to Bn; see Figure 6	6.0	8.5	11.5	5.5	12.5	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Figure 5	3.0	5.0	8.0	2.5	8.5	ns
		Bn to An; see Figure 5	2.5	4.5	7.5	2.5	8.0	ns
		$\overline{LEBA}$ to An; see Figure 6	4.0	6.0	9.0	4.0	9.5	ns
		$\overline{LEAB}$ to Bn; see Figure 6	4.5	6.5	9.5	4.0	10.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn; see Figure 7	2.0	4.0	7.5	1.5	8.0	ns
		$\overline{EBA}$ to An, $\overline{EAB}$ to Bn; see Figure 7	4.5	7.0	10.5	4.0	11.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn; see Figure 8	3.5	5.0	8.5	3.0	9.0	ns
		$\overline{EBA}$ to An, $\overline{EAB}$ to Bn; see Figure 8	5.0	7.0	10.5	4.5	11.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn; see Figure 7	1.0	3.0	6.5	1.0	7.5	ns
		$\overline{EBA}$ to An, $\overline{EAB}$ to Bn; see Figure 7	2.5	5.0	8.5	2.0	9.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn; see Figure 8	1.5	4.0	7.5	1.0	8.5	ns
		$\overline{EBA}$ to An, $\overline{EAB}$ to Bn; see Figure 8	4.5	7.0	11.0	3.0	12.0	ns
$t_{su(H)}$	set-up time HIGH	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$; see Figure 9	0.0	-	-	0.0	-	ns
		An to $\overline{EAB}$, Bn to $\overline{EBA}$; see Figure 9	1.0	-	-	1.5	-	ns
$t_{su(L)}$	set-up time LOW	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$; see Figure 9	2.5	-	-	3.0	-	ns
		An to $\overline{EAB}$, Bn to $\overline{EBA}$; see Figure 9	2.5	-	-	3.0	-	ns
$t_{h(H)}$	hold time HIGH	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$; see Figure 9	0.0	-	-	0.0	-	ns
		An to $\overline{EAB}$, Bn to $\overline{EBA}$; see Figure 9	0.0	-	-	0.0	-	ns
$t_{h(L)}$	hold time LOW	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$; see Figure 9	1.5	-	-	2.0	-	ns
		An to $\overline{EAB}$, Bn to $\overline{EBA}$; see Figure 9	1.5	-	-	2.0	-	ns
t_{WL}	pulse width LOW	latch enable; see Figure 9	4.0	-	-	4.5	-	ns

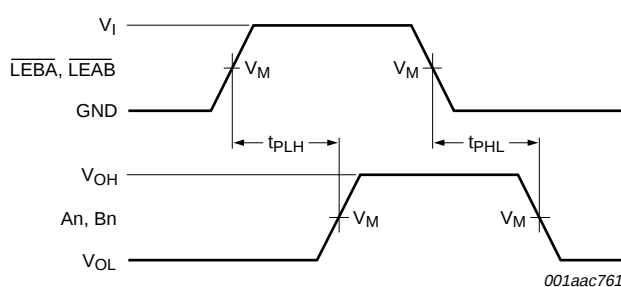
11. Waveforms



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

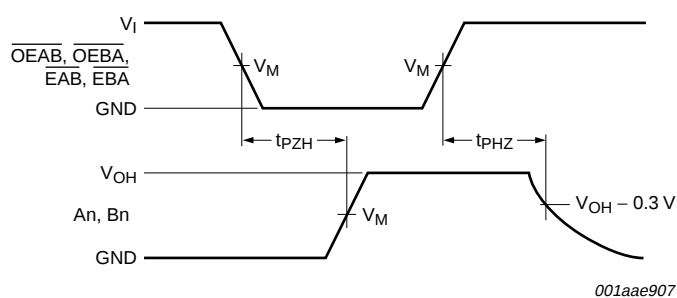
Fig 5. Propagation delay input (An, Bn) to output (Bn, An)



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

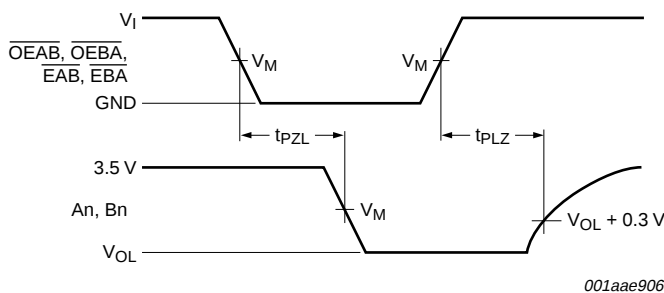
Fig 6. Propagation delay latch enable ($\overline{LEAB}$, $\overline{LEBA}$) to output (An, Bn)



$V_M = 1.5\text{ V}$

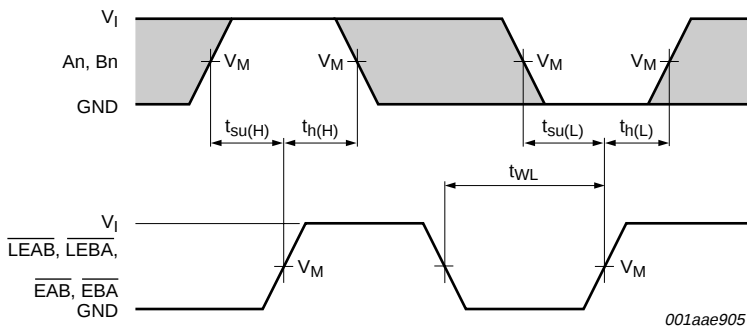
V_{OH} is a typical voltage output level that occurs with the output load.

Fig 7. Propagation delay 3-state output enable to HIGH-level and output disable from HIGH-level



$V_M = 1.5 V$
 V_{OL} is a typical voltage output level that occurs with the output load.

Fig 8. Propagation delay 3-state output enable to LOW-level and output disable from LOW-level



$V_M = 1.5 V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times and latch enable pulse width

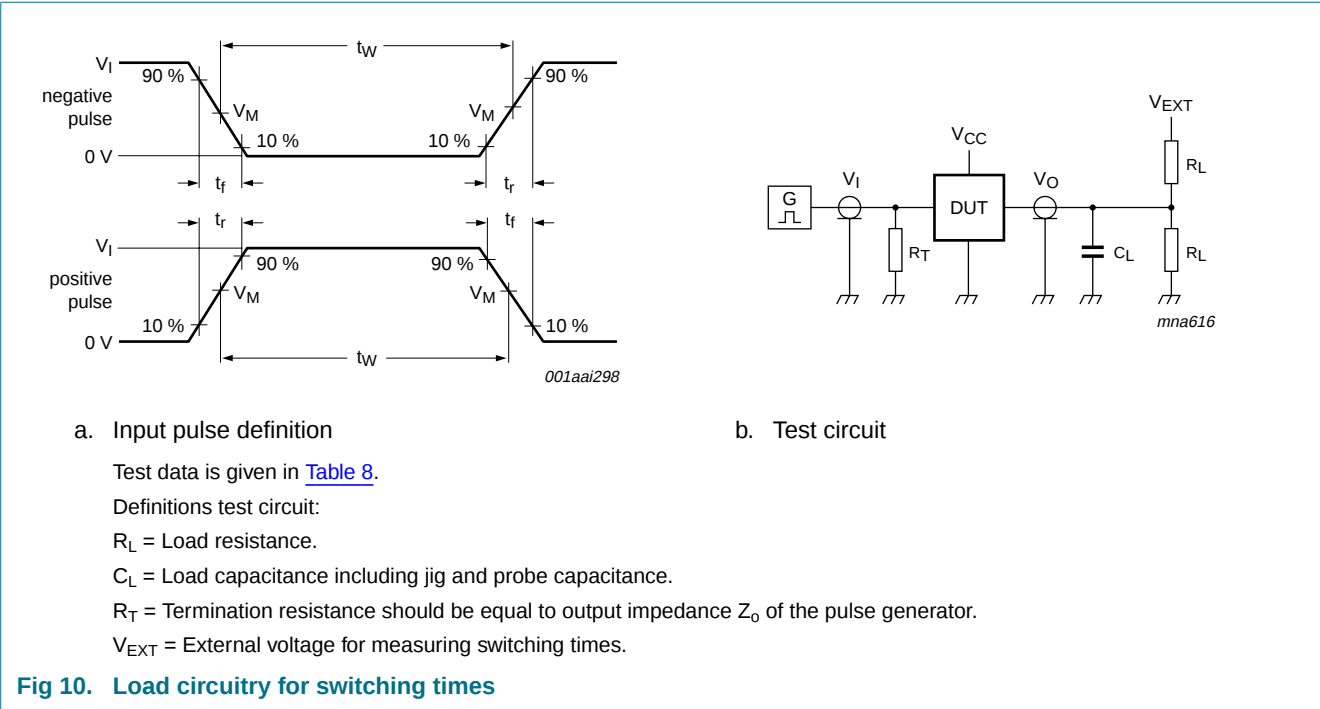


Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1

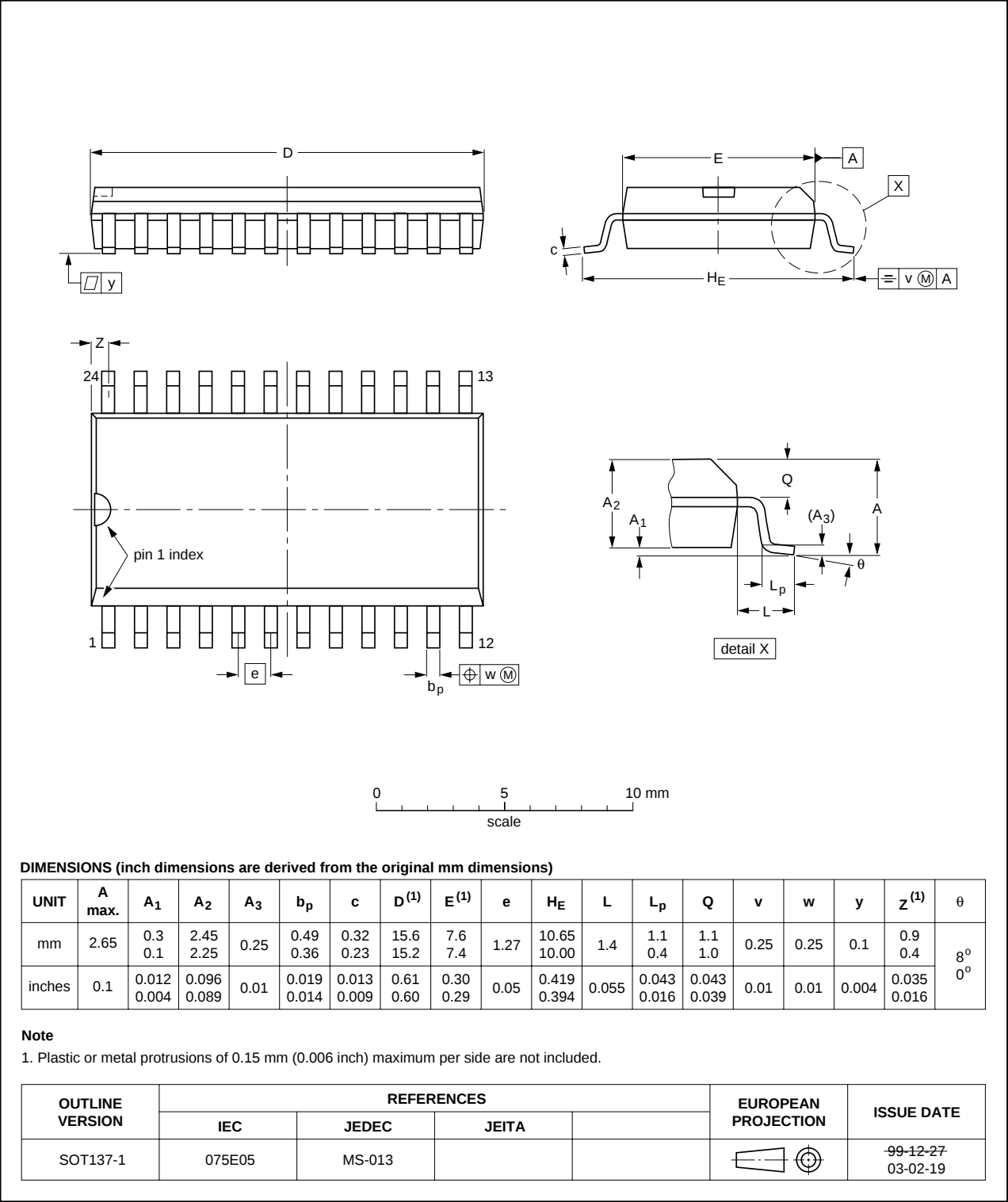


Fig 11. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

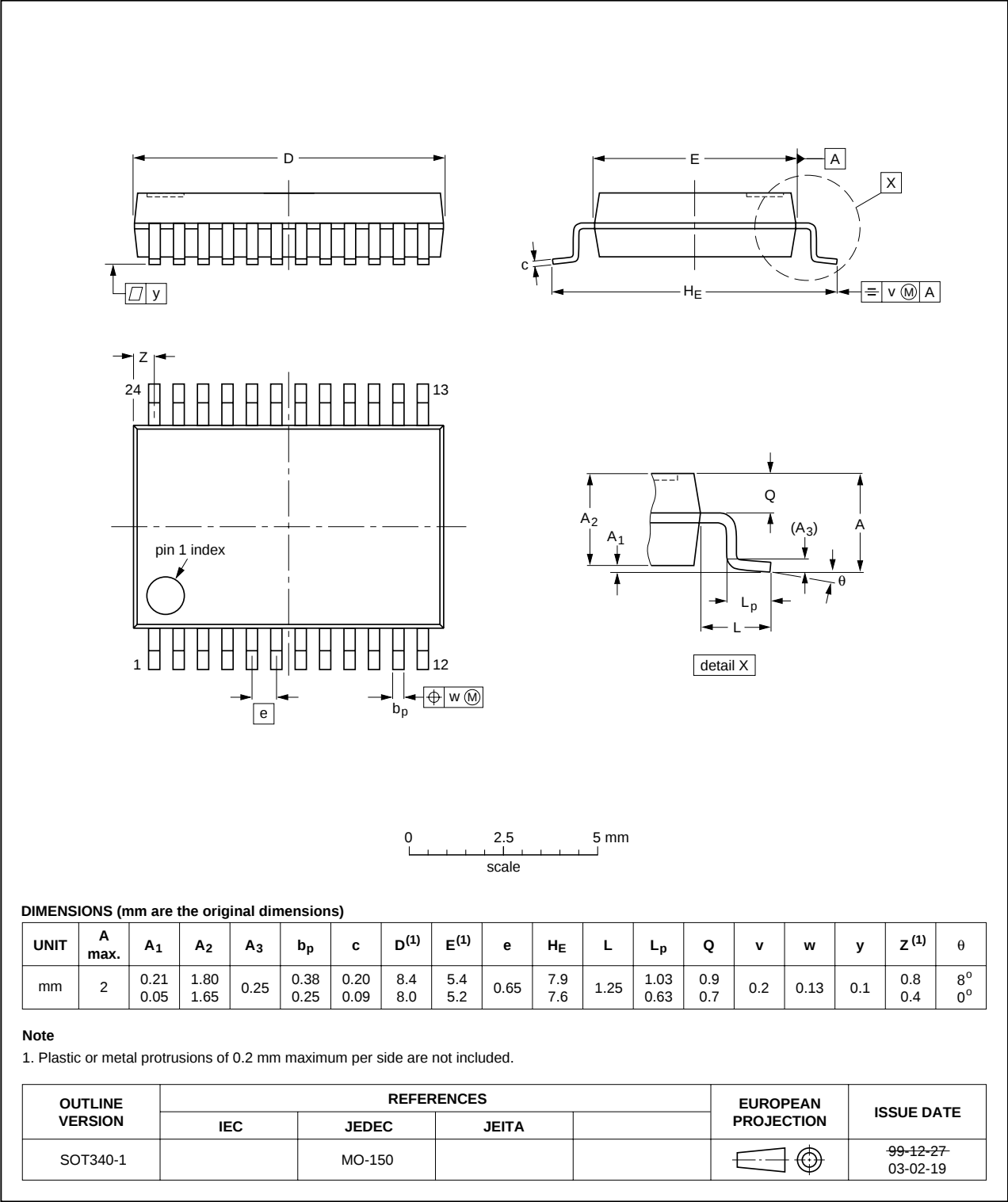


Fig 12. Package outline SOT340-1 (SSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F543_4	20100126	Product data sheet	-	74F543_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline”			
74F543_3	20040722	Product specification	-	74F543_544_2
74F543_544_2	19941205	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1 General description 1

2 Features 1

3 Ordering information 1

4 Functional diagram 2

5 Pinning information 3

5.1 Pinning 3

5.2 Pin description 3

6 Functional description 4

6.1 Function table 4

6.2 Description 4

7 Limiting values 5

8 Recommended operating conditions 5

9 Static characteristics 6

10 Dynamic characteristics 7

11 Waveforms 8

12 Package outline 11

13 Abbreviations 13

14 Revision history 13

15 Legal information 14

15.1 Data sheet status 14

15.2 Definitions 14

15.3 Disclaimers 14

15.4 Trademarks 14

16 Contact information 14

17 Contents 15



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.