iC-NQL

13-bit Sin/D CONVERTER WITH SSI INTERFACE

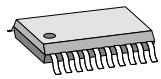
FEATURES

- Resolution of up to 8192 angle steps per sine/cosine period
- Binary and decimal resolution settings, e.g. 500, 512, 1000, 1024; programmable angle hysteresis
- Conversion time of just 250 ns including amplifier settling
- Count-safe vector follower principle, realtime system with 70 MHz sampling rate
- Direct sensor connection; selectable input gain
- Front-end signal conditioning features offset (8 bit), amplitude ratio (5 bit) and phase (6 bit) calibration
- 250 kHz input frequency
- Absolute angle output via fast SSI interface
- A QUAD B incremental outputs with selectable minimum transition distance (e.g. 0.25 µs for 1 MHz at A)
- Index signal processing adjustable in position and width
- Fault monitoring: frequency, amplitude, configuration (CRC)
- Setup via serial EEPROM
- ESD protection and TTL-/CMOS-compatible outputs

APPLICATIONS

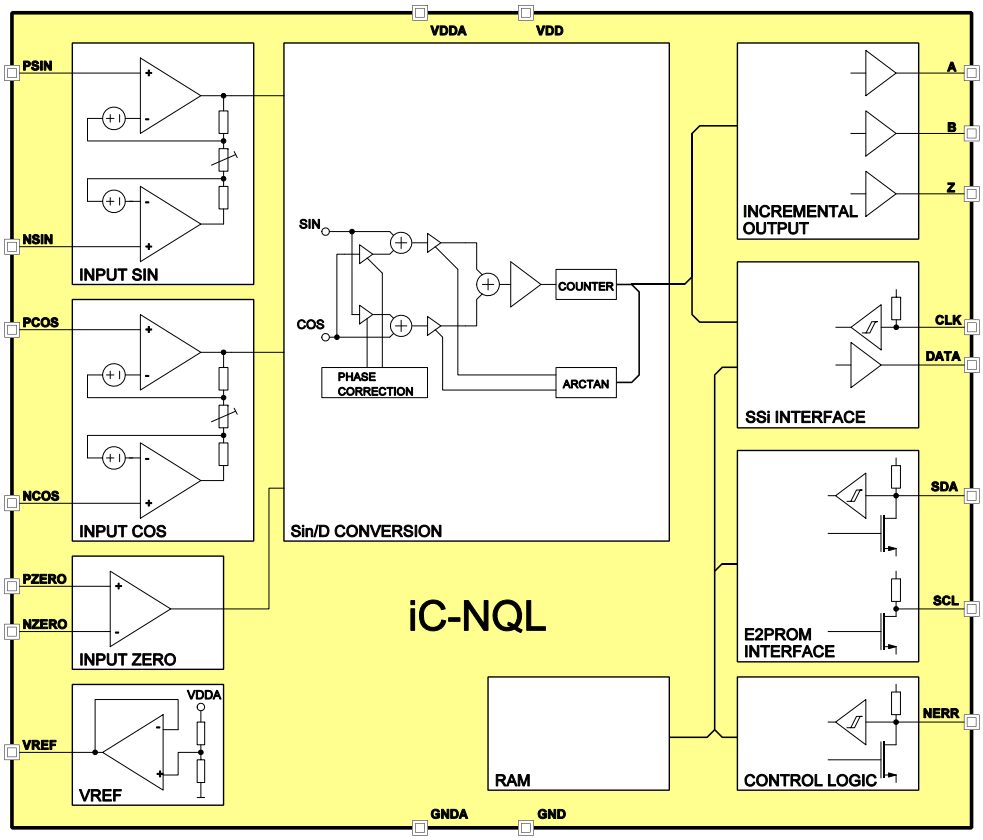
- Interpolator IC for position data acquisition from analog sine/cosine sensors
- Optical linear/rotary encoders
- MR sensor systems

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

iC-NQL is a monolithic A/D converter which, by applying a count-safe vector follower principle, converts sine/cosine sensor signals with a selectable resolution and hysteresis into angle position data. This absolute value is output via a synchronous-serial SSI interface and trails a master clock rate of up to 4 Mbit/s.

At the same time any changes in output data are converted into incremental A QUAD B encoder signals. Here, the minimum transition distance can be adapted to suit the system on hand (cable length, external counter). A synchronised zero index is generated and output to Z if enabled by the PZERO and NZERO inputs.

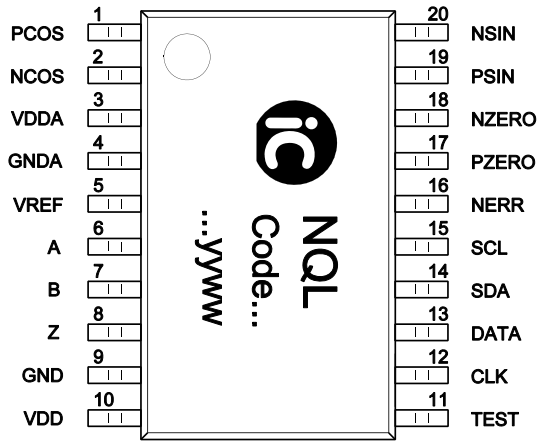
The front-end amplifiers are configured as instrumentation amplifiers, permitting sensor bridges to be directly connected without the need for external resistors. Various programmable D/A converters are available for the conditioning of sine/cosine sensor signals with regard to offset, amplitude ratio and phase errors. Front-end gain can be set in stages graded to suit all common differential sensor signals from approximately 20 mVpp to 1.5 Vpp, and also single-ended sensor signals from 40 mVpp to 3 Vpp respectively.

The device reads its configuration data via the serial EEPROM interface when cycling power, respectively following an undervoltage reset. The read in cycle is repeated up to three times when data correctness is not confirmed by a CRC validation. A permanent CRC error as well as the configuration phase itself is displayed at the error message output NERR by a low level signal.

CONTENTS

PACKAGES TSSOP20 (according to JEDEC Standard)

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm



PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine -
3	VDDA	+5 V Supply Voltage (analog)
4	GNDA	Ground (analog)
5	VREF	Reference Voltage Output
6	A	Incremental Output A Analog signal COS+ (TMA mode) PWM signal for Offset Sine (Calib.)
7	B	Incremental Output B Analog signal COS- (TMA mode) PWM signal for Offset Cosine (Calib.)
8	Z	Output Index Z PWM signal for Phase/Ratio (Calib.)
9	GND	Ground
10	VDD	+5 V Supply Voltage (digital)
11	TEST	Test Input
12	CLK	SSI interface, clock line
13	DATA	SSI interface, data output
14	SDA	EEPROM interface, data line Analog signal SIN+ (TMA mode)
15	SCL	EEPROM interface, clock line Analog signal SIN- (TMA mode)
16	NERR	Error Input/Output, active low
17	PZERO	Input Zero Signal +
18	NZERO	Input Zero Signal -
19	PSIN	Input Sine +
20	NSIN	Input Sine -

External connections linking VDDA to VDD and GND to GNDA are required. The test input may remain unwired or can be linked to VDD (please note the hints given by chapter Design Review regarding the signal of pin DATA).

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDA	Voltage at VDDA		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	6	V
G003	Vpin()	Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, CLK, DATA, A, B, Z	V() < VDDA + 0.3 V V() < VDD + 0.3 V	-0.3	6	V
G004	Imx(VDDA)	Current in VDDA		-50	50	mA
G005	Imx(GNDA)	Current in GNDA		-50	50	mA
G006	Imx(VDD)	Current in VDD		-50	50	mA
G007	Imx(GND)	Current in GND		-50	50	mA
G008	Imx()	Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, CLK, DATA, A, B, Z		-10	10	mA
G009	Ilu()	Pulse Current in all pins (Latch-up Strength)	according to Jedec Standard No. 78; Ta = 25 °C, pulse duration to 10 µs, VCC = VCCmax, VDD = VDDmax, Vlu() = (-0.5...+1.5) x Vpin()max	-100	100	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDDA = VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range of -40 to 125 °C available on request)		-25		85	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Functionality and parameters beyond the operating conditions (with reference to independent voltage supplies, for instance) are to be verified within the individual application using FMEA methods.							
001	VDDA, VDD	Permissible Supply Voltage		4.5		5.5	V
002	I(VDDA)	Supply Current in VDDA	fin() = 200 kHz; A, B, Z open			15	mA
003	I(VDD)	Supply Current in VDD	fin() = 200 kHz; A, B, Z open			20	mA
004	Von	Turn-on Threshold VDDA, VDD		3.2		4.4	V
005	Vhys	Turn-on Threshold Hysteresis		200			mV
006	Vc()hi	Clamp Voltage hi at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF	Vc()hi = V() - VDDA; I() = 1 mA, other pins open	0.3		1.6	V
007	Vc()lo	Clamp Voltage lo at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, A, B, Z	I() = -1 mA, other pins open	-1.6		-0.3	V
008	Vc()hi	Clamp Voltage hi at NERR, SCL, SDA, A, B, Z	Vc()hi = V() - VDD; I() = 1 mA, other pins open	0.3		1.6	V
Input Amplifiers PSIN, NSIN, PCOS, NCOS							
101	Vos()	Input Offset Voltage	Vin() and G() in accordance with table GAIN; G ≥ 20 G < 20	-10 -15		10 15	mV mV
102	TCos	Input Offset Voltage Temperature Drift	see 101		±10		µV/K
103	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
104	GA	Gain Accuracy	G() in accordance with table GAIN	95		102	%
105	GArel	Gain SIN/COS Ratio Accuracy	G() in accordance with table GAIN	97		103	%
106	fhc	Cut-off Frequency	G = 80 G = 2.667	150 630			kHz kHz
107	SR	Slew Rate	G = 80 G = 2.667	2.3 8.0			V/µs V/µs
Sin/D Conversion: Accuracy							
201	AAabs	Absolute Angle Accuracy without calibration	referred to 360° input signal, G = 2.667, Vin = 1.5 Vpp, HYS = 0	-1.0		1.0	DEG
202	AAabs	Absolute Angle Accuracy after calibration	referred to 360° input signal, HYS = 0, internal signal amplitude of 2 ... 4 Vpp	-0.5	±0.35	+0.5	DEG
203	AArel	Relative Angle Accuracy	referred to output signal period of A/B, G = 2.667, Vin = 1.5 Vpp, SELRES = 1024, FCTR = 0x0004 ... 0x00FF, fin < fin_{max} (see table 14)	-10		10	%
Reference Voltage VREF							
801	VREF	Reference Voltage	I(VREF) = -1 mA ... +1 mA	48		52	% VDDA
Oscillator							
A01	fosc()	Oscillator Frequency	presented at SCL with subdivision of 2048; VDDA = VDD = 5 V ±10 % VDDA = VDD = 5 V	52 60	72	90 83	MHz MHz
A02	TCosc	Oscillator Frequency Temperature Drift	VDDA = VDD = 5 V		-0.1		%/K
A03	VCosc	Oscillator Frequency Power Supply Dependance			+10.6		%/V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Zero Comparator							
B01	Vos()	Input Offset Voltage	V() = Vcm()	-20		20	mV
B02	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
B03	Vcm()	Common-Mode Input Voltage Range		1.4		VDDA-1.5	V
B04	Vdm()	Differential Input Voltage Range		0		VDDA	V
Incremental Outputs A, B, Z SSI Interface Output DATA							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA			0.4	V
D02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
D03	tr()	Rise Time	CL() = 50 pF			60	ns
D04	tf()	Fall Time	CL() = 50 pF			60	ns
D05	RL()	Permissible Load at A, B	TMA = 1 (calibration mode)	1			MΩ
SSI Interface: Input CLK							
E01	Vt()hi	Threshold Voltage hi				2	V
E02	Vt()lo	Threshold Voltage lo		0.8			V
E03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
E04	Ipu()	Pull-up Current in CLK	V() = 0 ... VDD - 1 V	-240	-120	-25	µA
E05	fclk()	Permissible Clock Frequency at CLK				4	MHz
E06	tp(CLK-DATA)	Propagation Delay: CLK edge vs. DATA output	all modes, RL(SLO) ≥ 1 kΩ	10		50	ns
E07	tbusy()	Processing Time			0		
E08	ttos()	Timeout	CFGTOS = 0x01 iC-NQL_X3 CFGTOS = 0x01, iC-NQL_3		16 20		µs µs
EEPROM Interface, Control Logic: Inputs SDA, NERR							
F01	Vt()hi	Threshold Voltage hi				2	V
F02	Vt()lo	Threshold Voltage lo		0.8			V
F03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
F04	tbusy()cfg	Duration of Startup Configuration	error free EEPROM access		5	7	ms
EEPROM Interface, Control Logic: Outputs SDA, SCL, NERR							
G01	f()	Write/Read Clock at SCL			20	100	kHz
G02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.45	V
G03	Ipu()	Pull-up Current	V() = 0 ... VDD - 1 V	-600	-300	-75	µA
G04	ft()	Fall Time	CL() = 50 pF			60	ns
G05	tmin()lo	Error Signal Indication Time at NERR (lo signal)	CLK = hi, no amplitude or frequeny error	10			ms
G06	Tpwm()	Duty Cycle Of Error Indication at NERR	fosc() subdivided by 2^{22}		60.7		ms
G07	t()lo	Duty Cycle Of Error Indication at NERR	signal duration low to high; AERR = 0 (amplitude error) FERR = 0 (frequency error)		 75 50		 % %
G08	RL()	Permissible Load at SDA, SCL	TMA = 1 (calibration mode)	1			MΩ

ELECTRICAL CHARACTERISTICS: Diagrams

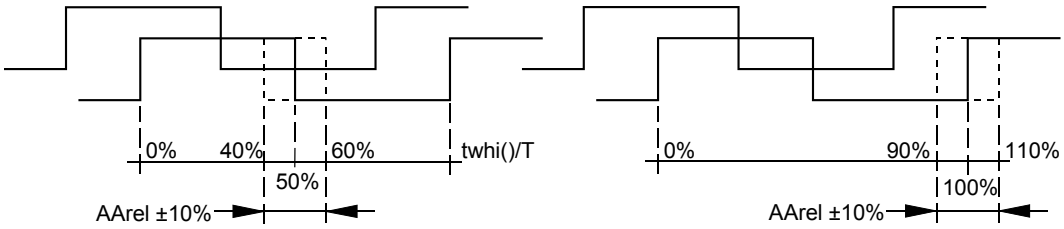


Figure 1: Definition of relative angle error.

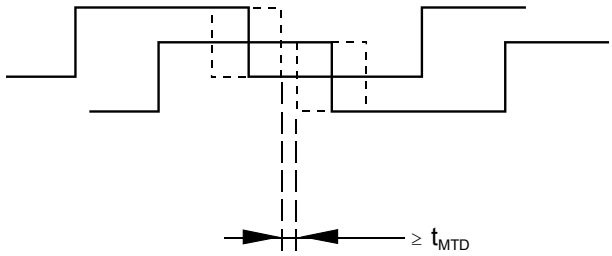


Figure 2: Definition of minimum transition distance.

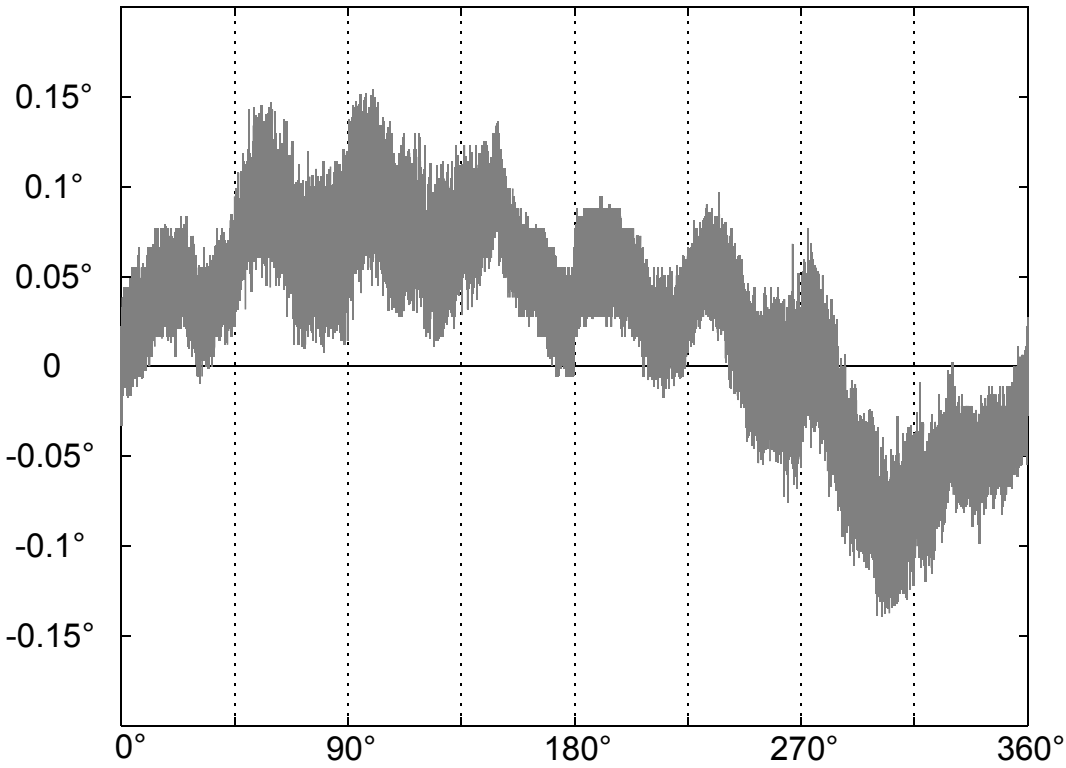


Figure 3: Typical residual absolute angle error after calibration.

OPERATING REQUIREMENTS: SSI INTERFACE

Operating Conditions: VDD = 5 V ±10 %, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I001	T_{CLK}	Permissible Clock Period	CFGTOS = 0x01	4	250	2x t_{tos}	ns
I002	t_{CLKhi}	Clock Signal Hi Level Duration		4	25	t_{tos}	ns
I003	t_{CLKlo}	Clock Signal Lo Level Duration		4	25	t_{tos}	ns

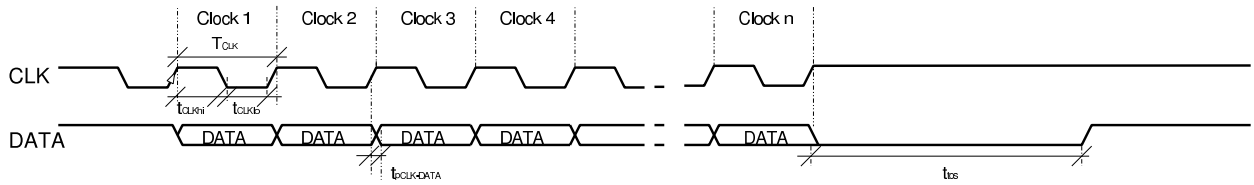


Figure 4: Timing diagram of SSI output.

PARAMETERS and REGISTERS

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0	0	0	SELRES(4:0)				
0x01	HYS(2:0)			ZPOS(4:0)				
0x02	ENRESDEL	1	ROT	0	CFGABZ(1:0)		CFGZ(1:0)	
0x03	CFGSSI(1:0)		CFGAB(1:0)		0	0	AERR	FERR
0x04	FCTR(7:0)							
0x05	0	FCTR(14:8)						
0x06	0	0	CFGTOS(1:0)		TMODE(2:0)			TMA
0x07	0	0	0	0	0	0	0	0
0x08	GAIN(3:0)				RATIO(3:0)			
0x09	SINOFFS(7:0)							
0x0A	COSOFFS(7:0)							
0x0B	PHASE(5:0)						REFOFFS	RATIO(4)
0x0C	0	0	0	0	0	SELAMPL	AMPL(1:0)	
0x0D	0	0	0	0	0	0	0	0
0x0E	0	0	0	0	0	0	0	0
0x0F	CRC_E2P(7:0) - check value read from the EEPROM for addresses 0x00 to 0x0E							
Note	Registers not in use must be set to zero unless otherwise noted.							

Table 5: Register layout

SIGNAL CONDITIONING

Input stages SIN and COS are configured as instrumentation amplifiers. The amplifier gain must be selected in accordance with the sensor signal level and programmed to register GAIN according to the following table. Half of the supply voltage is output to VREF as center voltage to help DC level adaptation.

GAIN	Adr 0x08, Bit 7:4				
		Sine/Cosine Input Signal Levels Vin()			
		Amplitude		Average value (DC)	
Code	Amplification	Differential	Single-ended	Differential	Single-ended
0x0F	80.000	up to 50 mVpp	up to 100 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0E	66.667	up to 60 mVpp	up to 120 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0D	53.333	up to 75 mVpp	up to 0.15 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0C	40.000	up to 0.1 Vpp	up to 0.2 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0B	33.333	up to 0.12 Vpp	up to 0.24 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0A	28.571	up to 0.14 Vpp	up to 0.28 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x09	26.667	up to 0.15 Vpp	up to 0.3 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x08	20.000	up to 0.2 Vpp	up to 0.4 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x07	14.287	up to 0.28 Vpp	up to 0.56 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.4 V
0x06	10.000	up to 0.4 Vpp	up to 0.8 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.5 V
0x05	8.000	up to 0.5 Vpp	up to 1 Vpp	0.8 V ... VDDA - 1.4 V	1.0 V ... VDDA - 1.6 V
0x04	6.667	up to 0.6 Vpp	up to 1.2 Vpp	0.8 V ... VDDA - 1.4 V	1.1 V ... VDDA - 1.7 V
0x03	5.333	up to 0.75 Vpp	up to 1.5 Vpp	0.9 V ... VDDA - 1.5 V	1.3 V ... VDDA - 1.9 V
0x02	4.000	up to 1 Vpp	up to 2 Vpp	1.2 V ... VDDA - 1.6 V	1.7 V ... VDDA - 2.1 V
0x01	3.333	up to 1.2 Vpp	up to 2.4 Vpp	1.2 V ... VDDA - 1.7 V	1.8 V ... VDDA - 2.3 V
0x00	2.667	up to 1.5 Vpp	up to 3 Vpp	1.3 V ... VDDA - 1.8 V	2.0 V ... VDDA - 2.6 V

Table 6: Gain Select

SINOFFS	Adr 0x09, Bit 7:0	
COSOFFS	Adr 0x0A, Bit 7:0	
Code	Output Offset	Input Offset
0x00	0 V	0 V
0x01	-7.8125 mV	-7.8125* mV / GAIN
...	...	...
0x7F	-0.9922 V	-0.9922 V / GAIN
0x80	0 V	0 V
0x81	+7,8125 mV	+7.8125 mV / GAIN
...	...	...
0xFF	+0.9922 V	+0.9922 V / GAIN
Notes	*) With REFOFFS = 0x00 und VDDA = 5 V.	

Table 7: Offset Calibration Sine/Cosine

REFOFFS	Adr 0x0B, Bit 1
Code	Reference Voltage
0x00	Depending on VDDA (example of application: MR sensors)
0x01	Not depending on VDDA (example of application: Sin/Cos encoders)

Table 8: Offset Calibration Reference

RATIO	Adr 0x0B, Bit 0, Adr 0x08, Bit 3:0		
Code	COS / SIN	Code	COS / SIN
0x00	1.0000	0x10	1.0000
0x01	1.0067	0x11	0.9933
...	...	...	...
0x0F	1.1	0x1F	0.9000

Table 9: Amplitude Calibration

PHASE	Adr 0x0B, Bit 7:2		
Code	Phase Shift	Code	Phase Shift
0x00	90°	0x20	90°
0x01	90.703125°	0x21	89.296875°
...	...	...	...
0x12	102.65625°	0x32	77.34375°
...	102.65625°	...	77.34375°
0x1F	102.65625°	0x3F	77.34375°

Table 10: Phase Calibration

CONVERTER FUNCTIONS

SELRES	Adr 0x00, Bit 4:0	
Code	Binary Resolutions	Examples of Permissible Input Frequencies fin_{max} (FCTR 0x0004, 0x4304)
0x00	-	
0x01	-	
0x02	-	
0x03	8192	158 Hz, 635 Hz
0x04	4096	317 Hz, 1.27 kHz
0x05	2048	634 Hz, 2.54 kHz
0x06	1024	1.27 kHz, 5.1 kHz
0x07	512	2.54 kHz, 10.2 kHz
0x08	256	5.1 kHz, 20.3 kHz
0x09	128	10.2 kHz, 40.6 kHz
0x0A	64	20.3 kHz, 81.3 kHz
0x0B	32	40.6 kHz, 162.5 kHz
0x0C	16	81.3 kHz (max. 250 kHz @ 0x4202)
0x0D	8	162 kHz (max. 250 kHz @ 0x4102)
0x0E	-	
0x0F	-	

Table 11: Binary Resolutions

SELRES	Adr 0x00, Bit 4:0	
Code	Decimal Resolutions	Examples of Permissible Input Frequencies fin_{max} (FCTR 0x0004, 0x4304)
0x10	2000	650 Hz, 2.6 kHz
0x11	1600	812 Hz, 3.3 kHz
0x12	1000	1.3 kHz, 5.2 kHz
0x13	800	1.6 kHz, 6.5 kHz
0x14	500	2.6 kHz, 10.4 kHz
0x15	400	3.2 kHz, 13 kHz
0x16	250 *1	5.2 kHz, 20.8 kHz
0x17	125 *1,2	5.2 kHz, 20.8 kHz
0x18	320	4.1 kHz, 16.3 kHz
0x19	160 *2	4.1 kHz, 16.3 kHz
0x1A	80 *4	4.1 kHz, 16.3 kHz
0x1B	40 *8	4.1 kHz, 16.3 kHz
0x1C	200	6.5 kHz, 26 kHz
0x1D	100 *2	6.5 kHz, 26 kHz
0x1E	50 *1,4	6.5 kHz, 26 kHz
0x1F	25 *1,8	6.5 kHz, 26 kHz
Notes	*1 Not useful with incremental A quad B output. *2,4,8 The internal converter resolution is higher by a factor of 2, 4 or 8.	

Table 12: Decimal Resolutions

HYS	Adr 0x01, Bit 7:5		
Code	Hysteresis in degree	Hysteresis in LSB	Absolute Angle Error*
0x00	0°		
0x01	0.0879°	1 LSB @ 12 bit	0.044°
0x02	0.1758°	1/2 LSB @ 10 bit	0.088°
0x03	0.3516°	1 LSB @ 10 bit	0.176°
0x04	0.7031°	1/2 LSB @ 8 bit	0.352°
0x05	1.4063°	1 LSB @ 8 bit	0.703°
0x06	5.625°		2.813°
0x07	45°	only recommended for calibration	22.5°
Notes	*) The absolute angle error is equivalent to one half the angle hysteresis		

Table 13: Hysteresis

MAXIMUM POSSIBLE CONVERTER FREQUENCY

The converter frequency automatically adjusts to the value necessary for the input frequency and resolution. This value ranges from zero to a maximum dependent on the oscillator frequency which can be set using register FCTR.

Serial data output

For SSI output the maximum possible converter frequency can be adjusted to suit the maximum input frequency; an automatic converter resolution step-down feature can be enabled via the FCTR register. Should the input frequency exceed the frequency limit of the selected converter resolution, the LSB is kept stable and not resolved any further; the interpolation resolution halves.

If the next frequency limit is overshot, the LSB and the LSB+1 are kept stable and so on. When the input frequency again sinks below this frequency limit, the fine resolution automatically returns.

Max. Possible Converter Frequency For Serial Data Output

	Resolution Requirements			Protocol	Max. Input Frequency	Restrictions at high input frequency	Examples* fin_{max} [kHz] at resol.		
FCTR	**Min. Res.**	**bin**	**dec**	**SSI**	**fin_{max}**		**8192**	**1024**	**200**
0x0004		X	X	X	fosc()min / 40 / Resolution	–	0.16	1.27	6.5
0x4102	≥ 8	X	X	X	fosc()min / 24 / Resolution	Rel. angle error 2x increased	0.26	2.1	10.8
0x4202	≥ 16	X	X	X	2 x fosc()min / 24 / Res.	Rel. angle error 4x increased	0.53	4.2	21.6
0x4304	≥ 32	X	X	X	4 x fosc()min / 40 / Res.	Rel. angle error 8x increased	0.64	5.1	26.0
0x4602	≥ 64	X	-	X	4 x fosc()min / 24 / Res.	Resolution lowered by factor of 2	1.1	8.5	-
0x4A02	≥ 128	X	-	X	8 x fosc()min / 24 / Res.	Res. lowered by factor of 2-4	2.1	16.9	-
0x4E02	≥ 256	X	-	X	16 x fosc()min / 24 / Res.	Res. lowered by factor of 2-8	4.2	33.8	-
0x5202	≥ 512	X	-	X	32 x fosc()min / 24 / Res.	Res. lowered by factor of 2-16	8.5	67.7	-
0x5602	≥ 1024	X	-	X	64 x fosc()min / 24 / Res.	Res. lowered by factor of 2-32	16.9	135	-
0x5A02	≥ 2048	X	-	X	128 x fosc()min / 24 / Res.	Res. lowered by factor of 2-64	33.8	250	-
0x5E02	≥ 4096	X	-	X	256 x fosc()min / 24 / Res.	Res. lowered by factor of 2-128	67.7	-	-
0x6202	8192	X	-	X	512 x fosc()min / 24 / Res.	Res. lowered by factor of 2-256	135	-	-
Notes	*) Calculated with fosc()min taken from Electrical Characteristics item A01.								

Table 14: Maximum converter frequency for serial data output.

Incremental output to A, B and Z

There are two criteria which must be considered when setting the maximum possible converter frequency via the FCTR register:

1. The maximum input frequency
2. System limitations, e.g. due to slow counters or cable transmission

When facing system limitations it is useful to preselect a minimum transition distance for the output signals. A digital zero-delay glitch filter then takes care of a temporal edge-to-edge separation, guaranteeing spike-free output signals after an ESD impact to the sensor, for instance.

A serial data output is simultaneously possible at any time. However, for the transfer of angle data to the output register the incremental output is halted for one period of the clock signal applied to pin CLK.

1. Max. Possible Converter Frequency Defined By The Maximum Input Frequency								
	Output Frequency fout @ fin_{max}	Resolution Requirem.		Maximum Input Frequency	Restrictions at high input frequency	Examples* fin_{max} [kHz] at resol.		
FCTR	**A, B**	**bin**	**dec**	**fin_{max}**		**8192**	**1024**	**200**
0x0004	325 kHz	X	X	fosc()min / 40 / Resolution	None	0.16	1.27	6.5
0x4102	542 kHz	X	X	fosc()min / 24 / Resolution	Relative angle error 2x increased	0.26	2.1	10.8
0x4202	1.08 MHz	X	X	2 x fosc()min / 24 Res.	Relative angle error 4x increased	0.53	4.2	21.6
0x4304	1.3 MHz	X	X	4 x fosc()min / 40 / Res.	Relative angle error 8x increased	0.64	5.1	26.0
Notes	*) Calculated with fosc()min taken from Electrical Characteristics item A01.							

Table 15: Max. converter frequency for incremental A/B/Z output, defined by the max. input frequency

2. Max. Possible Converter Frequency Defined By The Minimum Transition Distance						
	Output Frequency fout @ t_{MTD}	Resolution Requirem.		Minimum Transition Distance at A, B	Restrictions at high input frequency	Example* t_{MTD} [µsec]
FCTR	**A, B**	**bin**	**dec**	**t_{MTD}**		
0x00FF	11 kHz	X	X	2048 / fosc()max	None	22.8
0x00FE	11.03 kHz	X	X	2040 / fosc()max	None	22.7
0x00FD	11.07 kHz	X	X	2032 / fosc()max	None	22.6
...	...	...	...	...	...	...
0x0006	402 kHz	X	X	56 / fosc()max	None	0.62
0x0005	536 kHz	X	X	48 / fosc()max	None	0.53
0x0004	562 kHz	X	X	40 / fosc()max	None	0.44
0x4102	938 kHz	X	X	24 / fosc()max	Relative angle error 2x increased	0.27
0x4202	1.87 MHz	X	X	12 / fosc()max	Relative angle error 4x increased	0.13
0x4304	2.25 MHz	X	X	10 / fosc()max	Relative angle error 8x increased	0.11
Notes	*) Calculated with fosc()max taken from El.Char. item A01; the min. transition distance refers to output A vs. output B without reversing the sense of rotation.					

Table 16: Max. converter frequency for incremental A/B/Z output, defined by the min. transition distance

INCREMENTAL SIGNALS

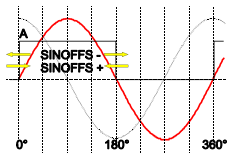
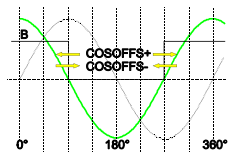
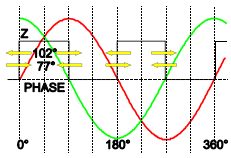
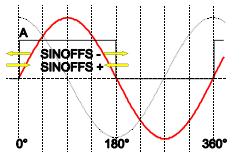
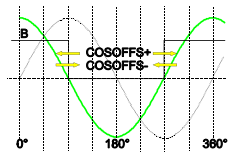
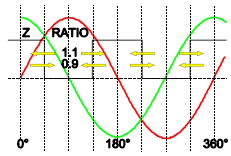
CFGABZ	Adr 0x02, Bit 3:2			
Code	Mode	Pin A	Pin B	Pin Z
0x00	Normal	A	B	Z
0x01	Control signals for external period counters	CA	CB	CZ
0x02	Calibration mode **Offset+Phase** The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 CFGAB = 0x00 AERR = 0x00	 Figure 5: Offset SIN*	 Figure 6: Offs. COS*	 Figure 7: Phase*
0x03	Calibration mode **Offset+Amplitude** The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 CFGAB = 0x00 AERR = 0x00	 Figure 8: Offset SIN*	 Figure 9: Offs. COS*	 Figure 10: Amplit.*
Notes	*) Trimmed accurately when duty cycle is 50 %; Recommended trimming order (after selecting GAIN): Offset, Phase, Amplitude Ratio, Offset;			

Table 17: Outputs A, B, Z

ROT	Adr 0x02, Bit 5
Code	Direction
0x00	Not inverted
0x01	Inverted

Table 18: Direction of Rotation

ENRESDEL	Adr 0x02, Bit 7	
Code	Output*	Function
0x00	immediately	An external counter displays the absolute angle following power on.
0x01	after 5 ms	An external counter only displays changes vs. the initial power-on condition (moving halted to reapply power is precondition.)
Notes	*) Output delay after device configuration and internal reset.	

Table 19: Output Turn-On Delay A, B, Z

ZPOS	Adr 0x01, Bit 4:0
Code	Position
0x00	0°
0x08	90°
0x10	180°
0x18	270°
Notes	The zero signal is only output if released by the input pins (for instance with PZERO = 5 V, NZERO = VREF).

Table 20: Zero Signal Position

CFGZ	Adr 0x02, Bit 1:0
Code	Length
0x00	90°
0x01	180°
0x02.. 03	Synchronization

Table 21: Zero Signal Length

CFGAB	Adr 0x03, Bit 5:4
Code	Z = 1 for
0x00	B = 1, A = 1
0x01	B = 0, A = 1
0x02	B = 1, A = 0
0x03	B = 0, A = 0

Table 22: Zero Signal Logic

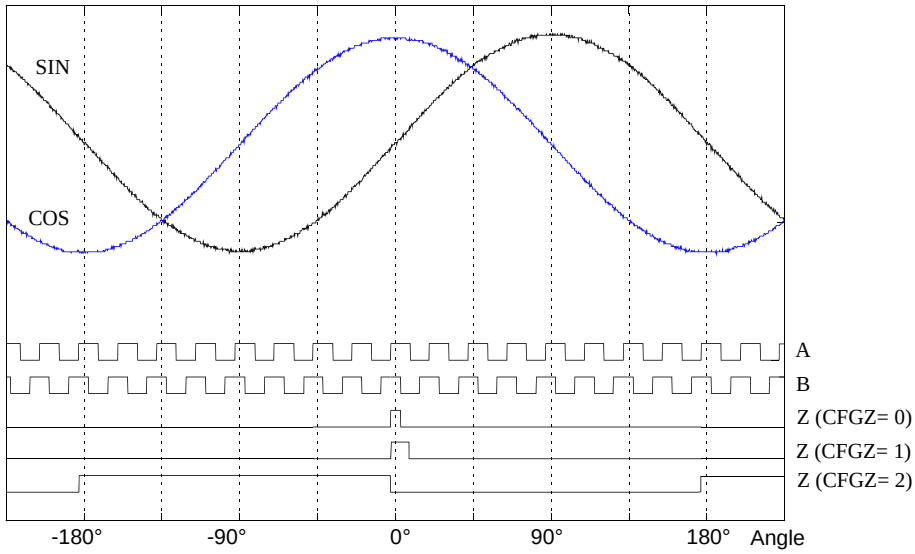


Figure 11: Incremental output signals for various length of the zero signal.
Example for a resolution of 64 (SELRES = 0x0A), a zero signal position of 0° (ZPOS = 0x00, CFGAB = 0x00) and no reversal of the rotational sense (ROT = 0x00, COS leads SIN).

SIGNAL MONITORING and ERROR MESSAGES

SELAMPL **AMPL**	Adr 0x0C, Bit 2 Adr 0x0C, Bit 1:0	
	Max (|Sin| , |Cos|)	
Code	Voltage threshold V_{th}	Output amplitude*
0x00	0.60 x VDDA	1.4 Vpp
0x01	0.64 x VDDA	2.0 Vpp
0x02	0.68 x VDDA	2.6 Vpp
0x03	0.72 x VDDA	3.1 Vpp
	$Sin^2 + Cos^2$	
Code	$V_{thmin} \leftrightarrow V_{thmax}$	Output amplitude*
	Design iC-NQL_X3:	
0x04	(0.48 ↔ 0.68) x VDDA	2.4 Vpp ↔ 3.4 Vpp
0x05	(0.56 ↔ 0.76) x VDDA	2.8 Vpp ↔ 3.8 Vpp
0x06	(0.64 ↔ 0.84) x VDDA	3.2 Vpp ↔ 4.2 Vpp
0x07	(0.72 ↔ 0.92) x VDDA	3.6 Vpp ↔ 4.6 Vpp
	Design iC-NQL_3:	
0x04	(0.20 ↔ 0.9) x VDDA	$1.0\,V_{ss} \leftrightarrow 4.5\,V_{ss}$
0x05	(0.30 ↔ 0.9) x VDDA	$1.5\,V_{ss} \leftrightarrow 4.5\,V_{ss}$
0x06	(0.40 ↔ 0.9) x VDDA	$2.0\,V_{ss} \leftrightarrow 4.5\,V_{ss}$
0x07	(0.50 ↔ 0.9) x VDDA	$2.5\,V_{ss} \leftrightarrow 4.5\,V_{ss}$
Notes	*) Entries are calculated with VDDA = 5 V.	

Table 23: Signal Amplitude Monitoring

AERR	Adr 0x03, Bit 1
Code	Amplitude error message
0x00	disabled
0x01	enabled

Table 24: Amplitude Error

FERR	Adr 0x03, Bit 0
Code	Excessive frequency error message
0x00	disabled
0x01	enabled
Note	Input frequency monitoring is operational for resolutions ≥ 16

Table 25: Frequency Error

Configuration Error	
-	Messaging always released

Table 26: Configuration Error

Error Indication at NERR	
Failure Mode	Pin signal NERR
No error	HI
Amplitude error	LO/HI = 75 %
Frequency error	LO/HI = 50 %
Configuration	LO
Undervoltage	LO
System error	NERR = low by external error signal

Table 27: Error indication at NERR

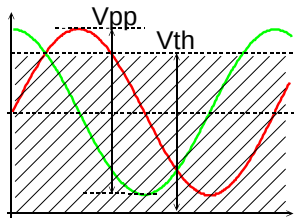


Figure 12: Signal monitoring of minimum amplitude.

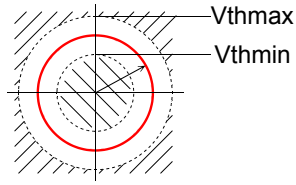


Figure 13: $Sin^2 + Cos^2$ signal monitoring.

To enable the diagnosis of faults, the various types of error are signaled at NERR using a PWM code as given in the key table.

Two error bits are provided to enable communication via the SSI interface; these bits can decode four different types of error. If NERR is held at low by an external source, such as an error message from the system, for example, this can also be verified via the SSI interface.

Error events are stored for the SSI data output and deleted afterwards. Errors at NERR are displayed for a minimum of ca. 10 ms, as far as no SSI readout causes a deletion.

If an error in amplitude occurs the conversion process is terminated and the incremental output signals halted. An error in amplitude rules out the possibility of an error in frequency.

Error Messages SSI	
Failure Mode	Error bits E1, E0 (actice low)
No error	1, 1
Amplitude error	0, 1
Frequency error	1, 0
Configuration	0, 0
System error	0, 0 (NERR pulled low by external signal)
Line Signal SLO	iC-NQL_3: Data output is deactivated and SLO permanently high in case of: configuration phase, invalid configuration, undervoltage.

Table 28: Error Messages SSI

TEST FUNCTIONS

TMODE	Adr 0x06, Bit 3:1	
Code	Signal at Z	Description
0x00	Z	no test mode
0x01	A xor B	Output A EXOR B
0x02	ENCLK	iC-Haus device test
0x03	NLOCK	iC-Haus device test
0x04	CLK	iC-Haus device test
0x05	DIVC	iC-Haus device test
0x06	PZERO - NZERO	iC-Haus device test
0x07	TP	iC-Haus device test
Condition	CFGABZ = 0x00	

Table 29: Test Mode

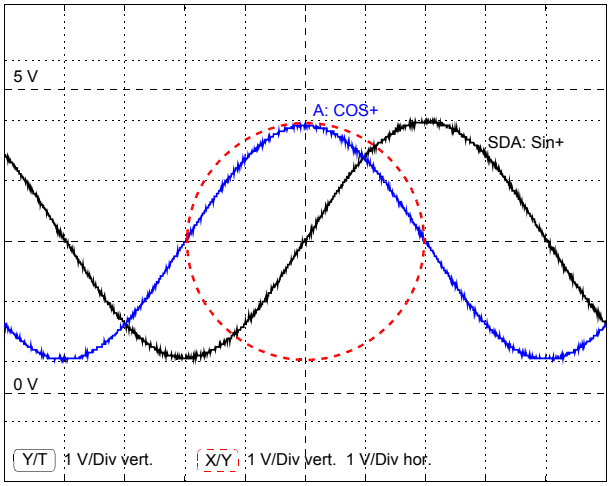


Figure 14: Calibrated signals with TMA mode.

TMA	Adr 0x06, Bit 0			
Code	**Pin A**	**Pin B**	**Pin SDA**	**Pin SCL**
0x00	A	B	SDA	SCL
0x01	COS+	COS-	SIN+	SIN-
Notes	To permit the verification of GAIN and OFFSET settings, the input amplifier outputs are available at the pins. To operate the converter a signal of 4 Vpp is the ideal here and should not be exceeded. Pin loads above 1 MΩ are adviceable for accurate measurements.			

Table 30: Analog Test Mode

Parameter GAIN ideally adjusts the signal levels to ca. 4 Vpp and should not be touched afterwards.

Both scope display modes are feasible for OFFS (positive values) or RATIO adjustments; regarding the adjustment of PHASE the X/Y mode may be preferred.

For OFFS adjustment towards negative values the test signals COS- (pin B) and SIN- (pin SCL) are relevant.

SSI INTERFACE

After each communication cycle the SSI interface returns to its idle state when the monoflop timeout t_{tos} has elapsed. This temporal condition also determines up to which clock line pause duration the iC-NQL retains the current data output cycle - the master may thus not undershoot a minimum clock frequency of f(CLK)min.

CFGTOS	Adr 0x06, Bit 5:4		
Code	Timeout t_{tos}	Ref. clock counts	f(CLK) min*
	Design iC-NQL_X3:		
0x00	typ. 128 µs	256-259	11 kHz
0x01	typ. 16 µs	32-35	88 kHz
0x02	typ. 4 µs	8-11	352 kHz
0x03	typ. 1 µs	2-5	1.41 MHz
	Design iC-NQL_3:		
0x00	typ. 20 µs	46-46	50 kHz
0x01	typ. 20 µs	46-47	50 kHz
0x02	typ. 1.5 µs	3-4	660 kHz
0x03	typ. 1.5 µs	3-4	660 MHz
Notes	A ref. clock count is equal to $\frac{32}{fosc}$ (see El. Char., A01). The permissible max. clock frequency is specified by E05. *) A low clock frequency can reduce the permissible maximum input frequency since conversion is paused after the first falling edge on CLK for a half clock cycle.		

Table 31: Monoflop Time (SSI Timeout)

The iC-NQL position data output contains the angle value (S) with a bit length of 2 to 13 bits (depending on SELRES), and up to 3 add-on bits (error messages E1 and E0 plus a zero bit). Generally, the data output is in binary format starting with the MSB.

Signal Names	
Name	Description
S	Sensor data (S0 is LSB)
E	Error messages
Stop	Low signal

Table 32: Signal Names

The angle conversion is halted for a half clock cycle as soon as the interface receives the first falling edge on CLK, what is the trigger signal to output updated position data. The halt duration must be taken into consideration when calculating the maximum input frequency.

CFGSSI	Adr 0x03, Bit 7:6	
Code	Additional bits	Ring register operation
0x00	E1, E0, zero bit	no
0x01	none	no
0x02	not permissible	
0x03	none	yes

Table 33: SSI Output Options

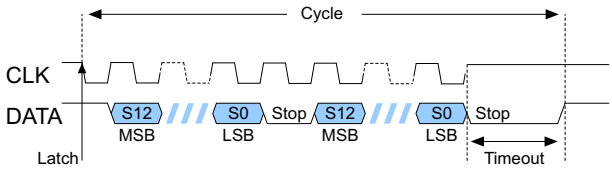


Figure 15: SSI output format during ring register operation. The example displays the transmission of a 13-bit angle value; error messages are switched off herein (SELRES = 0x03, CFGSSI = 0x03)

SSI Output Formats																							
Res	**Mode**	**Error**	**CRC**	**T1**	**T2**	**T3**	**T4... T10**	**T11**	**T12**	**T13**	**T14**	**T15**	**T16**	**T17**	**T18**	**T19**	**T20**	**T21**	**T22**	**T23**	**T24**	**T25**
10 bit	SSI	X	-	S9	S8	S7	S6 ... S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example							0	0	0	0	0	0	0	0	0	0	0	0	0
13 bit	SSI *1	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example								0	0	0	0	0	0	0	0	0	0	0	0
	SSI-R *2	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2
			Example								0											
			Configuration	CFGSSI = 0x00; *1) CFGSSI = 0x01; *2) CFGSSI = 0x03																			
			Legend	SSI = SSI protocol, SSI-R = SSI ring register operation																			

Table 34: SSI Output Formats

EEPROM INTERFACE and STARTUP BEHAVIOUR

Serial EEPROM components permitting operation from 3.3 V to 5 V can be connected (such as 24C02, for example). When the device is switched on the memory area of bytes 0 to 15 is mapped onto iC-NQL's registers.

After the supply has been turned on (power on reset), iC-NQL reads the configuration data from the EEPROM and during this phase halts error pin NERR actively on a low signal (open drain output).

After a successful CRC the data output to SLO is released and the error indication at pin NERR reset; an external pull-up resistor can supply a high signal. iC-NQL then switches to normal operation and determines the current angle position, providing that a sensor is connected up to it and there is no amplitude error (or this is deactivated).

Should the CRC prove unsuccessful due to a data error (disrupted transmission, no EEPROM or the EEPROM is not programmed), the configuration phase is automatically repeated. After a third failed attempt, the procedure is aborted and error pin NERR remains active, displaying a permanent low.

After startup, iC-NQL does not recognize a defined configuration; the configuration RAM can contain any values.

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x127;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 0; // start value !!!
for (iReg = 0; iReg<15; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

CRC_E2P	Adr 0x0F, Bit 7:0
Code	Description
0x00 ... 0xFF	Check value formed by CRC polynomial 0x127

Table 35: Check value for EEPROM data

APPLICATION HINTS

Principle Input Circuits

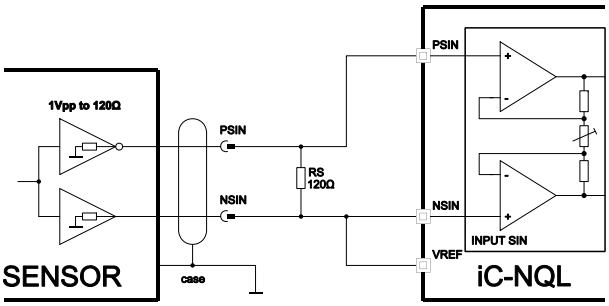


Figure 16: Input circuit for voltage signals of 1 Vpp with no ground reference. When grounds are not separated the connection NSIN to VREF must be omitted.

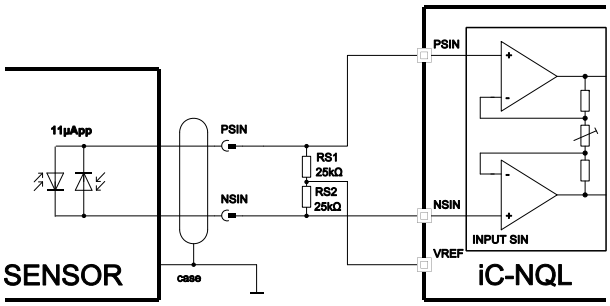


Figure 17: Input circuit for current signals of 11 µA. This circuit does not permit offset calibration.

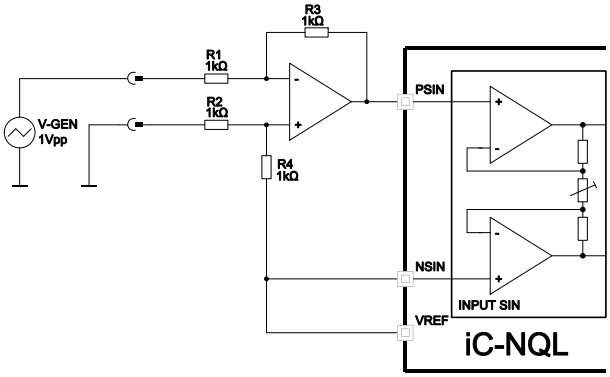


Figure 18: Input circuit for single-sided voltage or current source signals with ground reference (adaptation via resistors R3, R4).

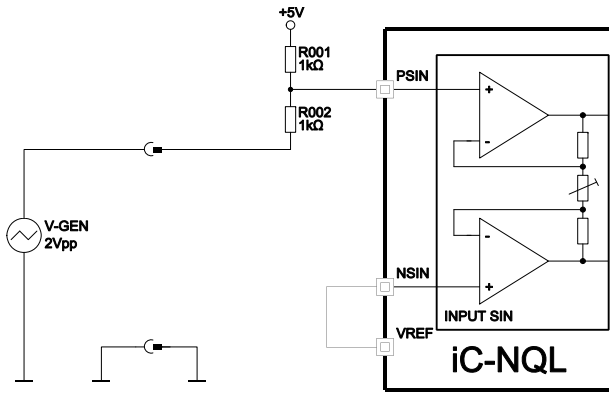


Figure 19: Simplified input wiring for single-sided voltage signals with ground reference.

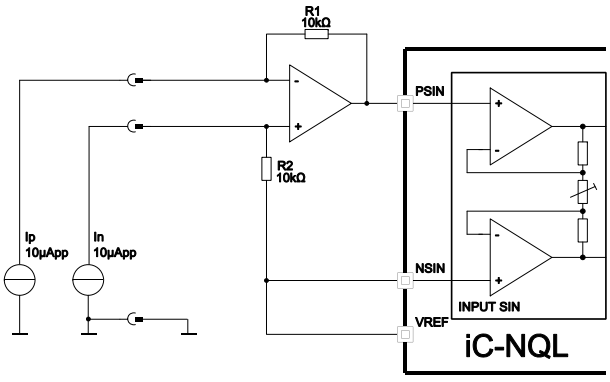


Figure 20: Input circuit for differential current sink sensor outputs, eg. using Opto Encoder iC-WG.

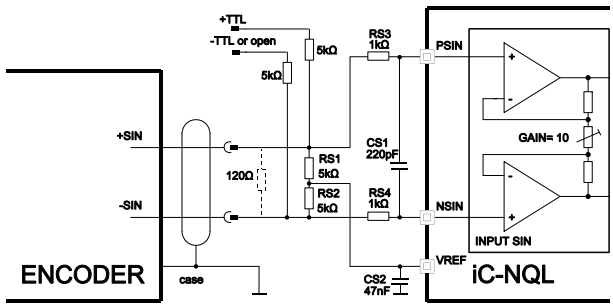


Figure 21: Combined input circuit for 11 µA, 1 Vpp (with 120 Ω termination) or TTL encoder signals. RS3/4 and CS1 serve as protection against ESD and transients.

Basic Circuit

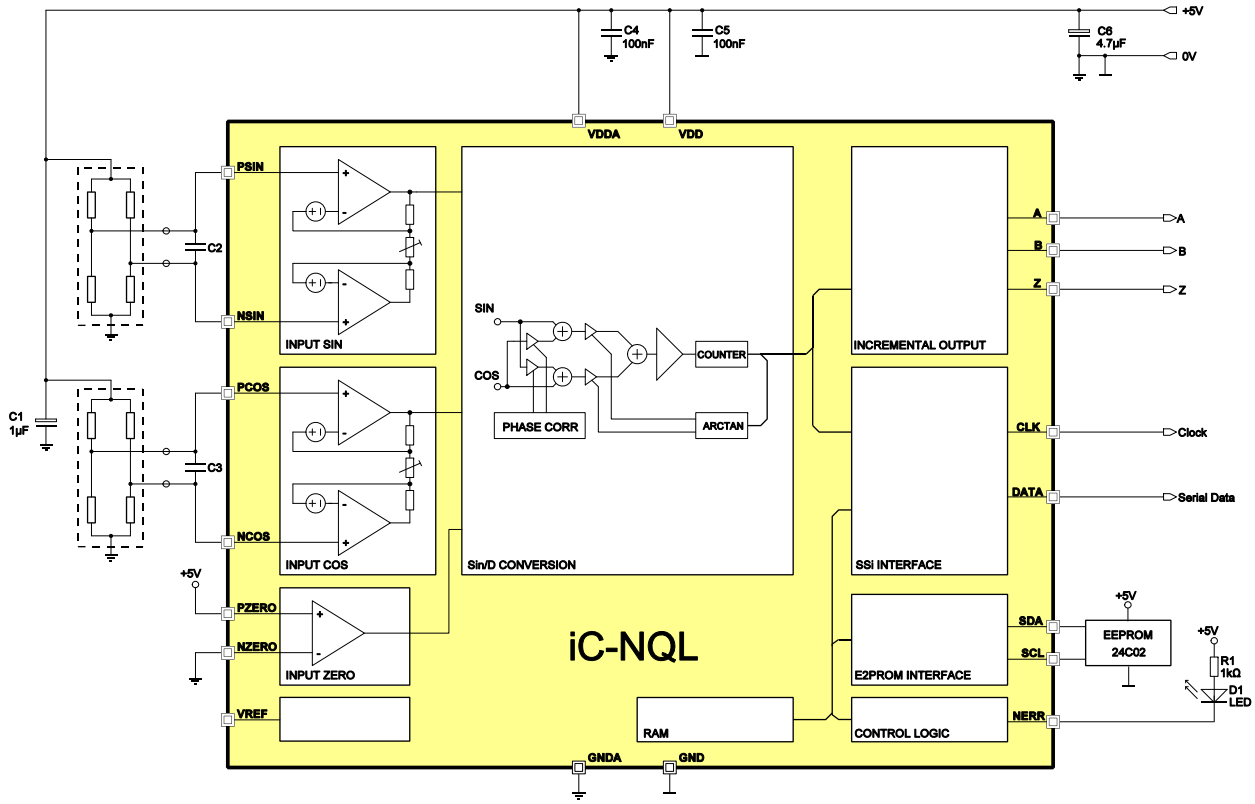


Figure 22: Basic circuit for evaluation of magneto-resistor bridge sensors.

DESIGN REVIEW: Notes On Chip Functions

iC-NQL X3		
No.	Function, Parameter/Code	Description and Application Hints
1	**ZPOS** Illegal settings: 0x01...0x07, 0x09...0x0F, 0x11...0x17, 0x19...0x1F	Illegal settings of ZPOS delay accurate converter operation following power on. Depending on the sin/cos input signals (phase angle) the A/B outputs can provide pulses causing an external counter to alternately count up and down. This may disturb the startup of a drive if the motion controller tolerates only single A/B edges during standstill checking. The converter operation is again accurate when the sin/cos input signals have changed, by a maximum of 45 angular degrees.
2	**Pin DATA**	When cycling power pin DATA may show high or low level initially. With pin TEST = low (e.g. pin open) at least a single low pulse at pin CLK is required to trigger pin DATA to show a high level after the timeout has elapsed. When continuing the clock signal after completion of data output, additional zero bits are output. With pin TEST = high (e.g. pin wired to VDD) only the timeout needs to elapse to trigger pin DATA showing high level. When continuing the clock signal after completion of data output, additional one bits are output.
3	**M2S** obsolete	Bits 5 to 7 of address 0x00 must be programmed to zero; period counting is not available.

Table 36: Notes on chip functions iC-NQL_X3

iC-NQL 3		
No.	Function, Parameter/Code	Description and Application Hints
1	**Pin DATA**	When cycling power pin DATA shows high level initially and remains on a permanent high if CRC verification does not confirm the configuration data.
3	**M2S** obsolete	Bits 5 to 7 of address 0x00 must be programmed to zero; period counting is not available.

Table 37: Notes on chip functions iC-NQL_3

ORDERING INFORMATION

Type	Package	Order Designation
iC-NQL	TSSOP20 4.4 mm	iC-NQL TSSOP20

For technical support, information about prices and terms of delivery please contact:

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