Cascadable IF VGAs with Programmable RMS Detectors

Data Sheet

ADL5336

FEATURES

Pair of VGAs with rms AGC detectors
VGA and AGC modes of operation
Continuous gain control range: 48 dB
Noise figure = 6.8 dB at maximum gain
IMD3 >62 dBc for 1.0 V p-p composite output
Differential input and output
Multiplexed inputs for VGA2
Programmable detector AGC setpoints
Programmable VGA maximum gain
Power-down feature
Single 5 V supply operation

APPLICATIONS

Point-to-multipoint radios
Instrumentation
Medical

FUNCTIONAL BLOCK DIAGRAM

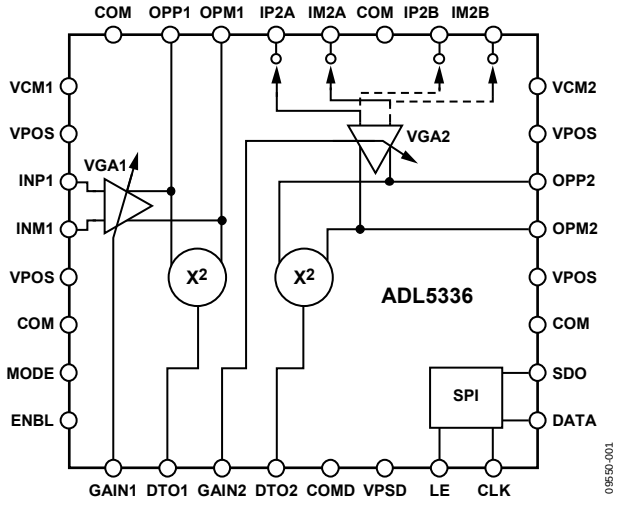


Figure 1.

GENERAL DESCRIPTION

The ADL5336 consists of a pair of variable gain amplifiers (VGAs) designed for cascaded IF applications. The amplifiers have linear-in-dB gain control and operate from low frequencies to 1 GHz. Their excellent gain conformance over the control range and flatness over frequency are due to Analog Devices, Inc., patented X-AMP® architecture, an innovative technique for implementing high performance variable gain control.

Each VGA has 24 dB of gain control range. Their maximum gain can be independently programmable over a 6 dB range via the SPI. The VGAs can be cascaded to provide a total range of 48 dB. When connected to a 50 Ω source through a 1:4 balun, the gain is 6 dB higher. The second VGA has an SPI programmable input switch that selects one of two external inputs.

When driven from a 200 Ω source or from a 50 Ω source through a 1:4 balun, the noise figure (NF) for the composite amplifier is 6.8 dB at maximum gain. The output of each VGA can drive 100 Ω loads to 5 V p-p maximum.

Each VGA has an independent square law detector for autonomous, automatic gain control (AGC) operation. Each detector setpoint can be programmed independently through the SPI from −24 dBV to −3 dBV in 3 dB steps. When both VGAs are arranged in AGC mode and are programmed to the same setpoint, the composite NF increases to 9 dB when backed off by 18 dB from maximum gain.

The ADL5336 operates from a 5 V supply and consumes a typical supply current of 80 mA. When disabled, it consumes 4 mA. It is fabricated in an advanced silicon-germanium BiCMOS process and is available in a 32-lead exposed paddle LFCSP package. Performance is specified over a −40°C to +85°C temperature range.

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REVISION HISTORY

4/2018—Rev. B to Rev. C

Changes to Figure 4 ... 7
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Changes to Ordering Guide ... 30

2/2012—Rev. A to Rev. B

Changes to Figure 70 ... 25
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6/2011—Rev. 0 to Rev. A

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2/2011—Revision 0: Initial Version

SPECIFICATIONS

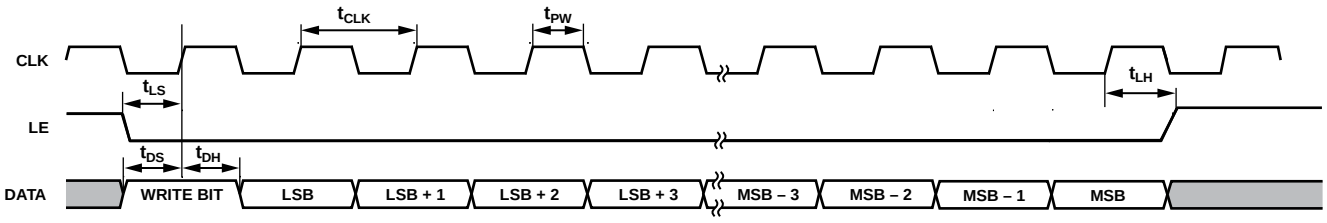
V_S = 5 V, T_A = 25°C, Z_S = 200 Ω, $Z_{L\ VGA1}$ = 200 Ω, $Z_{L\ VGA2}$ = 100 Ω, RF input = −20 dBm at 140 MHz, maximum gain setting for both VGAs, unless otherwise noted. 1:4 balun voltage gain is not included. All dBm numbers are with respect to each VGA's load impedance.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range	3 dB bandwidth	LF		1000	MHz
Maximum Input	INP1/INM1, IP2A/IM2A, IP2B/IM2B differential		8		V p-p
Maximum Output	OPP1/OPM1, OPP2/OPM2 differential at P1dB		5		V p-p
AC Input Impedance					
VGA1	Differential across INP1, INM1		200		Ω
VGA2 Selected Input	Differential across IP2A, IM2A or IP2B, IM2B		200		Ω
VGA2 Unselected Input			10		kΩ
AC Output Impedance	VGA1		1		Ω
	VGA2		3.5		Ω
GAIN CONTROL INTERFACE	GAIN1/GAIN2, MODE				
Voltage Gain Range	GAIN1/GAIN2 from 0 V to 1 V				
VGA1	Gain Code 00	−14.6		+9.7	dB
	Gain Code 01	−12.2		+12	dB
	Gain Code 10	−10.3		+13.8	dB
	Gain Code 11	−8.9		+15.2	dB
VGA2	Gain Code 00	−10.8		+13.4	dB
	Gain Code 01	−8.2		+15.9	dB
	Gain Code 10	−6.6		+17.7	dB
	Gain Code 11	−4.7		+19.5	dB
Gain Step Response Time	8.5 dB Gain Step		5		ns
Gain Slope					
VGA1	MODE = V_S		35		mV/dB
VGA2			35		mV/dB
Gain Error	V_{GAINx} from 0.2 V to 0.8 V		±0.2		dB
Input Impedance	V_{GAINx} to COM		4.6		MΩ
f = 140 MHz					
Noise Figure	VGA1, Gain Code 00, V_{GAIN} = 1 V		7.4		dB
	VGA2, Gain Code 11, V_{GAIN} = 1 V		7.1		dB
Output IP3	VGA1, Gain Code 00, V_{GAIN} = 1 V		21 (28)		dBV (dBm)
Output Voltage Level of 1.0 V p-p					
	VGA1, Gain Code 11, V_{GAIN} = 1 V		18 (25)		dBV (dBm)
	VGA2, Gain Code 00, V_{GAIN} = 1 V		26 (36)		dBV (dBm)
	VGA2, Gain Code 11, V_{GAIN} = 1 V		24 (34)		dBV (dBm)
Output P1dB	VGA1, Gain Code 00, V_{GAIN} = 1 V		3.5 (10.5)		dBV (dBm)
	VGA1, Gain Code 11, V_{GAIN} = 1 V		3.5 (10.5)		dBV (dBm)
	VGA2, Gain Code 00, V_{GAIN} = 1 V		4 (14)		dBV (dBm)
	VGA2, Gain Code 11, V_{GAIN} = 1 V		4 (14)		dBV (dBm)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f = 350 MHz					
Noise Figure	VGA1, Gain Code 00, V_{GAIN} = 1 V		8		dB
	VGA2, Gain Code 11, V_{GAIN} = 1 V		7.7		dB
Output IP3	VGA1, Gain Code 00, V_{GAIN} = 1 V		12 (19)		dBV (dBm)
Output Voltage Level of 1.0 V p-p	VGA1, Gain Code 11, V_{GAIN} = 1 V		10.5 (17.5)		dBV (dBm)
	VGA2, Gain Code 00, V_{GAIN} = 1 V		18 (28)		dBV (dBm)
	VGA2, Gain Code 11, V_{GAIN} = 1 V		16 (26)		dBV (dBm)
Output P1dB	VGA1, Gain Code 00, V_{GAIN} = 1 V		0 (7)		dBV (dBm)
	VGA1, Gain Code 11, V_{GAIN} = 1 V		0 (7)		dBV (dBm)
	VGA2, Gain Code 00, V_{GAIN} = 1 V		−1.5 (+8.5)		dBV (dBm)
	VGA2, Gain Code 11, V_{GAIN} = 1 V		−1.5 (+8.5)		dBV (dBm)
SQUARE LAW DETECTORS	DTO1, DTO2				
Output Setpoint	SPI controlled, 3 dB steps	−24		−3	dBV
Output Range		0.1		$V_S/2$	V
AGC Step Response Range	5 dB input step, C_{AGC} = 0.1 µF		1.5		ms
DIGITAL LOGIC	LE, CLK, DATA, SDO				
Input High Voltage, V_{INH}			>2.2		V
Input Low Voltage, V_{INL}			<1.8		V
Input Current, I_{INH}/I_{INL}				<1	µA
Input Capacitance, C_{IN}				2	pF
SPI TIMING	LE, CLK, DATA, SDO				
f_{CLK}			20		MHz
t_{DH}	DATA hold time		5		ns
t_{DS}	DATA setup time		5		ns
t_{LH}	LE hold time		5		ns
t_{LS}	LE setup time		5		ns
t_{PW}	CLK high pulse width		5		ns
t_D	CLK-to-SDO delay		5		ns
POWER AND ENABLE	VPOS, VPSD, COM, COMD, ENBL				
Supply Voltage Range		4.5	5	5.5	V
Total Supply Current	ENBL = 5 V		80		mA
Disable Current	ENBL = 0 V		4		mA
Disable Threshold			2.3		V
Enable Response Time	Delay following low-to-high transition until device meets full specifications in VGA mode		800		ns
Disable Response Time	Delay following high-to-low transition until device produces full attenuation in VGA mode		20		ns

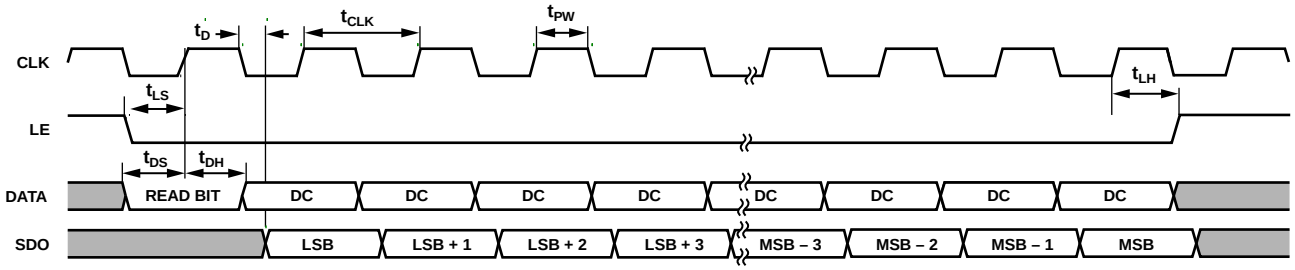
TIMING DIAGRAMS



NOTES
1. THE FIRST DATA BIT DETERMINES WHETHER THE PART IS WRITING TO OR READING FROM THE INTERNAL 8-BIT REGISTER. FOR A WRITE OPERATION, THE FIRST BIT SHOULD BE A LOGIC 1. THE 8-BIT WORD IS THEN REGISTERED INTO THE DATA PIN ON CONSECUTIVE RISING EDGES OF THE CLOCK.

09550-002

Figure 2. Write Mode Timing Diagram



NOTES
1. THE FIRST DATA BIT DETERMINES WHETHER THE PART IS WRITING TO OR READING FROM THE INTERNAL 8-BIT REGISTER. FOR A READ OPERATION, THE FIRST BIT SHOULD BE A LOGIC 0. THE 8-BIT WORD IS THEN UPDATED AT THE SDO PIN ON CONSECUTIVE FALLING EDGES OF THE CLOCK.

09550-003

Figure 3. Read Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages (VPOS, VPSD)	5.5 V
LE, CLK, DATA, SDO	VPOS + 0.5 V
ENBL, MODE	VPOS + 0.5 V
INP1, INM1, IP2A, IM2A, IP2B, IM2B	VPOS + 0.5 V
OPP1, OPM1, OPP2, OPM2	VPOS + 0.5 V
DTO1, DTO2, GAIN1, GAIN2	VPOS/2 + 0.5 V
Internal Power Dissipation	530 mW
θ_{JA} (With Pad Soldered to Board)	37.4°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

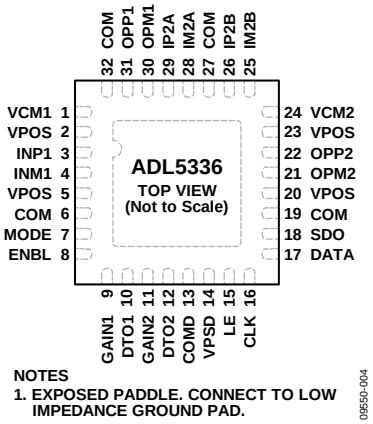


Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 24	VCM1, VCM2	Common-Mode Voltages. Decouple to common for ac-coupled operation.
2, 5, 14, 20, 23	VPOS, VPSD	Analog and Digital Positive Supply Voltage (4.5 V to 5.5 V).
3, 4, 25, 26, 28, 29	INP1, INM1, IM2B, IP2B, IM2A, IP2A	Differential Inputs. 200 Ω input impedance; ac coupling recommended.
6, 13, 19, 27, 32	COM, COMD	Analog and Digital Common. Connect via lowest possible impedance to external circuit common.
7	MODE	Gain Mode Control. Pull high for VGA mode, and pull low for AGC mode.
8	ENBL	Chip Enable. Pull high to enable.
9, 11	GAIN1, GAIN2	Analog Gain Control (0 V to 1 V).
10, 12	DTO1, DTO2	Detector Outputs (0.1 V to VPOS/2 Range).
15, 16, 17, 18	LE, CLK, DATA, SDO	SPI Programming and Data Readout Pins. CMOS levels V_{LOW} < 1.8 V, V_{HIGH} > 2.2 V.
21, 22, 30, 31	OPM2, OPP2, OPM1, OPP1	Differential Outputs. Low output impedance; ac coupling recommended.
	EPAD	Exposed Paddle. Connect to low impedance ground pad.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, Z_S = 200 Ω, $Z_{L\ VGA1}$ = 200 Ω, $Z_{L\ VGA2}$ = 100 Ω, RF input = −20 dBm at 140 MHz, unless otherwise noted. Gain code = 11, V_{GAIN} = 1 V, setpoint code = 000, MODE = 5 V (VGA mode) for both amplifiers, unless otherwise noted.

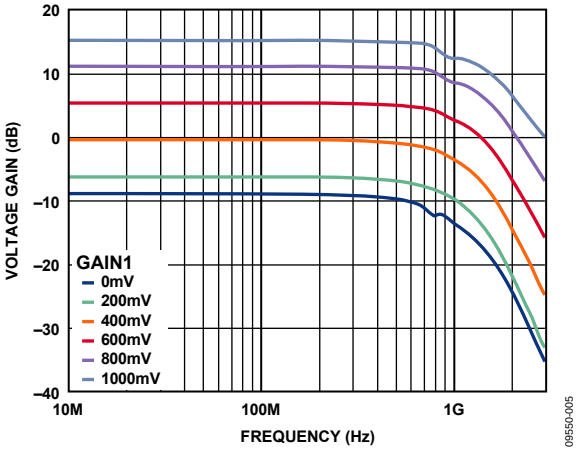


Figure 5. Gain vs. Frequency over V_{GAIN} at Gain Code 11 for VGA1

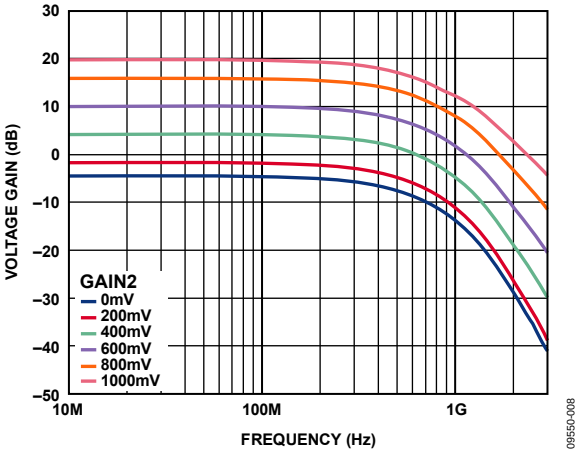


Figure 8. Gain vs. Frequency over V_{GAIN} at Gain Code 11 for VGA2

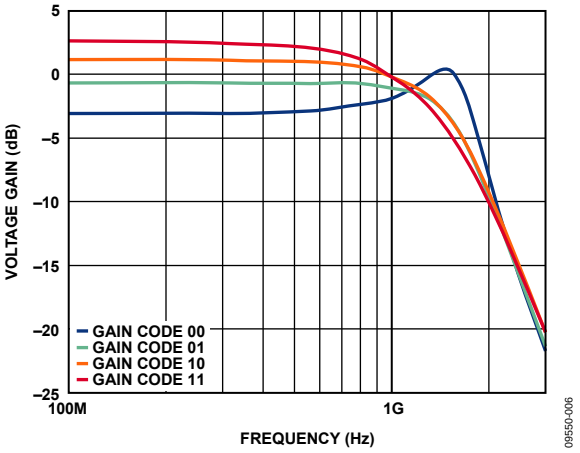


Figure 6. Gain vs. Frequency over Gain Code at V_{GAIN} = 0.5 V for VGA1

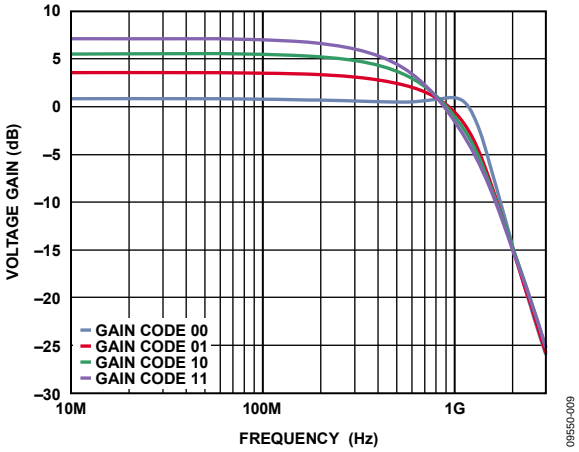


Figure 9. Gain vs. Frequency over Gain Code at V_{GAIN} = 0.5 V for VGA2

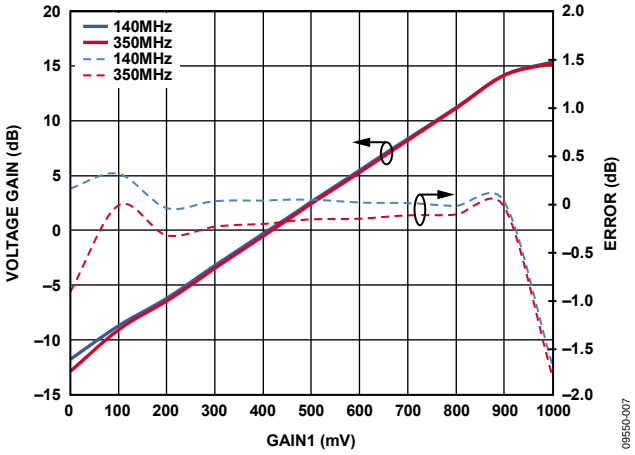


Figure 7. Gain vs. V_{GAIN} over Frequency at Gain Code 11 for VGA1

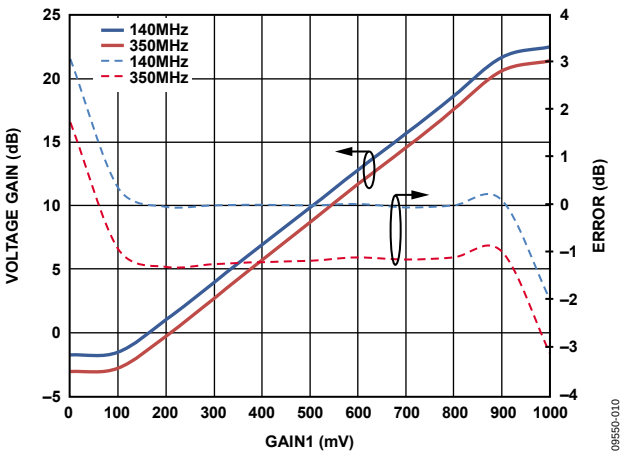


Figure 10. Gain vs. V_{GAIN} over Frequency at Gain Code 11 for VGA2

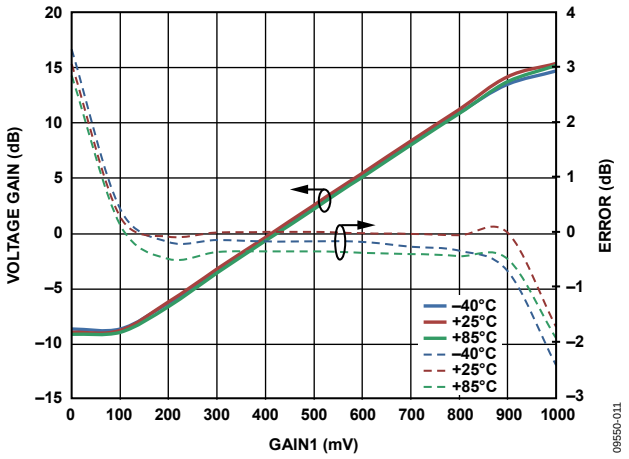


Figure 11. Gain Conformance over Temperature for VGA1

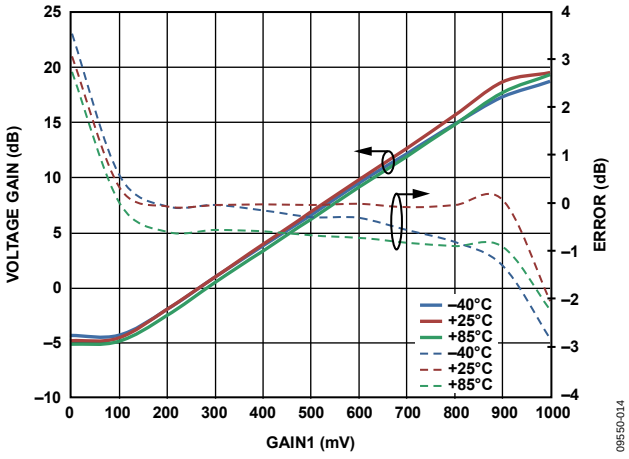


Figure 14. Gain Conformance over Temperature for VGA2

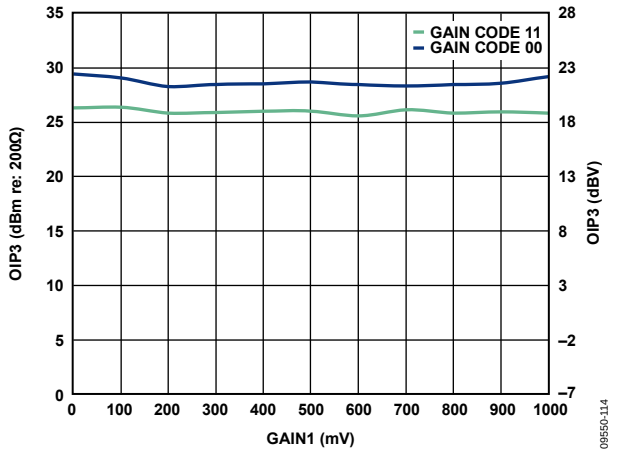


Figure 12. OIP3 vs. V_{GAIN} over Gain Code for VGA1

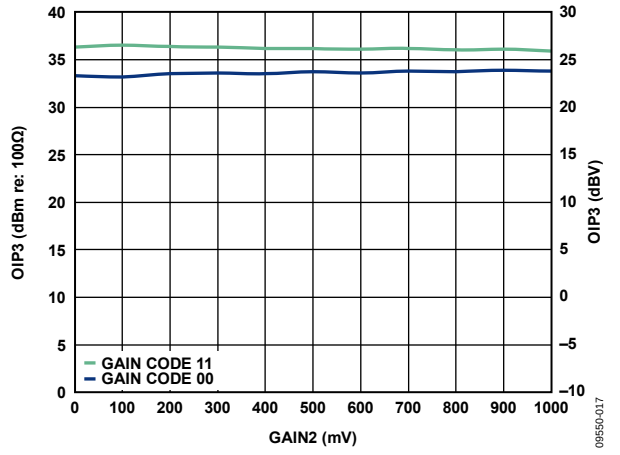


Figure 15. OIP3 vs. V_{GAIN} over Gain Code for VGA2

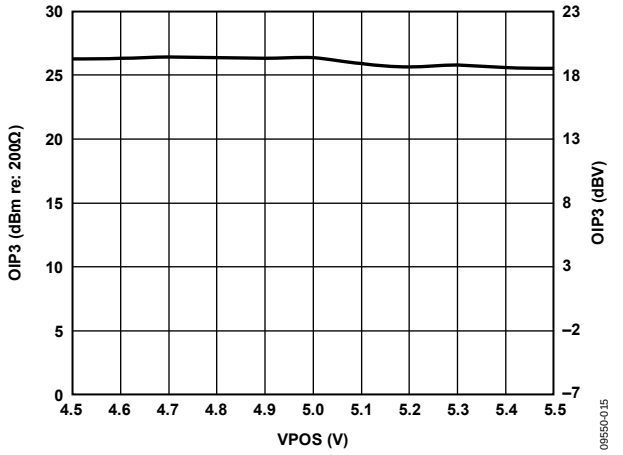


Figure 13. OIP3 vs. Supply Voltage at V_{GAIN} = 0.5 V for VGA1

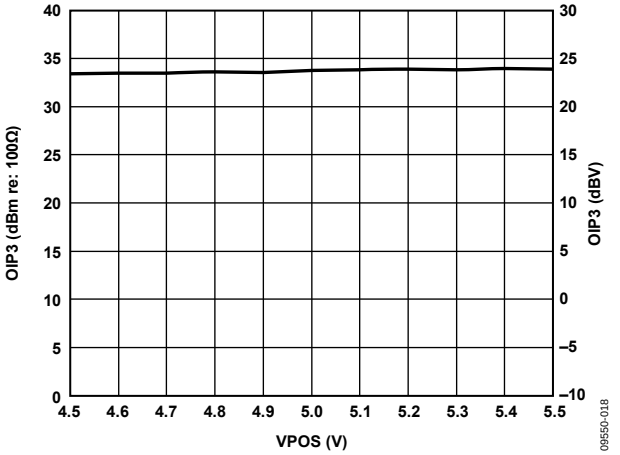


Figure 16. OIP3 vs. Supply Voltage at V_{GAIN} = 0.5 V for VGA2

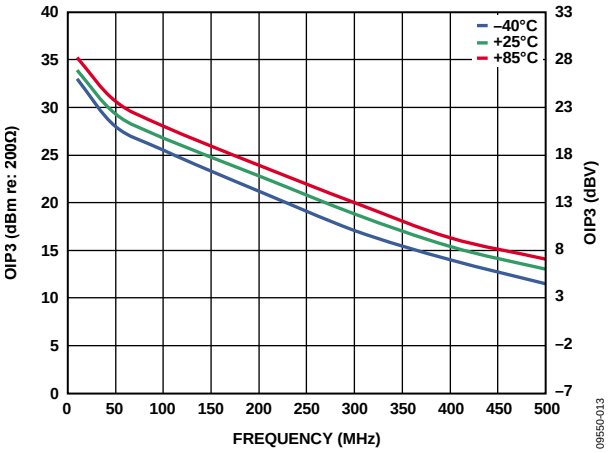


Figure 17. OIP3 vs. Frequency over Temperature for VGA1

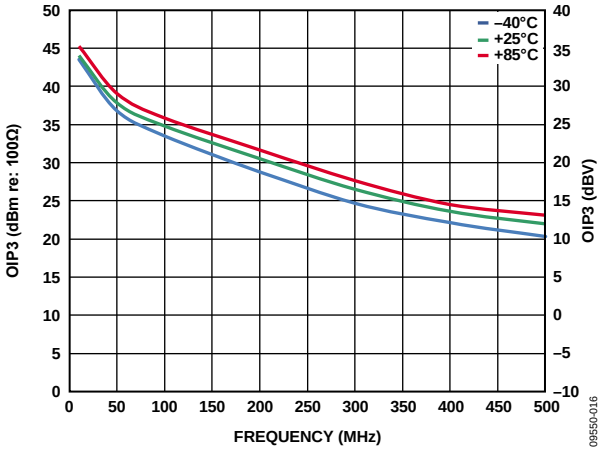


Figure 20. OIP3 vs. Frequency over Temperature for VGA2

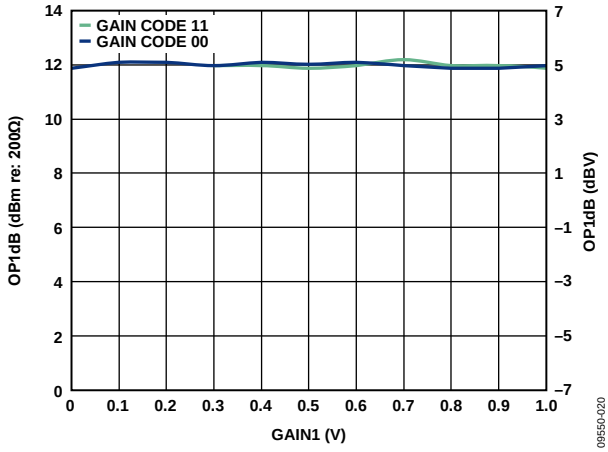


Figure 18. OP1dB vs. V_{GAIN} over Gain Code for VGA1

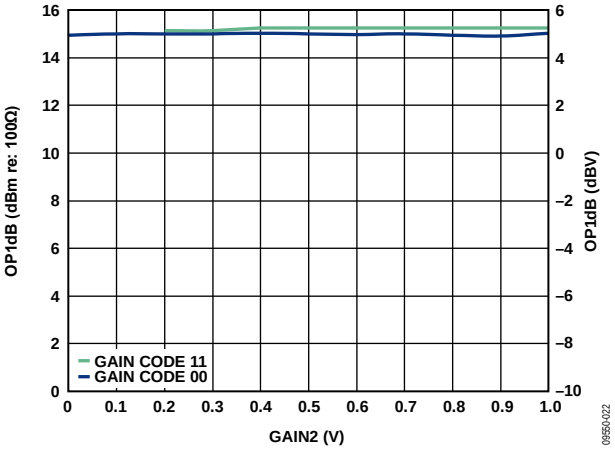


Figure 21. OP1dB vs. V_{GAIN} over Gain Code for VGA2

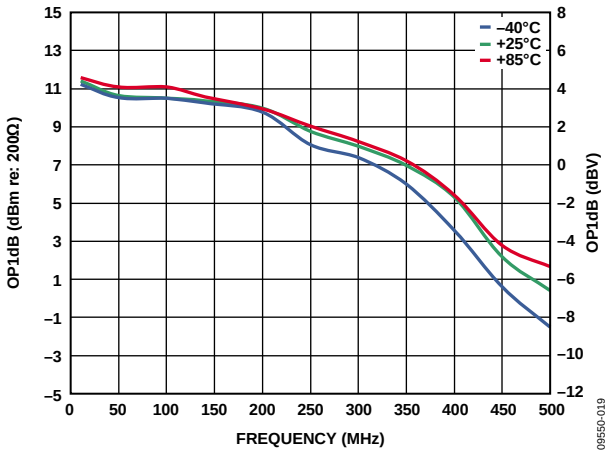


Figure 19. OP1dB vs. Frequency over Temperature for VGA1

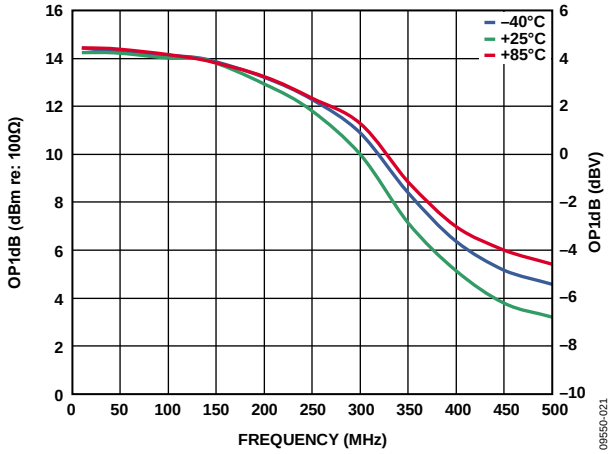


Figure 22. OP1dB vs. Frequency over Temperature for VGA2

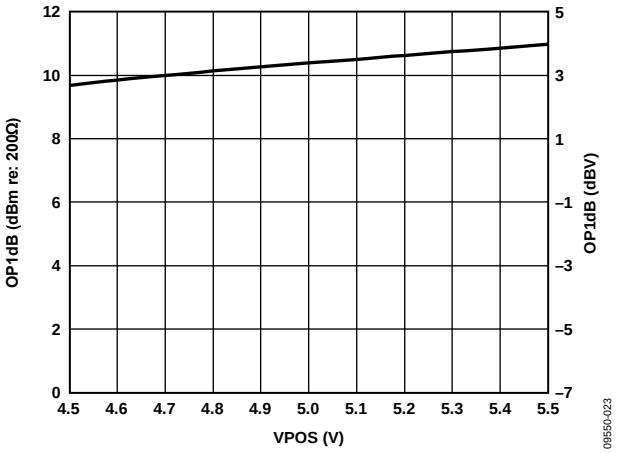


Figure 23. OP1dB vs. Supply Voltage for VGA1

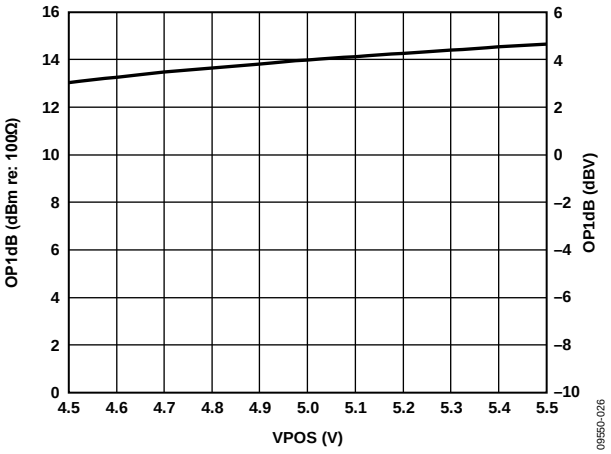


Figure 26. OP1dB vs. Supply Voltage for VGA2

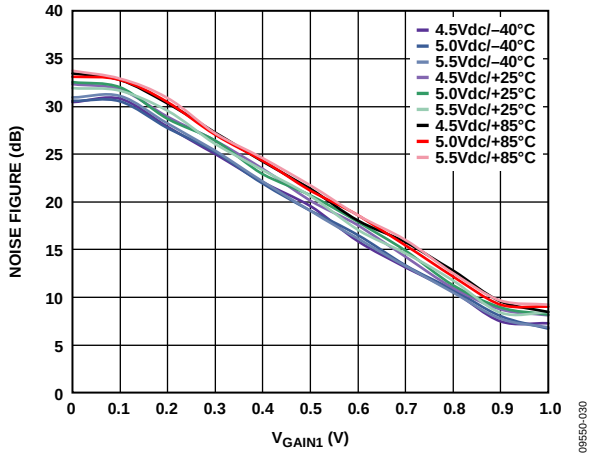


Figure 24. Noise Figure vs. V_{GAIN1} over Supply and Temperature for VGA1

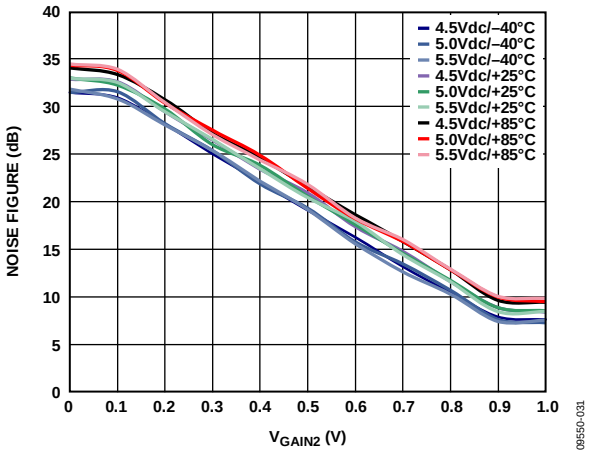


Figure 27. Noise Figure vs. V_{GAIN2} over Supply and Temperature for VGA2

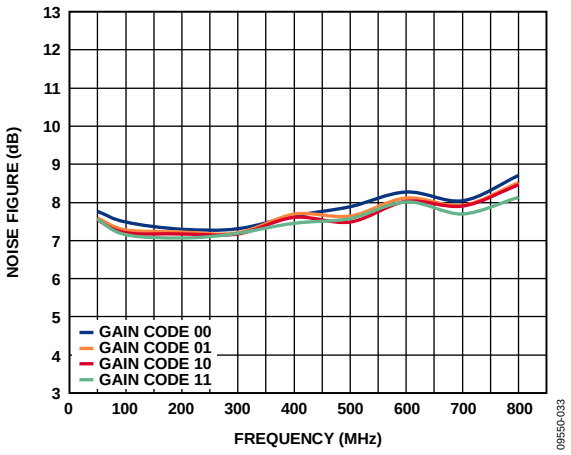


Figure 25. Noise Figure vs. Frequency over Maximum Gains for VGA1

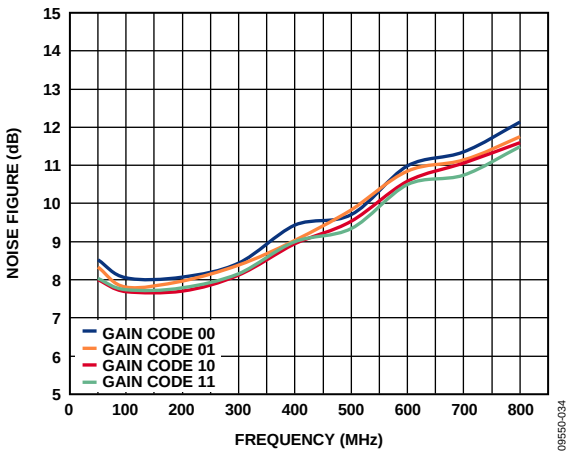


Figure 28. Noise Figure vs. Frequency over Maximum Gains for VGA2

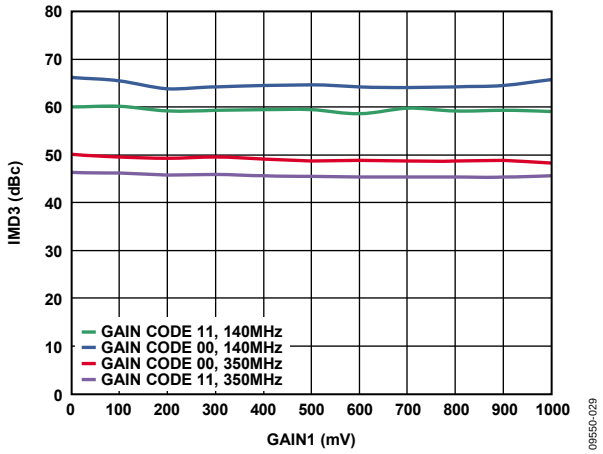


Figure 29. IMD3 vs. V_{GAIN} over Frequency and Gain Code, V_{OUT} = 1 V p-p Composite, 2 MHz Spacing for VGA1

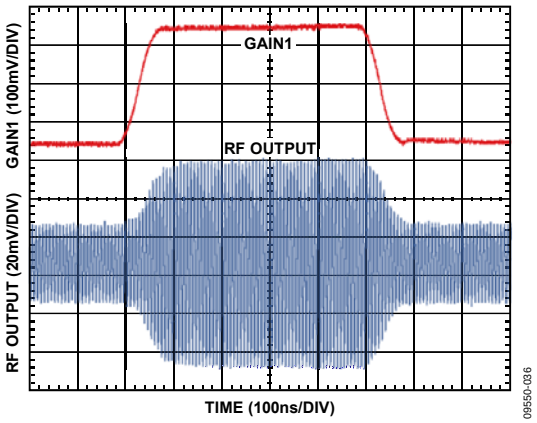


Figure 30. V_{GAIN} Step Response (VGA Mode) over Gain Step, V_{IN} = 100 mV p-p for VGA1

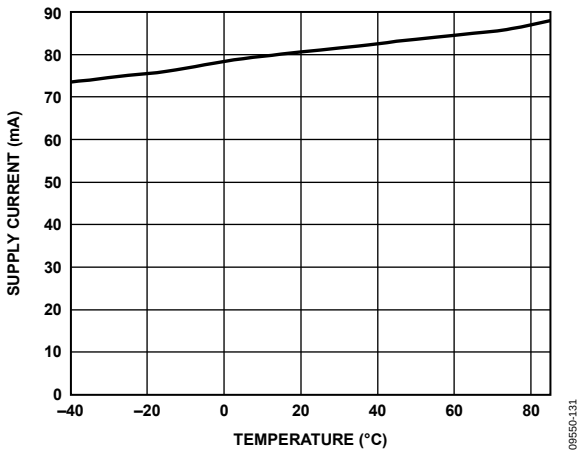


Figure 31. Supply Current (VGA1 Switch Disabled) over Temperature

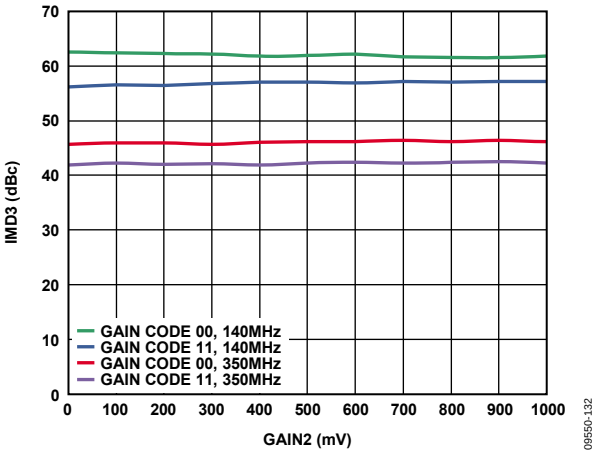


Figure 32. IMD3 vs. V_{GAIN} over Frequency and Gain Code, V_{OUT} = 1 V p-p Composite, 2 MHz Spacing for VGA2

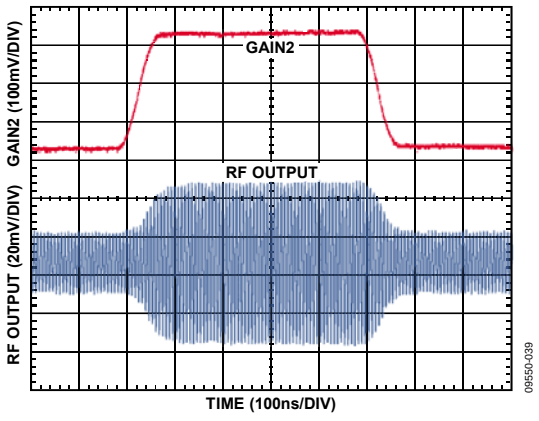


Figure 33. V_{GAIN} Step Response (VGA Mode) over Gain Step, V_{IN} = 100 mV p-p for VGA2

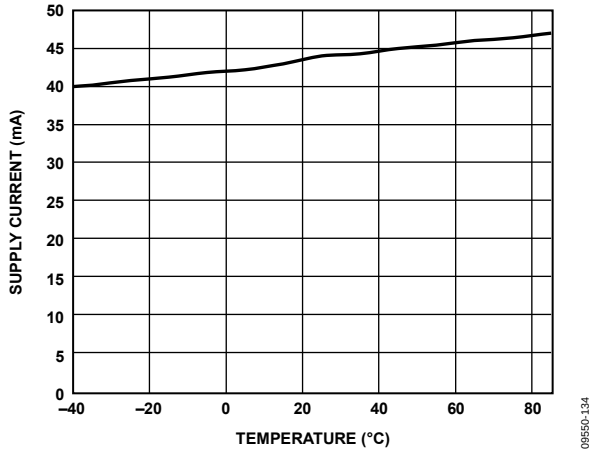


Figure 34. Supply Current (VGA2 Switch Enabled) over Temperature

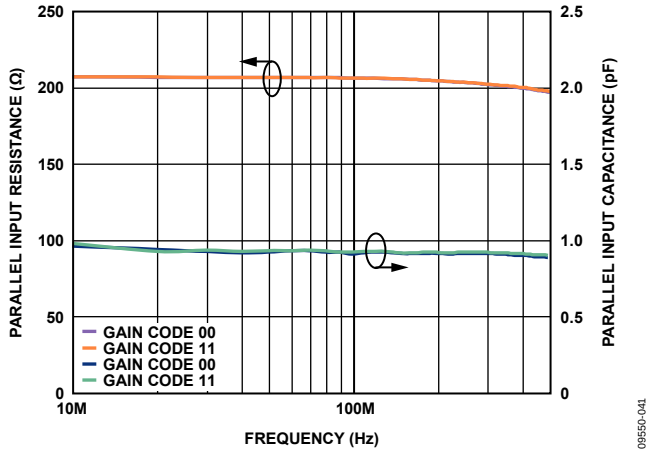


Figure 35. Input Resistance and Capacitance vs. Frequency for VGA1

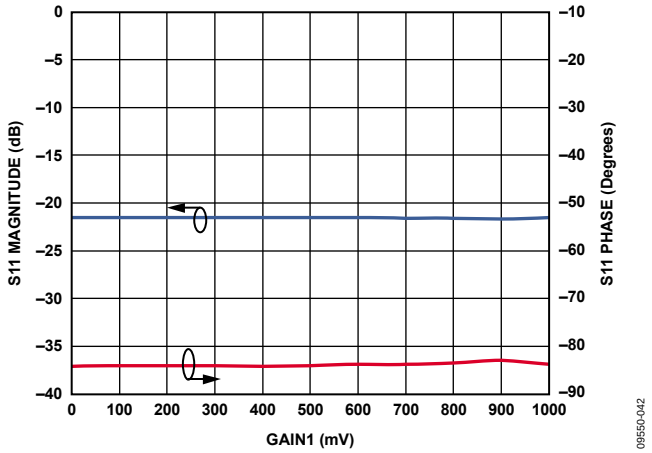


Figure 36. S11 (re: 200 Ω) Magnitude and Phase vs. V_{GAIN} for VGA1

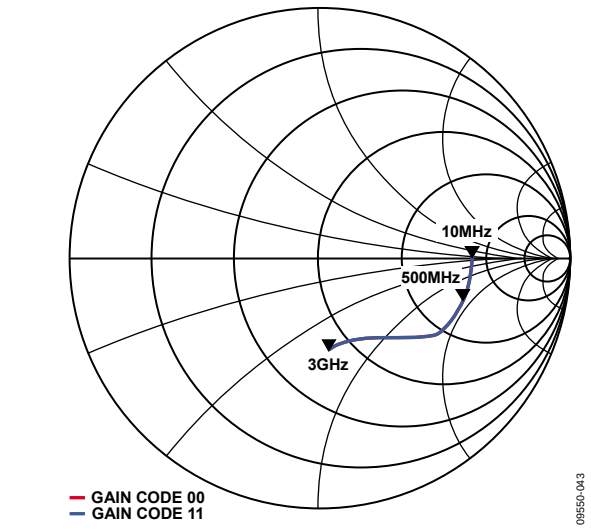


Figure 37. S11 (re: 50 Ω) vs. Frequency over V_{GAIN} for VGA1

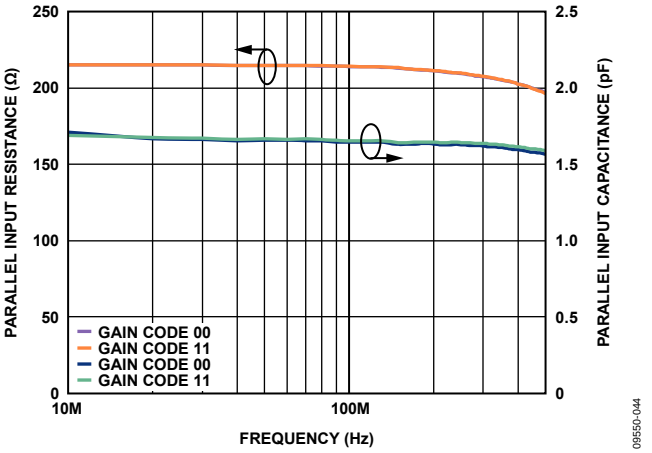


Figure 38. Input Resistance and Capacitance vs. Frequency for VGA2

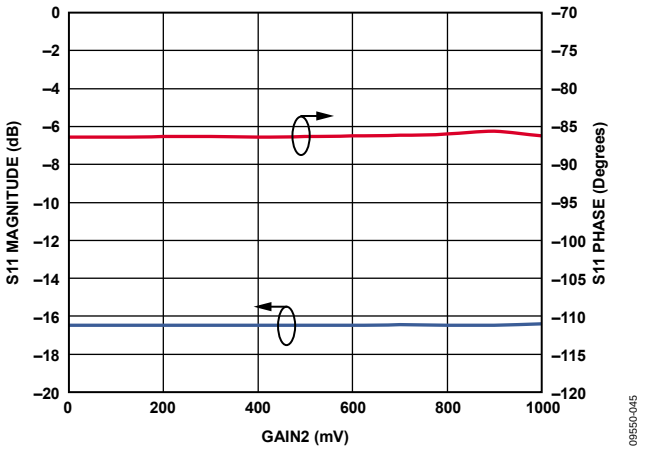


Figure 39. S11 (re: 200 Ω) Magnitude and Phase vs. V_{GAIN} for VGA2

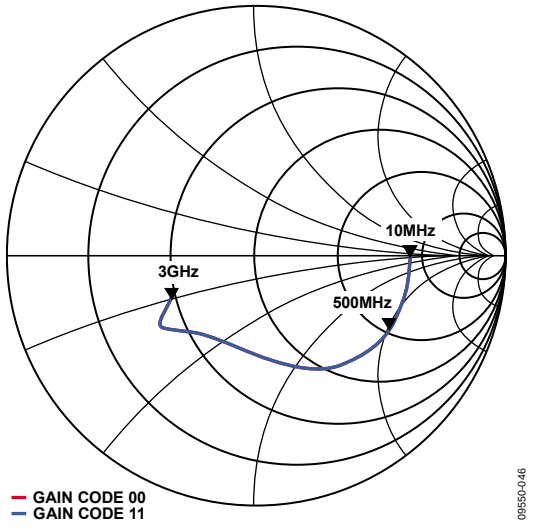


Figure 40. S11 (re: 50 Ω) vs. Frequency over V_{GAIN} for VGA2

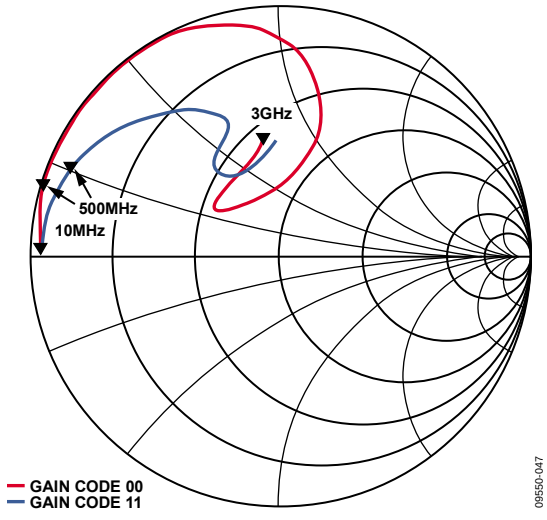


Figure 41. S22 (re: 50 Ω) vs. V_{GAIN} over Gain Code for VGA1

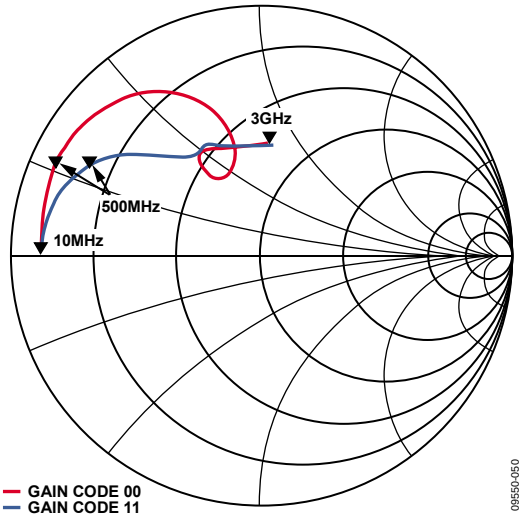


Figure 44. S22 (re: 50 Ω) vs. V_{GAIN} over Gain Code for VGA2

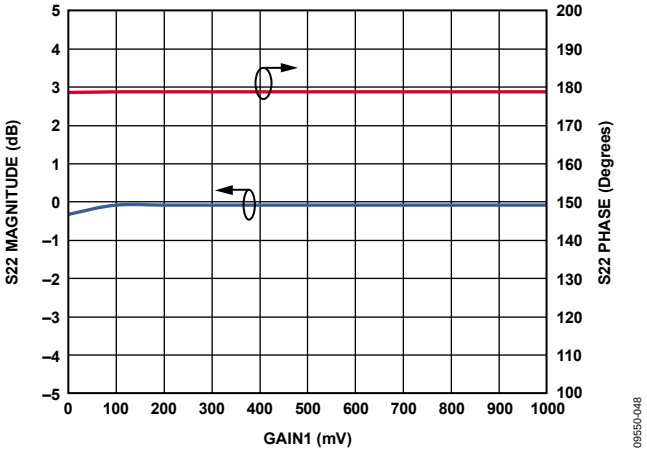


Figure 42. S22 (re: 200 Ω) Magnitude and Phase vs. V_{GAIN} for VGA1

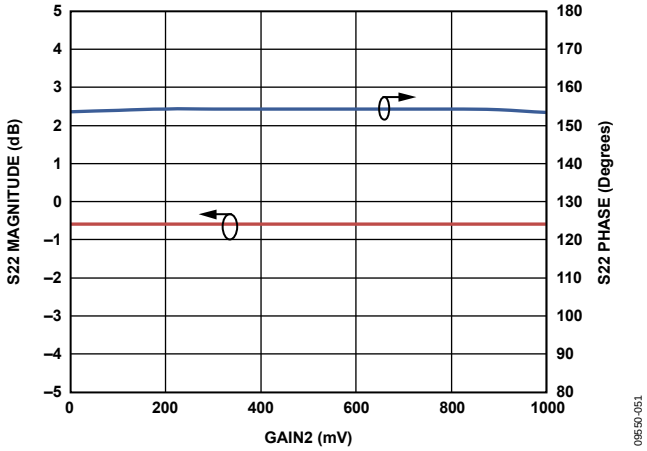


Figure 45. S22 (re: 100 Ω) Magnitude and Phase vs. V_{GAIN} for VGA2

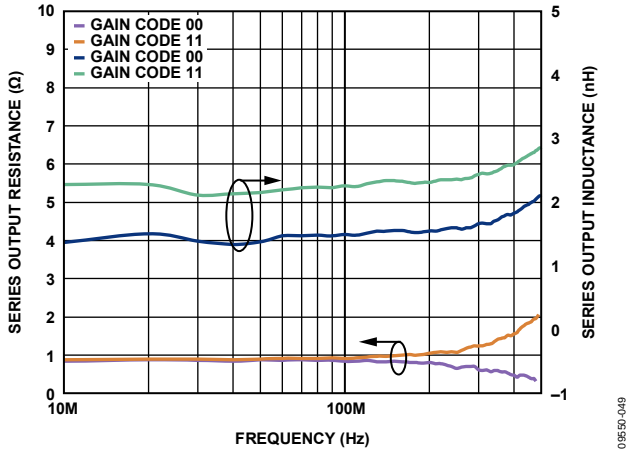


Figure 43. Series Output Resistance and Inductance vs. Frequency over V_{GAIN} for VGA1

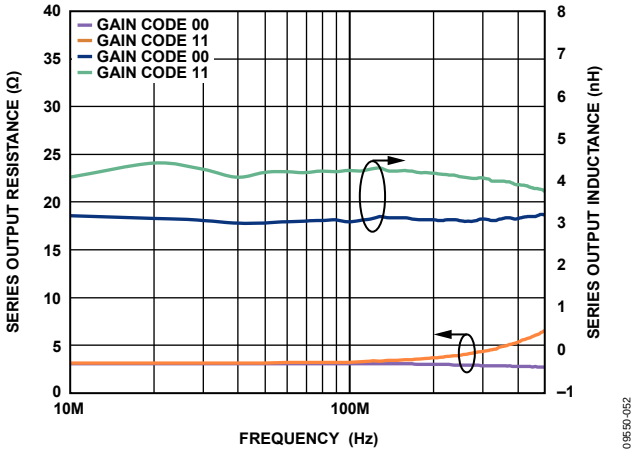


Figure 46. Series Output Resistance and Inductance vs. Frequency over V_{GAIN} for VGA2

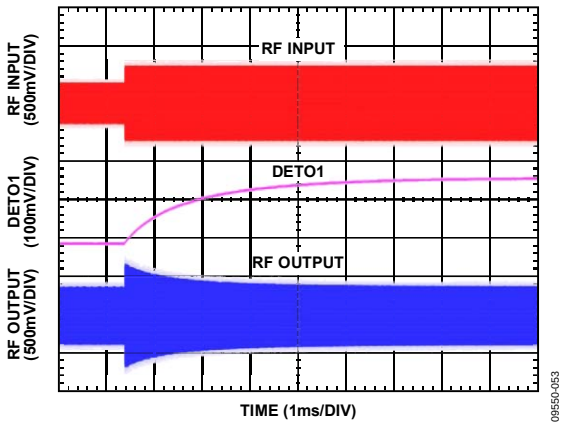


Figure 47. RSSI Step Response (AGC Mode) for VGA1

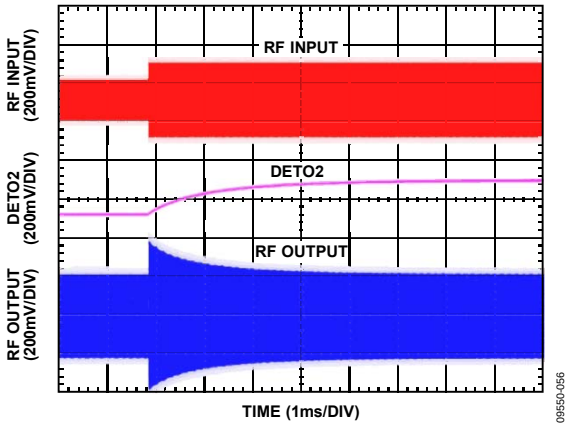


Figure 50. RSSI Step Response (AGC Mode) for VGA2

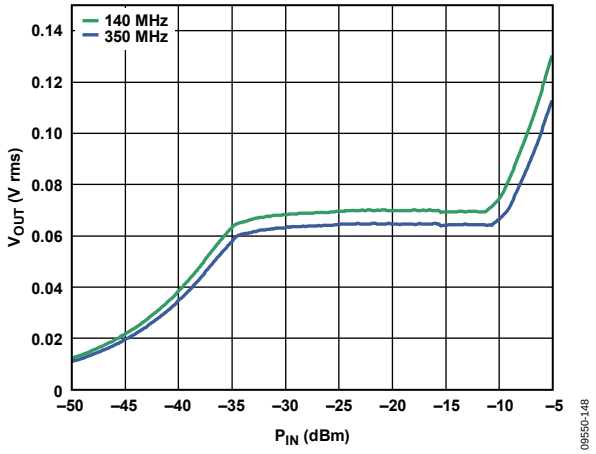


Figure 48. V_{OUT} vs. Input Power (P_{IN}) over Frequency (AGC Mode) for VGA1

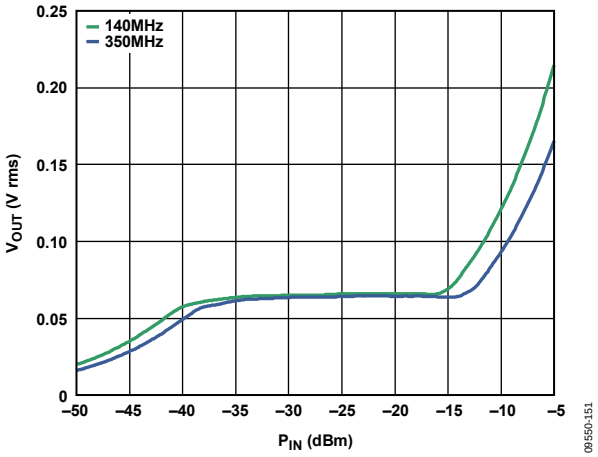


Figure 51. V_{OUT} vs. Input Power (P_{IN}) over Frequency (AGC Mode) for VGA2

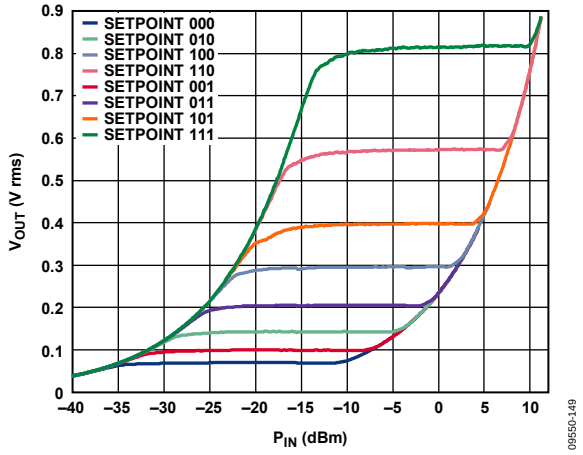


Figure 49. V_{OUT} vs. Input Power (P_{IN}) over Setpoint (AGC Mode) for VGA1

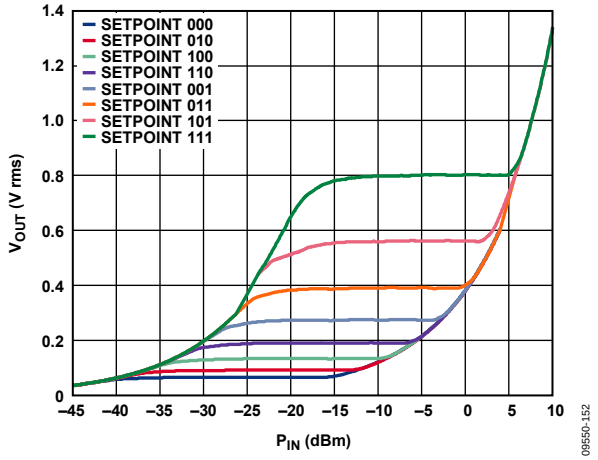


Figure 52. V_{OUT} vs. Input Power (P_{IN}) over Setpoint (AGC Mode) for VGA2

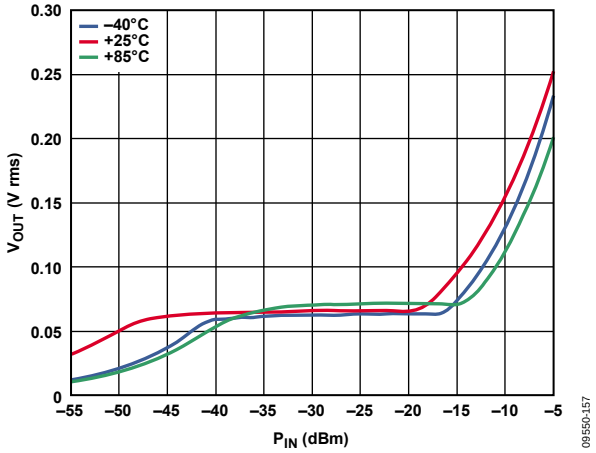


Figure 53. V_{OUT} vs. Input Power (P_{IN}) over temperature for VGA1

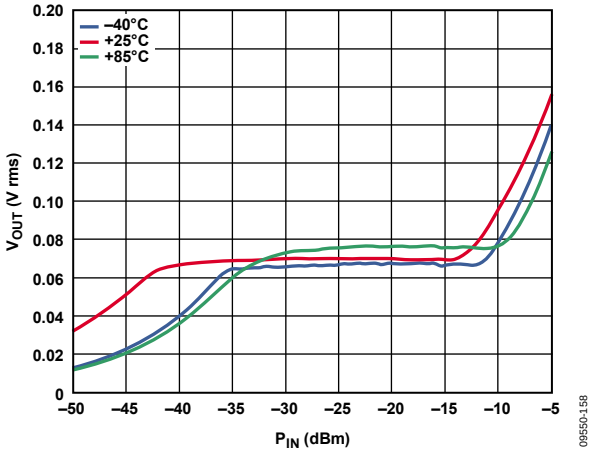


Figure 56. V_{OUT} vs. Input Power (P_{IN}) over temperature for VGA2

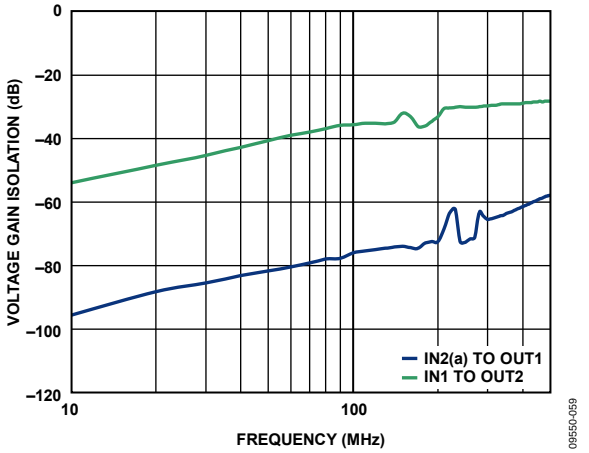


Figure 54. Amplifier Isolation vs. Frequency; VGA1 Differential Input (IN1) to VGA2 Differential Output (OUT2); VGA2 Differential Input A (IN2(a)) to VGA1 Differential Output (OUT1)

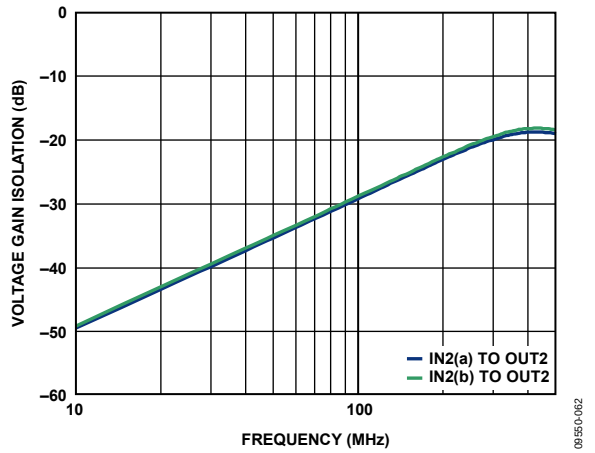


Figure 57. VGA2 Input Switch Isolation vs. Frequency; VGA2 Disabled Differential Input (IN2(a), IN2(b)) to VGA2 Differential Output (OUT2)

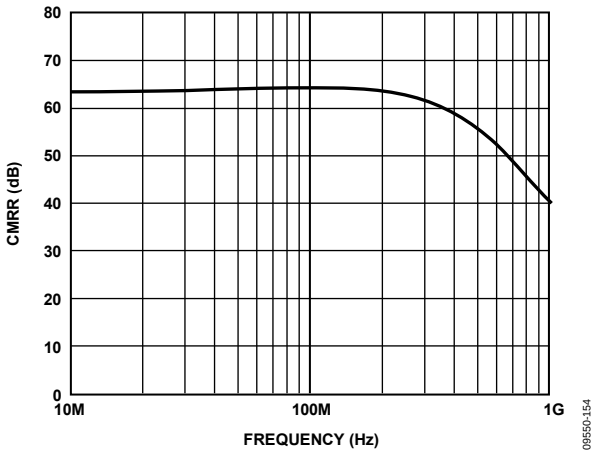


Figure 55. CMRR vs. Frequency for VGA1

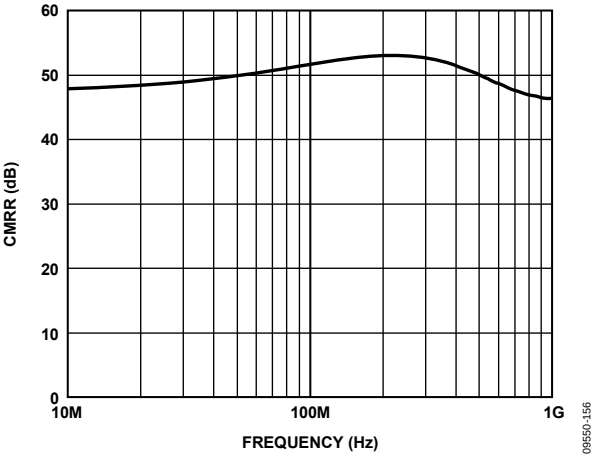


Figure 58. CMRR vs. Frequency for VGA2

THEORY OF OPERATION

CIRCUIT DESCRIPTION

The ADL5336 contains two differential VGAs, each with a programmable, internally connected, square law detector. VGA2 includes an input select switch that allows the user to choose between two sets of differential inputs.

The signal path of each VGA, shown in Figure 59 and Figure 60, consists of a variable input attenuator followed by a programmable gain amplifier (PGA).

The input attenuator is built from an 18-section resistor ladder, providing 1.34 dB of attenuation at each successive tap point. The resistor ladder acts as a linear input attenuator, in addition to providing an accurate 200 Ω input impedance. The variable transconductance (g_m) stages are used to select the attenuated signal from the appropriate tap point along the ladder and feed this signal to the fixed gain amplifier. To realize a continuous gain control function from discrete tap points, the gain interpolator creates a weighted sum of signals appearing on adjacent tap points by carefully controlling the variable g_m stages.

The weighted sum of the different tap points is fed into the programmable gain stage. The programmable gain stage achieves its different gain settings by changing the feedback network of the amplifier.

The input attenuator and g_m stages provide analog gain control of 24 dB, whereas the programmable gain amplifier sets the maximum gain of each VGA.

Table 4. VGA Gain Range

Maximum Gain Word			
VGA1	VGA2	VGA1 Range (dB)	VGA2 Range (dB)
0	0	−14.5 to +9.5	−10 to +14
0	1	−12 to +12.0	−7.1 to +16.9
1	0	−10 to +14.0	−5 to +19
1	1	−8.4 to +15.6	−3.1 to +20.9

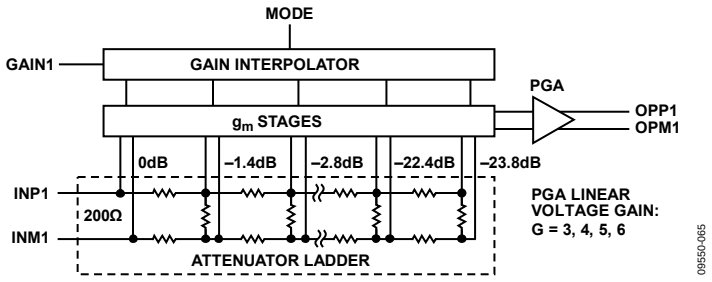


Figure 59. VGA1 Functional Block Diagram

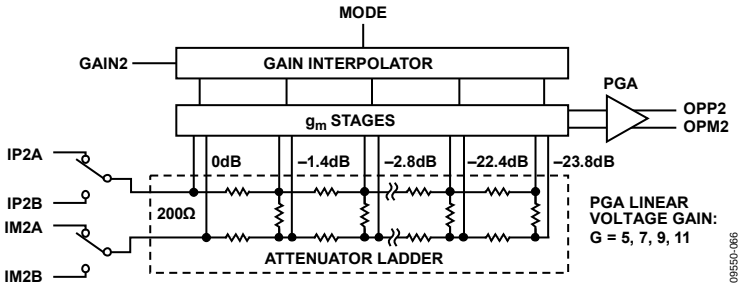


Figure 60. VGA2 Functional Block Diagram

GAIN CONTROL INTERFACE

The ADL5336 has a linear-in-dB gain control interface that can operate in either a gain-up mode or gain-down mode. In the gain-up mode, with the MODE pin pulled high, the gain increases with increasing gain voltages. In the gain-down mode, with the MODE pin pulled low, the gain decreases with increasing gain voltages. In both modes of operation, the gain control slope is maintained at +37.5 dB/V or −38 dB/V (depending on mode selection) over temperature, supply, and process as V_{GAIN} varies from 100 mV to 900 mV. To form an AGC loop with the on-board detector around the VGA, the MODE pin has to be pulled low.

Each VGA has 24 dB of gain range that can be shifted as the maximum gain is programmed.

The gain functions for MODE pulled high and low are given respectively by

$$Gain_{HIGH}\ (\text{dB}) = 37.5 \times V_{GAIN} - 14$$

$$Gain_{LOW}\ (\text{dB}) = -38 \times V_{GAIN} + 24.8$$

where V_{GAIN} is expressed in volts.

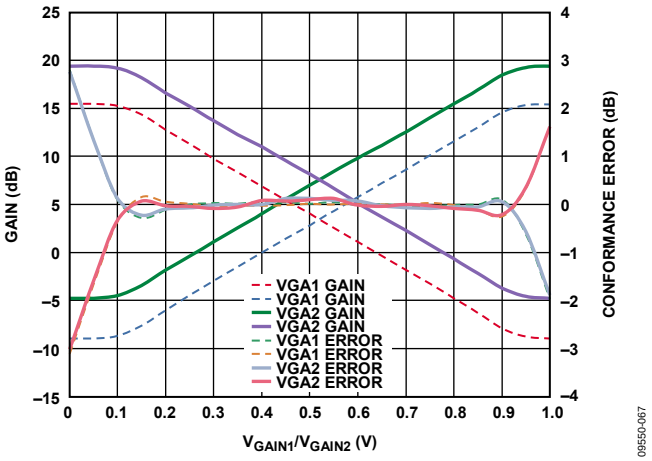


Figure 61. Gain and Conformance Error vs. V_{GAIN1}/V_{GAIN2} for Gain Code 11, and MODE = 0 V and MODE = 5 V for Both VGAs

INPUT AND OUTPUT IMPEDANCES

The ADL5336 offers differential broadband, 200 Ω input impedance. The output of each VGA is a low impedance buffer with negative feedback within the programmable gain amplifier. The negative feedback reduces the output impedance at low frequencies, but the output impedance increases with increasing frequency above 300 MHz.

AGC OPERATION

The internally connected square law detectors are connected to the outputs of the VGAs through a programmable attenuator. The detector compares the output of the attenuator to an internal reference of 63 mV rms. The AGC loop is closed by connecting the DTO1/DTO2 pins to the GAIN1/GAIN2 pins, and having the MODE pin pulled low, configuring the VGAs for a negative gain slope.

If the attenuator is programmed to pass the full VGA output, the AGC forces the output of the VGA to 63 mV rms, as long as the gain required is within the gain range of the VGA. If the attenuator is programmed to attenuate the VGA output by 21 dB (Setpoint Word 111) and the AGC loop is closed, the AGC function forces the VGA output to 707 mV rms. If the gain required to achieve the programmed target output level is out of the VGA range, the GAINx pin rails to either VPOS/2 or GND.

If the amplifier is operated in VGA mode or the detector is not otherwise being used, the setpoint should be programmed to maximum attenuation so that the VGA output does not overdrive the input to the detector, adversely affecting both the detector and VGA output.

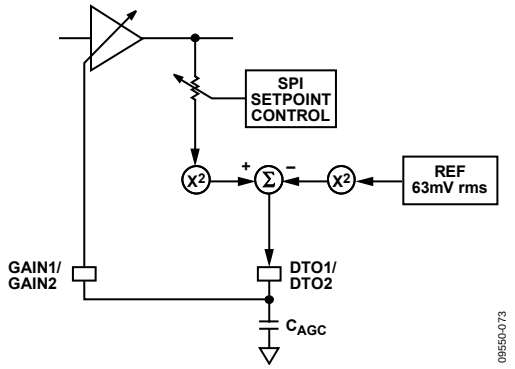


Figure 62. RMS Detection Diagram (Shows the Signal Path from VGA1/VGA2 Output to Squarer Cell)

REGISTER MAP AND CODES

Table 5. Register Map

MSB										LSB
B10	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
VGA2 Maximum Gain		VGA1 Maximum Gain		VGA2 Switch	VGA2 Setpoint			VGA1 Setpoint		

Table 6. RMS Output Setpoint Map

Setpoint Word			RMS Output (mV rms/dBV)
0	0	0	+62.5/−24
0	0	1	+88/−21
0	1	0	+125/−18
0	1	1	+176/−15
1	0	0	+250/−12
1	0	1	+353/−9
1	1	0	+500/−6
1	1	1	+707/−3

Table 7. VGA2 Input Switch Logic

VGA2 Switch	Selected Input
0	IP2A, IM2A
1	IP2B, IM2B

Table 8. Maximum Gain Map

Maximum Gain Word		VGA1 Maximum Gain (dB)	VGA2 Maximum Gain (dB)
0	0	9.5	14
0	1	12.0	16.9
1	0	14.0	19
1	1	15.6	20.9

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for a typical ADL5336 application are shown in Figure 63.

SUPPLY DECOUPLING

A nominal supply voltage of 5.0 V should be applied to the supply pins. The supply voltage should be between the limits of 4.5 V and 5.5 V. All of the supply pins must be decoupled to ground with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF. Place these decoupling capacitors as close as possible to the ADL5336 device. The ADL5336 has an analog supply and a digital supply. Take care to separate the two supplies with a large surface-mount inductor of 33 µH, and each supply must then be decoupled separately to their respective grounds through a 10 µF capacitor. The ADL5336 also has two separate grounds: an analog ground and a digital ground. Again, a large surface-mount inductor of 33 µH should be used to separate the grounds.

INPUT SIGNAL PATH

The ADL5336 has three input signal paths, two of which inputs go to VGA2 via an internal switch, and the other input goes to VGA1. Each of the three pairs of input pins (INP1/INM1, IP2A/IM2A, and IP2B/IM2B) has a differential input impedance of 200 Ω. To obtain maximum power transfer, the driving source impedance also needs to be 200 Ω. On the evaluation board, this is achieved via a 4:1 impedance ratio balun. The evaluation board schematic is shown in Figure 70. For more information on the input signal paths, refer to the Input Signal Path section. The input common-mode voltage sits at roughly VPOS/2 for both VGAs, except on VGA2; the nonselected input of VGA2 has an input common-mode voltage that sits at roughly ground.

OUTPUT SIGNAL PATH

There are two output signal paths on the ADL5336: one signal path per VGA. The output of VGA1 can be ac-coupled into either of the inputs of VGA2, which cascades the two VGAs, or ac-coupled into a 200 Ω termination impedance. VGA1 is designed to drive a 200 Ω differential load, whereas VGA2 is designed to drive a 100 Ω differential load. On the evaluation board, a 100 Ω differential impedance is presented to the output of VGA2. This is achieve via a 1:1 balun and a resistive matching network. For more information on the evaluation board, see the evaluation board schematic in Figure 70. The output common-mode voltage on both VGAs sits at roughly VPOS/2.

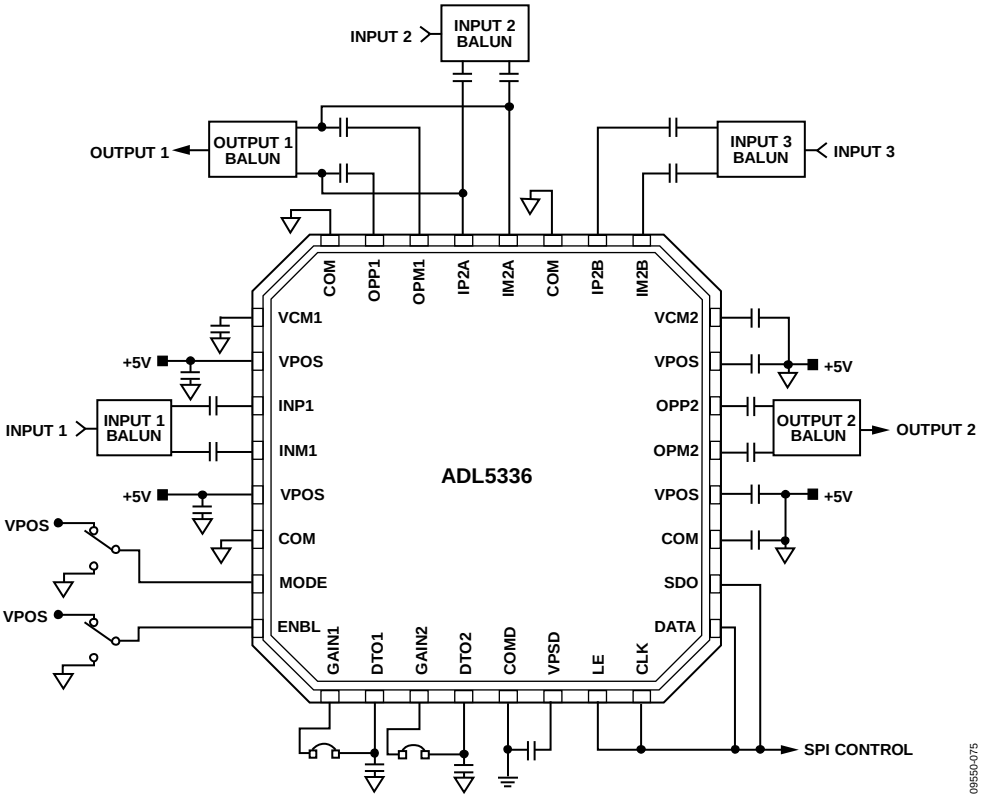


Figure 63. Basic Connections Schematic

DETECTOR OUTPUT AND GAIN PIN

The ADL5336 has a pair of detector squaring cells. Each squaring cell has a VGA output applied to its input. This is shown Figure 1 and Figure 62. These on-board detector squaring cells are used to achieve an AGC function with the VGAs. Each of the squared output signals is compared to a reference signal and the difference is then output in a current-mode signal. The DTO1 pin is the detector squaring cell output that taps off of the output VGA1, and the DTO2 pin is the detector squaring cell output that taps off of the output of VGA2. By shorting the DTO1 and GAIN1 pins together and putting a capacitor to ground on the DTO1/GAIN1 node, the AGC function can be achieved using VGA1. The same connections can be done to DTO2 and GAIN2 to achieve the AGC function using VGA2. The MODE pin must be pulled low for the AGC function. For more information on the detector squaring cells and the AGC function, refer to the AGC Operation section. For information concerning the capacitor value used, refer to the Theory of Operation section.

COMMON-MODE BYPASSING

Decouple the two common-mode pins, VCM1 (Pin 1) and VCM2 (Pin 24), of the ADL5336 using low inductance, surface-mount ceramic capacitors. The evaluation board has 0.1 µF capacitor values for each of the common-mode pins (see Figure 70).

SERIAL PORT CONNECTIONS

The SPI port of the ADL5336 writes data into the device and reads data out of it. The SPI port controls maximum VGA gain levels, output setpoint levels, and VGA2 input selection. It is recommended to put low-pass RC filtering on the SPI lines to filter out any high frequency glitches if reading and writing to the SPI port becomes problematic. Capacitors C26 through C29, shown in Figure 70, can be populated, along with replacing the standard 0 Ω jumper resistors (R9 to R12) to make an appropriate low-pass RC filter network on each SPI line.

MODE AND ENABLE CONNECTIONS

The ADL5336 can have both a positive and negative gain slope. This function is controlled by the MODE pin. When the MODE is pulled high, it puts each VGA into traditional VGA mode, where the gain slope is positive. When the MODE pin is pulled to ground, both VGAs have a negative gain slope, which is needed to obtain an AGC function with either VGA. The MODE threshold voltage levels are $V_{MODE} > 3$ V for the positive gain slope and $V_{MODE} < 2$ V for the negative gain slope.

Pulling the ENBL pin high enables the part and allows for normal operation. If the ENBL pin is pulled low, then the ADL5336 powers down and only draws approximately 4 mA of supply current.

ERROR VECTOR MAGNITUDE (EVM)

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver by measuring the fidelity of the digital signal transmitted or received. Various imperfections in the link, such as magnitude and phase imbalance, noise, and distortion, cause the constellation points to deviate from their ideal locations.

In general, as signal power increases, the distortion components increase. A typical receiver exhibits the three following distinct EVM limitations vs. the received input signal power:

- At large enough signal levels, where the distortion components due to the harmonic nonlinearities in the device are falling in-band, EVM degrades as signal levels increase.
- At medium signal levels, where the signal chain behaves in a linear manner and the signal is well above any notable noise contributions, EVM has a tendency to reach an optimal level determined dominantly by either the quadrature accuracy and I/Q gain match of the signal chain or the precision of the test equipment.
- As signal levels decrease, such that noise is a major contributor, EVM performance vs. the signal level exhibits a decibel-for-decibel degradation with decreasing signal level. At these lower signal levels, where noise is the dominant limitation, decibel EVM is directly proportional to the SNR.

EFFECT OF C_{AGC} ON EVM

The choice of C_{AGC} is a compromise of averaging time constant, response time, and carrier leakage. If C_{AGC} is selected to be too small to speed up the response time, the AGC loop could start tracking and leveling any amplitude envelope and corrupt the constellation. The AGC loop bandwidth (BW) is given by the equation

$$BW_{LOOP} = 1/(2\pi \times R_{AGC} \times C_{AGC})$$

where R_{AGC} is the on-chip equivalent resistance of the loop.

By increasing C_{AGC} (which decreases the loop BW), EVM can be improved because the signal is outside of the AGC loop BW, and therefore, the AGC no longer levels the amplitude envelope of the signal. Figure 64 illustrates this behavior with three different AGC capacitor values while the ADL5336 VGAs are cascaded. There is a drastic degradation of EVM when the smaller capacitor values are used. This example uses a 16 QAM modulated signal at 4.5 Msym/sec using a pulse shaping filter and an alpha of 0.35. The frequency used was 140 MHz and output setpoints for both VGAs were 250 mV rms. Both VGAs were set to maximum gain codes of 11.

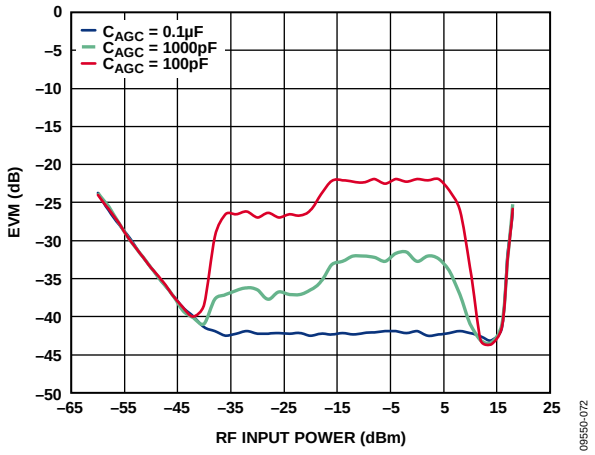


Figure 64. EVM vs. RF Input Power over Several C_{AGC} Values

AGC INSENSITIVITY TO MODULATION TYPE

Given that C_{AGC} is chosen correctly for the symbol rate of the modulated signal and carrier frequency, EVM should not degrade much with different modulation types. The four different modulation types, and how EVM changes with each, are shown in Figure 65. There is an approximately 4 dB spread across the curves. All modulated signals were set to 4.5 Msym/sec using a pulse shaping filter and an alpha of 0.35. The frequency used was 140 MHz. C_{AGC} = 0.1 µF and output setpoints for both VGAs were 250 mV rms. Both VGAs were set to maximum gain codes of 11.

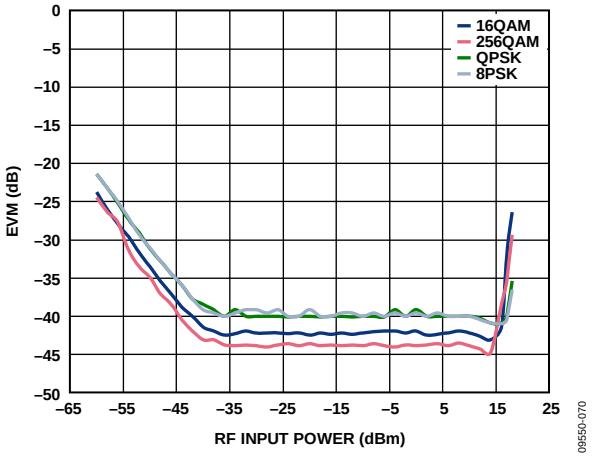


Figure 65. EVM vs. RF Input Power Over Several Modulation Types

EFFECT OF SETPOINT ON EVM

While in AGC mode, the EVM can degrade depending on the output setpoint each VGA is set to. There is a strong relationship between the output setpoint of VGA2 and EVM performance while the output setpoint of VGA1 is held constant. Conversely, the EVM does not change much while the output setpoint of the VGA2 is held constant and the output setpoint of VGA1 is changed. This behavior can be seen in Figure 66 where several different setpoints of both VGAs were tested. This example uses a 16 QAM modulated signal at 4.5 Msym/sec using a pulse shaping filter and an alpha of 0.35.The frequency used was 140 MHz and C_{AGC} = 0.1 µF. Both VGAs were set to maximum gain codes of 11.

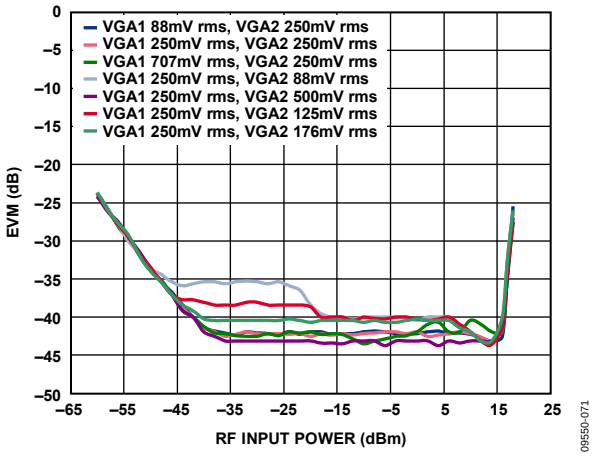


Figure 66. EVM vs. RF Input Power over Several Setpoints

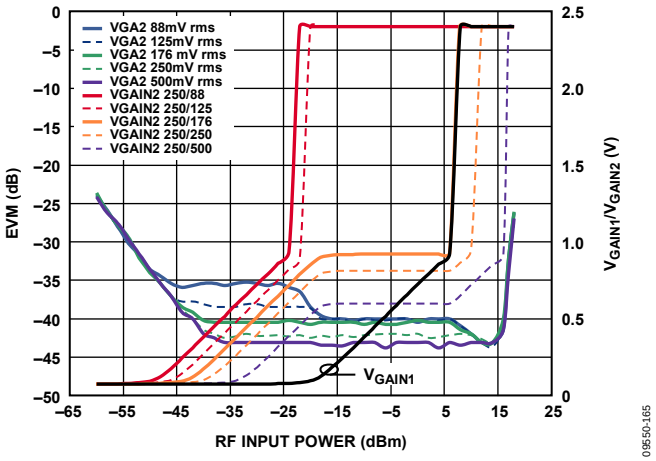


Figure 67. EVM vs. RF Input Power While VGA1 Setpoint Held Constant to 250 mV rms and VGA2 Setpoint Swept; VGA1/VGA2 Gain Code = 11

CASCADED VGA/AGC PERFORMANCE

The ADL5336 is designed for easy cascading of the two VGAs. Cascading VGAs decreases the overall noise figure by keeping as much gain as possible before the final gain stage/noise source. A single X-AMP has constant output referred noise. For an 8 dB NF amplifier, with 36 dB maximum gain, in a 200 Ω matched system, output referred noise $V_{N, RTO}$ = 144 nV/√Hz. RTO, the noise contribution from the source, is the constant source noise multiplied by the gain (as the gain is reduced, the noise contribution from the source decreases). Measuring noise figure as 20 × log10 (total noise/noise from source), the dB-for-dB degradation in NF typical of this architecture can be seen.

When the gain is partitioned into two VGAs, consider 18 dB each. If each has an 8 dB NF, then each has an RTO noise of 18 nV/√Hz, including the source noise, and 16.5 nV/√Hz, excluding the source noise. At maximum gain, the total RTO noise is 145 nV/√Hz. As overall gain is decreased, the gain of VGA2 is decreased first. When the gain of VGA2 is decreased by 6 dB, the noise contributions from the source and VGA1 both decrease by 6 dB for an overall RTO noise of the system that falls to 74 nV/√Hz.

When VGA1 and VGA2 are cascaded and operating in AGC mode, setpoint programming affects dynamic range. The noise measured at the output of VGA1 is relatively constant across gain, which is a feature common to X-AMP VGAs. However, measured at the output of VGA2, the noise contribution from VGA2 is constant, but the noise contribution from VGA1 depends on the gain of VGA2. For a given overall gain (VGA1 and VGA2), the gain partitioning between VGA1 and VGA2 controls total RTO noise and distortion.

To illustrate, consider the case where both VGAs are programmed to a maximum gain of 14 dB and the setpoint of VGA2 is 101, or 353 mV rms. Gain and signal levels can also be looked at when the setpoint of VGA1 is programmed to 011, 101, and 111, 176 mV rms, 353 mV rms, and 707 mV rms (see Table 9).

Table 9. Total Cascaded Output Noise

V_i (mV rms)	A_{V1} (dB)	V_{O1} (mV rms)	A_{V2} (dB)	V_O (mV rms)	n_1	n_2	n_{TOTAL}
176	0	176	+6	353	20	10	22.4
176	6	353	0	353	10	10	14.1
176	12	707	−6	353	5	10	11.2

As the setpoint of VGA1 increases, the total output noise decreases.

Linearity limits how high the setpoint of VGA1 for a given system can be programmed. For two equal sinusoidal tones, 353 mV rms corresponds to 1.4 V p-p, whereas 707 mV rms corresponds to 2.8 V p-p. For a 1.4 V p-p composite output, IMD3 is approximately −65 dBc; however, for a 2.8 V p-p composite output, IMD3 is theoretically 12 dB worse at −53 dBc.

For each VGA, total RTO noise increases at higher maximum-gain settings; therefore, the overall combination of maximum gain should be minimized while still satisfying all system requirements with adequate margin.

In linear terms, the noise figure of the cascaded amplifiers can be given by

$$NF_{CAS} = NF_{VGA1} + (NF_{VGA2} - 1)/G_{VGA1}$$

Because both VGAs are X-AMPs, the noise figure of each VGA degrades dB-for-dB as the gain of each VGA decreases. This is due to the attenuation ladder on the input that attenuates the signal before the signal is gained up. If only the gain of the second VGA is changing, the cascaded noise figure does not change appreciably because the noise figure of the second VGA is being divided by the constant gain of the first VGA. When the gain of VGA2 drops to the minimum and the input signal level is still decreasing, VGA1 takes over and its gain starts to change. The cascaded noise figure increases dB-for-dB while the gain of VGA1 decreases.

While cascading the VGAs, keeping intermodulation distortion components low is at direct odds with keeping noise figure and output noise density low. It can be shown that the third-order intercept of a cascaded system in linear terms is

$$P3 = 1/(1/(G_{VGA2}P_{3_VGA1}) + 1/P_{3_VGA2})$$

where P_{3_VGA1} and P_{3_VGA2} are the third-order intercept points of each VGA in watts. Thus, when the overall IP3 is the largest (distortion is the smallest), the gain of VGA2 is at its maximum. Vice-versa, when the gain of VGA2 is at its minimum, the overall IP3 is the smallest, and distortion is at its maximum.

Table 10 provides conditions for optimization for the output noise density, noise figure, and distortion parameters.

Table 10. Optimized Conditions

	VGA1 Gain	VGA2 Gain
Output Noise	Minimum	Minimum
Noise Figure	Maximum	Maximum[1]
IMD/IP3	Maximum[2]	Maximum

1 Having the gain of VGA2 at maximum does not change the overall noise figure much due to the noise figure contribution of VGA2 being divided by the gain of VGA1.
2 IMD levels do not change much over the X-Amp gain range, but best IMD levels are achieved at high gains.

When starting from a very small input power, such that neither VGA has reached their respective setpoints, and the analog gain of both VGAs is forced to its maximum, the cascaded OIP3 is at its maximum, while the cascaded noise figure is at its minimum. As the input power is increased, each VGA keeps its gain at maximum until its respective setpoint is reached, at which point the gain of the VGA (whose setpoint has been reached) decreases to accomodate the increased input power and changes the cascaded OIP3 and noise figure.

Figure 68 shows how the OIP3 changes while input power is varied in AGC mode, which consequently changes the analog gains of the VGAs. The setpoint of VGA2 is fixed to 100 (or 250 mV rms), and the setpoint of VGA1 is changed from 001 (88 mV rms) to 100 (250 mV rms), and finally, to 111 (707 mV rms).

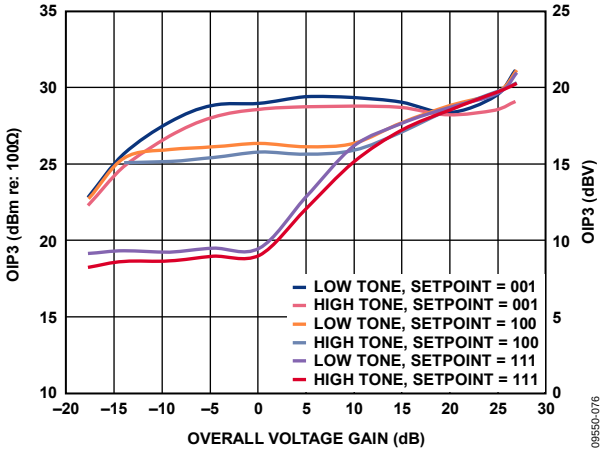


Figure 68. OIP3 vs. Overall Voltage Gain over Several Setpoints; VGA1 Gain Code = 11 and VGA2 Gain Code = 00

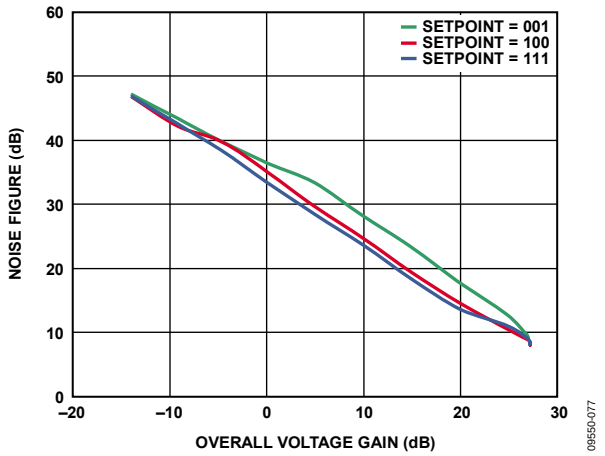


Figure 69. Noise Figure vs. Overall Voltage Gain over Several Setpoints; VGA1 Gain Code = 11 and VGA2 Gain Code = 00

Figure 69 shows how the NF changes while the input power is varied in AGC, which again, consequently changes the analog gains of the VGAs. The setpoint of VGA2 is still fixed to 100 (250 mV rms), and the changes made to the setpoint of VGA1 is the same as before.

EVALUATION BOARD LAYOUT

An evaluation board is available for testing the ADL5336. The evaluation board schematic is shown in Figure 70. Table 11 provides the component values and suggestions for modifying the component values for the various modes of operation.

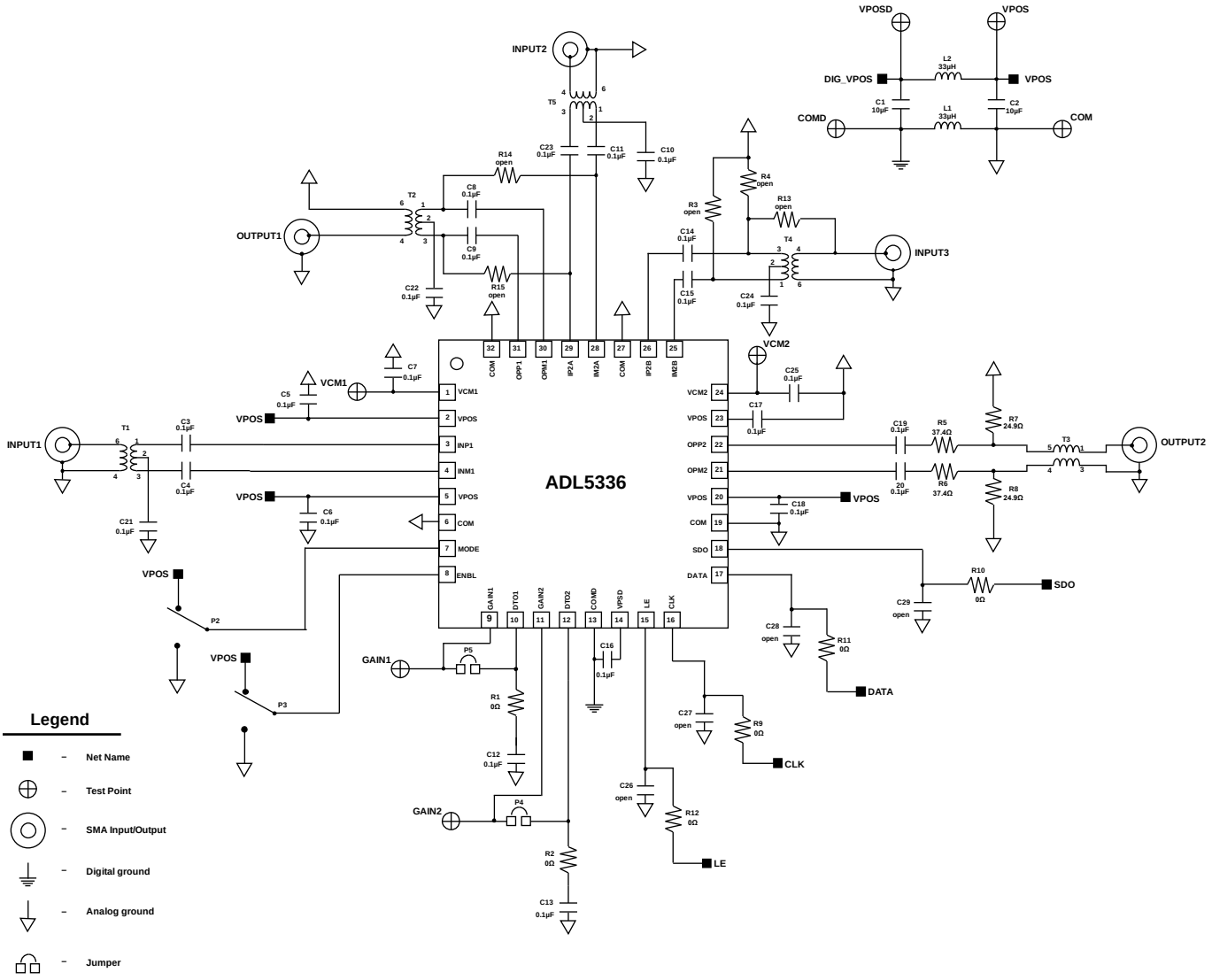


Figure 70. Evaluation Board Schematic

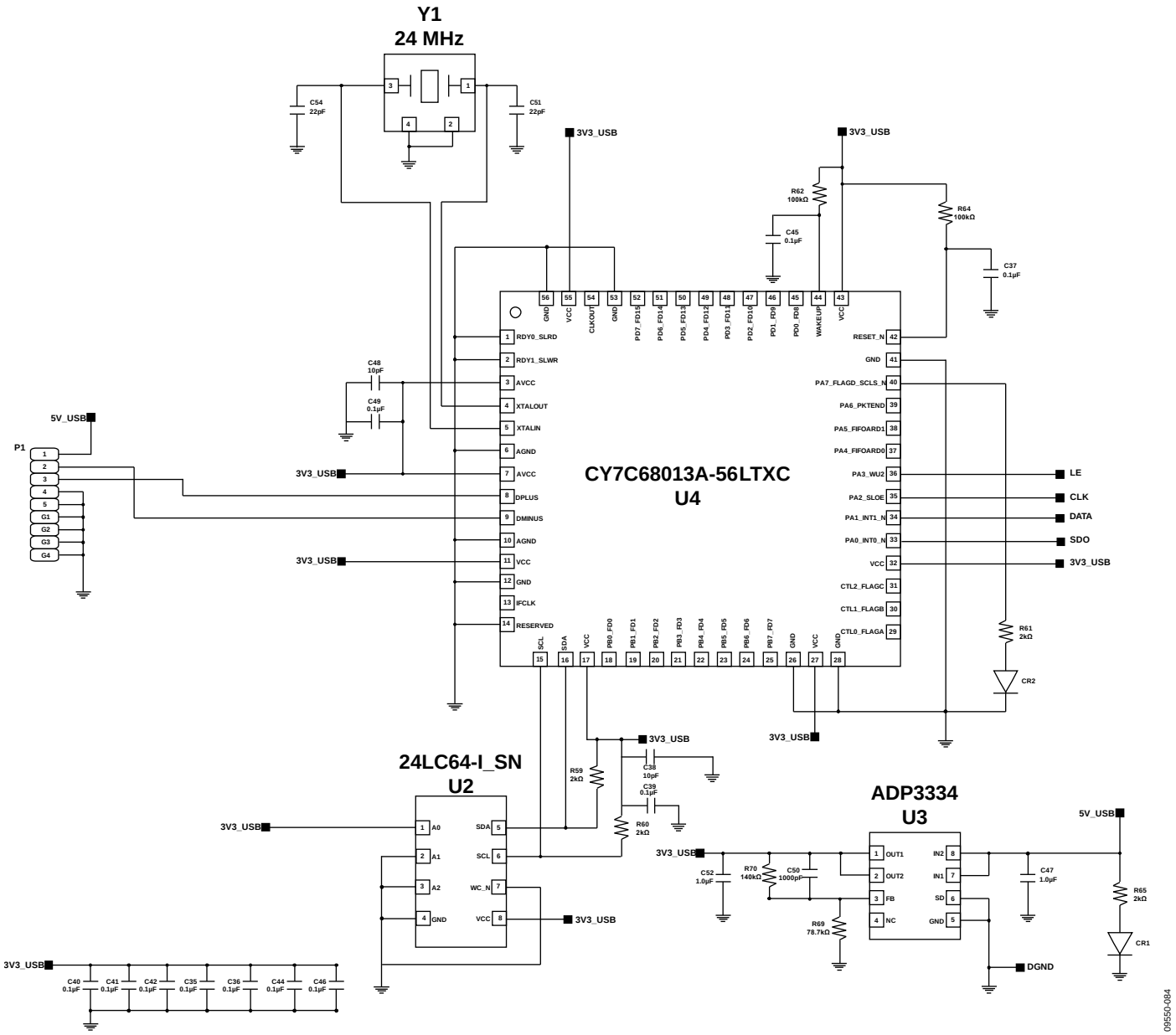


Figure 71. Evaluation Board Schematic USB

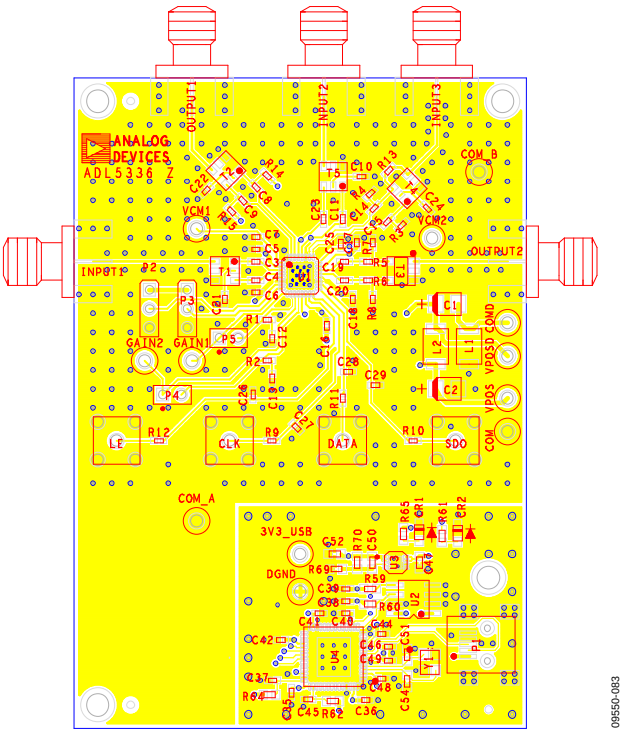


Figure 72. Silkscreen Top

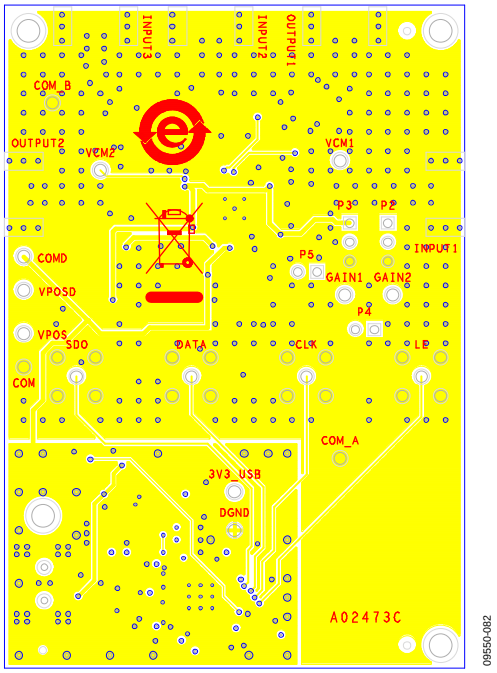


Figure 73. Silkscreen Bottom

BILL OF MATERIALS (BOM)

Table 11. Evaluation Board Configuration Options

Components	Function	Default Conditions
C1, C2, C5, C6, C7, C16, C17, C18, C25, L1, L2	Power supply and ground decoupling. Nominal supply decoupling consists of 0.1 µF capacitor to ground.	C1, C2 = 10 µF (0805), C5, C6, C7, C16, C17 = 0.1 µF (0402), C18, C25 = 0.1 µF (0402), L1, L2 = 33 µH (0805)
C3, C4, C21, T1	VGA1 input interface. The balun T1 has a 4:1 impedance ratio that transforms a single-ended signal in a 50 Ω system into a differential signal in a 200 Ω system. C3 and C4 provide ac coupling into VGA1, and C21 provides an ac ground for the balun.	C3, C4, C21 = 0.1 µF (0402), T1 = Mini-Circuits TC4-1W
C10, C11, C14, C15, C23, C24, R3, R4, R13, T4, T5	VGA2 input interface. The T4 and T5 baluns have 4:1 impedance ratios that transform single-ended signals in a 50 Ω system into differential signals in a 200 Ω system. The user has a choice of either Input A or Input B, which is set by Bit B6 in the internal register (see the register map in Table 5). C11, C14, C15, and C23 provide ac coupling into VGA2, and C10 and C24 provide an ac ground for the baluns. R3, R4, and R13 are left open by default. AC ground can be achieve by placing 0 Ω jumpers at R3 and R4. A 0 Ω jumper can be installed at R13 to drive Input B of VGA2 single ended. Note that R4 must be open and R3 must have a 0 Ω jumper installed.	C10, C11, C14 = 0.1 µF (0402), C15, C23, C24 = 0.1 µF (0402), R3, R4, R13 = open (0402), T4, T5 = Mini-Circuits TC4-1W
C8, C9, C22, R14, R15, T2	VGA1 output interface. The T2 balun has a 4:1 impedance ratio that transforms a differential signal in a 200 Ω system into a single-ended signal in a 50 Ω system. C8 and C9 provide ac coupling out of VGA1, and C22 provides an ac ground for the balun. R14 and R15 can be made 0 Ω and dc-couple the output of VGA1 into the input of VGA2 in cascading applications.	C8, C9, C22 = 0.1 µF (0402), R14, R15 = open (0402), T2 = Mini-Circuits TC4-1W
C19, C20, R5, R6, R7, R8, T3	VGA2 output interface. The transmission line transformer, T3, has a 1:1 impedance ratio that transforms a differential signal to a single-ended signal. The 50 Ω impedance is the same on both the primary and secondary side balun. C19 and C20 provide ac coupling out of VGA2. R5, R6, R7, and R8 raise the impedance that the output of VGA2 sees to 100 Ω differential.	C19, C20 = 0.1 µF (0402), R5, R6 = 37.4 Ω (0402), R7, R8 = 24.9 Ω (0402), T3 = M/A-COM ETC1-1-13
R1, C12	Detector 1 interface. R1 serves as a 0 Ω jumper to connect the integrating capacitor, C12, that is needed when VGA1 is being used in AGC mode.	R1 = 0 Ω (0402), C12 = 0.1 µF (0402)
R2, C13	Detector 2 interface. R2 serves as a 0 Ω jumper to connect the integrating capacitor, C13, that is needed when VGA2 is being used in AGC mode.	R2 = 0 Ω (0402), C13 = 0.1 µF (0402)
P3	Enable interface. The ADL5336 is powered up by applying a logic high voltage to the ENBL pin. Jumper P3 is connected to VPOS.	P3 = installed for enable
P2	MODE interface. The MODE pin must be pulled to a logic high to be used in VGA mode. If AGC mode is desired, a logic low must be applied to the MODE pin. The P2 jumper must be connected to either VPOS (logic high) or ground (logic low).	P2 = installed
R9, R10, R11, R12, C26, C27, C28, C29, P1	Serial control interface. The digital interface sets the VGA1 setpoint, VGA2 setpoint, VGA2 input selection, VGA1 maximum gain, and the VGA2 maximum gain of the device using the serial interface lines CLK, LE, DATA, and SDO. RC filter networks are provided on CLK and LE lines to filter the PC signals (possibly on all the lines). CLK, DATA, SDO, and LE signals can be observed via SMB connectors for debug purposes.	R9, R10, R11, R12 = 0 Ω (0402), C26, C27, C28, C29 = open (0402)
P5	Analog VGA1 gain control. The range of the GAIN1 pin is from 0 V to 1 V, creating a gain scaling of 35 mV/dB.	P5 installed
P4	Analog VGA2 gain control. The range of the GAIN2 pin is from 0 V to 1 V, creating a gain scaling of 35 mV/dB.	P4 installed

Components	Function	Default Conditions
U2, U3, U4, P1	Cypress microcontroller, EEPROM and LDO	U2 = MICROCHIP MICRO24LC64 U3 = Analog Devices, Inc., ADP3334ACPZ U4 = Cypress Semiconductor CY7C68013A-56LTXC P1 = Mini USB Connector
C35, C36, C40, C41, C42, C44, C46	3.3 V supply decoupling; several capacitors are used for decoupling on the 3.3 V supply	C35, C36, C40, C41, C42, C44, C46 = 0.1 µF (0402)
C37, C45, C38, C39, C48, C49, R59, R60, R61, R62, R64, CR2	Cypress and EEPROM components	C38, C48 = 10 pF (0402) C37, C39, C45, C49 = 0.1 µF (0402) R59, R60, R61 = 2 kΩ (0402) R62, R64 = 100 kΩ (0402) CR2 = ROHM SML-21OMTT86
C47, C50, C52, R65, R69, R70, CR1	LDO components	C47, C52 = 1 µF (0402) C50 = 1000 pF (0402) R65 = 2 kΩ (0402) R69 = 78.7 kΩ (0402) R70 = 140 kΩ (0402) CR1 = ROHM SML-21OMTT86
Y1, C51, C54	Crystal oscillator and components. 24 MHz crystal oscillator	Y1 = NDK NX3225SA-24MHz C51, C54 = 22 pF (0402)

EVALUATION BOARD CONTROL SOFTWARE

The ADL5336 evaluation board is controlled through the parallel port on a PC. The parallel port is programmed via the ADL5336 evaluation software. This software controls the following:

- The setpoints of VGA1 and VGA2
- The maximum gains of VGA1 and VGA2
- The input control switch of VGA2

For information about the register map, see Table 5, Table 6, Table 7, and Table 8. For information about SPI port timing and control, see Figure 2 and Figure 3.

After the software is downloaded and installed, start the basic user interface to program the maximum gains, setpoints, and the input of VGA2, see Figure 74.

To program the setpoints of each VGA, click on the respective pull-down menu of the desired VGA under **RMS Out (mVrms/dBV)**, select the desired setpoint, and click **Write Bits**.

To program the maximum gain of each VGA, click on the respective pull-down menu of the desired VGA under the **VGA 1 Max Gain (dB)/VGA 2 Max Gain (dB)**, select the desired maximum gain, and click **Write Bits**.

When the user clicks **Write Bits**, a write operation executes, immediately followed by a read operation. The updated information is displayed in the **VGA1 Current State** and **VGA2 Current State** fields. The gain displayed does not represent the analog VGA gain, only the digital maximum gain.

On VGA2, the user can switch to either **Input A** or **Input B** by selecting the slider switch, **VGA 2 Switch**.

Because the speed of the parallel port varies from PC to PC, the **Clock Stretch** function can be used to change the effective frequency of the CLK line. The CLK line has a scalar range from 1 to 10; 10 is the fastest speed, and 1 is the slowest.

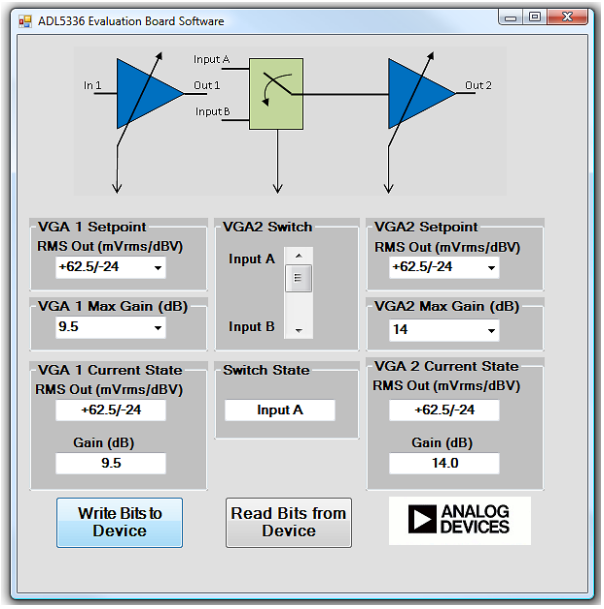


Figure 74. ADL5336 Software Screen Capture

OUTLINE DIMENSIONS

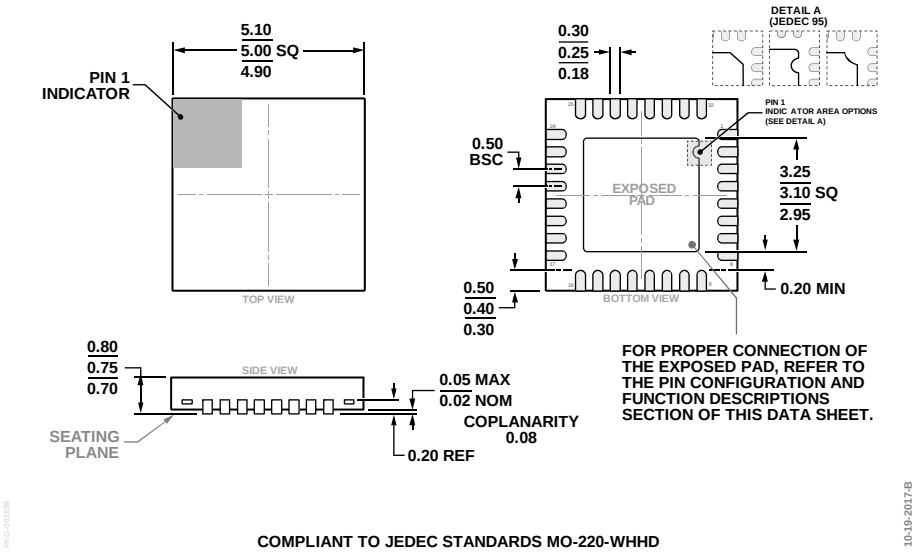


Figure 75. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5336ACPZ-R7	−40°C to +85°C	32-Lead LFCSP, 7″ Tape and Reel	CP-32-7
ADL5336-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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D09550-0-4/18(C)