TQL9047

High Linearity Gain Block

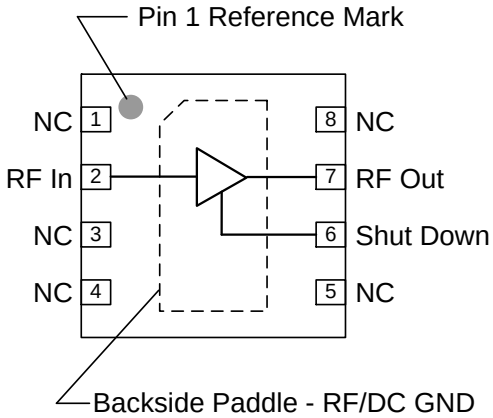
Product Overview

The TQL9047 is a cascadable, high linearity gain block amplifier in a low-cost surface mount package. At 1.9 GHz, the amplifier typically provides 14.5 dB gain, +35.5 dBm OIP3 and 1.6 dB Noise Figure while drawing 70 mA current from a 5V supply.

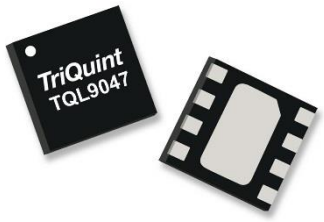
The TQL9047 features medium gain across a broad range of frequencies with the integration of a shut-down biasing capability to allow for operation for TDD applications. The low noise figure and high linearity performance allows the device to be used in both receiver and transmitter chains for high performance systems. The internal active bias circuit also enables stable operation over bias and temperature variations and can be biased from a single positive supply ranging from +3.3 to +5 volts. The amplifier is internally matched using a high performance E-pHEMT process and is housed in a small 2 x 2 mm surface-mount package.

The TQL9047 covers the 700 – 4200 MHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Functional Block Diagram



Top View



8 pin 2x2 mm DFN Package

Key Features

- 50 – 4200 MHz Operational Bandwidth
- Flat Gain (14.5 ± 1 dB) from 0.7 to 2.7 GHz
- High Linearity, +35.5 dBm Output IP3
- 1.6 dB Noise Figure
- Integrated On-chip Matching, 50 ohm In/Out
- Integrated Active Bias
- Integrated Shutdown Control Pin

Applications

- Base Station Transceivers and Repeaters
- Defense Communications
- General Purpose Wireless
- Test Instrumentation
- TDD or FDD systems

Ordering Information

Part No.	Description
TQL9047	2,500 pieces on a 7” reel (standard)
TQL9047-PCB_RF	0.5 – 4.0 GHz Evaluation Board
TQL9047-PCB_IF	50 – 500 MHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150 °C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω, T=25°C	+20 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.0	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
Tj at T_{CASE} max			+138	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions[1]	Min	Typ	Max	Units
Operational Frequency Range		50		4200	MHz
Test Frequency			1900		MHz
Gain		13.0	14.5	16.0	dB
Input Return Loss			11		dB
Output Return Loss			13		dB
Noise Figure			1.6	3.0	dB
Output P1dB		+18	+20.8		dBm
Output IP3	Pout = +4 dBm / tone, Δf = 1 MHz	+32	+35.5		dBm
Power Shutdown Control (Pin 6)	On state	0		+0.5	V
	Off state (Power down)	+1.4	+3.3	V_{DD}	V
Current, I_{DD}	On state		70	100	mA
	Off state (Power down)		3	5	mA
Shutdown pin current, I_{SD}	V_{PD} ≥ +1.4 V		250		µA
Thermal Resistance, θ_{jc}	Channel to case			62	°C/W

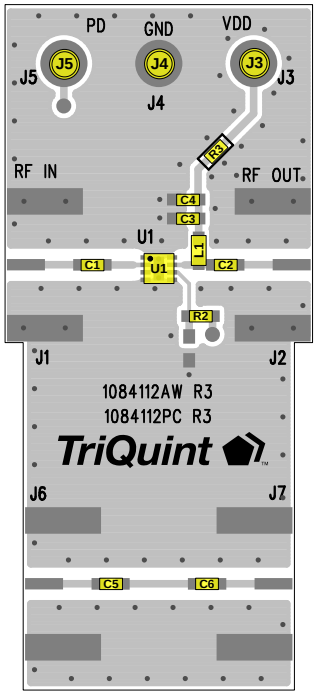
Notes:
1. Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25 °C, 50 Ω system.

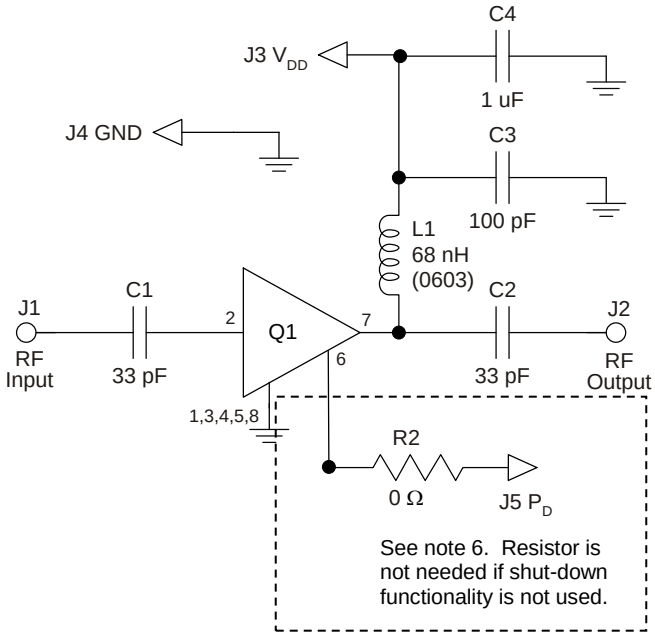
S-Parameters

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.05	-14.7	-82.4	17.5	163.7	-20.4	10.7	-24.7	-89.6
0.1	-19.4	-117.5	16.9	164.3	-20.0	3.6	-18.2	-156.9
0.2	-22.9	-146.3	16.7	159.8	-19.8	-2.1	-18.6	173.6
0.3	-25.2	-165.5	16.6	153.1	-19.8	-6.1	-19.2	153.6
0.4	-26.5	-174.9	16.5	145.7	-19.7	-9.4	-19.1	137.5
0.5	-29.3	179.8	16.4	138.2	-19.7	-12.5	-19.1	121.5
0.6	-32.8	172.9	16.3	130.7	-19.7	-15.7	-19.5	107.6
0.7	-40.1	-174.1	16.2	123.1	-19.7	-18.7	-19.7	93.5
0.8	-43.3	-61.6	16.1	115.6	-19.6	-21.9	-19.8	78.8
0.9	-33.6	-45.7	16.0	108.1	-19.6	-25.0	-20.0	64.2
1.0	-28.8	-45.4	15.9	100.6	-19.6	-28.3	-20.2	50.0
1.1	-25.7	-48.8	15.8	93.1	-19.6	-31.5	-20.3	35.7
1.2	-23.3	-51.6	15.6	85.7	-19.6	-34.8	-20.3	21.1
1.3	-21.4	-55.3	15.5	78.3	-19.6	-38.1	-20.4	6.1
1.4	-19.9	-59.1	15.4	71.0	-19.6	-41.4	-20.3	-8.8
1.5	-18.7	-63.2	15.3	63.6	-19.6	-44.8	-20.0	-23.9
1.6	-17.6	-67.2	15.2	56.4	-19.6	-48.2	-19.7	-38.4
1.7	-16.7	-71.3	15.1	49.1	-19.6	-51.7	-19.2	-52.2
1.8	-15.9	-75.5	14.9	41.9	-19.7	-55.2	-18.7	-65.6
1.9	-15.3	-79.7	14.8	34.6	-19.7	-58.6	-18.1	-78.2
2.0	-14.7	-84.0	14.7	27.4	-19.7	-62.1	-17.5	-89.8
2.1	-14.2	-88.2	14.6	20.1	-19.8	-65.6	-16.9	-100.9
2.2	-13.8	-92.5	14.5	12.8	-19.8	-69.1	-16.3	-111.1
2.3	-13.5	-96.8	14.4	5.5	-19.8	-72.6	-15.8	-120.8
2.4	-13.2	-101.1	14.3	-1.8	-19.8	-76.2	-15.3	-130.2
2.5	-13.0	-105.5	14.3	-9.2	-19.9	-79.8	-14.8	-138.9
2.6	-12.9	-109.9	14.2	-16.7	-19.9	-83.6	-14.4	-147.7
2.7	-12.8	-114.3	14.1	-24.2	-19.9	-87.2	-13.9	-156.5
2.8	-12.7	-118.6	14.1	-32.0	-19.9	-91.0	-13.6	-165.2
2.9	-12.7	-122.8	14.0	-39.7	-19.9	-94.7	-13.2	-173.9
3.0	-12.7	-126.9	13.9	-47.6	-19.9	-98.7	-13.0	177.1
3.1	-12.7	-130.7	13.8	-55.7	-19.9	-102.7	-12.7	168.1
3.2	-12.8	-134.3	13.8	-64.0	-19.9	-106.8	-12.4	158.8
3.3	-12.9	-137.7	13.7	-72.4	-19.8	-111.0	-12.2	149.4
3.4	-13.0	-140.3	13.6	-81.0	-19.8	-115.4	-12.0	139.8
3.5	-13.0	-142.4	13.5	-89.7	-19.7	-119.9	-11.8	129.8
3.6	-13.0	-143.9	13.3	-98.8	-19.7	-124.7	-11.7	119.6
3.8	-12.8	-144.2	13.0	-117.3	-19.5	-134.7	-11.5	98.0
4.0	-11.8	-143.1	12.5	-136.6	-19.4	-145.8	-11.5	75.3
4.2	-10.1	-140.1	12.0	-160.1	-19.5	-160.5	-12.5	49.0

Test Conditions: V_{DD}=+5 V, I_{DD}=70 mA (typ.), Temp.=+25 °C, unmatched 50 Ohm system, reference plane at device leads

TQL9047-PCB_RF Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
5. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
6. R2 is optional and does not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R2 is not loaded, the LNA will operate in its standard “ON” state.
7. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material − TQL9047-PCB_RF

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	N/A
U1	N/A	High Linearity Gain Block	Qorvo	TQL9047
R1	N/A	Do not load	N/A	N/A
R2	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
L1	68 nH	Inductor, 0603, 5%, Ceramic	various	various
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	Various
C1, C2, C3, C5, C6	33 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	Various

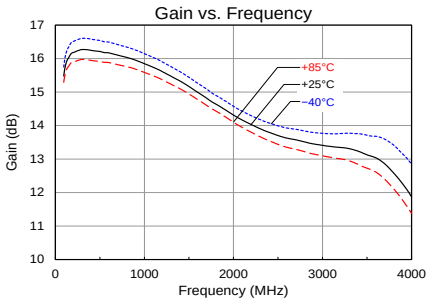
Typical Performance – TQL9047-PCB_RF

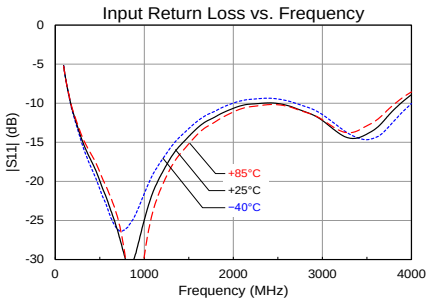
Parameter	Conditions[1]	Typical Values					Units
Frequency		900	1900	2700	3500	4200	MHz
Gain		16	14.5	13.5	13.0	11.2	dB
Input Return Loss		28	11	10	14	8.0	dB
Output Return Loss		19	13	13	20	10.2	dB
Output P1dB		+21	+20.8	+20.5	+19.2	+17.9	dBm
OIP3	Pout = +4 dBm / tone, Δf = 1 MHz	+35.8	+35.5	+35.5	+33.3	+31.4	dBm
Noise figure [2]		1.5	1.6	1.9	2.7	3.7	dB

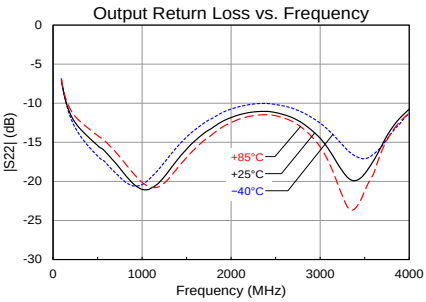
Notes:
1. Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 70 mA (typ.), Temp. = +25 °C
2. Noise figure data shown in the table above is de-embedded from the eval board loss.

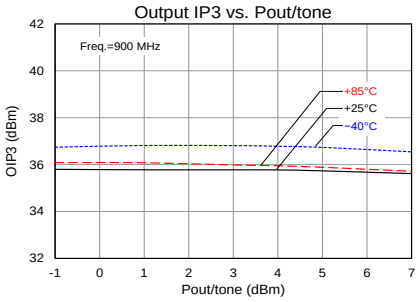
Performance Plots – TQL9047-PCB_RF

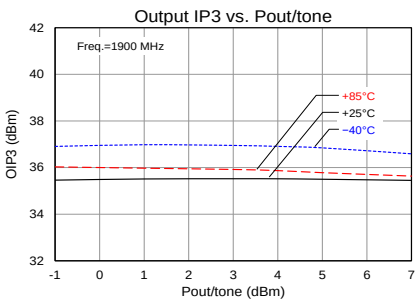
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 70 mA (typ.), Temp. = +25 °C

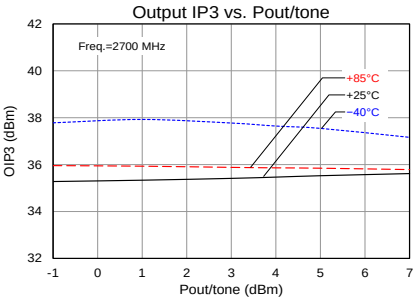






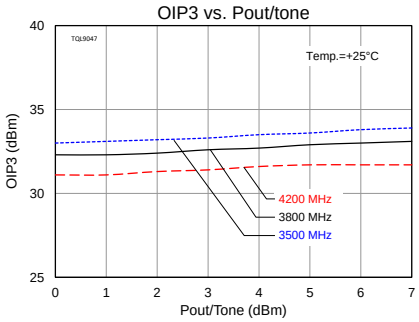


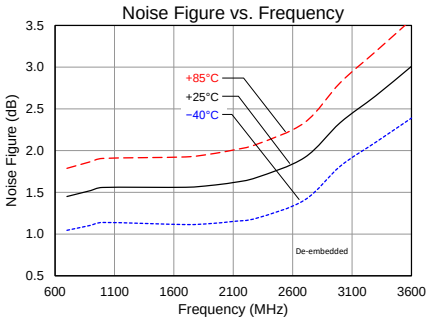


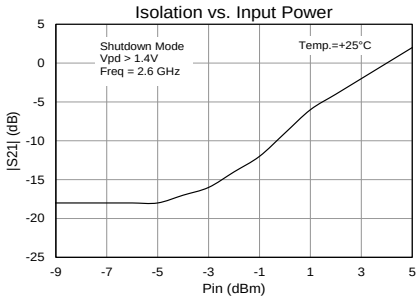


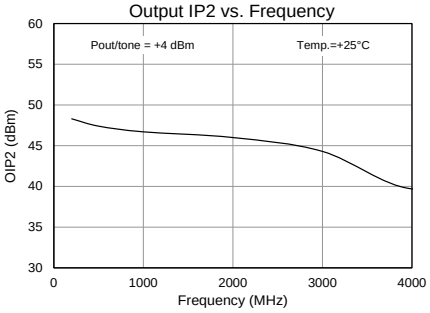
Performance Plots − TQL9047-PCB_RF (cont'd)

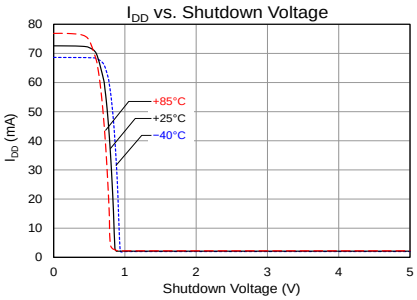
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 70 mA (typ.), Temp. = +25 °C











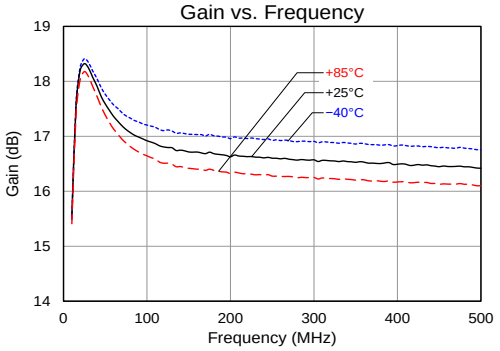
Typical Performance – TQL9047-PCB_IF

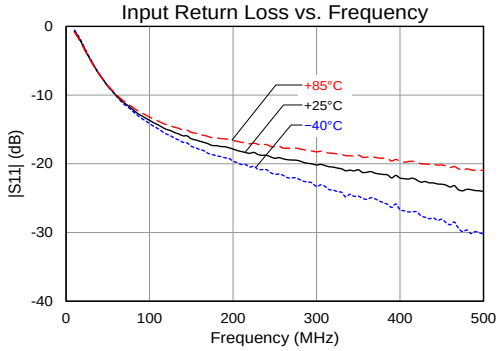
Parameter	Conditions[1]	Typical Values				Units
Frequency		50	100	150	500	MHz
Gain		17.5	17	16.7	16.4	dB
Input Return Loss		8	13	16	23	dB
Output Return Loss		18	17	17	18	dB
Output P1dB		+20.4	+20.7	+20.8	+20.8	dBm
OIP3	Pout = +3 dBm / tone, Δf = 1 MHz	+36.3	+36.4	+36.5	+36.5	dBm
Noise Figure [2]	Eval board losses de-embedded	1.4	1.4	1.4	1.6	dB

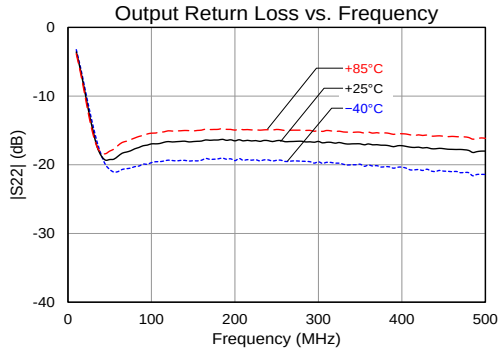
Notes:
1. Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 70 mA (typ.), Temp. = +25 °C
2. Noise figure data shown in the table above is de-embedded from the eval board loss.

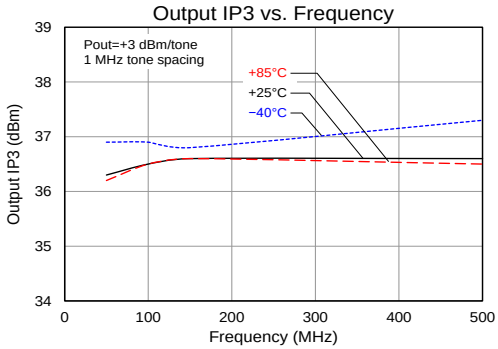
Performance Plots – TQL9047-PCB_IF

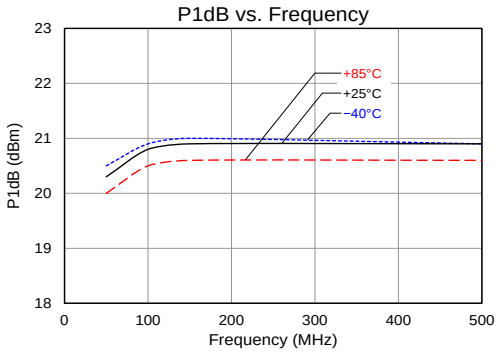
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 70 mA (typ.), Temp. = +25 °C, C1 and C2 = 1000 pF, L1 = 330 nH

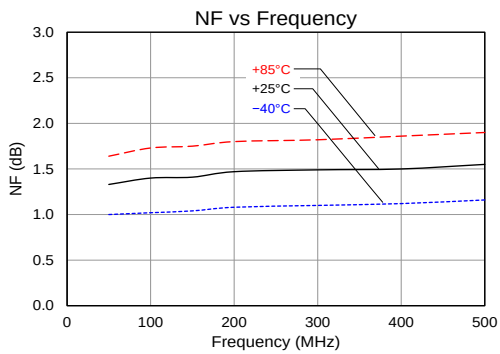












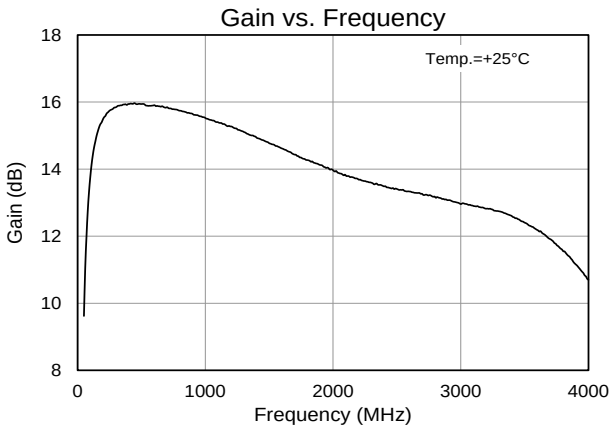
Typical Performance – TQL9047-PCB_RF V_{DD} = +3.3V

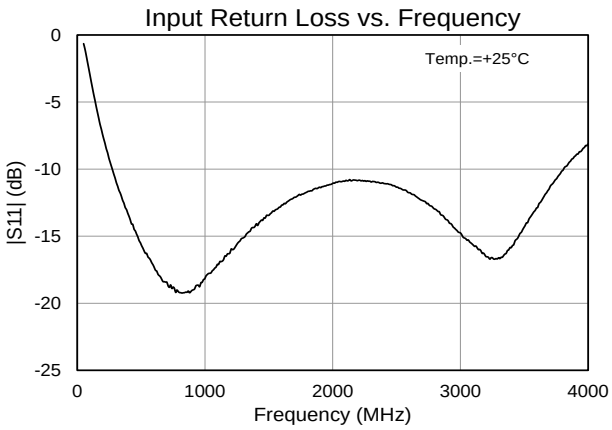
Parameter	Conditions[1]	Typical Values	Units
Frequency		1900	MHz
Gain		14.0	dB
Input Return Loss		11	dB
Output Return Loss		12.5	dB
Output P1dB		+16.7	dBm
OIP3	Pout = +3 dBm / tone, Δf=1 MHz	+29	dBm
Noise figure [2]		1.7	dB

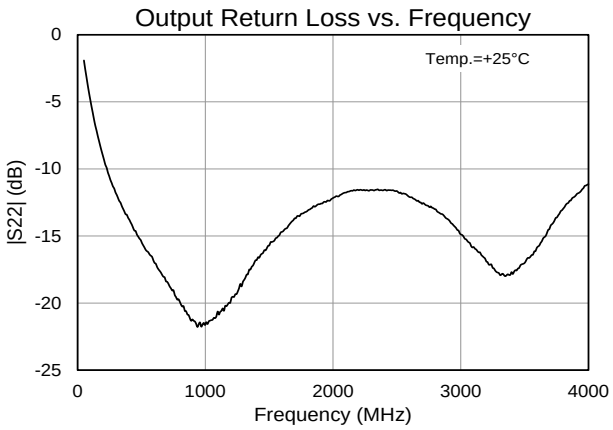
Notes:
1. Test conditions unless otherwise noted: VDD = +3.3V, IDD = 42 mA (typ.), Temp= +25°C
2. Noise figure data shown in the table above is de-embedded from the eval board loss.

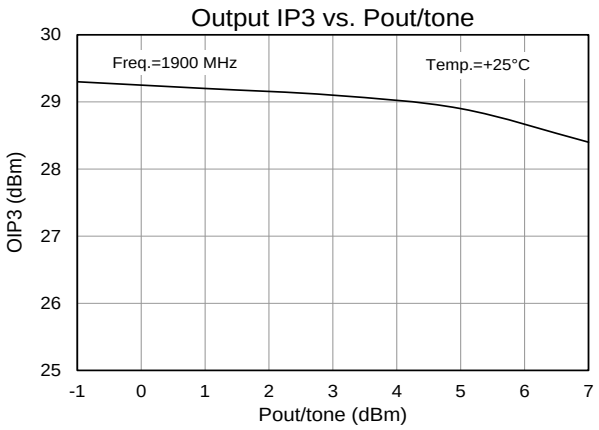
Performance Plots – TQL9047-PCB_RF V_{DD} = +3.3V

Test conditions unless otherwise noted: V_{DD} = +3.3 V, I_{DD} = 42 mA (typ.), Temp. = +25 °C







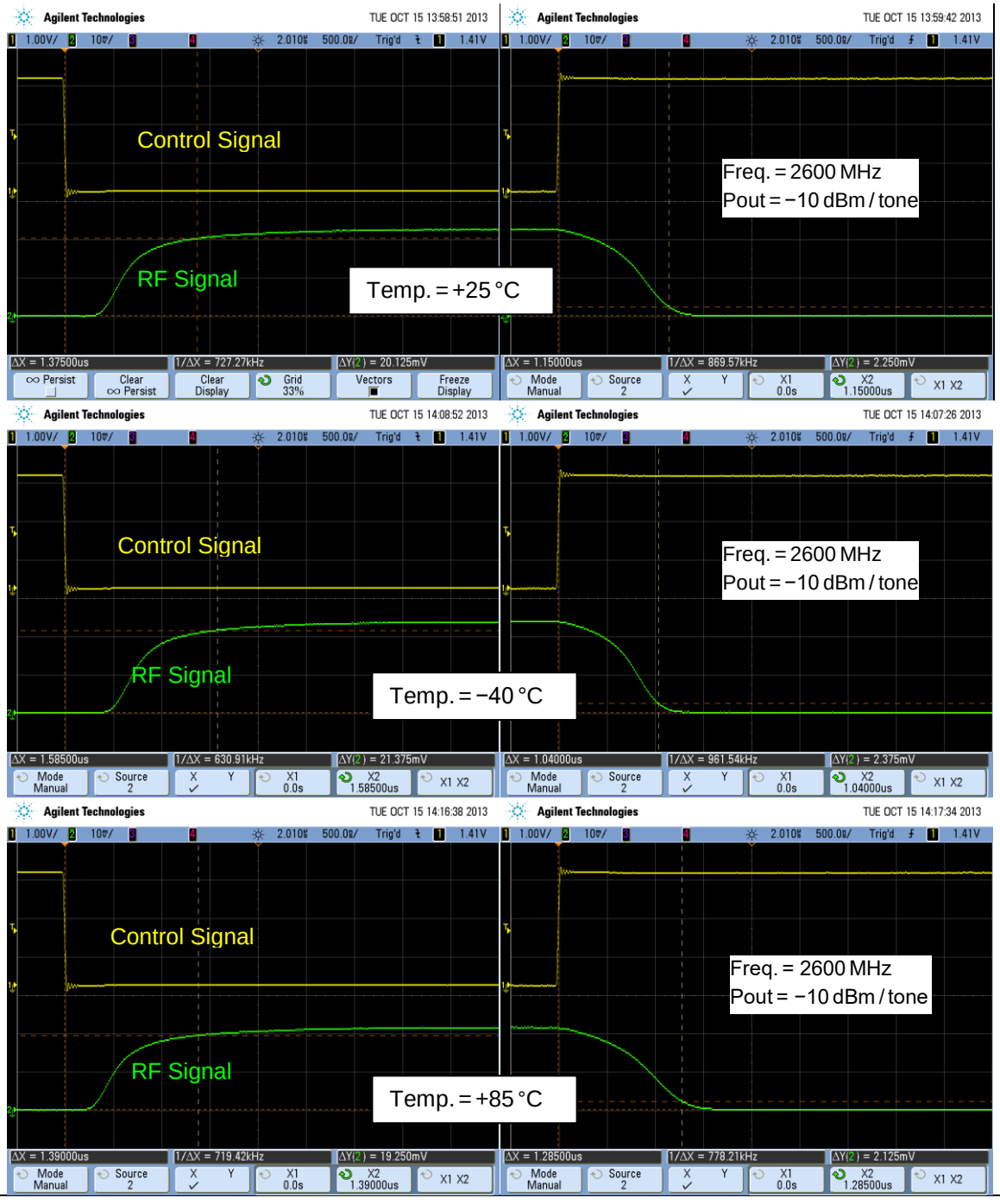


Switching Speed

Switching Speed Measurement based on TQS Application Board

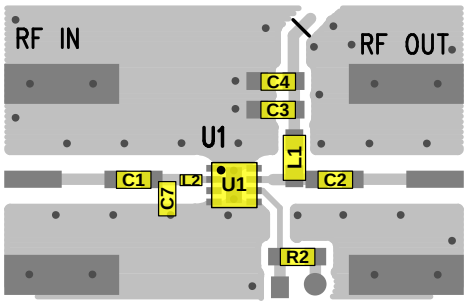
Using Shutdown Circuit: V_{PD} = +3 V, V_{DD} = +5 V

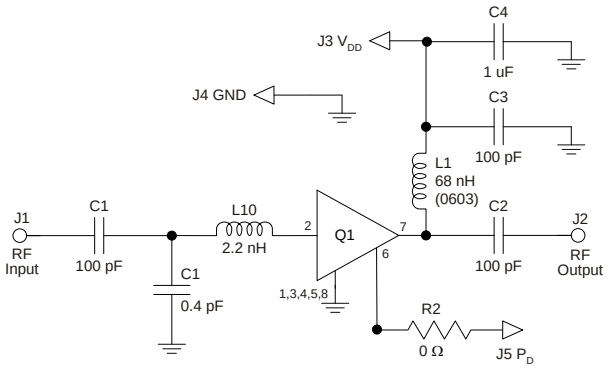
Parameter	−40 °C	+25 °C	+85 °C
Turn-off Transition (50% CNTR – 10% RF)	1.04 µs	1.15 µs	1.28 µs
Turn-on Transition (50% CNTR – 90% RF)	1.58 µs	1.37 µs	1.39 µs



Reference Design – Optimized Return Loss

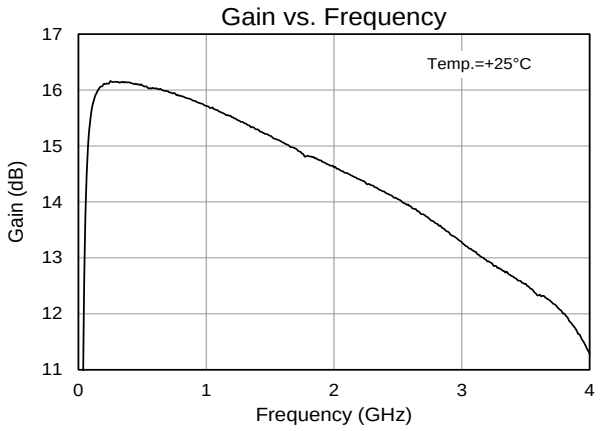
Input return loss over the 500 – 2700 MHz band can be optimized using a 2 element input tune.

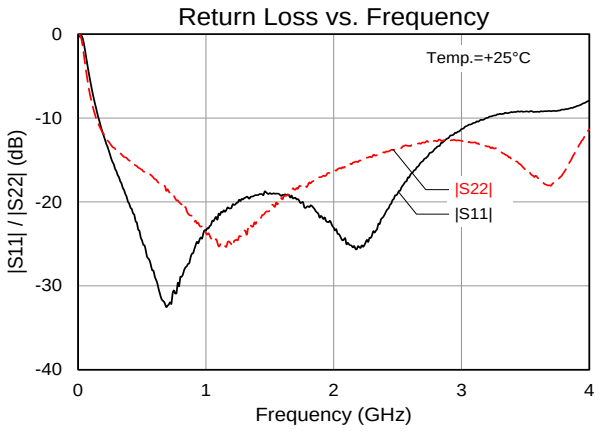


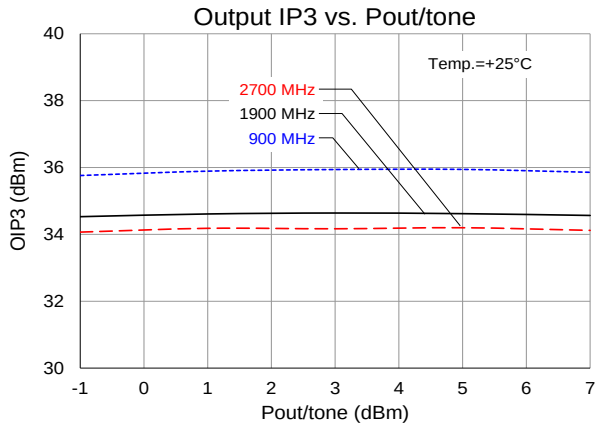


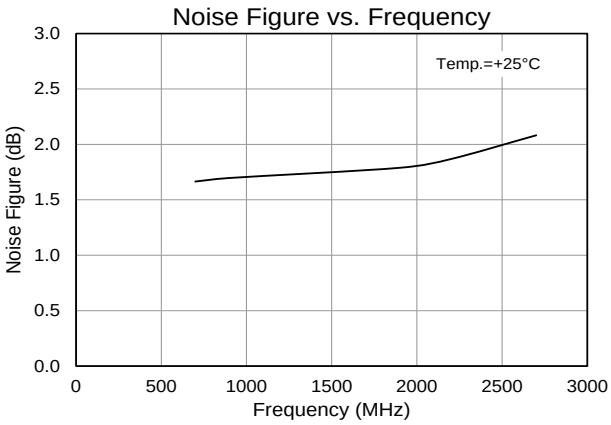
Performance Plots

Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 70 mA (typ.), Temp. = +25 °C

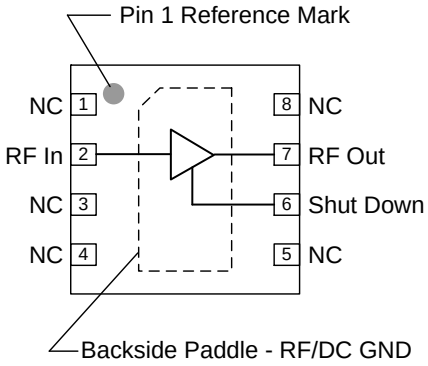








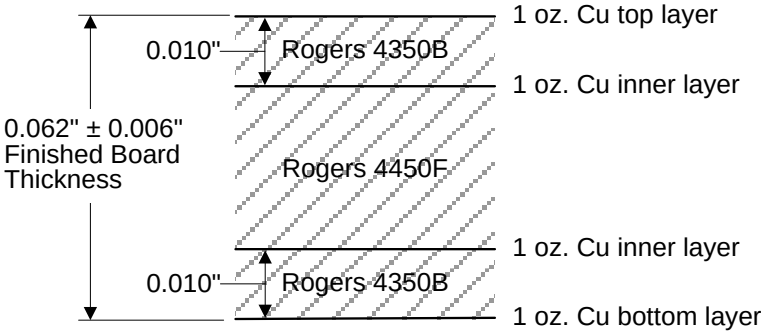
Pin Configuration and Description



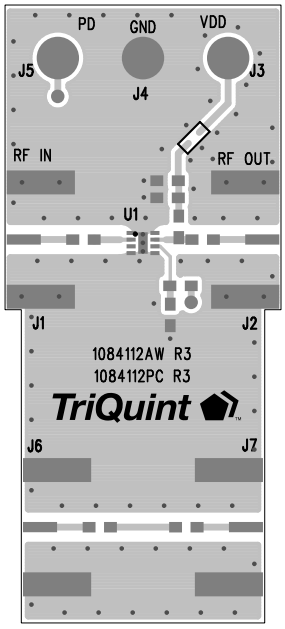
Pin No.	Label	Description
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage turns off the device. If the pin is not connected or is less than 0.5V, then the device will operate under its normal operating condition.
7	RF Out	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

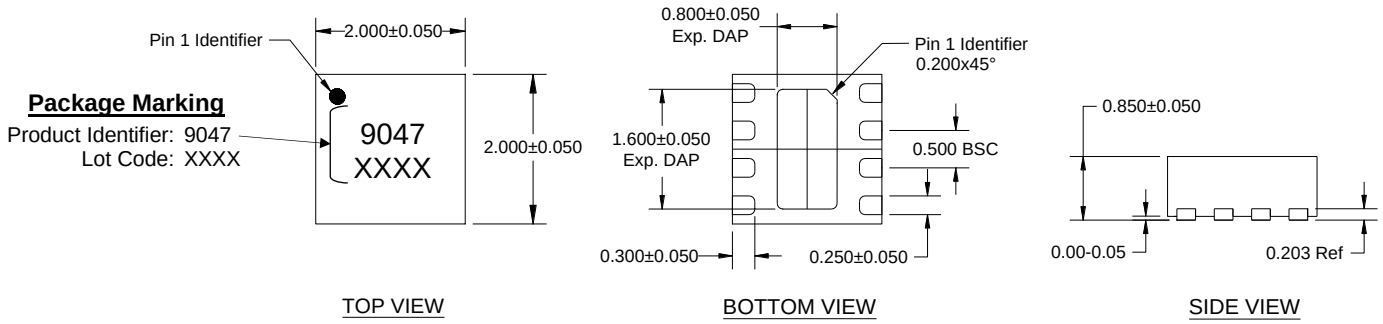
Qorvo PCB 1084112 Material and Stack-up



50 ohm line dimensions: width = 0.020”, spacing = 0.032”

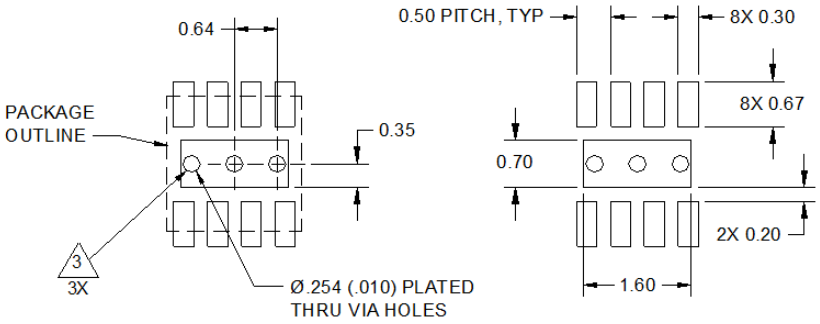


Package Marking and Dimensions



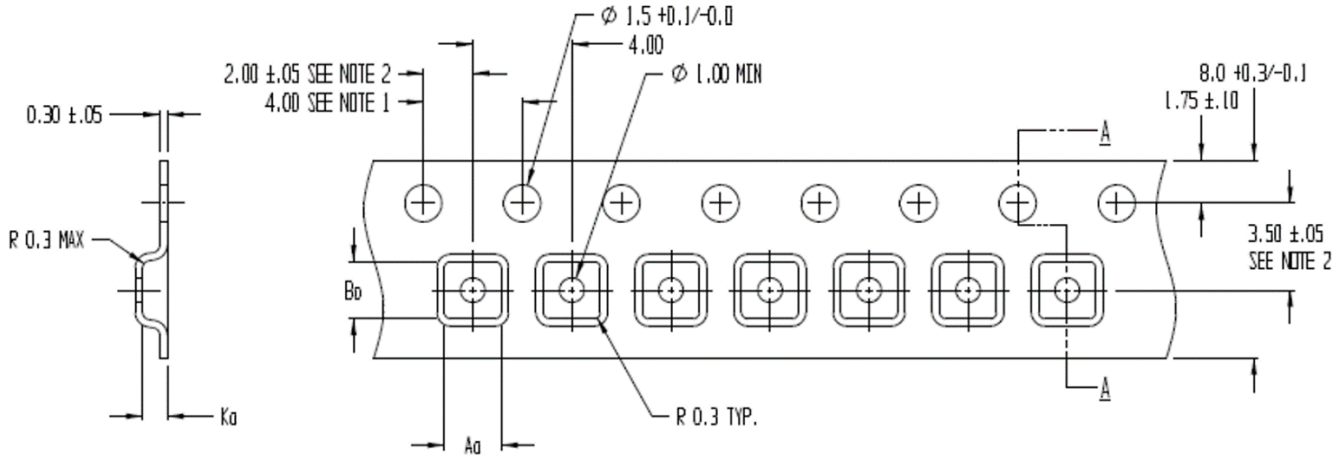
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

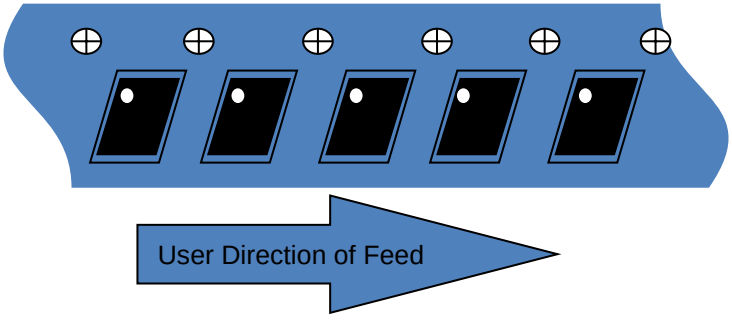


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

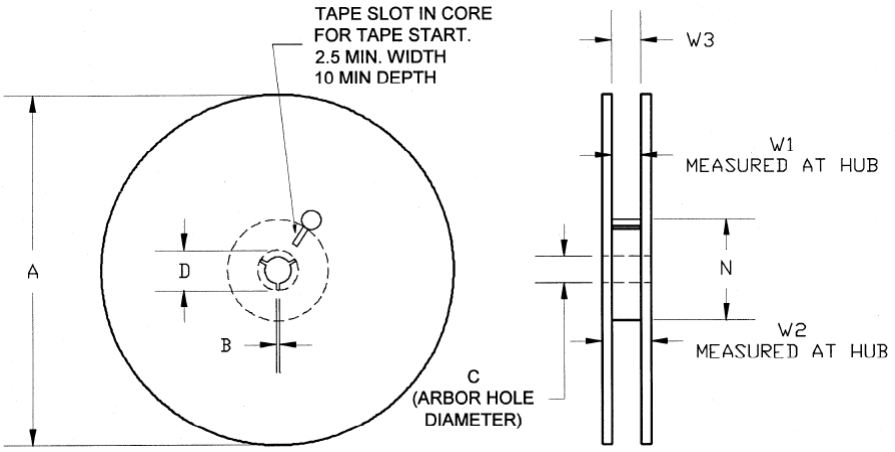


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.30
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.00
	Thickness	W2	0.559	14.20
	Space Between Flange	W1	0.346	8.80
Hub	Outer Diameter	N	2.283	58.00
	Arbor Hole Diameter	C	0.512	13.00
	Key Slit Width	B	0.079	2.00
	Key Slit Diameter	D	0.787	20.00

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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