

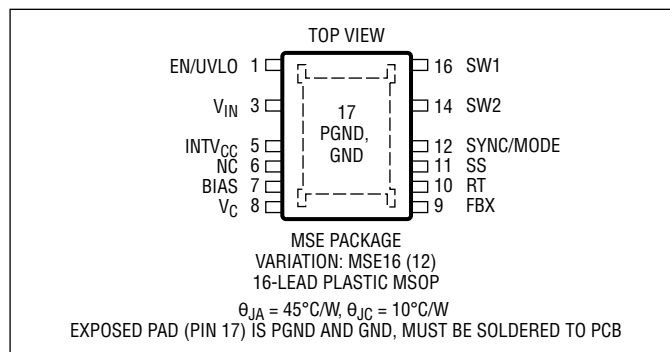


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

|                                            |                |
|--------------------------------------------|----------------|
| SW .....                                   | 150V           |
| $V_{IN}$ , EN/UVLO .....                   | 60V            |
| BIAS .....                                 | 60V            |
| EN/UVLO Pin Above $V_{IN}$ Pin, SYNC ..... | 6V             |
| INTV <sub>CC</sub> .....                   | (Note 2)       |
| $V_C$ .....                                | 4V             |
| FBX .....                                  | ±4V            |
| Operating Junction Temperature (Note 3)    |                |
| LT8365E .....                              | −40°C to 125°C |
| LT8365J, LT8365H .....                     | −40°C to 150°C |
| Storage Temperature Range .....            | −65°C to 150°C |

## PIN CONFIGURATION



## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL    | PART MARKING* | PACKAGE DESCRIPTION                      | TEMPERATURE RANGE |
|------------------|------------------|---------------|------------------------------------------|-------------------|
| LT8365EMSE#PBF   | LT8365EMSE#TRPBF | 8365          | 16-Lead Plastic MSOP with 4 Pins Removed | −40°C to 125°C    |
| LT8365JMSE#PBF   | LT8365JMSE#TRPBF | 8365          | 16-Lead Plastic MSOP with 4 Pins Removed | −40°C to 150°C    |
| LT8365HMSE#PBF   | LT8365HMSE#TRPBF | 8365          | 16-Lead Plastic MSOP with 4 Pins Removed | −40°C to 150°C    |

### AUTOMOTIVE PRODUCTS\*\*

|                 |                   |      |                                          |                |
|-----------------|-------------------|------|------------------------------------------|----------------|
| LT8365EMSE#WPBF | LT8365EMSE#WTRPBF | 8365 | 16-Lead Plastic MSOP with 4 Pins Removed | −40°C to 125°C |
| LT8365JMSE#WPBF | LT8365JMSE#WTRPBF | 8365 | 16-Lead Plastic MSOP with 4 Pins Removed | −40°C to 150°C |
| LT8365HMSE#WPBF | LT8365HMSE#WTRPBF | 8365 | 16-Lead Plastic MSOP with 4 Pins Removed | −40°C to 150°C |

Contact the factory for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

**Tape and reel specifications.** Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**\*\*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.**

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ ,  $EN/UVLO = 12\text{V}$  unless otherwise noted.

| PARAMETER                                                      | CONDITIONS                                          |   | MIN             | TYP   | MAX    | UNITS   |
|----------------------------------------------------------------|-----------------------------------------------------|---|-----------------|-------|--------|---------|
| V <sub>IN</sub> Operating Voltage Range                        |                                                     | ● | 2.8             |       | 60     | V       |
| V <sub>IN</sub> Quiescent Current at Shutdown                  | V <sub>EN/UVLO</sub> = 0.2V                         | ● |                 | 1     | 2      | μA      |
|                                                                |                                                     | ● |                 | 1     | 15     | μA      |
|                                                                | V <sub>EN/UVLO</sub> = 1.5V                         | ● |                 | 2     | 5      | μA      |
|                                                                |                                                     | ● |                 | 2     | 25     | μA      |
| V <sub>IN</sub> Quiescent Current                              |                                                     |   |                 |       |        |         |
| Sleep Mode (Not Switching)                                     | SYNC = 0V                                           | ● |                 | 9     | 15     | μA      |
|                                                                |                                                     |   |                 | 9     | 30     | μA      |
| Active Mode (Not Switching)                                    | SYNC = 0V or INTV <sub>CC</sub> , BIAS = 0V         | ● |                 | 1200  | 1600   | μA      |
|                                                                |                                                     | ● |                 | 1200  | 1850   | μA      |
|                                                                | SYNC = 0V or INTV <sub>CC</sub> , BIAS = 5V         | ● |                 | 22    | 40     | μA      |
|                                                                |                                                     |   |                 | 22    | 65     | μA      |
| BIAS Threshold                                                 | Rising, BIAS Can Supply INTV <sub>CC</sub>          |   |                 | 4.4   | 4.65   | V       |
|                                                                | Falling, BIAS Cannot Supply INTV <sub>CC</sub>      |   |                 | 4     | 4.25   | V       |
| V <sub>IN</sub> Falling Threshold to Supply INTV <sub>CC</sub> | BIAS = 12V                                          |   | BIAS – 2V       |       |        | V       |
| BIAS Falling Threshold to Supply INTV <sub>CC</sub>            | V <sub>IN</sub> = 12V                               |   | V <sub>IN</sub> |       |        | V       |
| FBX Regulation                                                 |                                                     |   |                 |       |        |         |
| FBX Regulation Voltage                                         | FBX > 0V                                            | ● | 1.568           | 1.6   | 1.636  | V       |
|                                                                | FBX < 0V                                            | ● | –0.822          | –0.80 | –0.780 | V       |
| FBX Line Regulation                                            | FBX > 0V, 2.8V < V <sub>IN</sub> < 60V              |   |                 | 0.005 | 0.015  | %/V     |
|                                                                | FBX < 0V, 2.8V < V <sub>IN</sub> < 60V              |   |                 | 0.005 | 0.015  | %/V     |
| FBX Pin Current                                                | FBX = 1.6V, –0.8V                                   | ● | –10             |       | 10     | nA      |
| Oscillator                                                     |                                                     |   |                 |       |        |         |
| Switching Frequency (f <sub>OSC</sub> )                        | R <sub>T</sub> = 432k                               | ● | 92              | 100   | 113    | kHz     |
|                                                                | R <sub>T</sub> = 143k                               | ● | 279             | 300   | 321    | kHz     |
|                                                                | R <sub>T</sub> = 84.5k                              | ● | 465             | 500   | 535    | kHz     |
| SSFM Maximum Frequency Deviation                               | (Δf/f <sub>OSC</sub> ) • 100, R <sub>T</sub> = 143k |   | 14              | 20    | 28     | %       |
| Minimum On-Time                                                | Burst Mode, V <sub>IN</sub> = 24V (Note 6)          |   |                 | 110   | 200    | ns      |
|                                                                | Pulse-Skipping Mode, V <sub>IN</sub> = 24V (Note 6) |   |                 | 110   | 200    | ns      |
| Minimum Off-Time                                               |                                                     | ● |                 | 100   | 115    | ns      |
| SYNC/Mode, Mode Thresholds (Note 5)                            | High (Rising), V <sub>IN</sub> = 24V                | ● |                 | 1.3   | 1.7    | V       |
|                                                                | Low (Falling), V <sub>IN</sub> = 24V                | ● | 0.14            | 0.2   |        | V       |
| SYNC/Mode, Clock Thresholds (Note 5)                           | Rising, V <sub>IN</sub> = 24V                       | ● |                 | 1.3   | 1.7    | V       |
|                                                                | Falling, V <sub>IN</sub> = 24V                      | ● | 0.4             | 0.8   |        | V       |
| f <sub>SYNC</sub> /f <sub>OSC</sub> Allowed Ratio              | R <sub>T</sub> = 84.5k                              |   | 0.95            | 1     | 1.25   | kHz/kHz |
| SYNC Pin Current                                               | SYNC = 2V                                           |   |                 | 10    | 25     | μA      |
|                                                                | SYNC = 0V, Current Out of Pin                       |   |                 | 10    | 25     | μA      |
| Switch                                                         |                                                     |   |                 |       |        |         |
| Maximum Switch Current Limit Threshold                         |                                                     | ● | 1.5             | 2     | 2.7    | A       |
| Switch Overcurrent Threshold                                   | Discharges SS Pin                                   |   |                 | 3     |        | A       |
| Switch R <sub>DS(ON)</sub>                                     | I <sub>SW</sub> = 0.5A                              |   |                 | 700   |        | mΩ      |
| Switch Leakage Current                                         | V <sub>SW</sub> = 150V                              |   |                 | 0.1   | 1      | μA      |

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ ,  $EN/UVLO = 12\text{V}$  unless otherwise noted.

| PARAMETER                          | CONDITIONS                               |   | MIN   | TYP        | MAX   | UNITS                              |
|------------------------------------|------------------------------------------|---|-------|------------|-------|------------------------------------|
| <b>EN/UVLO Logic</b>               |                                          |   |       |            |       |                                    |
| EN/UVLO Pin Threshold (Rising)     | Start Switching                          | ● | 1.576 | 1.68       | 1.90  | V                                  |
| EN/UVLO Pin Threshold (Falling)    | Stop Switching                           | ● | 1.545 | 1.6        | 1.645 | V                                  |
| EN/UVLO Pin Current                | $V_{EN/UVLO} = 1.6\text{V}$              | ● | -50   |            | 50    | nA                                 |
| <b>Soft-Start</b>                  |                                          |   |       |            |       |                                    |
| Soft-Start Charge Current          | SS = 0.5V                                |   |       | 2          |       | $\mu\text{A}$                      |
| Soft-Start Pull-Down Resistance    | Fault Condition, SS = 0.1V               |   |       | 220        |       | $\Omega$                           |
| <b>Error Amplifier</b>             |                                          |   |       |            |       |                                    |
| Error Amplifier Transconductance   | FBX = 1.6V<br>FBX = -0.8V                |   |       | 75<br>60   |       | $\mu\text{A/V}$<br>$\mu\text{A/V}$ |
| Error Amplifier Voltage Gain       | FBX = 1.6V<br>FBX = -0.8V                |   |       | 185<br>145 |       | V/V<br>V/V                         |
| Error Amplifier Max Source Current | $V_C = 1.1\text{V}$ , Current Out of Pin |   |       | 7          |       | $\mu\text{A}$                      |
| Error Amplifier Max Sink Current   | $V_C = 1.1\text{V}$                      |   |       | 7          |       | $\mu\text{A}$                      |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:**  $\text{INTV}_{CC}$  cannot be externally driven. No additional components or loading is allowed on this pin.

**Note 3:** The LT8365E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8365J and the LT8365H are guaranteed over the full  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  operating junction temperature range.

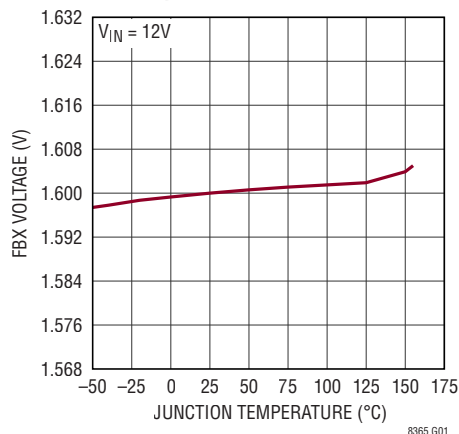
**Note 4:** The IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed  $150^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

**Note 5:** For SYNC/MODE inputs required to select modes of operation see the Pin Functions and Applications Information sections.

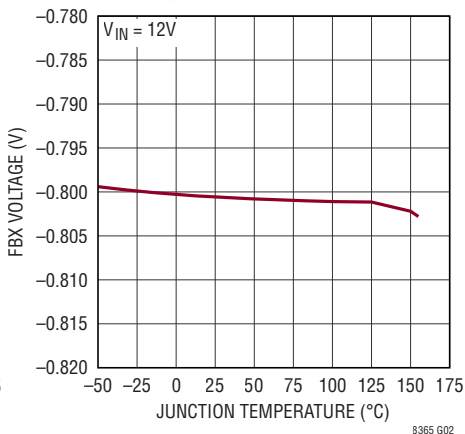
**Note 6:** The IC is tested in a Boost converter configuration with the output voltage programmed for 24V.

# TYPICAL PERFORMANCE CHARACTERISTICS

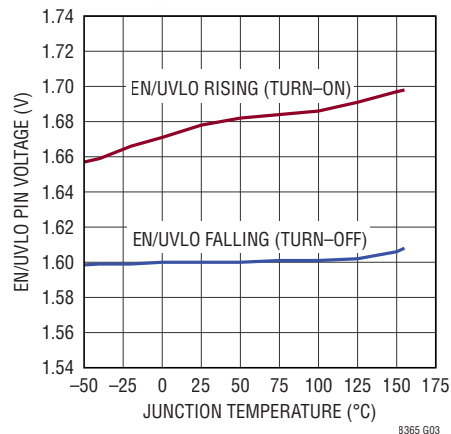
**FBX Positive Regulation Voltage vs Temperature**



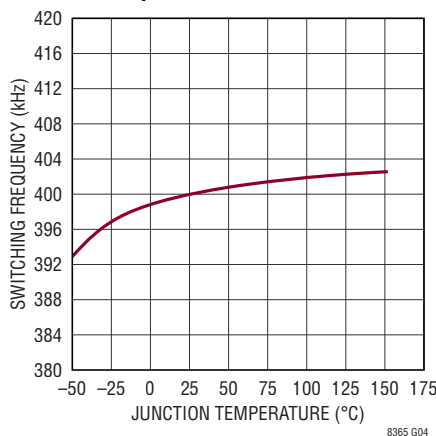
**FBX Negative Regulation Voltage vs Temperature**



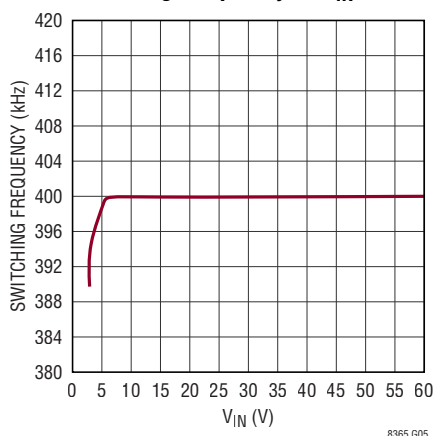
**EN/UVLO Pin Thresholds vs Temperature**



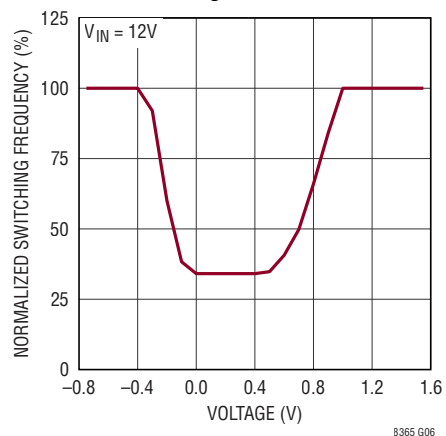
**Switching Frequency vs Temperature**



**Switching Frequency vs V\_IN**



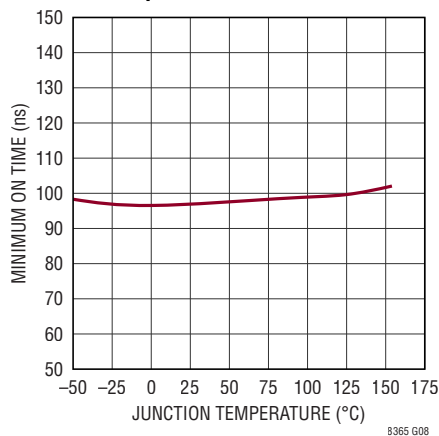
**Normalized Switching Frequency vs FBX Voltage**



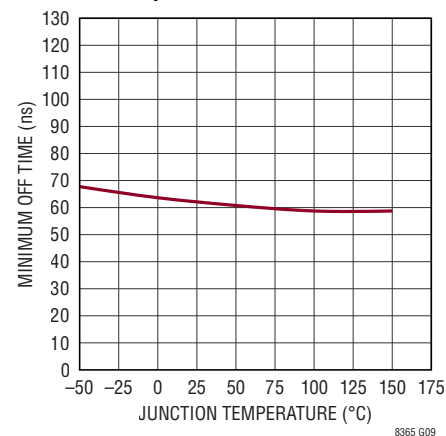
**Switch Current Limit vs Duty Cycle**



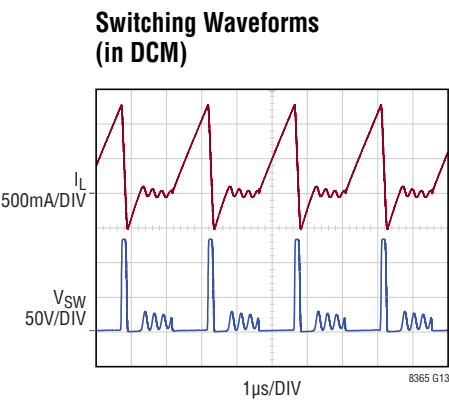
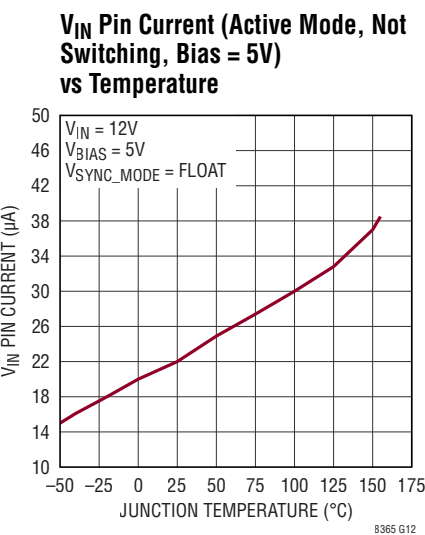
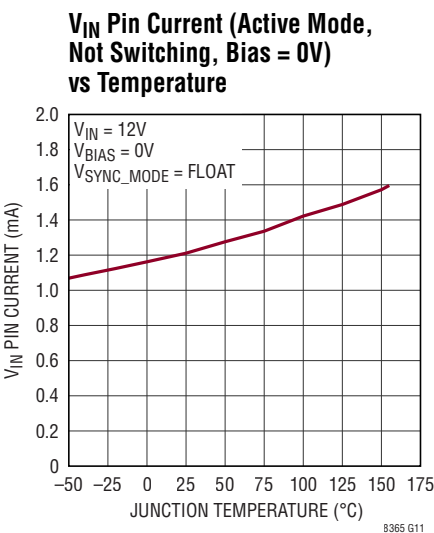
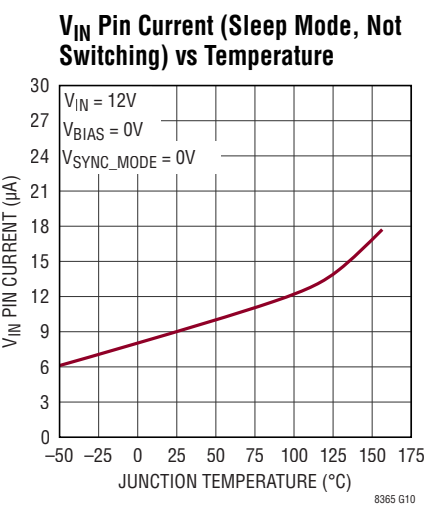
**Switch Minimum On-Time vs Temperature**



**Switch Minimum Off-Time vs Temperature**



TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**EN/UVLO:** Shutdown and Undervoltage Detect Pin. The LT8365 is shut down when this pin is low and active when this pin is high. Below an accurate 1.6V threshold, the part enters undervoltage lockout and stops switching. This allows an undervoltage lockout (UVLO) threshold to be programmed for system input voltage by resistively dividing down system input voltage to the EN/UVLO pin. An 80mV pin hysteresis ensures part switching resumes when the pin exceeds 1.68V. EN/UVLO pin voltage below 0.2V reduces  $V_{IN}$  current below 1 $\mu$ A. If shutdown and UVLO features are not required, the pin can be tied directly to system input.

**$V_{IN}$ :** Input Supply. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the  $V_{IN}$  pin, and the negative terminal as close as possible to the exposed pad PGND copper (near EN/UVLO).

**INTV<sub>CC</sub>:** Regulated 3.8V Supply for Internal Loads. The INTV<sub>CC</sub> pin must be bypassed with a 1 $\mu$ F low ESR ceramic capacitor to GND. No additional components or loading is allowed on this pin. INTV<sub>CC</sub> draws power from the BIAS pin if  $4.4V \leq BIAS \leq V_{IN}$ , otherwise INTV<sub>CC</sub> is powered by the  $V_{IN}$  pin.

**NC:** No Internal Connection. Leave this pin open.

**BIAS:** Second Input Supply for Powering INTV<sub>CC</sub>. Removes the majority of INTV<sub>CC</sub> current from the  $V_{IN}$  pin to improve efficiency when  $4.4V \leq BIAS \leq V_{IN}$ . If unused, tie the pin to GND.

**$V_C$ :** Error Amplifier Output Pin. Tie external compensation network to this pin.

**FBX:** Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor divider between the output and the exposed pad GND copper (near FBX). FBX reduces the switching frequency during start-up and fault conditions when FBX is close to 0V.

**RT:** A resistor from this pin to the exposed pad GND copper (near FBX) programs switching frequency.

**SS:** Soft-Start Pin. Connect a capacitor from this pin to GND copper (near FBX) to control the ramp rate of inductor current during converter start-up. SS pin charging current is 2 $\mu$ A. An internal 220 $\Omega$  MOSFET discharges this pin during shutdown or fault conditions.

**SYNC/MODE:** This pin allows five selectable modes for optimization of performance.

| SYNC/MODE PIN INPUT             | CAPABLE MODE(S) OF OPERATION |
|---------------------------------|------------------------------|
| (1) GND or <0.14V               | Burst                        |
| (2) External Clock              | Pulse-Skipping/Sync          |
| (3) 100k Resistor to GND        | Burst/SSFM                   |
| (4) Float (Pin Open)            | Pulse-Skipping               |
| (5) INTV <sub>CC</sub> or >1.7V | Pulse-Skipping/SSFM          |

where the selectable modes of operation are:

Burst = low  $I_Q$ , low output ripple operation at light loads  
Pulse-skipping = skipped pulse(s) at light load (aligned to clock)  
Sync = switching frequency synchronized to external clock  
SSFM = Spread Spectrum Frequency Modulation for low EMI.

**SW1, SW2 (SW):** Output of the Internal Power Switch. Minimize the metal trace area connected to these pins to reduce EMI.

**PGND, GND:** Power Ground and Signal Ground for the IC. The package has an exposed pad underneath the IC which is the best path for heat out of the package. The pin should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8365. Connect power ground components to the exposed pad copper exiting near the EN/UVLO and SW pins. Connect signal ground components to the exposed pad copper exiting near the  $V_C$  and FBX pins.





## OPERATION

The LT8365 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram. An oscillator (with frequency programmed by a resistor at the RT pin) turns on the internal power switch at the beginning of each clock cycle. Current in the inductor then increases until the current comparator trips and turns off the power switch. The peak inductor current at which the switch turns off is controlled by the voltage on the  $V_C$  pin. The error amplifier servos the  $V_C$  pin by comparing the voltage on the FBX pin with an internal reference voltage (1.60V or  $-0.80V$ , depending on the chosen topology). When the load current increases it causes a reduction in the FBX pin voltage relative to the internal reference. This causes the error amplifier to increase the  $V_C$  pin voltage until the new load current is satisfied. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT8365 is capable of generating either a positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter to generate a positive output voltage, or as an inverting converter to generate a negative output voltage. When configured as a Boost converter, as shown in the Block Diagram, the FBX pin is pulled up to the internal bias voltage of 1.60V by a voltage divider (R1 and R2) connected from  $V_{OUT}$  to GND. Amplifier A2 becomes inactive and amplifier A1 performs (inverting) amplification from FBX to  $V_C$ . When the LT8365 is in an inverting configuration, the FBX pin is pulled down to  $-0.80V$  by a voltage divider from  $V_{OUT}$  to GND. Amplifier A1 becomes inactive and amplifier A2 performs (non-inverting) amplification from FBX to  $V_C$ .

If the EN/UVLO pin voltage is below 1.6V, the LT8365 enters undervoltage lockout (UVLO), and stops switching. When the EN/UVLO pin voltage is above 1.68V (typical), the LT8365 resumes switching. If the EN/UVLO pin voltage is below 0.2V, the LT8365 draws less than  $1\mu A$  from  $V_{IN}$ .

For the SYNC/MODE pin tied to ground or  $<0.14V$ , the LT8365 will enter low output ripple Burst Mode operation for ultra low quiescent current during light loads to maintain high efficiency. For a 100k resistor from SYNC/MODE pin to GND, the LT8365 uses Burst Mode operation for improved efficiency at light loads but seamlessly transitions to Spread-Spectrum Modulation of switching frequency for low EMI at heavy loads. For the SYNC/MODE pin floating (left open), the LT8365 uses pulse-skipping mode, at the expense of hundreds of microamps, to maintain output voltage regulation at light loads by skipping switch pulses. For the SYNC/MODE pin tied to  $INTV_{CC}$  or  $>1.7V$ , the LT8365 uses pulse-skipping mode and performs Spread-Spectrum Modulation of switching frequency. For the SYNC/MODE pin driven by an external clock, the converter switching frequency is synchronized to that clock and pulse-skipping mode is also enabled. See the Pin Functions section for SYNC/MODE pin.

The LT8365 includes a BIAS pin to improve efficiency across all loads. The LT8365 intelligently chooses between the  $V_{IN}$  and BIAS pins to supply the  $INTV_{CC}$  for best efficiency. The  $INTV_{CC}$  supply current can be drawn from the BIAS pin instead of the  $V_{IN}$  pin for  $4.4V \leq BIAS \leq V_{IN}$ .

Protection features ensure the immediate disable of switching and reset of the SS pin for any of the following faults: internal reference UVLO,  $INTV_{CC}$  UVLO, switch current  $> 1.5 \times$  maximum limit, EN/UVLO  $< 1.6V$  or junction temperature  $> 170^\circ C$ .

## APPLICATIONS INFORMATION

### ACHIEVING ULTRALOW QUIESCENT CURRENT

To enhance efficiency at light loads the LT8365 uses a low ripple Burst Mode architecture. This keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output ripple. In Burst Mode operation, the LT8365 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, the LT8365 consumes only 9μA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8365 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load. The largest contributor to leakage current can be due to the reverse biased leakage of the Schottky diode (see Diode Selection in the Applications Information section).

While in Burst Mode operation, the current limit of the switch is approximately 325mA resulting in the output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As the output load ramps upward from zero the switching frequency will increase but only up to the fixed frequency defined by the resistor at the

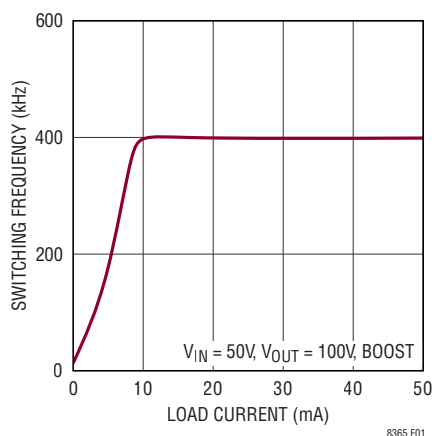


Figure 1. Burst Frequency vs Load Current

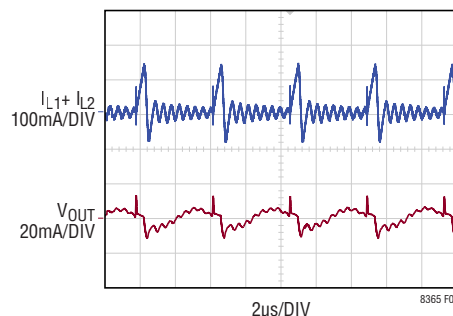


Figure 2. Burst Mode Operation

RT pin as shown in Figure 1. The output load at which the LT8365 reaches the fixed frequency varies based on input voltage, output voltage, and inductor choice.

### PROGRAMMING INPUT TURN-ON AND TURN-OFF THRESHOLDS WITH EN/UVLO PIN

The EN/UVLO pin voltage controls whether the LT8365 is enabled or is in a shutdown state. A 1.6V reference and a comparator A6 with built-in hysteresis (typical 80mV) allow the user to accurately program the system input voltage at which the IC turns on and off (see the Block Diagram). The typical input falling and rising threshold voltages can be calculated by the following equations:

$$V_{IN(FALLING, UVLO(-))} = 1.60 \cdot \frac{R3 + R4}{R4}$$

$$V_{IN(RISING, UVLO(+))} = 1.68 \cdot \frac{R3 + R4}{R4}$$

$V_{IN}$  current is reduced below 1μA when the EN/UVLO pin voltage is less than 0.2V. The EN/UVLO pin can be connected directly to the input supply  $V_{IN}$  for always-enabled operation. A logic input can also control the EN/UVLO pin.

When operating in Burst Mode operation for light load currents, the current through the R3 and R4 network can easily be greater than the supply current consumed by the LT8365. Therefore, R3 and R4 should be large enough to minimize their effect on efficiency at light loads.

## APPLICATIONS INFORMATION

### INTV<sub>CC</sub> REGULATOR

A low dropout (LDO) linear regulator, supplied from V<sub>IN</sub>, produces a 3.2V supply at the INTV<sub>CC</sub> pin. A minimum 1μF low ESR ceramic capacitor must be used to bypass the INTV<sub>CC</sub> pin to ground to supply the high transient currents required by the internal power MOSFET gate driver.

No additional components or loading is allowed on this pin. The INTV<sub>CC</sub> rising threshold (to allow soft-start and switching) is typically 2.65V. The INTV<sub>CC</sub> falling threshold (to stop switching and reset soft-start) is typically 2.5V.

To improve efficiency across all loads, the majority of INTV<sub>CC</sub> current can be drawn from the BIAS pin (4.4V ≤ BIAS ≤ V<sub>IN</sub>) instead of the V<sub>IN</sub> pin. For SEPIC applications with V<sub>IN</sub> often greater than V<sub>OUT</sub>, the BIAS pin can be directly connected to V<sub>OUT</sub>. If the BIAS pin is connected to a supply other than V<sub>OUT</sub>, be sure to bypass the pin with a local ceramic capacitor.

### Programming Switching Frequency

The LT8365 uses a constant frequency PWM architecture that can be programmed to switch from 100kHz to 500kHz by using a resistor tied from the R<sub>T</sub> pin to ground. A table showing the necessary R<sub>T</sub> value for a desired switching frequency is in Table 1.

The R<sub>T</sub> resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{45.2k}{f_{OSC}^{1.009}}$$

where R<sub>T</sub> is in kΩ and f<sub>OSC</sub> is the desired switching frequency in kHz.

**Table 1. SW Frequency vs R<sub>T</sub> Value**

| f <sub>OSC</sub> (kHz) | R <sub>T</sub> (kΩ) |
|------------------------|---------------------|
| 100                    | 432                 |
| 200                    | 215                 |
| 300                    | 143                 |
| 400                    | 107                 |
| 450                    | 95.3                |
| 500                    | 84.5                |

### Synchronization and Mode Selection

To select low ripple Burst Mode operation, for high efficiency at light loads, tie the SYNC/MODE pin below 0.14V (this can be ground or a logic low output).

To synchronize the LT8365 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.7V (up to 6V). The LT8365 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8365 may be synchronized over a 100kHz to 500kHz range. The R<sub>T</sub> resistor should be chosen to set the LT8365 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R<sub>T</sub> should be selected for 500kHz.

For some applications it is desirable for the LT8365 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. Firstly, the clock stays awake at all times and all switching cycles are aligned to the clock. Secondly, the full switching frequency is maintained at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, float the SYNC pin.

To improve EMI/EMC, the LT8365 can provide spread spectrum frequency modulation (SSFM). This feature varies the clock with a triangle frequency modulation of 20%. For example, if the LT8365's frequency was programmed to switch at 500kHz, spread spectrum mode will modulate the oscillator between 500kHz and 600kHz. The 20% modulation will occur at a frequency: f<sub>OSC</sub>/256 where f<sub>OSC</sub> is the switching frequency programmed using the R<sub>T</sub> pin.

The LT8365 can also be configured to operate in pulse-skipping/SSFM mode by tying the SYNC/MODE pin above 1.7V. The LT8365 can also be configured for Burst Mode operation at light loads (for improved efficiency) and SSFM at heavy loads (for low EMI) by tying a 100k from the SYNC/MODE pin to GND.

## APPLICATIONS INFORMATION

### DUTY CYCLE CONSIDERATION

The LT8365 minimum on-time, minimum off-time and switching frequency ( $f_{OSC}$ ) define the allowable minimum and maximum duty cycles of the converter (see Minimum On-Time, Minimum Off-Time, and Switching Frequency in the Electrical Characteristics table).

Minimum Allowable Duty Cycle =

$$\text{Minimum On-Time}_{(MAX)} \cdot f_{OSC(MAX)}$$

Maximum Allowable Duty Cycle =

$$1 - \text{Minimum Off-Time}_{(MAX)} \cdot f_{OSC(MAX)}$$

The required switch duty cycle range for a Boost converter operating in continuous conduction mode (CCM) can be calculated as:

$$D_{MIN} = 1 - \frac{V_{IN(MAX)}}{V_{OUT} + V_D}$$

$$D_{MAX} = 1 - \frac{V_{IN(MIN)}}{V_{OUT} + V_D}$$

where  $V_D$  is the diode forward voltage drop. If the above duty cycle calculations for a given application violate the minimum and/or maximum allowed duty cycles for the LT8365, operation in discontinuous conduction mode (DCM) might provide a solution. For the same  $V_{IN}$  and  $V_{OUT}$  levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid sub-harmonic oscillations and the right half plane zero (RHPZ). While DCM provides these benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

### SETTING THE OUTPUT VOLTAGE

The output voltage is programmed with a resistor divider from the output to the FBX pin. Choose the resistor values for a positive output voltage according to:

$$R1 = R2 \cdot \left( \frac{V_{OUT}}{1.60V} - 1 \right)$$

Choose the resistor values for a negative output voltage according to:

$$R1 = R2 \cdot \left( \frac{|V_{OUT}|}{0.80V} - 1 \right)$$

The locations of R1 and R2 are shown in the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

Higher-value FBX divider resistors result in the lowest input quiescent current and highest light-load efficiency. FBX divider resistors R1 and R2 are usually in the range from 25k to 1M.

### SOFT-START

The LT8365 contains several features to limit peak switch currents and output voltage ( $V_{OUT}$ ) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since  $V_{OUT}$  is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT8365 addresses this mechanism with a programmable soft-start function. As shown in the Block Diagram, the soft-start function controls the ramp of the power switch current by controlling the ramp of  $V_C$  through Q1. This allows the output capacitor to be charged gradually toward its final value while limiting the start-up peak currents. Figure 3 shows the output voltage and supply current for the first page Typical Application. It can be seen that both the output voltage and supply current come up gradually.

### FAULT PROTECTION

An inductor overcurrent fault ( $> 3A$ ) and/or  $INTV_{CC}$  undervoltage ( $INTV_{CC} < 2.5V$ ) and/or thermal lockout ( $T_J > 170^\circ C$ ) will immediately prevent switching, will reset the SS pin and will pull down  $V_C$ . Once all faults are removed, the LT8365 will soft-start  $V_C$  and hence inductor peak current.

## APPLICATIONS INFORMATION

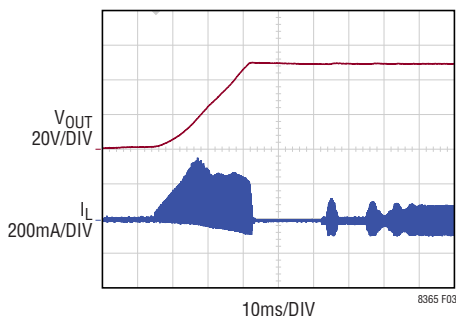


Figure 3. Soft-Start Waveforms

### FREQUENCY FOLDBACK

During start-up or fault conditions in which  $V_{OUT}$  is very low, extremely small duty cycles may be required to maintain control of inductor peak current. The minimum on-time limitation of the power switch might prevent these low duty cycles from being achievable. In this scenario inductor current rise will exceed inductor current fall during each cycle, causing inductor current to “walk up” beyond the switch current limit. The LT8365 provides protection from this by folding back switching frequency whenever FBX or SS pins are close to GND (low  $V_{OUT}$  levels or start-up). This frequency foldback provides a larger switch-off time, allowing inductor current to fall enough each cycle (see Normalized Switching Frequency vs FBX Voltage in the Typical Performance Characteristics section).

### THERMAL LOCKOUT

If the LT8365 die temperature reaches 170°C (typical), the part will stop switching and go into thermal lockout. When the die temperature has dropped by 5°C (nominal), the part will resume switching with a soft-started inductor peak current.

### COMPENSATION

Loop compensation determines the stability and transient performance. The LT8365 uses current mode control to regulate the output which simplifies loop compensation. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LT8365, a series resistor-capacitor

network is usually connected from the  $V_C$  pin to GND. The Block Diagram shows the typical  $V_C$  compensation network. For most applications, the capacitor should be in the range of 100pF to 10nF, and the resistor should be in the range of 5k to 100k. A small capacitor is often connected in parallel with the RC compensation network to attenuate the  $V_C$  voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 2.2pF to 22pF. A practical approach to designing the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. Application Note 76 is a good reference.

### THERMAL CONSIDERATIONS

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8365. Both packages have an exposed pad underneath the IC which is the best path for heat out of the package. The exposed pad should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8365. The ground plane should be connected to large copper layers to spread heat dissipated by the LT8365. Power dissipation within the LT8365 ( $P_{DISS\_LT8365}$ ) can be estimated by subtracting the inductor and Schottky diode power losses from the total power losses calculated in an efficiency measurement. The junction temperature of LT8365 can then be estimated by:

$$T_J(LT8365) = T_A + \theta_{JA} \cdot P_{DISS\_LT8365}$$

### APPLICATION CIRCUITS

The LT8365 can be configured for different topologies. The first topology to be analyzed will be the boost converter, followed by the SEPIC and inverting converters.

#### Boost Converter: Switch Duty Cycle

The LT8365 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are



## APPLICATIONS INFORMATION

not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage ( $V_{OUT}$ ) and the input voltage ( $V_{IN}$ ). The maximum duty cycle ( $D_{MAX}$ ) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies, higher switching currents, and lower available output power.

### Boost Converter: Maximum Output Current Capability and Inductor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)(AVG)} = I_{O(MAX)} \cdot \frac{1}{1-D_{MAX}} \cdot \frac{1}{\eta}$$

where  $\eta$  ( $< 1.0$ ) is the converter efficiency.

Due to the current limit of its internal power switch, the LT8365 should be used in a boost converter whose maximum output current ( $I_{O(MAX)}$ ) is:

$$I_{O(MAX)} \leq \frac{V_{IN(MIN)}}{V_{OUT}} \cdot (1.5A - 0.5 \cdot \Delta I_{SW}) \cdot \eta$$

Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current  $\Delta I_{SW}$ .

The inductor ripple current  $\Delta I_{SW}$  has a direct effect on the choice of the inductor value and the converter's maximum

output current capability. Choosing smaller values of  $\Delta I_{SW}$  increases output current capability, but requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of  $\Delta I_{SW}$  provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses, and reduces output current capability. It is recommended to choose a  $\Delta I_{SW}$  of approximately 0.60A.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \cdot f_{OSC}} \cdot D_{MAX}$$

The peak inductor current is the switch current limit (maximum 2.7A), and the RMS inductor current is approximately equal to  $I_{L(MAX)(AVG)}$ .

Choose an inductor that can handle at least 2.7A without saturating, and ensure that the inductor has a low DCR (copper-wire resistance) to minimize  $I^2R$  power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one-half of the total switch current. For better efficiency, use similar valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers (see Table 2). Choose a core material that has low losses at the programmed switching frequency, such as a ferrite core. The final value chosen for the inductor should not allow peak inductor currents to exceed 1.5A in steady state at maximum load. Due to tolerances, be sure to account for minimum possible inductance value, switching frequency and converter efficiency.

For inductor current operation in CCM and duty cycles above 50%, the LT8365's internal slope compensation prevents sub-harmonic oscillations provided the inductor value exceeds a minimum value given by:

$$L > \frac{V_{IN}}{(-5 \cdot D^2 + 10 \cdot D - 1) \cdot (f_{OSC})} \cdot \frac{(2 \cdot D - 1)}{(1-D)}$$

Lower L values are allowed if the inductor current operates in DCM or duty cycle operation is below 50%.

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**Table 2. Inductor Manufacturers**

|           |                |                   |
|-----------|----------------|-------------------|
| Sumida    | (847) 956-0666 | www.sumida.com    |
| TDK       | (847) 803-6100 | www.tdk.com       |
| Murata    | (714) 852-2001 | www.murata.com    |
| Coilcraft | (847) 639-6400 | www.coilcraft.com |
| Würth     | (605) 886-4385 | www.we-online.com |

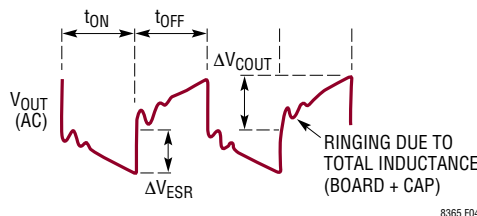
### BOOST CONVERTER: INPUT CAPACITOR SELECTION

Bypass the input of the LT8365 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the  $V_{IN}$  and GND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7 $\mu$ F to 10 $\mu$ F ceramic capacitor is adequate to bypass the LT8365 and will easily handle the ripple current. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8365. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8365 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8365's voltage rating. This situation is easily avoided (see Application Note 88).

### BOOST CONVERTER: OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they are small and have extremely low ESR. Use X5R or X7R types. This choice will provide low output ripple and good transient response. A 4.7 $\mu$ F to 47 $\mu$ F output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1 $\mu$ F or 2.2 $\mu$ F output capacitor. Solid tantalum or OS-CON capacitor can be used, but they will occupy more board area than a ceramic and will have a higher ESR. Always use a capacitor with a sufficient voltage rating. For High-Voltage DCM applications, smaller output capacitor values may be sufficient.



**Figure 4. The Output Ripple Waveform of a Boost Converter**

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 4.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step  $\Delta V_{ESR}$  and the charging/discharging  $\Delta V_{COUT}$ . For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between  $\Delta V_{ESR}$  and  $\Delta V_{COUT}$ . This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \cdot V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \cdot V_{OUT} \cdot f_{OSC}}$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 4. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \geq I_{O(MAX)} \cdot \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

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Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

### CERAMIC CAPACITORS

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8365 due to their piezoelectric nature. When in Burst Mode operation, the LT8365's switching frequency depends on the load current, and at very light loads the LT8365 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8365 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

**Table 3. Ceramic Capacitor Manufacturers**

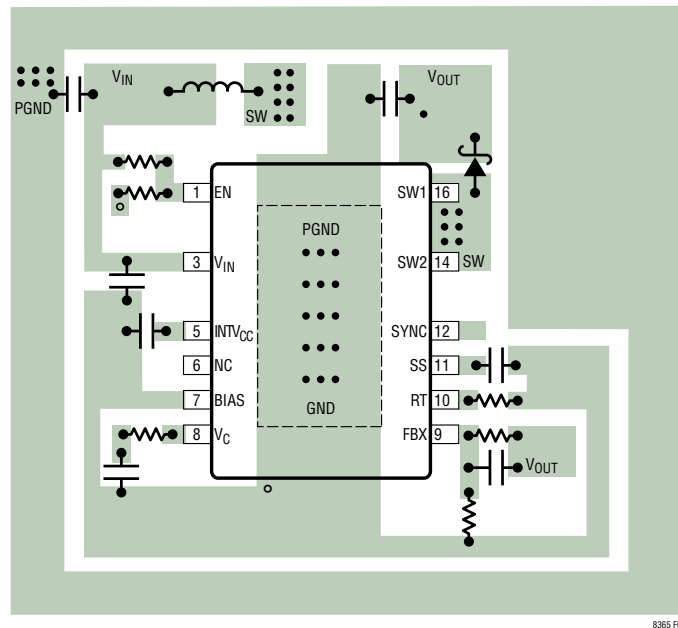
|             |                |                 |
|-------------|----------------|-----------------|
| Taiyo Yuden | (408) 573-4150 | www.t-yuden.com |
| AVX         | (803) 448-9411 | www.avxcorp.com |
| Murata      | (714) 852-2001 | www.murata.com  |

### BOOST CONVERTER: DIODE SELECTION

A Schottky diode is recommended for use with the LT8365. Low leakage Schottky diodes are necessary when low quiescent current is desired at low loads. The diode leakage appears as an equivalent load at the output and should be minimized. Choose Schottky diodes with sufficient reverse voltage ratings for the target applications.

**Table 4. Recommended Schottky Diodes**

| PART NUMBER   | AVERAGE FORWARD CURRENT (A) | REVERSE VOLTAGE (V) | REVERSE CURRENT (μA) | MANUFACTURER |
|---------------|-----------------------------|---------------------|----------------------|--------------|
| DFLS1150      | 1                           | 150                 | 2                    | Diodes, Inc. |
| RB068L150TE25 | 2                           | 150                 | 3                    | ROHM         |
| DFLS2100      | 2                           | 100                 | 1                    | Diodes, Inc. |



**Figure 5. Suggested Boost Converter Layout**



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### BOOST CONVERTER: LAYOUT HINTS

The high speed operation of the LT8365 demands careful attention to board layout. Careless layout will result in performance degradation. Figure 5 shows the recommended component placement for a boost converter. Note the vias under the exposed pad. These should connect to a local ground plane for better thermal performance.

### SEPIC CONVERTER APPLICATIONS

The LT8365 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 6. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1 - D}$$

in continuous conduction mode (CCM).

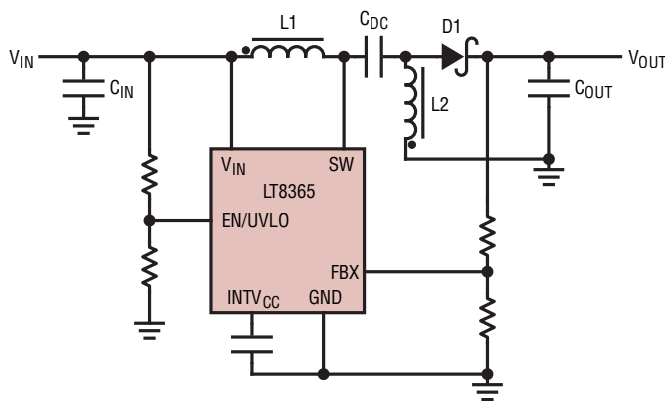


Figure 6. LT8365 Configured in a SEPIC Topology

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

### SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage ( $V_{OUT}$ ), the input voltage ( $V_{IN}$ ) and the diode forward voltage ( $V_D$ ).

The maximum duty cycle ( $D_{MAX}$ ) occurs when the converter operates at the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D}$$

Conversely, the minimum duty cycle ( $D_{MIN}$ ) occurs when the converter operates at the maximum input voltage:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_{OUT} + V_D}$$

Be sure to check that  $D_{MAX}$  and  $D_{MIN}$  obey:

$$D_{MAX} < 1 - \text{Minimum Off-Time}_{(MAX)} \cdot f_{OSC(MAX)}$$

and

$$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \cdot f_{OSC(MAX)}$$

where Minimum Off-Time, Minimum On-Time and  $f_{OSC}$  are specified in the Electrical Characteristics table.

### SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in Figure 6, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)(AVG)} = I_{IN(MAX)(AVG)} = I_{O(MAX)} \cdot \frac{D_{MAX}}{1 - D_{MAX}}$$

$$I_{L2(MAX)(AVG)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to  $I_{L1} + I_{L2}$  when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)(AVG)} = I_{L1(MAX)(AVG)} + I_{L2(MAX)(AVG)} \\ = I_{O(MAX)} \cdot \frac{1}{1 - D_{MAX}}$$

## APPLICATIONS INFORMATION

and the peak switch current is:

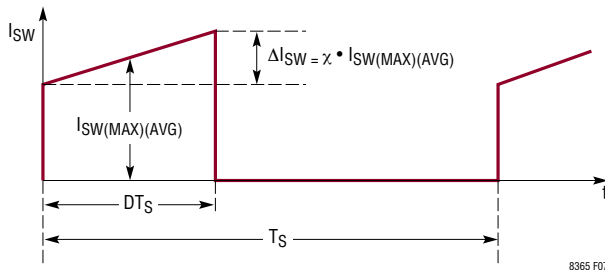
$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \cdot I_{O(MAX)} \cdot \frac{1}{1 - D_{MAX}}$$

The variable  $\chi$  in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to  $I_{SW(MAX)(AVG)}$ , as shown in Figure 7. Then, the switch ripple current  $\Delta I_{SW}$  can be calculated by:

$$\Delta I_{SW} = \chi \cdot I_{SW(MAX)(AVG)}$$

The inductor ripple currents  $\Delta I_{L1}$  and  $\Delta I_{L2}$  are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \cdot \Delta I_{SW}$$



**Figure 7. The Switch Current Waveform of the SEPIC Converter**

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of  $\Delta I_L$  requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of  $\Delta I_L$  allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that  $\chi$  falls in the range of 0.5 to 0.8.

Due to the current limit of its internal power switch, the LT8365 should be used in a SEPIC converter whose maximum output current ( $I_{O(MAX)}$ ) is:

$$I_{O(MAX)} < (1 - D_{MAX}) \cdot (1.5A - 0.5 \cdot \Delta I_{SW}) \cdot \eta$$

where  $\eta$  ( $< 1.0$ ) is the converter efficiency. Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current  $\Delta I_{SW}$ .

Given an operating input voltage range, and having chosen ripple current in the inductor, the inductor value ( $L1$  and  $L2$  are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \cdot \Delta I_{SW} \cdot f_{OSC}} \cdot D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 2.2 $\mu$ H to 100 $\mu$ H.

By making  $L1 = L2$ , and winding them on the same core, the value of inductance in the preceding equation is replaced by  $2L$ , due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \cdot f_{OSC}} \cdot D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \cdot \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \cdot \Delta I_{L2}$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

Similar to Boost converters, the SEPIC converter also needs slope compensation to prevent subharmonic oscillations while operating in CCM. The equation presented in the Boost Converter section defines the minimum inductance value to avoid sub-harmonic oscillations when coupled inductors are used. For uncoupled inductors, the minimum inductance requirement is doubled.

### SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current.

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It is recommended that the peak repetitive reverse voltage rating  $V_{RRM}$  is higher than  $V_{OUT} + V_{IN(MAX)}$  by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \cdot V_D$$

where  $V_D$  is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \cdot R_{\theta JA}$$

The  $R_{\theta JA}$  used in this equation normally includes the  $R_{\theta JC}$  for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure.  $T_J$  must not exceed the diode maximum junction temperature rating.

### SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter.

### SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor ( $C_{DC}$ , as shown in Figure 6) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

$C_{DC}$  has nearly a rectangular current waveform. During the switch off-time, the current through  $C_{DC}$  is  $I_{IN}$ , while approximately  $-I_O$  flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \cdot \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for  $C_{DC}$ .

### INVERTING CONVERTER APPLICATIONS

The LT8365 can be configured as a dual-inductor inverting topology, as shown in Figure 8. The  $V_{OUT}$  to  $V_{IN}$  ratio is:

$$\frac{|V_{OUT}| + V_D}{V_{IN}} = \frac{D}{1 - D}$$

in continuous conduction mode (CCM).

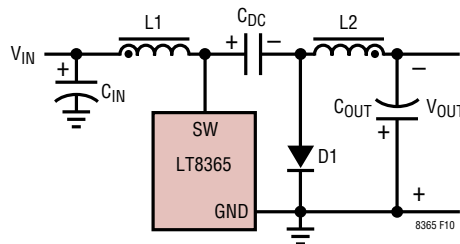


Figure 8. A Simplified Inverting Converter

### Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage ( $V_{OUT}$ ) and the input voltage ( $V_{IN}$ ).

The maximum duty cycle ( $D_{MAX}$ ) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MIN)}}$$

Conversely, the minimum duty cycle ( $D_{MIN}$ ) occurs when the converter operates at the maximum input voltage :

$$D_{MIN} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MAX)}}$$

Be sure to check that  $D_{MAX}$  and  $D_{MIN}$  obey :

$$D_{MAX} < 1 - \text{Minimum Off-Time}_{(MAX)} \cdot f_{OSC(MAX)}$$

and

$$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \cdot f_{OSC(MAX)}$$

where Minimum Off-Time, Minimum On-Time and  $f_{OSC}$  are specified in the Electrical Characteristics table.

### Inverting Converter: Inductor, Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC Converter sections.

## APPLICATIONS INFORMATION

### Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \cdot \left( ESR_{COUT} + \frac{1}{8 \cdot f_{OSC} \cdot C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \cdot \Delta I_{L2}$$

### Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor ( $C_{DC}$ , as shown in Figure 8) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} + |V_{OUT}|$$

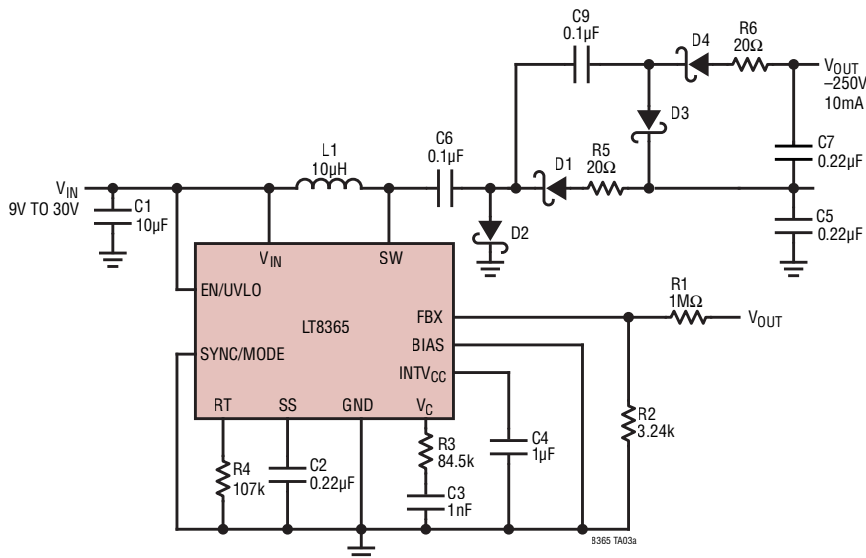
$C_{DC}$  has nearly a rectangular current waveform. During the switch off-time, the current through  $C_{DC}$  is  $I_{IN}$ , while approximately  $-I_O$  flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \cdot \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for  $C_{DC}$ .

## TYPICAL APPLICATIONS

### 400kHz, 9V to 30V Input, -250V Output Inverting Converter



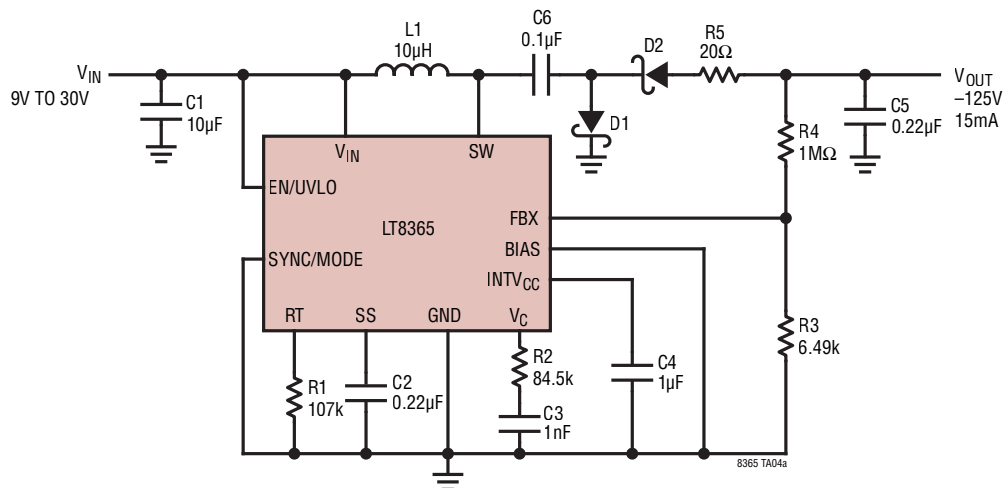
D1, D2, D3, D4: DIODES INC. DFSL1150  
L1: WURTH ELEKTRONIK WE-PD 74437324100  
C6, C9: 12062C104KAT2A  
C5, C7: CGJ5L3X7T2D224K160AA



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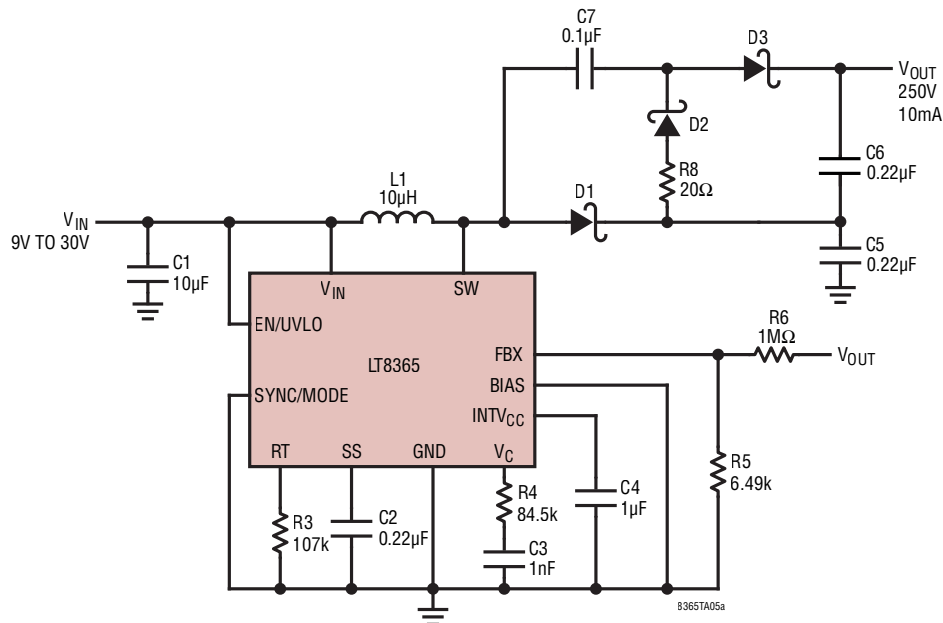
# TYPICAL APPLICATIONS

## 400kHz, 9V to 30V Input, -125V Output Inverting Converter



D1, D2: DIODES INC. DFLS1150  
L1: WURTH ELEKTRONIK WE-PD 74437324100  
C6: 12062C104KAT2A  
C5, C7: CGJ5L3X7T2D224K160AA

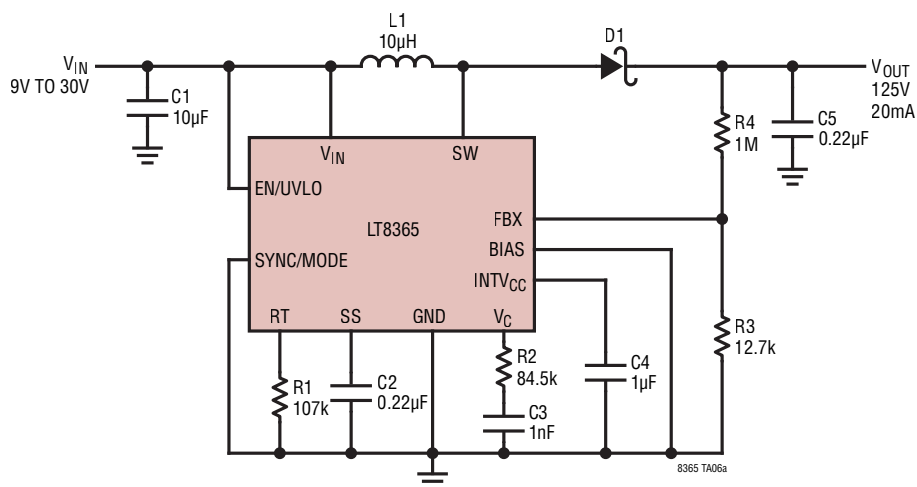
## 400kHz, 9V to 30V Input, 250V Output Boost Converter



D1, D2, D3: DIODES INC. DFLS1150  
L1: WURTH ELEKTRONIK WE-PD 74437324100  
C7: 12062C104KAT2A  
C5, C6: CGJ5L3X7T2D224K160AA

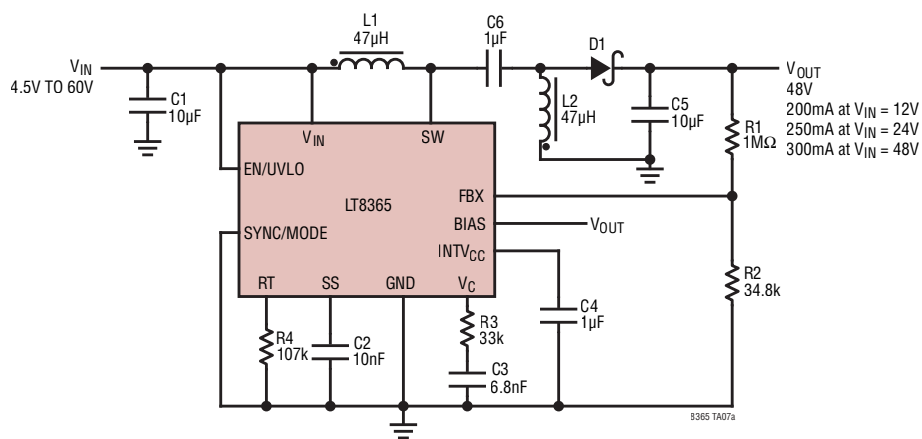
## TYPICAL APPLICATIONS

### 400kHz, 9V to 30V Input, 125V Output Boost Converter



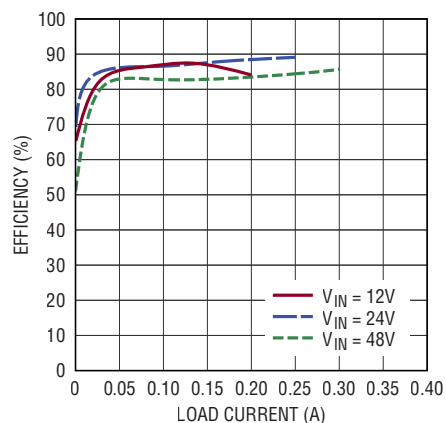
D1: DIODES INC. DFSL1150  
L1: WURTH ELEKTRONIK WE-PD 74437324100  
C5: CGJ5L3X7T2D224K160AA

### 400kHz, 4.5V to 60V Input, 48V Output SEPIC Converter



D1: DIODES INC. DFSL2100  
L1: WURTH ELEKTRONIK WE-DD 744873470  
C5: MURATA GRM32ER71H106KA12L

### Efficiency

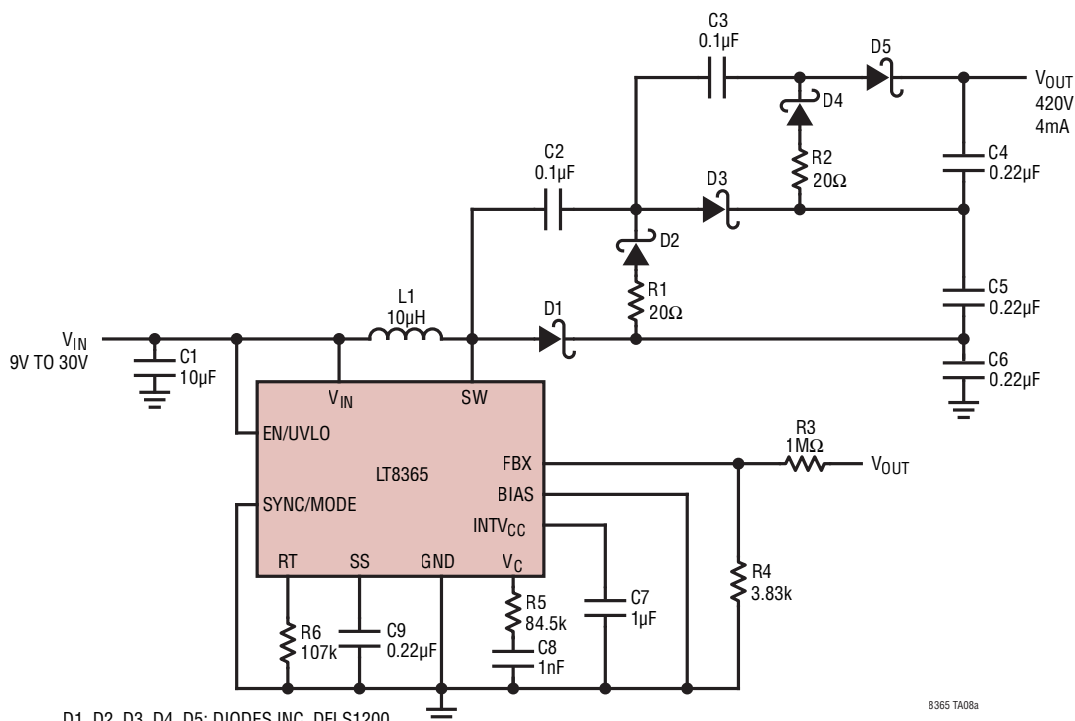


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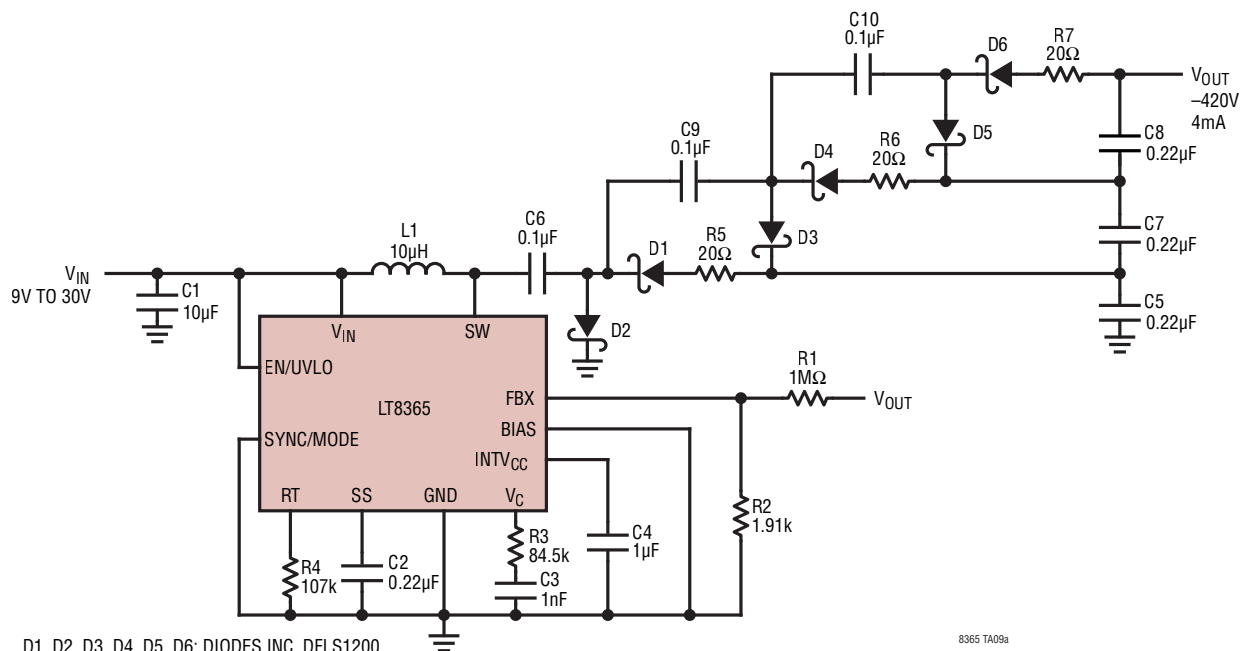


## TYPICAL APPLICATIONS

## 400kHz, 9V to 30V Input, 420V Output Boost Converter



## 400kHz, 9V to 30V Input, -420V Output Boost Converter

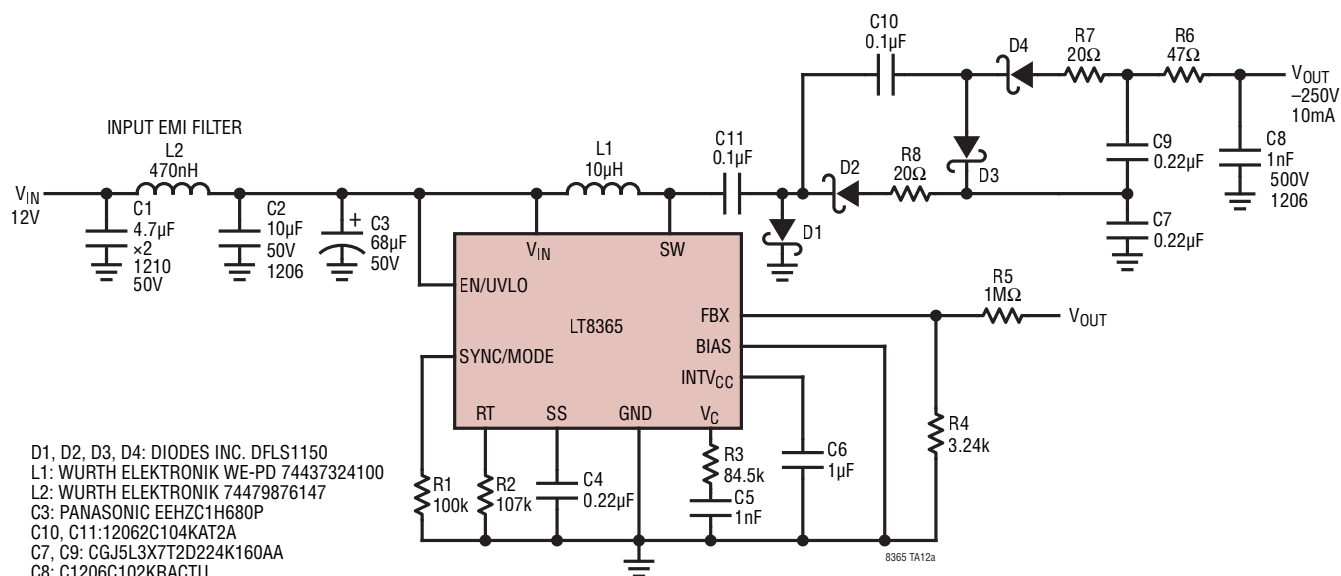




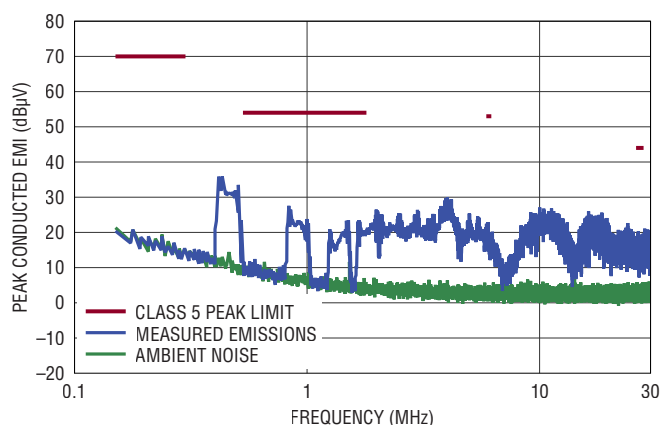
D1, D2, D3, D4: DIODES INC. DFLS1150  
L1: WURTH ELEKTRONIK WE-PD 74437324100  
L2: WURTH ELEKTRONIK 74479876147  
C2, C3, C9: 12062C104KAT2A  
C4, C5: CGJ5L3X7T2D224K160AA

8365 TA11a

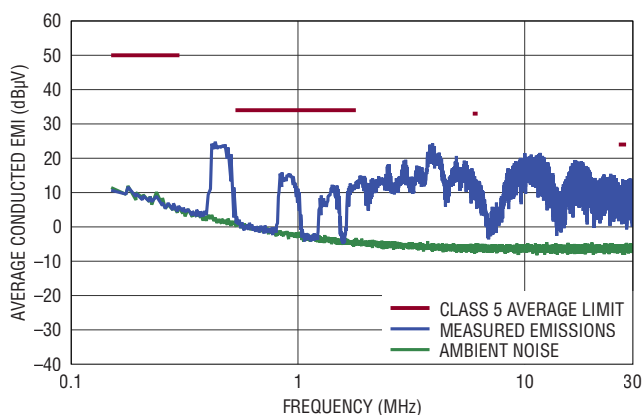
## TYPICAL APPLICATIONS

Low  $I_Q$ , Low EMI, 400kHz, -250V Output Inverting Converter with SSFM

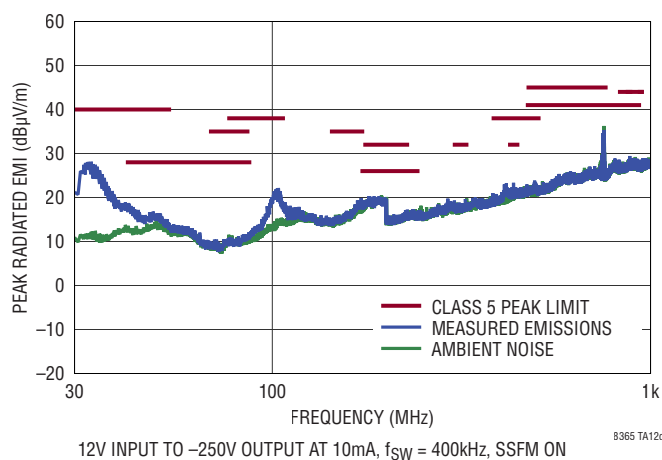
Conducted EMI Performance (CISPR25 Class 5 Peak)



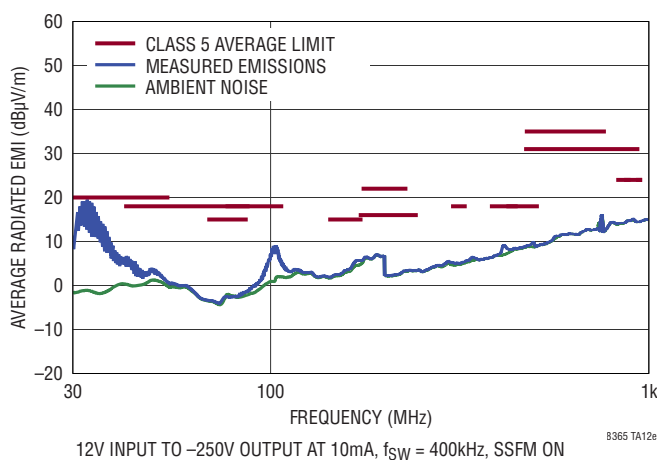
Conducted EMI Performance (CISPR25 Class 5 Average)



Radiated EMI Performance (CISPR25 Class 5 Peak)

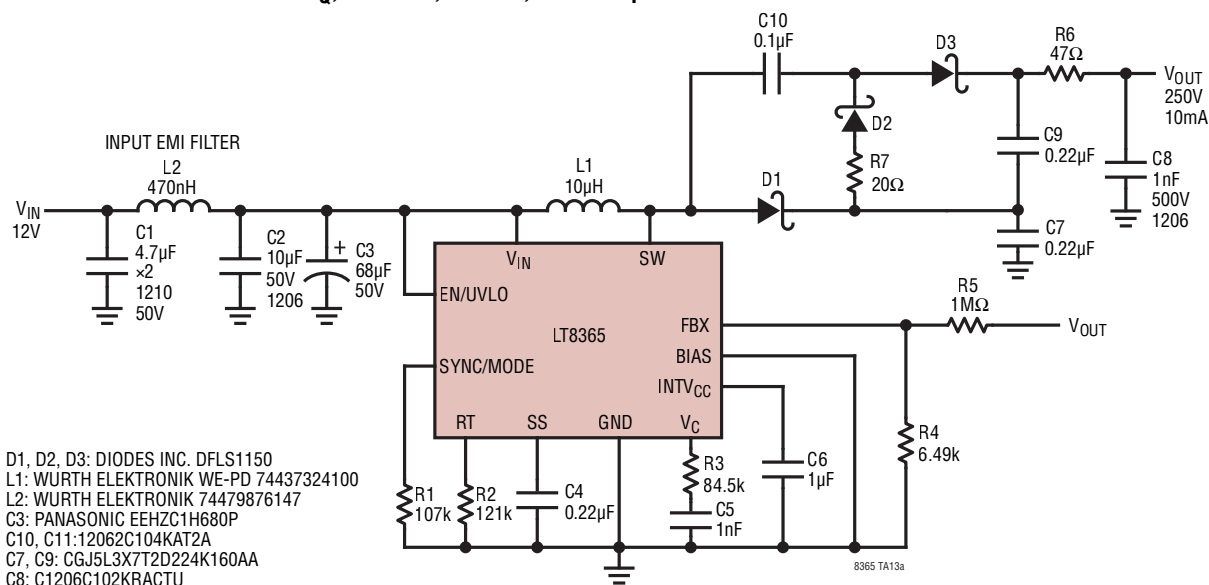


Radiated EMI Performance (CISPR25 Class 5 Average)

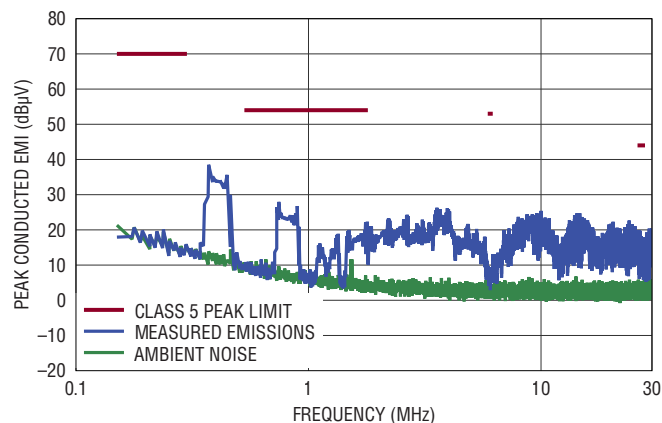


# TYPICAL APPLICATIONS

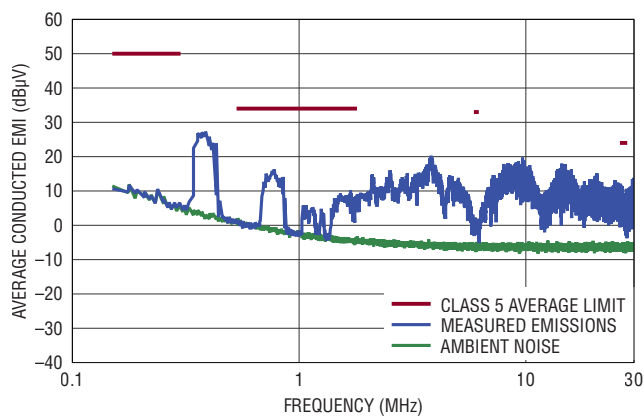
## Low $I_Q$ , Low EMI, 400kHz, 250V Output Boost Converter with SSFM



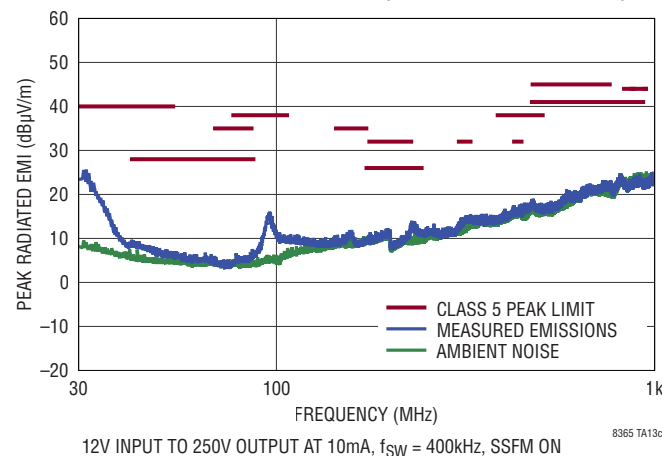
Conducted EMI Performance (CISPR25 Class 5 Peak)



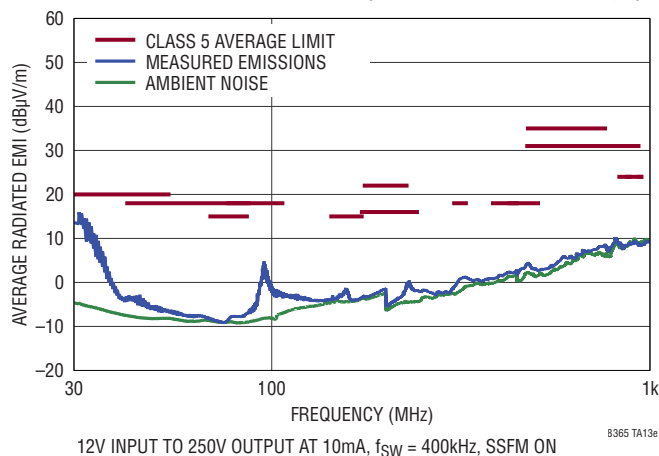
Conducted EMI Performance (CISPR25 Class 5 Average)



Radiated EMI Performance (CISPR25 Class 5 Peak)



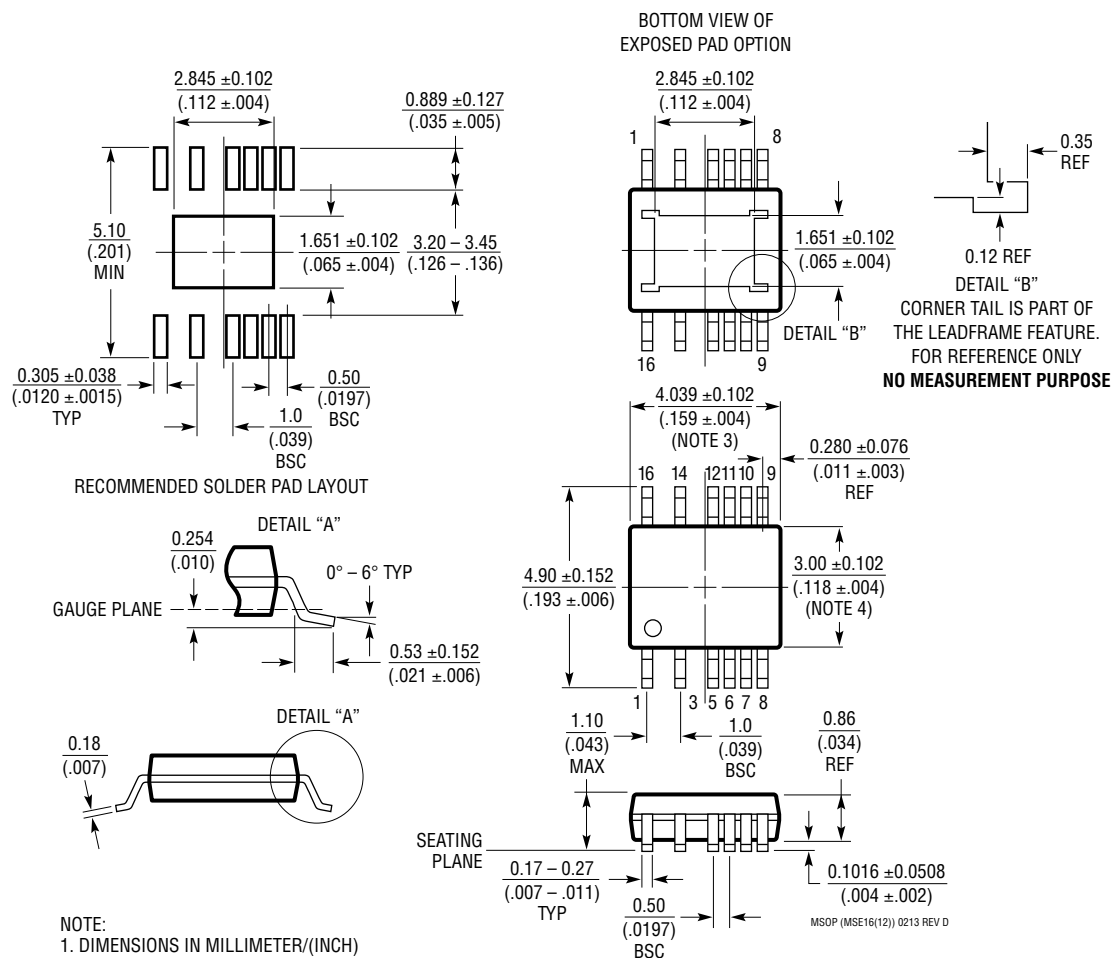
Radiated EMI Performance (CISPR25 Class 5 Average)



# PACKAGE DESCRIPTION

## MSE Package Variation: MSE16 (12) 16-Lead Plastic MSOP with 4 Pins Removed Exposed Die Pad

(Reference LTC DWG # 05-08-1871 Rev D)



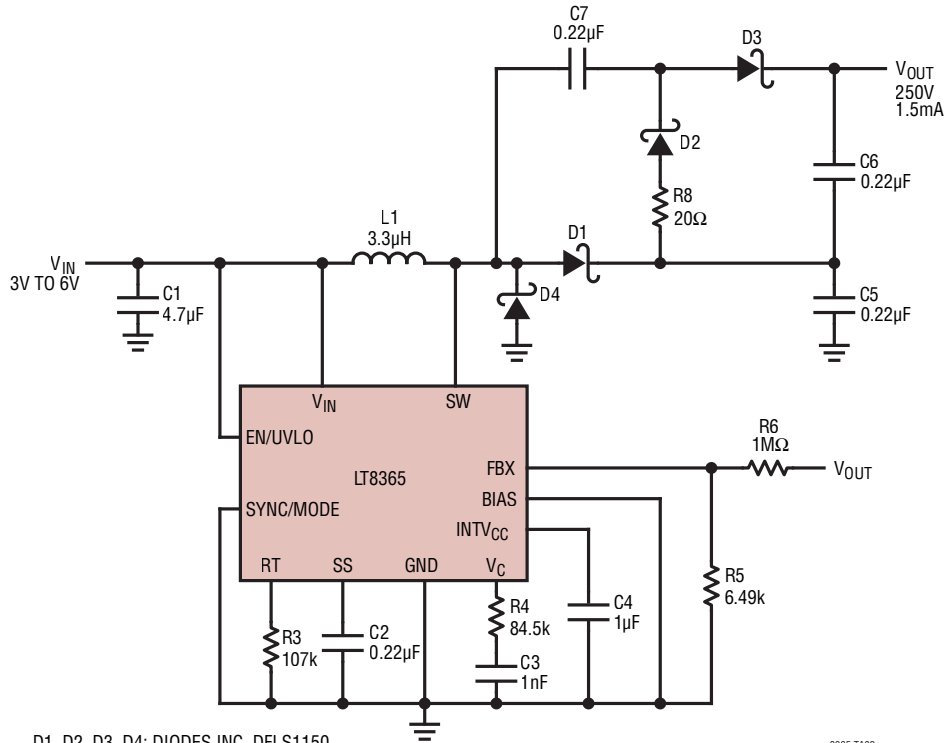
## REVISION HISTORY

| REV | DATE  | DESCRIPTION                                                | PAGE NUMBER |
|-----|-------|------------------------------------------------------------|-------------|
| A   | 09/21 | Updated to AEC-Q100 Qualified for Automotive Applications. | 1           |



## TYPICAL APPLICATION

### 400kHz, 3V to 6V Input, 250V Output Boost Converter



D1, D2, D3, D4: DIODES INC. DFSL1150  
L1: WURTH ELEKTRONIK WE-PD 74437324033  
C5, C6, C7: CGJ5L3X7T2D224K160AA

8365 TA02a

## RELATED PARTS

| PART NUMBER            | DESCRIPTION                                                                      | COMMENTS                                                                                                                                                            |
|------------------------|----------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">LT8300</a> | 100V <sub>IN</sub> Micropower Isolated Flyback Converter with 150V/260mA Switch  | V <sub>IN</sub> = 6V to 100V, Low I <sub>Q</sub> Monolithic No-Opto Flyback, 5-Lead TSOT-23                                                                         |
| <a href="#">LT8330</a> | 60V, 1A, Low I <sub>Q</sub> Boost/SEPIC/Inverting 2MHz Converter                 | V <sub>IN</sub> = 3V to 40V, V <sub>OUT(MAX)</sub> = 60V, I <sub>Q</sub> = 6µA (Burst Mode Operation), 6-Lead TSOT-23, 3mm × 2mm DFN Packages                       |
| <a href="#">LT8331</a> | Low I <sub>Q</sub> Boost/SEPIC/Flyback/Inverting Converter with 140V/0.5A Switch | V <sub>IN</sub> = 4.5V to 100V, V <sub>OUT(MAX)</sub> = 140V, I <sub>Q</sub> = 6µA (Burst Mode Operation), MSOP-16(12)E                                             |
| <a href="#">LT8361</a> | 100V, 2A, Low I <sub>Q</sub> Boost/SEPIC/Inverting Converter                     | V <sub>IN</sub> = 2.8V to 60V, V <sub>OUT(MAX)</sub> = 100V, I <sub>Q</sub> = 9µA (Burst Mode Operation), MSOP-16(12)E                                              |
| <a href="#">LT8362</a> | 60V, 2A, Low I <sub>Q</sub> Boost/SEPIC/Inverting Converter                      | V <sub>IN</sub> = 2.8V to 60V, V <sub>OUT(MAX)</sub> = 60V, I <sub>Q</sub> = 9µA (Burst Mode Operation), MSOP-16(12)E, 3mm × 3mm DFN-10 Packages                    |
| <a href="#">LT8364</a> | 60V, 4A, Low I <sub>Q</sub> Boost/SEPIC/Inverting Converter                      | V <sub>IN</sub> = 2.8V to 60V, V <sub>OUT(MAX)</sub> = 60V, I <sub>Q</sub> = 9µA (Burst Mode Operation), MSOP-16(12)E, 4mm × 3mm DFN-12 Packages                    |
| <a href="#">LT8494</a> | 70V, 2A Boost/SEPIC 1.5MHz High Efficiency Step-Up DC/DC Converter               | V <sub>IN</sub> = 1V to 60V (2.5V to 32V Start-Up), V <sub>OUT(MAX)</sub> = 70V, I <sub>Q</sub> = 3µA (Burst Mode Operation), I <sub>SD</sub> = <1µA, 20-Lead TSSOP |
| <a href="#">LT8580</a> | 1A (I <sub>SW</sub> ), 65V, 1.5MHz, High Efficiency Step-Up DC/DC Converter      | V <sub>IN</sub> : 2.55V to 40V, V <sub>OUT(MAX)</sub> = 65V, I <sub>Q</sub> = 1.2mA, I <sub>SD</sub> = <1µA, 3mm × 3mm DFN-8, MSOP-8E                               |
| <a href="#">LT3958</a> | 80V, 3.3A Boost/SEPIC/Inverting Flyback Converter                                | V <sub>IN</sub> : 5V to 80V, V <sub>OUT(MAX)</sub> = 83V, I <sub>Q</sub> = 1.6mA, 5mm × 6mm QFN-36 Package                                                          |