3-Output LVPECL Networking Clock Generator

Features

- Three differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 125MHz, 156.25MHz, 312.5MHz, 625MHz
- RMS phase jitter @ 156.25MHz, using a 31.25MHz or 26.041666MHz crystal (12kHz – 20MHz): 0.3ps (typical)
- Full 3.3V or 2.5V supply modes
- Commercial and industrial ambient operating temperature
- Available in lead-free package: 24-TSSOP

Description

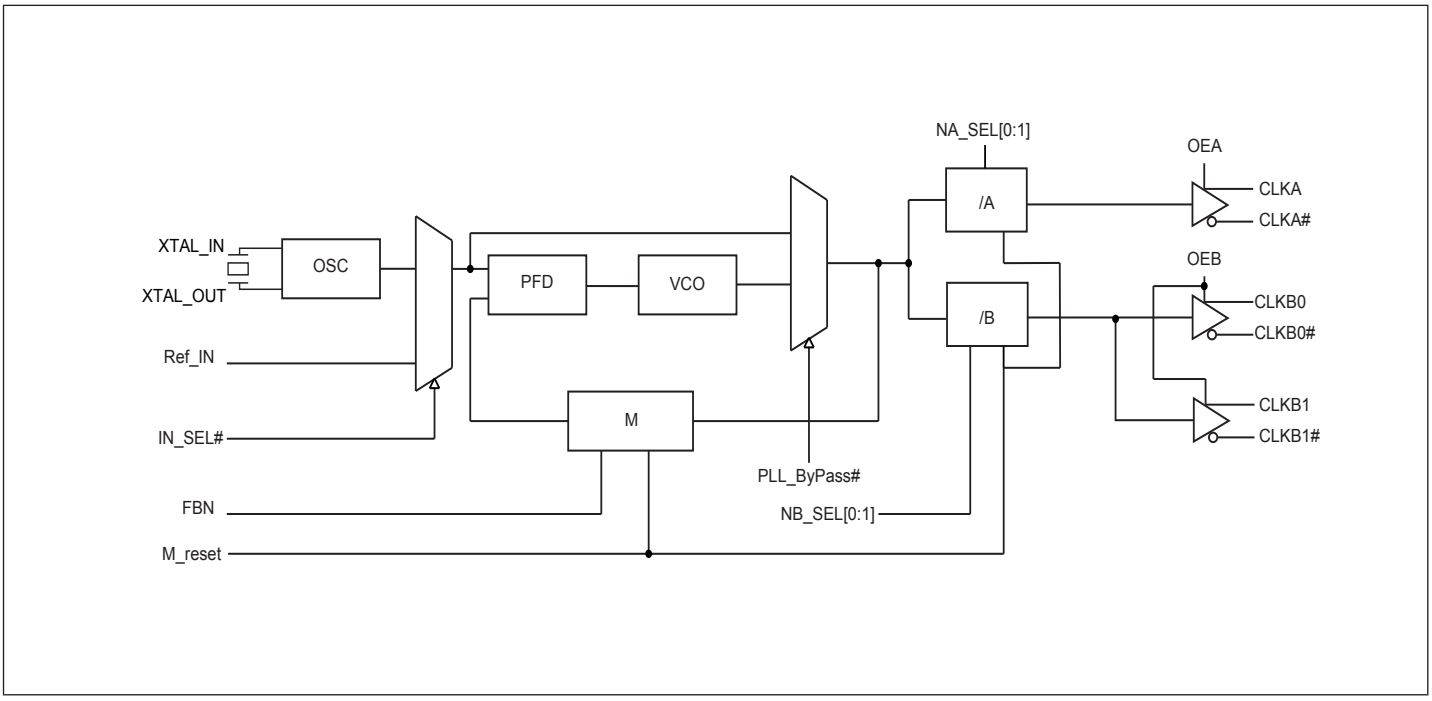
The PI6LC48P03 is a 3-output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 31.25MHz or 26.041666MHz crystal, the most popular Ethernet frequencies can be generated based on the settings of 4 frequency select pins.

The PI6LC48P03 uses Pericom's proprietary low phase noise PLL technology to achieve ultra low phase jitter, so it is ideal for Ethernet interface in all kind of systems.

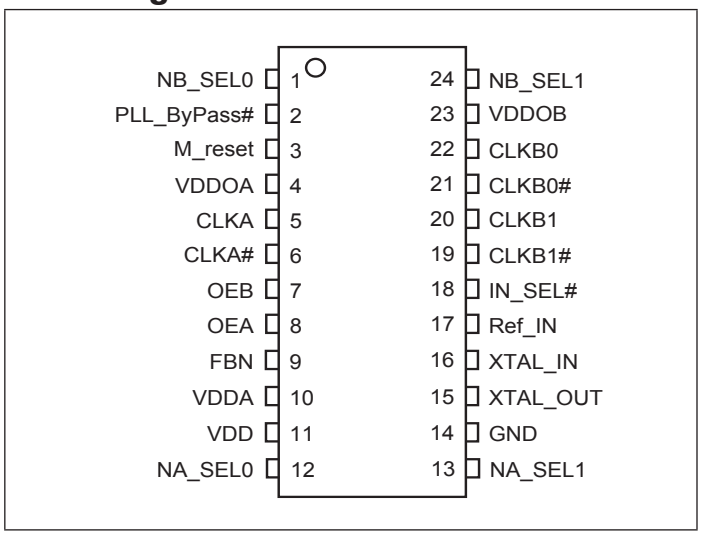
Applications

- Networking systems

Block Diagram



Pin Configuration



Pinout Table

Pin No.	Pin Name	I/O Type		Description
1	NB_SEL0	Input	Pull-down	Bank B Output Divider Select
2	PLL_ByPass#	Input	Pull-up	Active Low PLL Bypass
3	M_reset	Input	Pull-down	Master Reset. When HIGH, CLKx goes to “low” and CLKx# goes to “high”; When LOW outputs are enabled.
4	VDDOA	Power		Bank A Output Power Supply
5, 6	CLKA, CLKA#	Output		Bank A LVPECL Output Clock
7	OEB	Input	Pull-up	Bank B Output Enable. When LOW, output is differential low.
8	OEA	Input	Pull-up	Bank A Output Enable. When LOW, output is differential low.
9	FBN	Input	Pull-down	Feedback Divider Select
10	VDDA	Power		Analog Power Supply
11	VDD	Power		Core Power Supply
12	NA_SEL0	Input	Pull-up	Bank A Output Divider Select
13	NA_SEL1	Input	Pull-down	Bank A Output Divider Select
14	GND	Ground		Ground
15, 16	XTAL_OUT, XTAL_IN	Crystal		Crystal Input and Output
17	Ref_IN	Input	Pull-down	CMOS Reference Clock Input
18	IN_SEL#	Input	Pull-up	When HIGH, Crystal is selected; When LOW, reference input is selected.
19, 20	CLKB1#, CLKB1	Output		Bank B LVPECL Output Clock 1
21, 22	CLKB0#, CLKB0	Output		Bank B LVPECL Output Clock 0
23	VDDOB	Power		Bank B Output Power Supply
24	NB_SEL1	Input	Pull-up	Bank B Output Divider Select

Output Frequency Selection Table

Xtal Frequency (MHz)	NA_SEL1 / NB_ SEL1	NA_SEL0 / NB_ SEL0	FBN	Output Frequency (MHz)
31.25	0	0	0	625
31.25	0	1	0	312.5 (Bank A Default)
31.25	1	0	0	156.25 (Bank B Default)
31.25	1	1	0	125
26.041666	0	0	1	625
26.041666	0	1	1	312.5 (Bank A Default)
26.041666	1	0	1	156.25 (Bank B Default)
26.041666	1	1	1	125

Typical Crystal Requirement

Parameter		Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency	FBN = 0	28	31.25	35	MHz
	FBN = 1	23.33	26.04166	29.167	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Recomended Crystal Specification

Pericom recommends:

a) FY3120001, SMD 5x3.2(4P), 31.25MHz, CL=18pF, +/-20ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

b) FL2600155, SMD 3.2x2.5(4P), 26.041666MHz, CL18pF, +/-20ppm
https://www.pericom.com/assets/Datasheets/FL.pdf

Maximum Ratings (Over operating free-air temperature range)

Storage Temperature..... -65°C to+155°C
Ambient Temperature with Power Applied.....-40°C to+85°C
3.3V Analog Supply Voltage.....-0.5 to +3.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Power Supply DC Characterisitcs, (T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO_A} V_{DDO_B}	Output Supply Voltage		3.135	3.3	3.465	V
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO_A} V_{DDO_B}	Output Supply Voltage		2.375	2.5	2.625	V
I_{GND}	Power Supply Current				132	mA
I_{DDA}	Analog Supply Current				30	mA

LVCMOS/LVTTL DC Characterisitcs, (T_A = -40 to 85°C)

Symbol	Parameter		Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3 V +/- 5%	2		V_{DD}+ 0.3	V
			V_{DD} = 2.5 V +/- 5%	1.7		V_{DD}+ 0.3	
V_{IL}	Input Low Voltage		V_{DD} = 3.3 V +/- 5%	-0.3		0.8	V
			V_{DD} = 2.5 V +/- 5%	-0.3		0.7	V
I_{IH}	Input High Current	Ref_IN, FBN, M_reset, NA_SEL1, NB_SEL0	V_{DD} = V_{IN} = 3.465V			100	µA
		OEA, OEB, PLL_Bypass#, IN_SEL#, NB_SEL1, NA_SEL0	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	Ref_IN, FBN, M_reset, NA_SEL1, NB_SEL0	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OEA, OEB, PLL_Bypass#, IN_SEL#, NB_SEL1, NA_SEL0	V_{DD} = 3.465V, V_{IN} = 0V	-100			µA

LVPECL DC Characterisitcs, (T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage(1)	V_{DD} = 3.3V	1.9		2.4	V
		V_{DD} = 2.5V	1.1		1.6	
V_{OL}	Output Low Voltage(1)	V_{DD} = 3.3V	1.2		1.6	V
		V_{DD} = 2.5V	0.4		0.8	

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

AC Electrical Characteristics (T_A = -40 to 85°C)

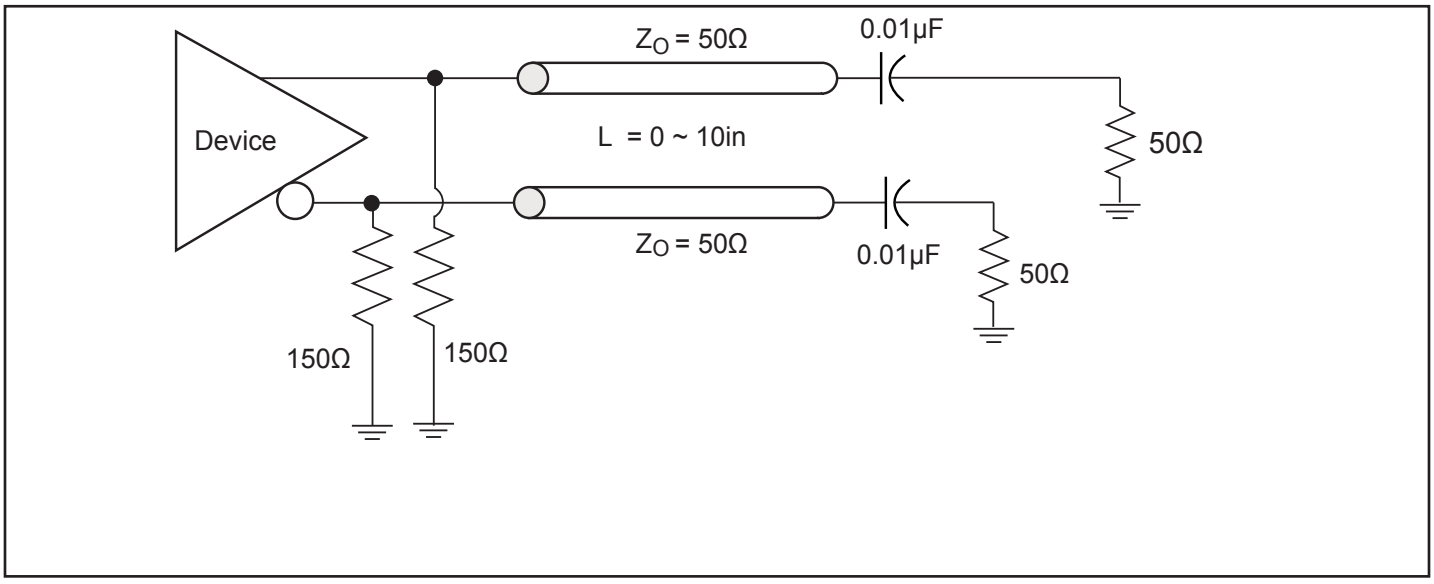
LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
f_{OUT}	Output Frequency	NA_SEL[1:0] / NB_SEL[1:0] = 00	560		700	MHz
		NA_SEL[1:0] / NB_SEL[1:0] = 01	280		350	MHz
		NA_SEL[1:0] / NB_SEL[1:0] = 10	140		175	MHz
		NA_SEL[1:0] / NB_SEL[1:0] = 11	112		140	MHz
$t_{sk(B)}$	Output Skew(1)	Output with same VDD and load			30	ps
$t_{sk(o)}$	Output Skew(2,4)	Output @ Same Frequencies			120	ps
		Output @ Different Frequencies			150	ps
$t_{jit(Ø)}$	RMS Phase Jitter, (Random)(3)	625MHz, (1.875MHz - 20MHz)		0.15		ps
		625MHz, (12kHz - 20MHz)		0.3		ps
		312.5MHz, (1.875MHz - 20MHz)		0.15		ps
		312.5MHz, (12kHz - 20MHz)		0.3		ps
		156.25MHz, (1.875MHz - 20MHz)		0.15		ps
		156.25MHz, (12kHz - 20MHz)		0.3		ps
		125MHz, Freq Select 110, (1.875MHz - 20MHz)		0.15		ps
		125MHz, Freq Select 110, (12kHz - 20MHz)		0.3		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%			400	ps
o_{DC}	Output Duty Cycle (5)		48		52	%

/

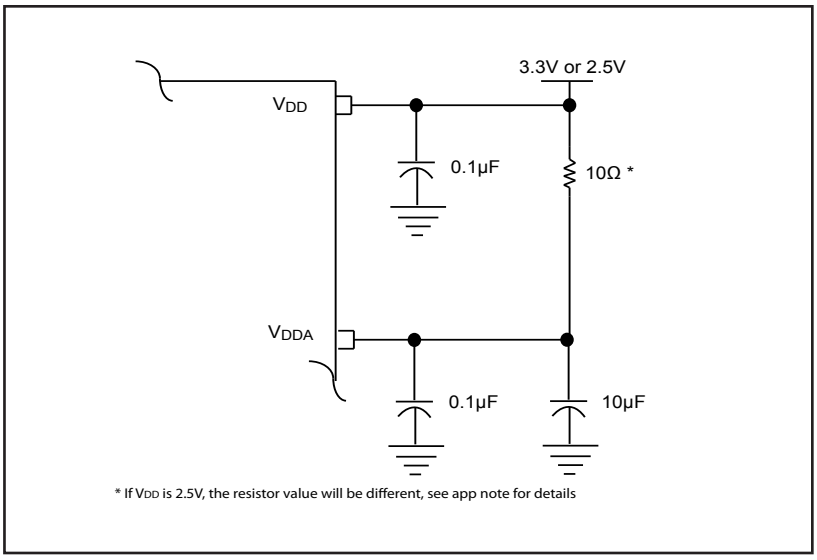
Note:
1. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
3. Please refer to the Phase Noise Plots.
4. This parameter is defined in accordance with JEDEC Standard 65. Measured at the differential cross points.
5. Measured at the differential cross points.

LVPECL Test Circuit



Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P03 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. A 1kΩ resistor can be tied from XTAL_IN to ground for additional protection.

Ref_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref_IN to ground can provide additional protection.

LVCMOS Control Pins:

All control pins have internal pulldowns/pullups; A 1kΩ resistor tied from internal pulldown control pins to ground, and a 4.7kΩ tied from internal pullup control pins to power supply can provide additional protection.

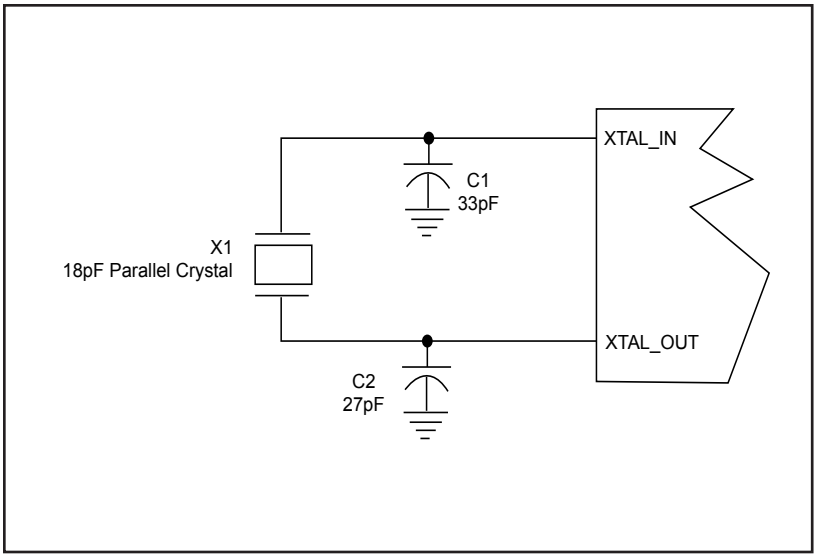
Outputs:

LVPECL Outputs:

All unused LVPECL outputs can be left floating.

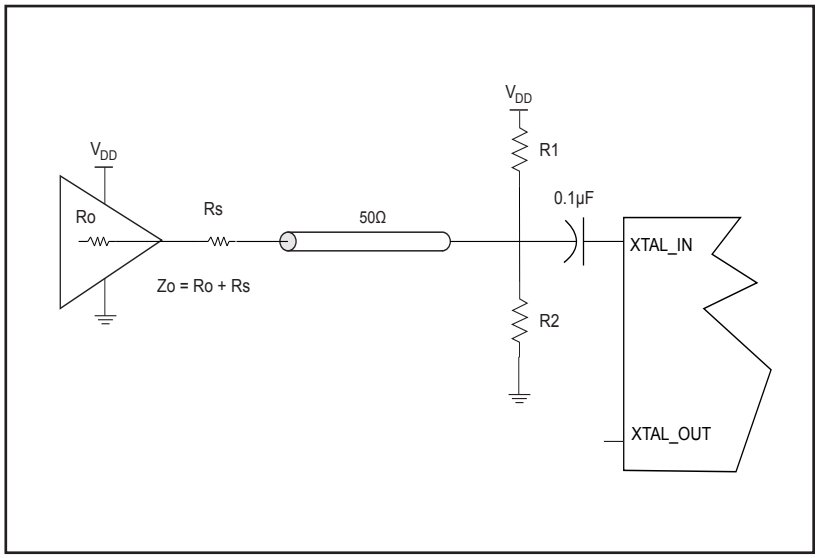
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 31.25MHz or 26.041666MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



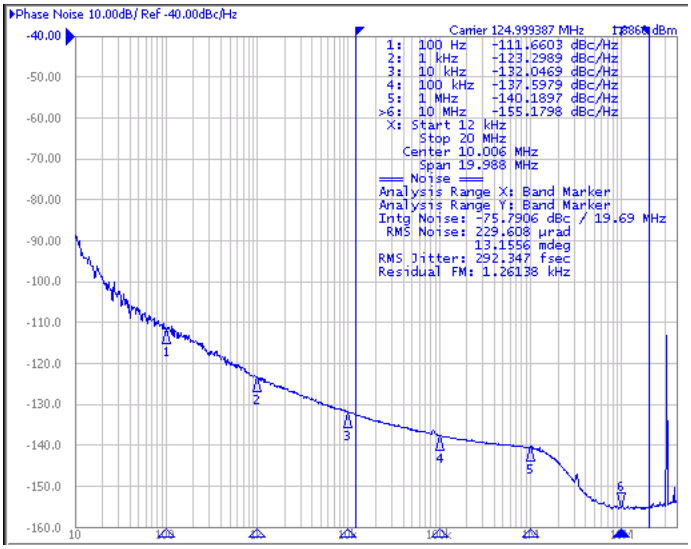
LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.

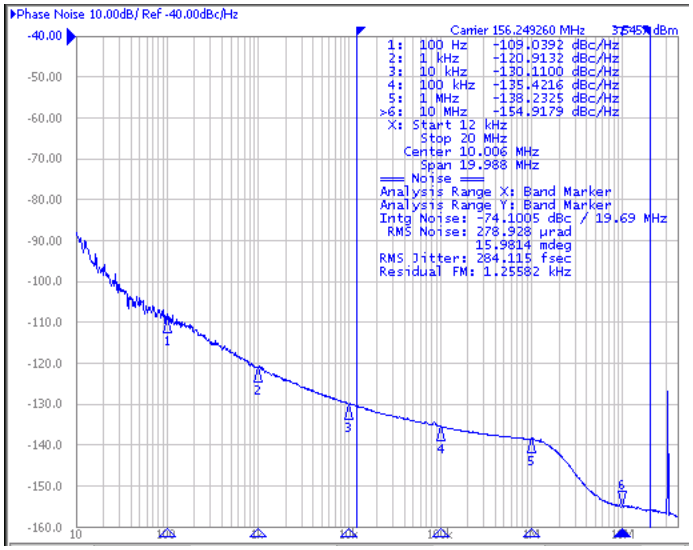


Phase Noise Plots

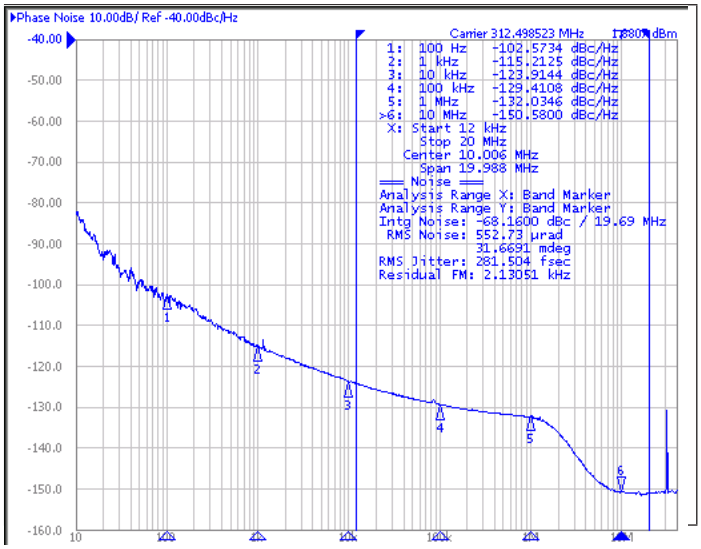
125MHz



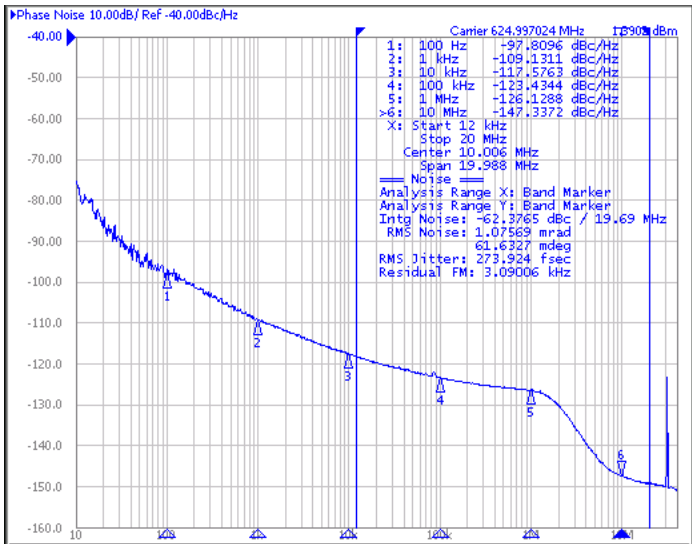
156.25MHz



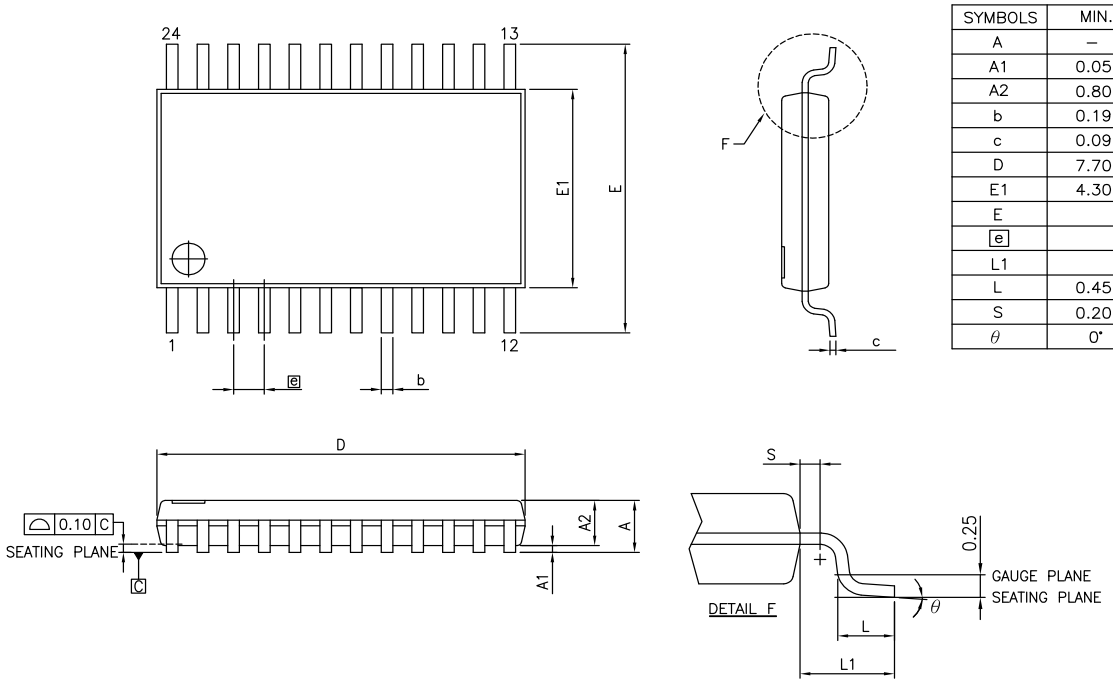
312.5MHz



625MHz



Packaging Mechanical: 24-Contact TSSOP (L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC: MO-153F/AD
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 24-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1312 **REVISION: F**

12-0374

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48P03LE	L	Pb-free & Green, 24-pin TSSOP	Commercial
PI6LC48P03LEX	L	Pb-free & Green, 24-pin TSSOP, Tape & reel	Commercial
PI6LC48P03LIE	L	Pb-free & Green, 24-pin TSSOP	Industrial
PI6LC48P03LIEX	L	Pb-free & Green, 24-pin TSSOP, Tape & reel	Industrial

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging