MP2324

High Efficiency 2A, 24V, 500kHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2324 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 2A continuous output current over a wide input supply range with excellent load and line regulation. The MP2324 has synchronous mode operation for higher efficiency over output current load range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include OCP and thermal shut down.

The MP2324 requires a minimum number of readily available standard external components and is available in a space saving 8-pin TSOT23 package.

FEATURES

- Wide 4.5V to 24V Operating Input Range
- 120mΩ/50mΩ Low Rds(on) Internal Power MOSFETs
- Low Quiescent Current
- High Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- Frequency Sync from 200kHz to 2MHz External Clock
- Power Save Mode at light load
- Internal Soft Start
- Power Good Indicator
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 package

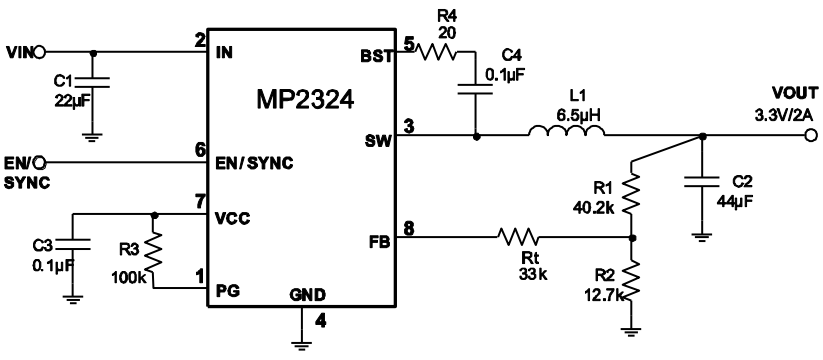
APPLICATIONS

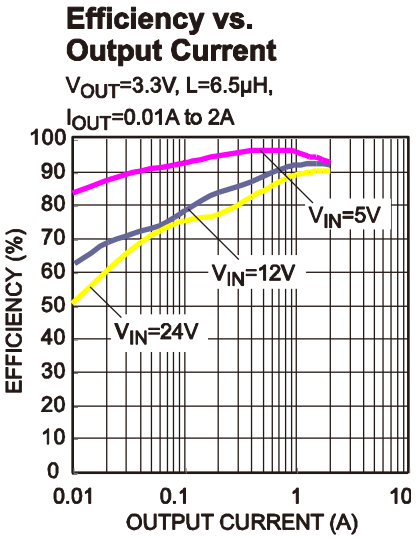
- Notebook Systems and I/O Power
- Digital Set Top Boxes
- Flat Panel Television and Monitors

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TYPICAL APPLICATION





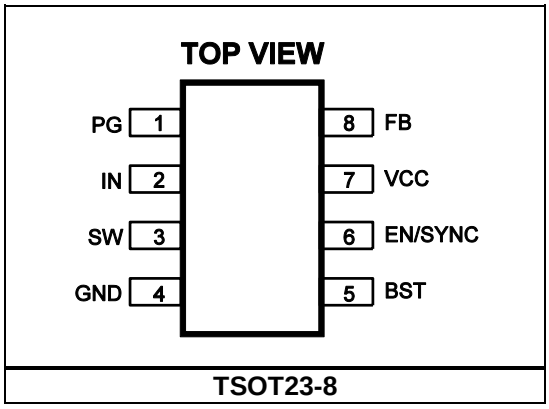
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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2324GJ	TSOT23-8	AHV

* For Tape & Reel, add suffix –Z (e.g. MP2324GJ–Z);

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... –0.3V to +28V
V_{SW} .....–0.3V (-5V<10ns) to +28V (30V <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins..... -0.3V to +6V
Continuous Power Dissipation (TA=+25°C) **(2)** ...
.....1.25W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5 to 24V
Output Voltage V_{OUT}..... 0.8V to V_{IN}*D_{MAX}
Operating Junction Temp (T_J). . -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-8……..……100…..55..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		5.5		μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V	130	180	240	μA
HS Switch On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		120		mΩ
LS Switch On Resistance	LS_{RDS-ON}	V_{CC}=5V		50		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit (5)	I_{LIMIT}	Duty Cycle=40%	3	4		A
Oscillator Frequency	f_{SW}	V_{FB}=750mV	420	500	620	kHz
Fold-back Frequency	f_{FB}	V_{FB}=200mV		0.5		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=750mV	90	95		%
Minimum On Time (5)	T_{ON_MIN}			60		ns
Sync Frequency Range	f_{SYNC}		0.2		2	MHz
Feedback Voltage	V_{FB}	T_A=25ºC	783	791	799	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	V_{EN_RISING}		1.2	1.4	1.6	V
EN Hysteresis	V_{EN_HYS}		80	150	220	mV
EN Input Current	I_{EN}	V_{EN}=2V	1.5	2	2.5	μA
		V_{EN}=0		0	50	nA
EN Turn Off Delay	EN_{Td-off}		6	10	14	μs
Power Good Rising Threshold	PG_{VTH-Hi}			0.9		V_{FB}
Power Good Falling Threshold	PG_{VTH-LO}			0.85		V_{FB}
Power Good Delay	PG_{Td}			40		μs
Power Good Sink Current Capability	V_{PG}	Sink 1mA			0.4	V
Power Good Leakage Current	$I_{PG-LEAK}$				1	μA
VIN Under Voltage Lockout Threshold-Rising	$INUV_{Vth}$		3.7	3.9	4.1	V
VIN Under Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$		550	650	750	mV
VCC Regulator	V_{CC}		4.65	4.9	5.15	V
VCC Load Regulation		I_{CC}=5mA	0	1	3	%
Soft-Start Period	T_{SS}		0.8	1.5	2.2	ms
Thermal Shutdown(5)				150		ºC
Thermal Hysteresis(5)				20		ºC

Notes:

5) Guaranteed by design

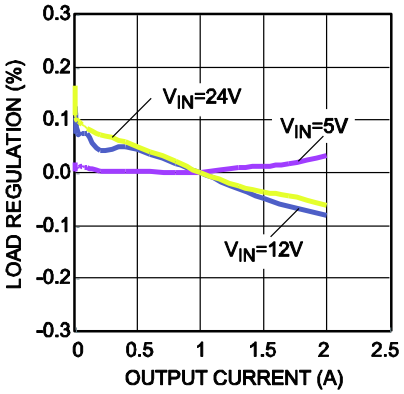
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TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 6.5µH, T_A = 25°C, unless otherwise noted.

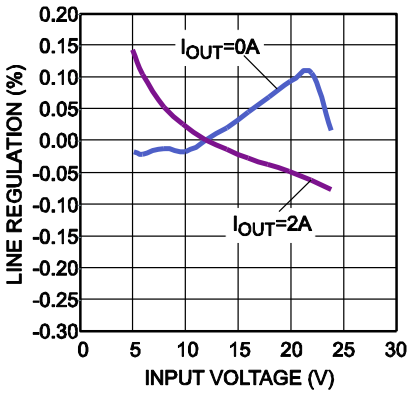
Load Regulation

V_{IN}=5V to 24V, I_{OUT}=0.1A to 2A

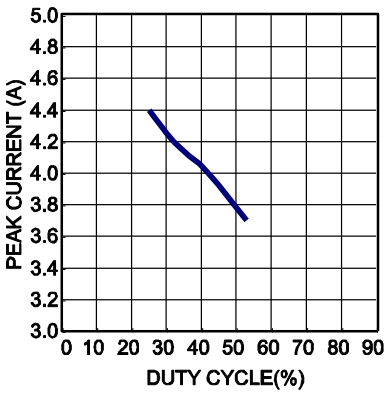


Line Regulation

V_{IN}=5V to 24V

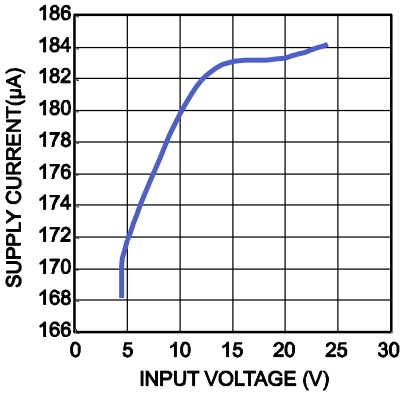


Peak Current vs. Duty Cycle



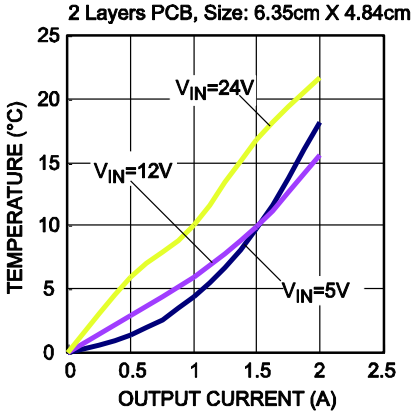
Enabled Supply Current vs. Input Voltage

V_{IN}=4.5V to 24V, EN=5V



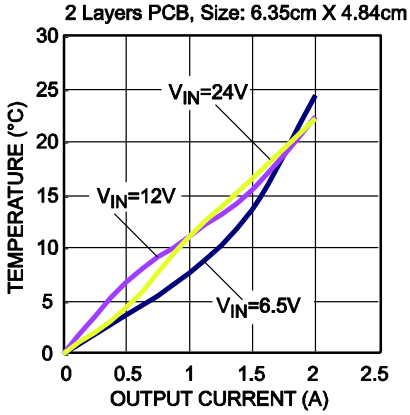
Case Temperature Rise vs. Output Current

V_{OUT}=3.3V, I_{OUT}=0 to 2A,
2 Layers PCB, Size: 6.35cm X 4.84cm



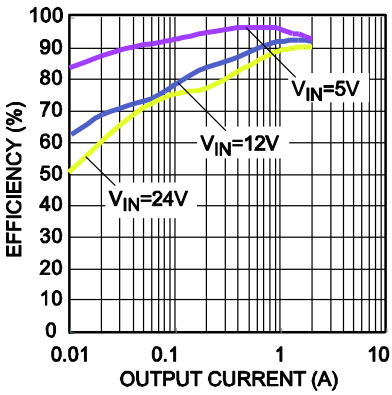
Case Temperature Rise vs. Output Current

V_{OUT}=5V, I_{OUT}=0 to 2A,
2 Layers PCB, Size: 6.35cm X 4.84cm



Efficiency vs. Output Current

I_{OUT}=0.01A to 2A

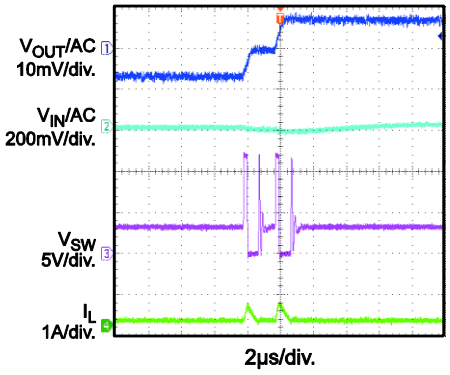


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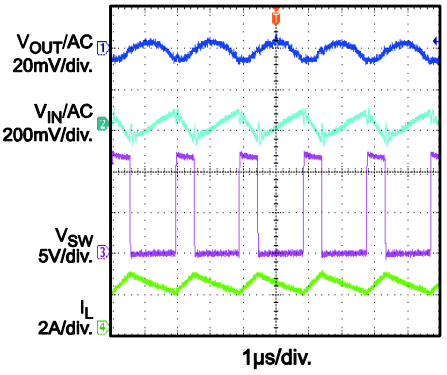
TYPICAL PERFORMANCE CHARACTERISTICS

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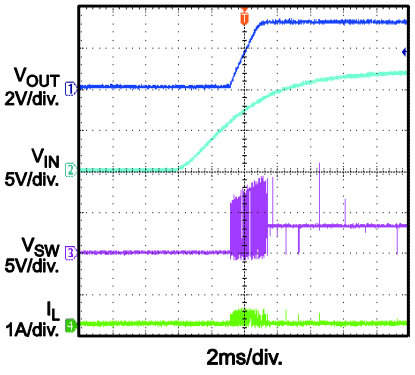
Input/Output Ripple
I_{OUT}= 0A



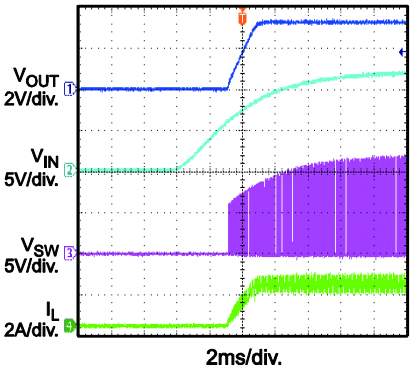
Input/Output Ripple
I_{OUT}= 2A



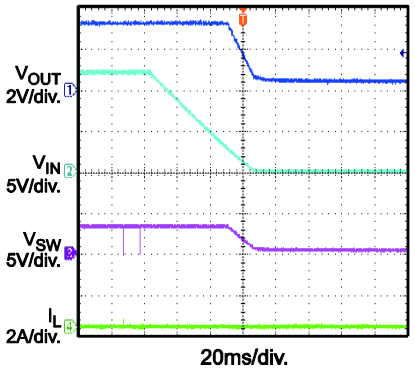
V_{IN} Start up
I_{OUT}= 0A



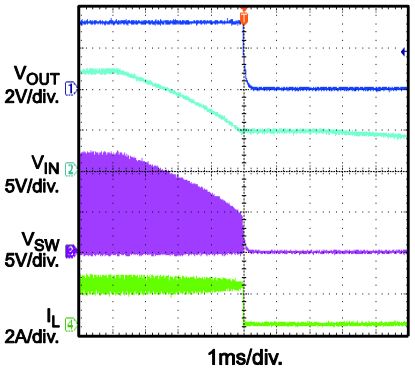
V_{IN} Start up
I_{OUT}= 2A



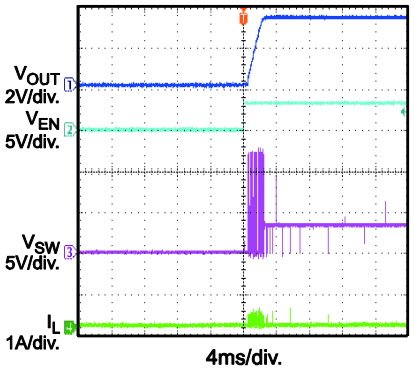
V_{IN} Shutdown
I_{OUT}= 0A



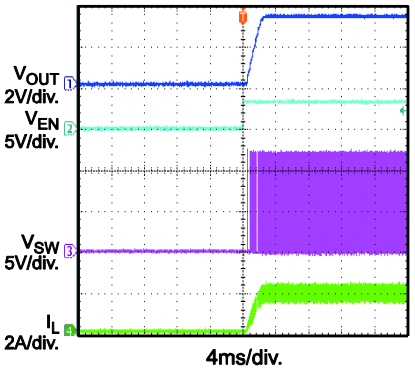
V_{IN} Shutdown
I_{OUT}= 2A



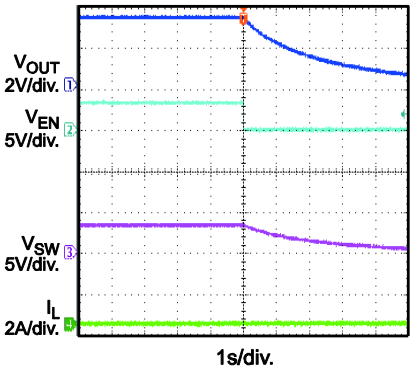
EN Start up
I_{OUT}= 0A



EN Start up
I_{OUT}= 2A



EN Shutdown
I_{OUT}= 0A

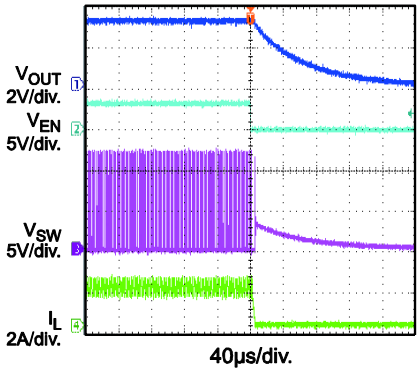


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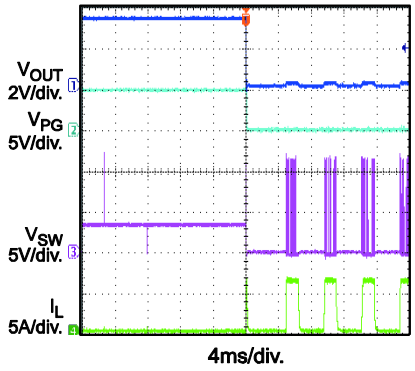
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 6.5µH, T_A = 25°C, unless otherwise noted.

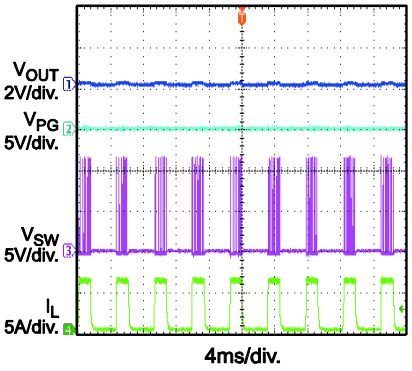
EN Shutdown
I_{OUT}= 2A



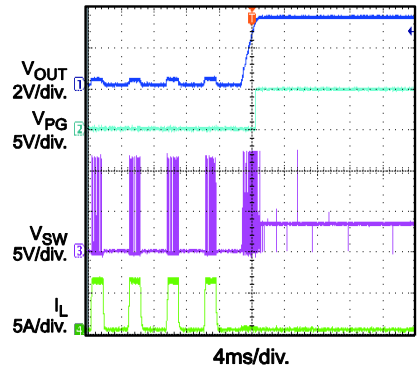
Short Circuit Entry



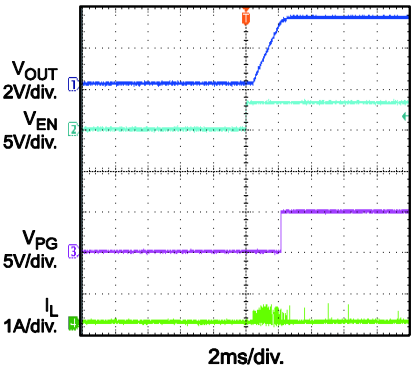
Short Circuit



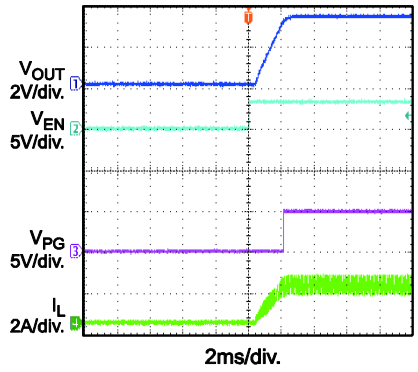
Short Circuit Recovery



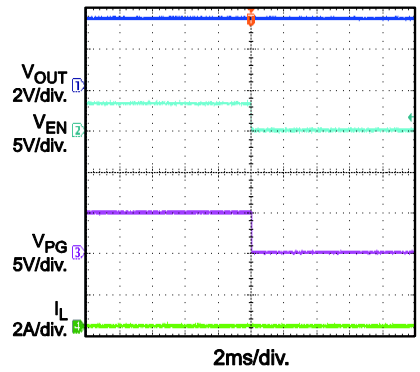
EN Start up (PG)
I_{OUT}= 0A



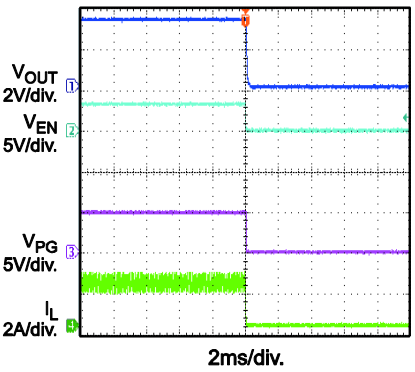
EN Start up (PG)
I_{OUT}= 2A



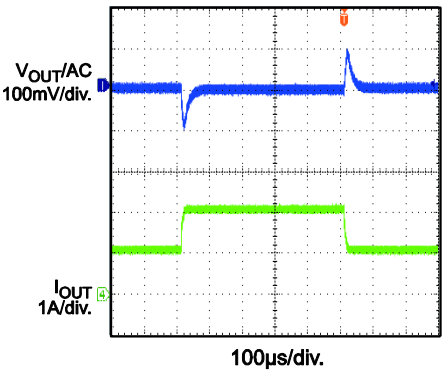
EN Shutdown(PG)
I_{OUT}= 0A



EN Shutdown(PG)
I_{OUT}= 2A



Load Transient Response
I_{OUT}= 1A to 2A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	Power Good Output. The output of this pin is an open drain. It's pulled up to Vcc by external resistor when the output voltage exceeds 90% of the normal voltage. There is a 40μs delay between FB≥90% to the PG pin goes high.
2	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP2324 operates from a +4.5V to +24V input rail. Requires a low-ESR, and low inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
3	SW	Switch Output. Connect to the inductor and bootstrap capacitor. This pin is driven up to VIN by the high-side switch during the PWM duty cycle ON time. The inductor current drives the SW pin negative during the OFF time. The ON resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect using wide PCB traces and multiple vias.
4	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Suggested to be connected to GND with copper and vias.
5	BST	Bootstrap. A capacitor and a 20Ω resistor connected between SW and BST pins are required to form a floating supply across the high-side switch driver.
6	EN/SYNC	EN=1 to enable the MP2324. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN with a 100kΩ resistor.
7	VCC	Bias Supply. Decouple with 0.1μF-0.22μF cap. And the capacitance should be no more than 0.22μF
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV.

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FUNCTION BLOCK DIAGRAM

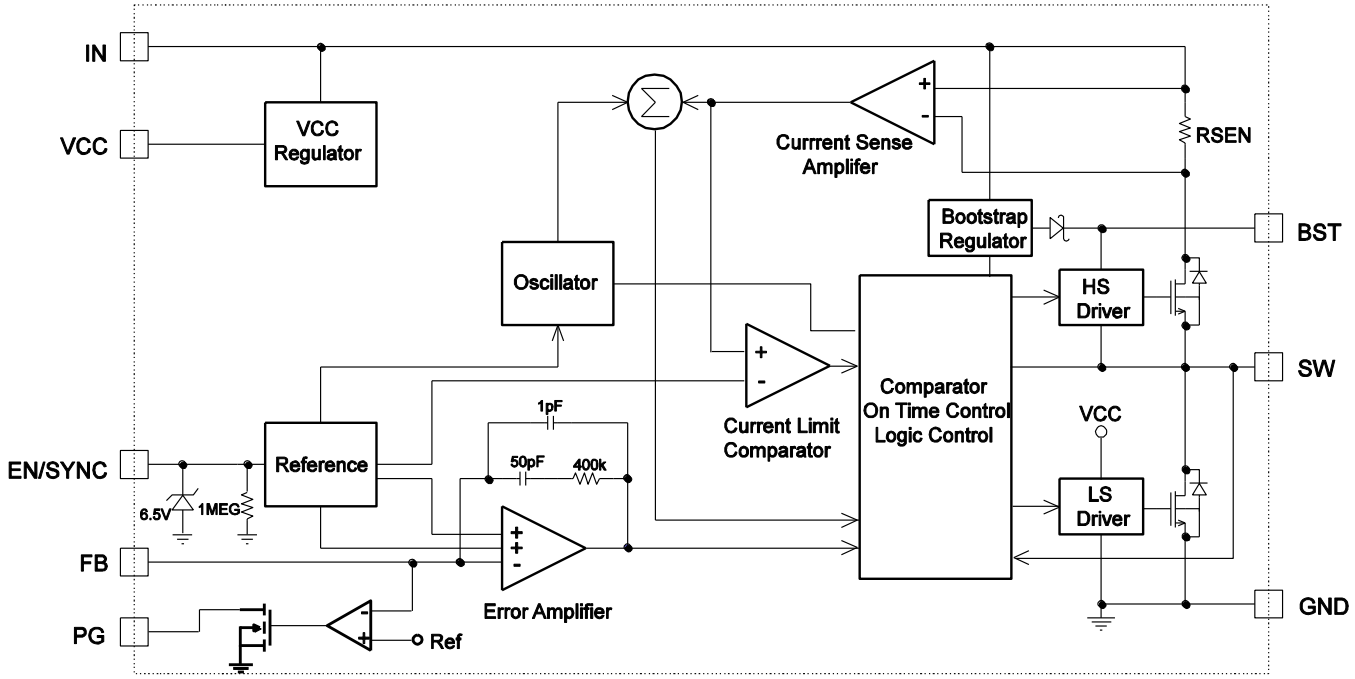


Figure 1: Functional Block Diagram

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OPERATION

The MP2324 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 2A continuous output current over a wide input supply range with excellent load and line regulation.

The MP2324 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 95% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, a 0.1uF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Power Save Mode for Light Load Condition

The MP2324 has AAM (Advanced Asynchronous Modulation) power-save mode for light load. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} is higher than V_{AAM}.

Under the light load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, thus the MP2324 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

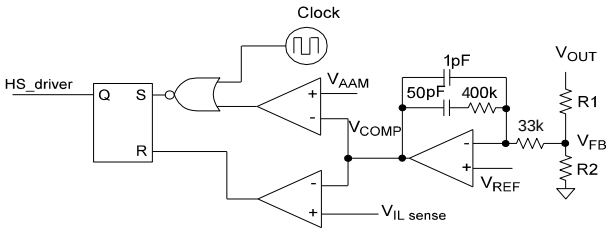


Figure 2: Simplified AAM Control Logic

For V_{IN}=12V, V_{OUT}=3.3V, L=4.9µH, the inductor peak current set internally is about 500mA at light load. The AAM voltage internally is varied with duty cycle for keeping the inductor peak current constant.

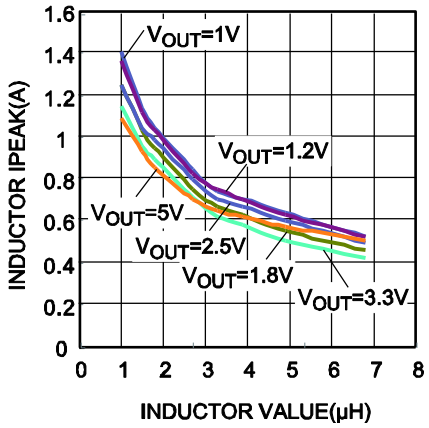


Figure 3: AAM Selection for Common Output Voltages (V_{IN}=4.5V-24V)

Enable/SYNC Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive it low to turn it off. There is an internal 1MEG resistor from EN to GND thus EN can be floated to shut down the chip. Also EN pin voltage was clamped to around 6.5V by an internal zener-diode. Please use large enough pull up resistor connecting between VIN and EN to limit the EN input current which

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should be less than 100uA. Generally, around 100k resistor should be large enough for all the applications.

The chip can be synchronized to external clock range from 200kHz up to 2MHz through this pin 2ms right after output voltage is set, with the internal clock rising edge synchronized to the external clock rising edge. EN synchronize logic high voltage should higher than 2V. EN synchronize logic low voltage should lower than 400mV. EN logic high pulse width must less than 1.6µs. Otherwise the internal clock may come and turn on high side MOSFET again. EN logic low pulse width must less than 6µs, otherwise MP2324 may EN shutdown.

Power Good Indicator

The MP2324 has an open drain pin for power good indicator. When FB pin is higher than 90% of regulation voltage, PG pin is pulled up to VCC by the external resistor. If FB pin voltage drop down to 85% of the regulation voltage, PG pin is pulled down to ground by an internal MOS FET.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP2324 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.9V while its falling threshold is consistent 3.25V.

Internal Soft-Start

The soft start is implemented to prevent the converter output voltage from overshooting during start up. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V. At this point the reference voltage takes over. The soft-start time is internally set to be around 1.5ms.

Over-Current-Protection and Hiccup

The MP2324 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 50% below the reference. Once a UV is triggered, the MP2324 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP2324 exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, R5, C5, L1 and C2 (Figure 4). If (VIN-VSW) is more than 5V, U1 will regulate M1 to maintain a 5V BST voltage across C5.

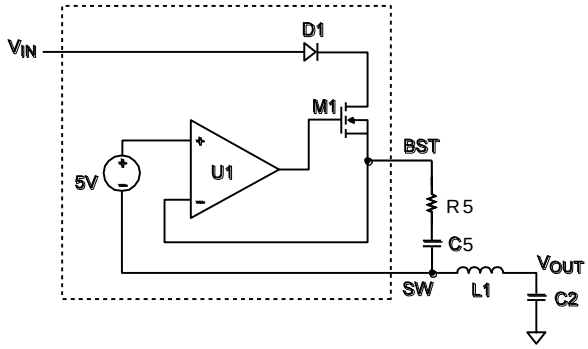


Figure 4: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

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Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

The T-type network is highly recommended, as Figure 5 shows.

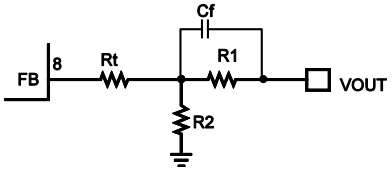


Figure 5: T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	Rt (kΩ)	L (µH)	Cf (µF)
1	20.5	76.8	100	2.2	15
1.2	20.5	39.2	100	2.2	15
1.8	40.2	31.6	56	4.7	15
2.5	40.2	18.7	56	4.7	15
3.3	40.2	12.7	33	6.5	15
5	40.2	7.5	33	6.5	15

Selecting the Inductor

A 1µH to 22µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at VIN = 2VOUT, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

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$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2324 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT} is 5V or 3.3V;
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 6.

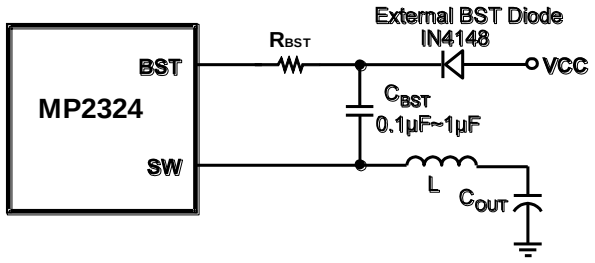


Figure 6: Add Optional External

Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1μF—1μF.

PC Board Layout [6]

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure 7 as reference.

1) Keep the connection of input ground and GND pin as short and wide as possible.

2) Keep the connection of input capacitor and IN pin as short and wide as possible.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) Route SW away from sensitive analog areas such as FB.

Notes:

6) The recommended layout is based on the Figure 8 Typical Application circuit on the next page.

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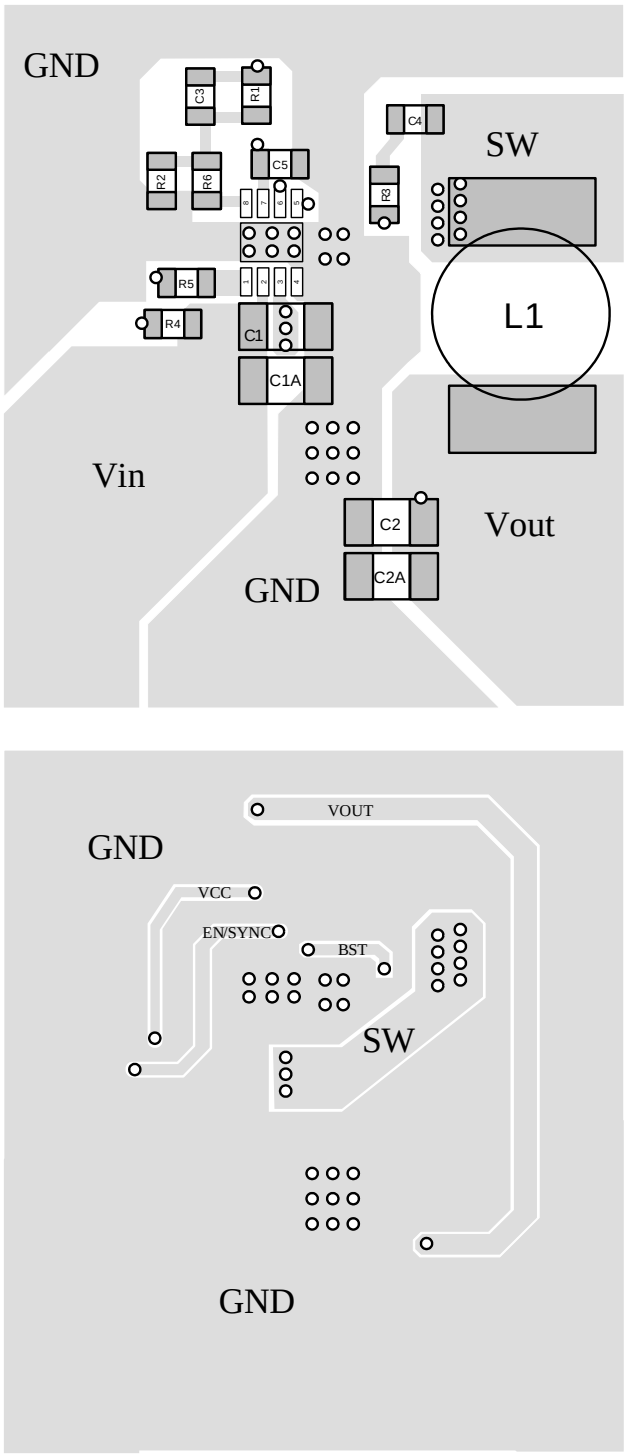


Figure 7: Sample Board Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	19V
V_{OUT}	5V
I_O	2A

The detailed application schematics are shown in Figures 8 through 13. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

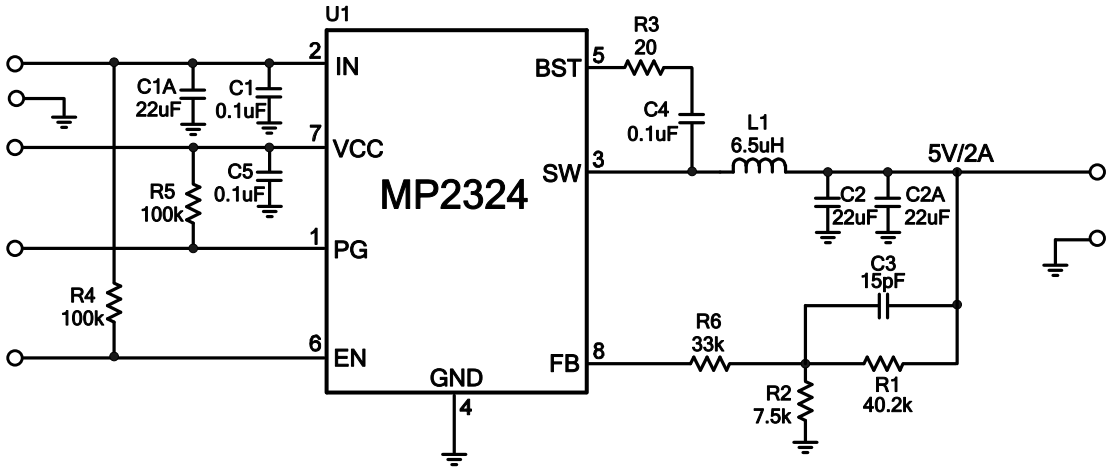


Figure 8: Vo=5V, Io=2A

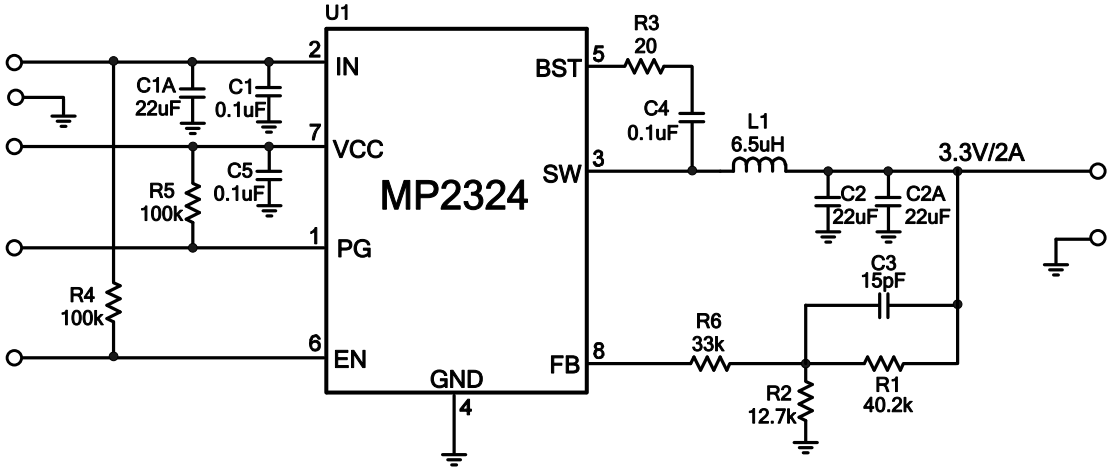


Figure 9: Vo=3.3V, Io=2A

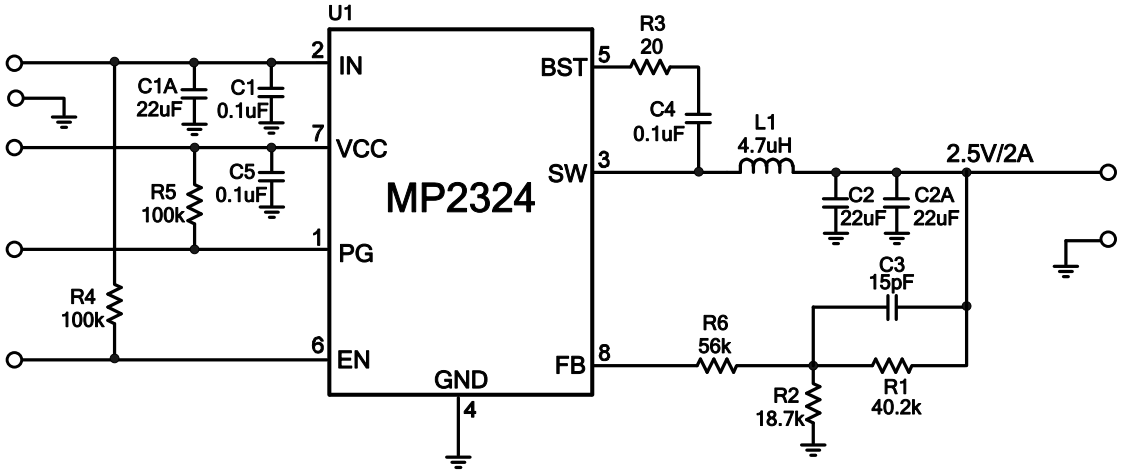


Figure 10: Vo=2.5V, Io=2A

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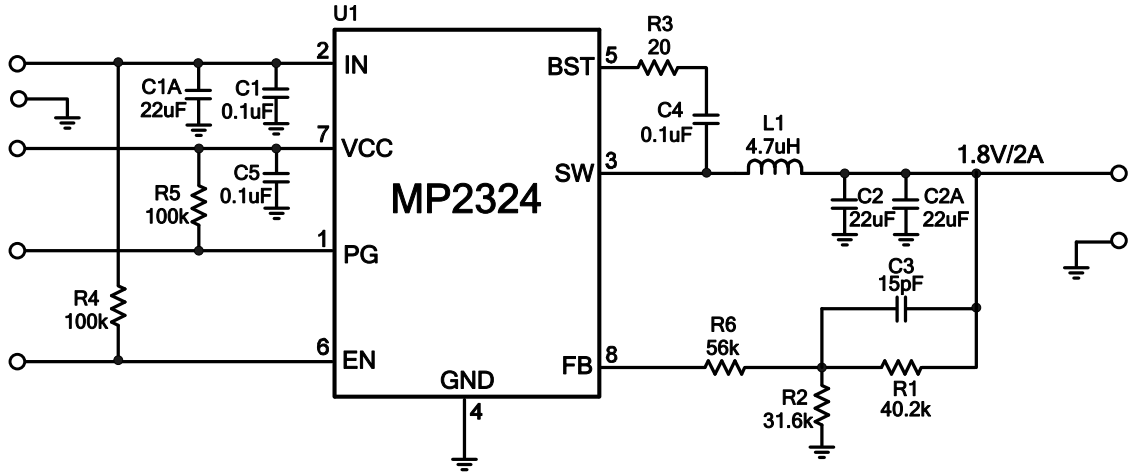


Figure 11: Vo=1.8V, Io=2A

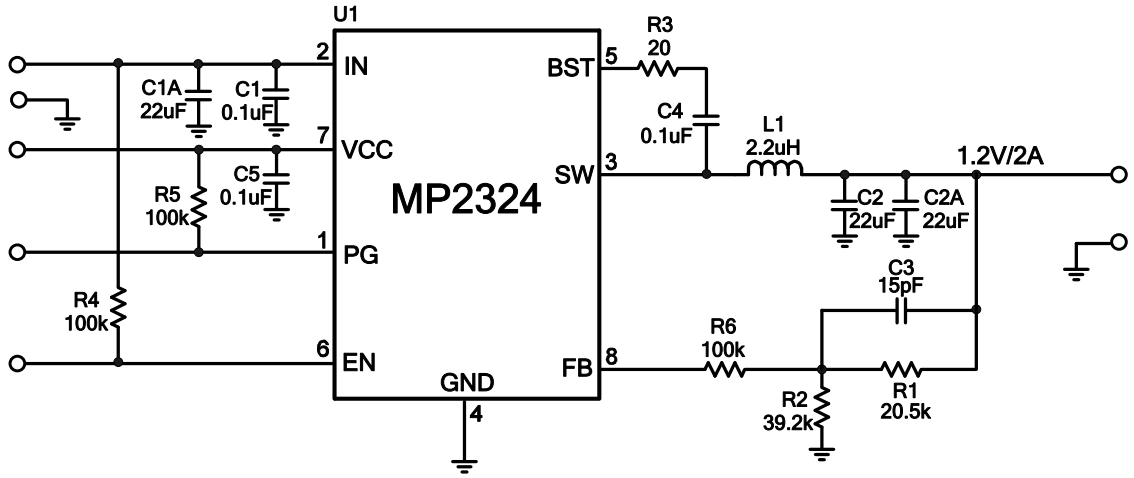


Figure 12: Vo=1.2V, Io=2A

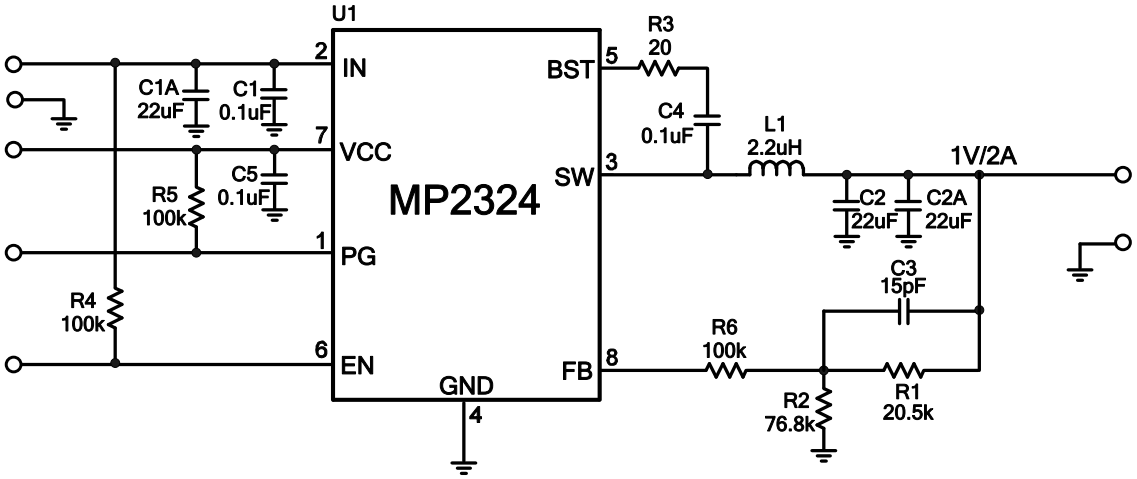
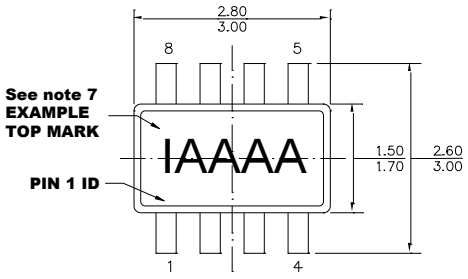


Figure 13: Vo=1V, Io=2A

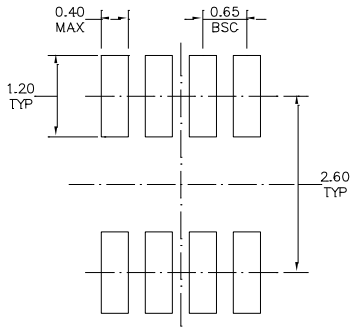
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PACKAGE INFORMATION

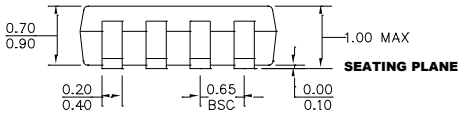
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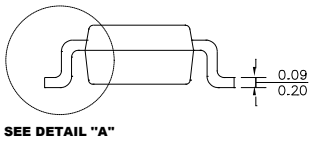
TOP VIEW



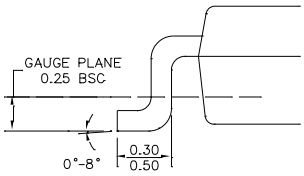
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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