Synchronous DRAM Module 512Mbyte (64Mx64bit), SMM, based on 32Mx8 ,4Banks, 4K Ref., 3.3V Part No. HSD64M64F8KA

GENERAL DESCRIPTION

The HSD64M64F8KA is a 64M x 64 bit Synchronous Dynamic RAM high-density memory module. The module consists of sixteen CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil packages on a 120-pin glass-epoxy. One 0.22uF and two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The HSD64M64F8KA is a SMM(Stackable Memory Module type) .Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTL-compatible.

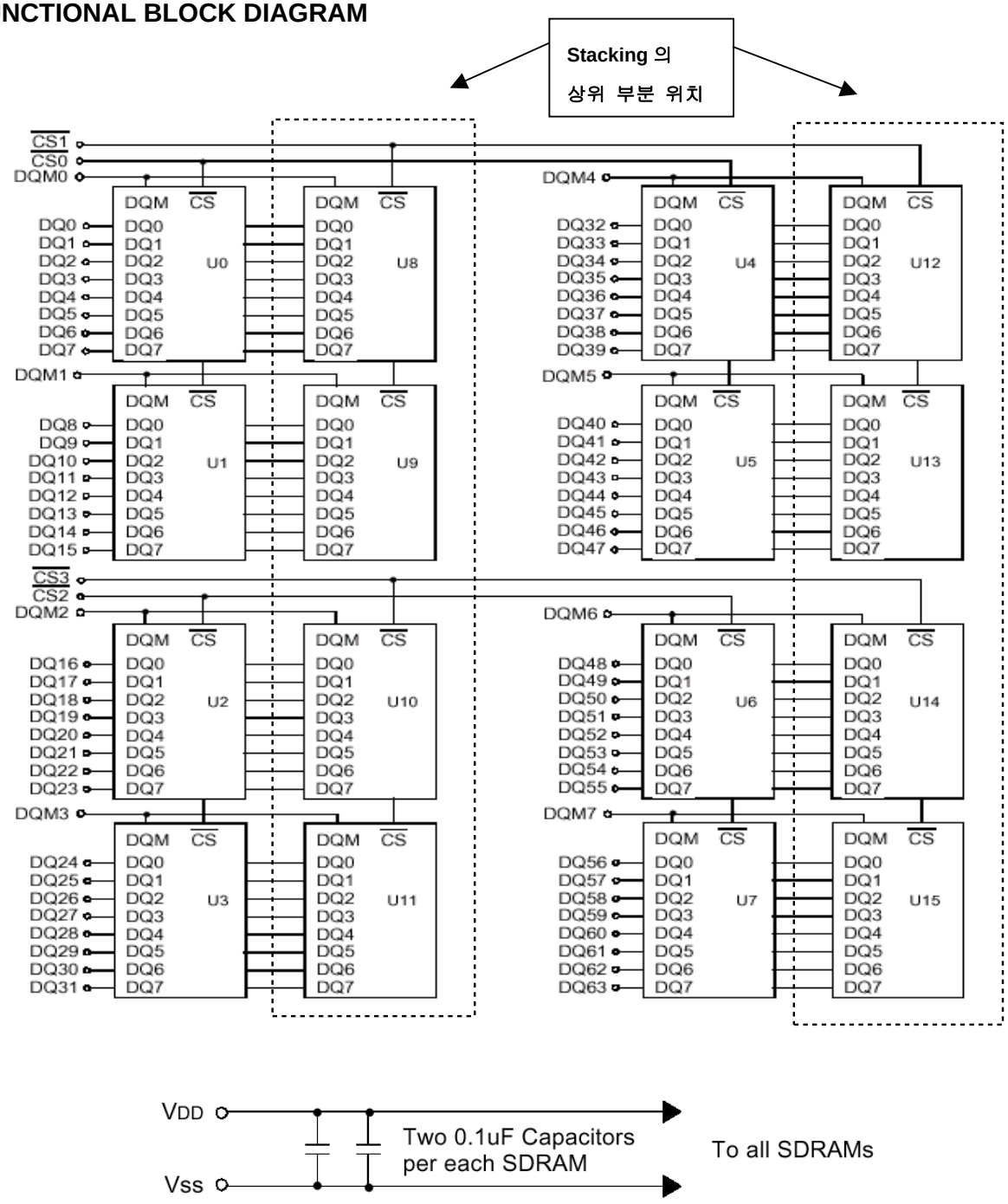
FEATURES

- Part Identification
  - HSD64M64F8KA –10L : 100MHz (CL=3)
  - HSD64M64F8KA –10 : 100MHz (CL=2)
  - HSD64M64F8KA –13 : 133MHz (CL=3)
- Burst mode operation
- Auto & self refresh capability (8192Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ±0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- The used device is stacked 8M x 8bit x 4Banks SDRAM

PIN ASSIGNMENT

60-PIN P1 Connector				60-PIN P2 Connector			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	31	Vss	1	Vss	31	Vcc
2	DQ32	32	DQ0	2	DQ16	32	DQ48
3	DQ33	33	DQ1	3	DQ17	33	DQ49
4	DQ34	34	DQ2	4	DQ18	34	DQ50
5	DQ35	35	DQ3	5	DQ19	35	DQ51
6	DQ36	36	DQ4	6	DQ20	36	DQ52
7	DQ37	37	DQ5	7	DQ21	37	DQ53
8	DQ38	38	DQ6	8	DQ22	38	DQ54
9	DQ39	39	DQ7	9	DQ23	39	DQ55
10	Vcc	40	Vss	10	Vss	40	Vcc
11	DQ40	41	DQ8	11	DQ24	41	DQ56
12	DQ41	42	DQ9	12	DQ25	42	DQ57
13	DQ42	43	DQ10	13	DQ26	43	DQ58
14	DQ43	44	DQ11	14	DQ27	44	DQ59
15	DQ44	45	DQ12	15	DQ28	45	DQ60
16	DQ45	46	DQ13	16	DQ29	46	DQ61
17	DQ46	47	DQ14	17	DQ30	47	DQ62
18	DQ47	48	DQ15	18	DQ31	48	DQ63
19	Vcc	49	Vss	19	Vss	49	Vcc
20	DQM4	50	DQM0	20	DQM2	50	DQM6
21	DQM5	51	DQM1	21	DQM3	51	DQM7
22	NC	52	/WE	22	NC	52	A12
23	CKE0	53	CLK0	23	BA0	53	A11
24	CKE1	54	CLK1	24	BA1	54	A9
25	Vcc	55	Vss	25	A10/AP	55	A8
26	NC	56	/CAS	26	A0	56	A7
27	NC	57	/RAS	27	A1	57	A6
28	/CS1	58	/CS1	28	A2	58	A5
29	/CS2	59	/CS2	29	A3	59	A4
30	Vcc	60	Vss	30	Vss	60	Vcc

FUNCTIONAL BLOCK DIAGRAM



*** /CS0 + /CS2(b'd) = /CS1(Module), /CS1 + /CS3(b'd) = /CS2(Module)**

**** Address (0:12), /RAS, /CAS, /WE, BA(0:1), CLK, CKE0 → U0~U15**

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
/CS	Chip enable	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tsHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
Vcc/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 4.6V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 4.6V
Power Dissipation	P_D	16W
Storage Temperature	T_{STG}	$-55^{O}C$ to $150^{O}C$
Short Circuit Output Current	I_{OS}	50mA

Notes:
Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C))

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Supply Voltage	Vcc	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	Vcc+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes :

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input capacitance(A0~A11)	C_{IN1}	40	80	pF
Input capacitance(/RAS, /CAS,/WE)	C_{IN2}	40	80	pF
Input capacitance(CKE0)	C_{IN3}	40	80	pF
Input capacitance(CLK0)	C_{IN4}	40	64	pF
Input capacitance(/CS0~/CS3)	C_{IN5}	40	80	pF
Input capacitance(DQM0~DQM7)	C_{IN3}	40	64	pF
Input capacitance(BA0~BA1)	C_{IN3}	40	64	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	64	104	pF

(Vcc = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	VERSION			UNIT	NOTE
			-10	-10L	-13		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0mA	720	720	800	mA	1
Precharge standby current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max) t_{CC}=10ns	16			mA	3
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max) t_{CC}=∞	16			mA	3

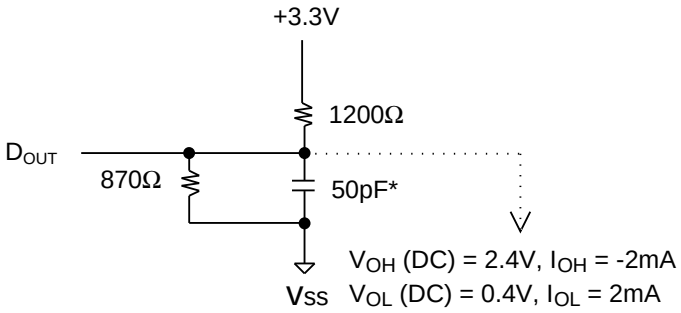
Precharge standby current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min) /CS ≥ V_{IH}(min), tcc=10ns Input signals are changed one time during 20ns	320			mA	3
	$I_{CC2}NS$	CKE ≥ V_{IH}(min) CLK ≤ V_{IL}(max), tcc=∞ Input signals are stable	112				
Active standby current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), tcc=10ns	80			mA	3
	$I_{CC3}PS$	CKE&CLK ≤ V_{IL}(max) tcc=∞	80				
Active standby current in non power-down mode (One bank active)	$I_{CC3}N$	CKE≥V_{IH}(min), /CS≥V_{IH}(min), tcc=10ns Input signals are changed one time during 20ns	480			mA	3
	$I_{CC3}NS$	CKE≥VIH(min) CLK ≤VIL(max), tcc=∞ Input signals are stable	320				
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	800	800	880	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1520	1520	1600	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	24			mA	3

Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1PLL & 3 Drive Ics.
4. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

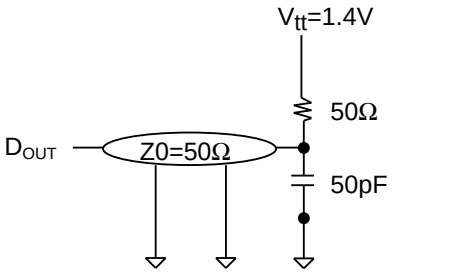
AC OPERATING TEST CONDITIONS

(vcc = 3.3V ± 0.3V, T_A = 0 to 70°C)

PARAMETER	Value	UNIT
AC Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VERSION			UNIT	NOTE
			-10	-10L	-13		
Row active to row active delay		t_{RRD}(min)	20	20	15	ns	1
/RAS to /CAS delay		t_{RCD}(min)	20	20	20	ns	1
Row precharge time		t_{RP}(min)	20	20	20	ns	1
Row active time		t_{RAS}(min)	50	50	45	ns	1
		t_{RAS}(max)	100			ns	
Row cycle time		t_{RC}(min)	70	70	65	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2,5
Last data in to Active delay		t_{DAL}(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		t_{CDL}(min)	1			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
   (recommend : tRDL=2CLK and tDAL=2CLK + 20ns.)

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-10		-10L		-13		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	10	1000	7.5	1000	ns	1
	CAS latency=2		10		12		10			
CLK to valid output delay	CAS latency=3	t_{SAC}		6		6		5.4	ns	1,2
	CAS latency=2			6		7		6		
Output data hold time	CAS latency=3	t_{OH}	3		3		3		ns	1,2
	CAS latency=2		3		3		3			
CLK high pulse width		t_{CH}	3		3	ns	2.5		ns	ns
CLK low pulse width		t_{CL}	3		3	ns	2.5		ns	ns
Input setup time		t_{SS}	2		2	ns	1.5		ns	ns
Input hold time		t_{SH}	1		1	ns	0.8		ns	ns
CLK to output in Low-Z		t_{SLZ}	1		1	ns	1		ns	ns
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6		5.4	ns	1
	CAS latency=2			6		7		6	ns	1

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DQM	BA 0,1	A10/AP	A11 A9~A0	NOTE
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge eable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :

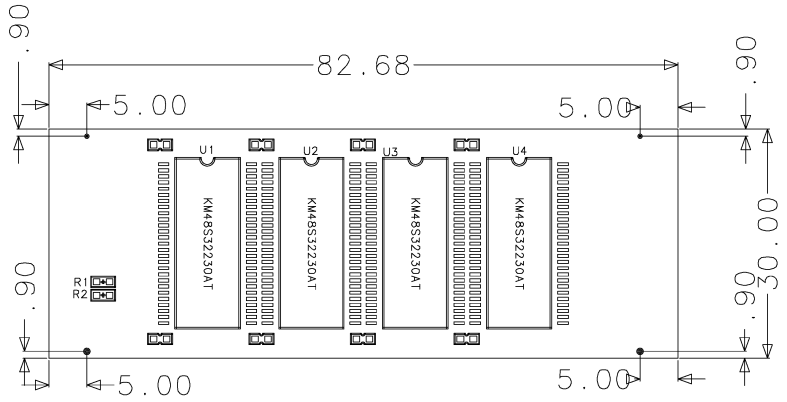
1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGING INFORMATION

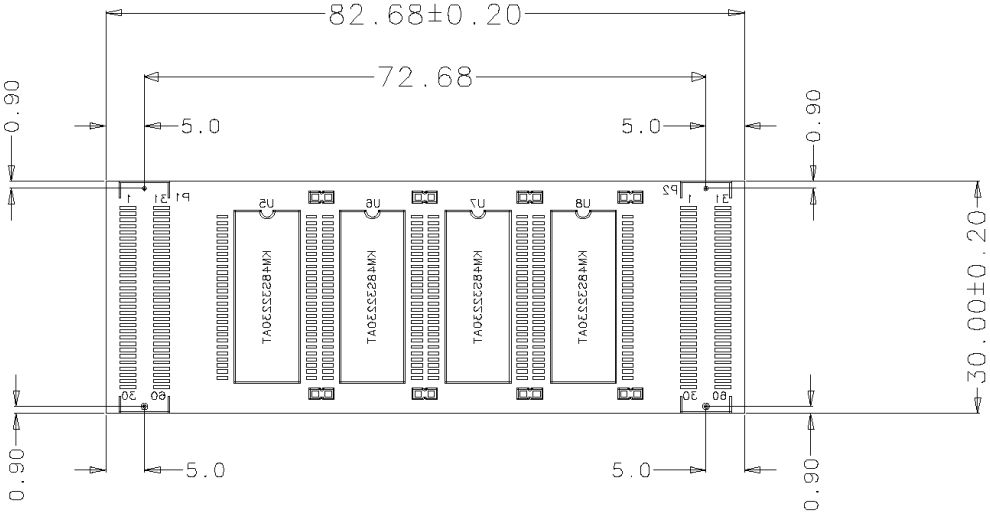
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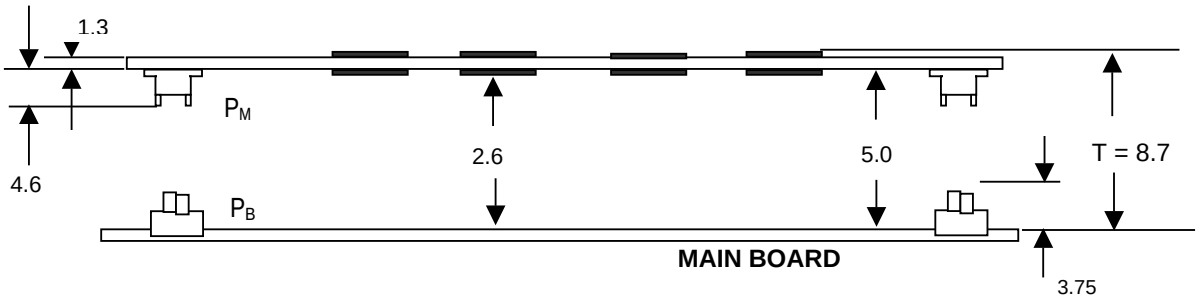
Front –Side

TOLERANCE : ±0.20



Rear–Side (Top view)





Connector Configuration

- Module PCB Bottom (**P_M**) : AMP 177984-2 (177986-2), 0.8mm Free Height Plugs, 60pins
- Main Board top (**P_B**) : AMP 177983-2(177985-2),0.8mm Free Height Receptacles , 60pins

ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HSD64M64F8KA-10L	512MByte	64M x 64	120PIN STACKABLE	4K	3.3V	Synch	100MHz / CL=3
HSD64M64F8KA-10	512MByte	64M x 64	120PIN STACKABLE	4K	3.3V	Synch	100MHz / CL=2
HSD64M64F8KA-13	512MByte	64M x 64	120PIN STACKABLE	4K	3.3V	Synch	133MHz / CL=3