HMCS404C (HD614042), HMCS404CL (HD614045), HMCS404AC (HD614048)

4-Bit CMOS Microcomputers

AUTOMOTIVE VERSION

The HMCS404C/CL/AC are CMOS 4-bit single-chip microcomputers which are members of the HMCS400 series.

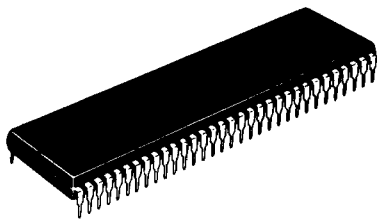
The HMCS404C/CL/AC have efficient and powerful architecture and its software is very similar to the HMCS40 series.

These microcomputers provide variety of on-chip resources such as ROM, RAM, I/O, two timer/counters and a serial interface to perform in wide users' applications. I/O pins of HMCS404C/CL/AC are able to drive fluorescent display tube directly.

The HMCS404CL is able to operate in low voltage and has the characteristics of wide-range operation voltage.

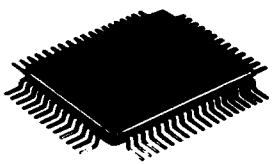
The HMCS404AC is a high-speed version of HMCS404C.

HMCS404C, HMCS404CL, HMCS404AC



(DP-64S)

HMCS404C, HMCS404CL, HMCS404AC



(FP-64)

■ HARDWARE FEATURES

- 4-bit Architecture
- 4,096 Words x 10-bit ROM
- 256 Digits x 4-bit RAM
- 58 I/O Pins, Including 26 High Voltage I/O Pins (40V Max)
- Two Timer/Counters
  - 11-bit Prescaler
  - 8-bit Free Running Timer
  - 8-bit Auto-Reload Timer/Event Counter
- Clock Synchronous 8-bit Serial Interface
- Five Interrupts
  - External 2
  - Timer/Counter 2
  - Serial Interface 1
- Subroutine Stack
  - Up to 16 Levels Including Interrupt
- Two Low Power Dissipation Modes
  - Standby – Stops instruction execution while keeping clock oscillation and interrupt functions in operation
  - Stop – Stops instruction execution and clock oscillation while retaining RAM data
- On-Chip Oscillator
  - External Connection of Crystal, Ceramic Filter or Re (externally drivable)
  - (Resistor oscillator is available only to the HMCS404C)

■ SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single-word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation – Table Look Up Capability –
- Bit Manipulation for Both RAM and I/O

■ VERSATILE PROGRAM DEVELOPMENT SUPPORT TOOLS

- H68SD Series Macro Assembler
- H68SD5A-use Emulator (With Real Time Trace Function)
- EPROM On Package Microcomputer; HD614P080S

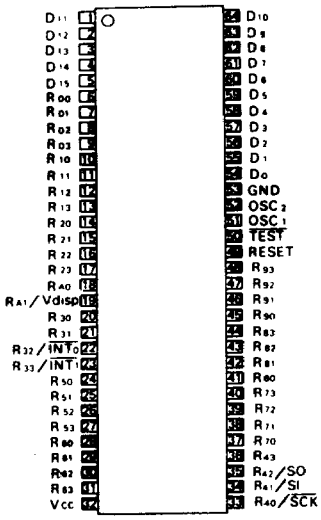
  Mask options are fixed as follows:
  - I/O pin : Open Drain
  - Oscillator : Crystal Oscillator or Ceramic Filter Oscillator (externally drivable)
  - Divider : Divided-by-8

■ HMCS404C/CL/AC CLASSIFICATIONS

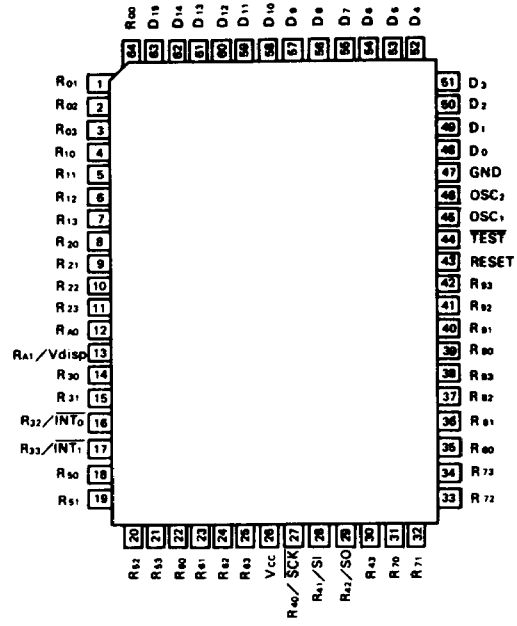
Item \ Type Name	HMCS404C (HD614042)	HMCS404CL (HD614045)	HMCS404AC (HD614048)
V_{CC} (V)	4 ~ 6	2.7 ~ 6	4.5 ~ 6
Minimum Instruction Execution Time (μs)	2	4	1.33

Data Sheets contain information for automotive operation only. Refer to **Reference Guide** (Section 9) for a listing of supplementary publications which provide complete specifications.

■ PIN ARRANGEMENT

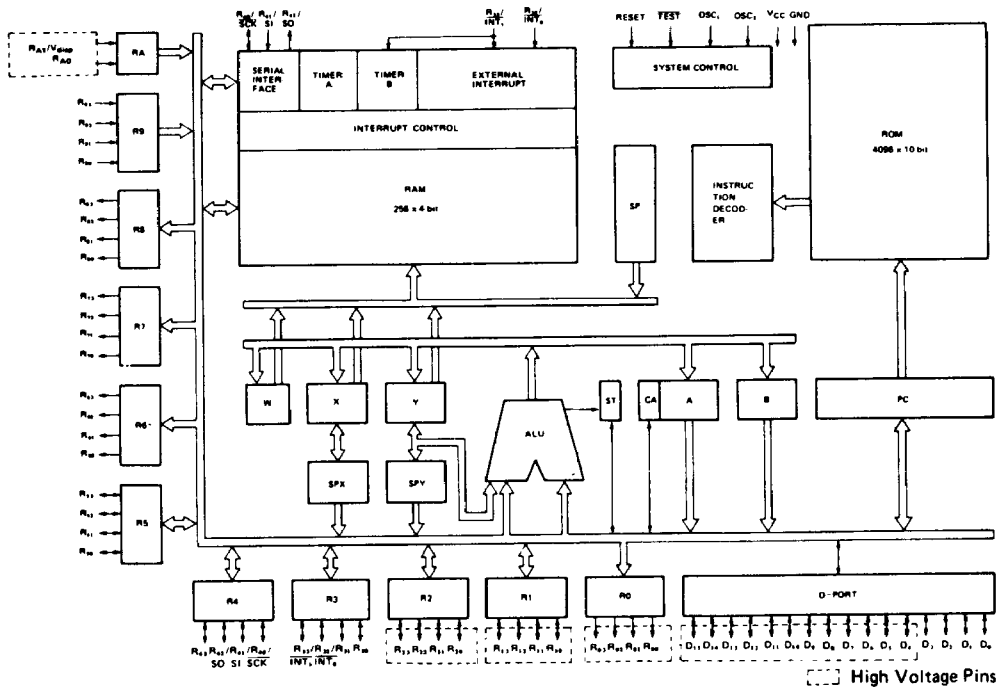


(Top View)



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage	V_T	−0.3 to V_{CC} +0.3	V	3
		V_{CC} −45 to V_{CC} +0.3	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	−40 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.
(Note 2) All voltages are with respect to GND.
(Note 3) Applied to standard pins.
(Note 4) Applied to high voltage pins.
(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.
(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.
(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.
(Note 8) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
(Note 10) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 11) Applied to R0 ~ R2.
(Note 12) Applied to $D_4 \sim D_{15}$.

4

■ HMCS404C ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} –40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions		Value min	Value typ	Value max	Unit	Note
Input "High" Voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$			0.7V_{CC}	–	V_{CC}+0.3	V	
		SI			0.7V_{CC}	–	V_{CC}+0.3	V	
		OSC_1			V_{CC}– 0.5	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$			–0.3	–	0.22V_{CC}	V	
		SI			–0.3	–	0.22V_{CC}	V	
		OSC_1			–0.3	–	0.5	V	
Output "High" Voltage	V_{OH}	$\overline{SCK}$, SO	$-I_{OH}$ = 1.0 mA		V_{CC}–1.0	–	–	V	
			$-I_{OH}$ = 0.01 mA		V_{CC}–0.3	–	–	V	
Output "Low" Voltage	V_{OL}	$\overline{SCK}$, SO	I_{OL} = 1.6 mA		–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	V_{in} = 0V to V_{CC}		–	–	1	µA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	V_{CC}=5V	Crystal or Ceramic Filter Oscillator Option f_{osc} = 4MHz	–	–	2.0	mA	2, 6
				Resistor Oscillator Option f_{osc} = 4MHz	–	–	2.4	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 5V	Crystal or Ceramic Filter Oscillator Option f_{osc} = 4MHz	–	–	1.2	mA	3, 6
				Resistor Oscillator Option f_{osc} = 4MHz	–	–	1.6	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 5V	Crystal or Ceramic Filter Oscillator Option f_{osc} =4MHz	–	–	0.9	mA	4, 6
				Resistor Oscillator Option f_{osc} = 4MHz	–	–	1.3	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in}(\overline{TEST})$ = V_{CC}–0.3V to V_{CC} V_{in}(RESET) = 0V to 0.3V		–	–	10	µA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}			2	–	–	V	

(Note 1) Pull-up MOS current and output buffer current are excluded.
(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage

(Note 5) Pull-down MOS current is excluded.
(Note 6) When f_{osc}=x [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value } (f_{osc}=x\,[\text{MHz}]) = \frac{x}{4} \times \text{max. value } (f_{osc}=4\,[\text{MHz}])$$

4

- **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
  (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "High" Voltage	V_{IH}	$D_0 \sim D_3$, R3 ~ R5, R9		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3$, R3 ~ R5, R9		−0.3	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 1.0 mA	V_{CC}−1.0	–	–	V	1
		$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 0.01 mA	V_{CC}−0.3	–	–	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3$, R3 ~ R8	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$D_0 \sim D_3$, R3 ~ R9	V_{in} = 0V to V_{CC}	–	–	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 5V, V_{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.
(Note 2) Pull-up MOS current and output buffer current are excluded.
(Note 3) Applied to I/O pins with "with Pull-up MOS" selected by mask option.

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
  (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "High" Voltage	V_{IH}	D_4 ~ D_{15}, R1 R2, R_{A0}, R_{A1}		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	D_4~D_{15}, R1 R2, R_{A0}, R_{A1}		V_{CC}−40	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	D_4 ~ D_{15}	$-I_{OH}$=15mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=9 mA	V_{CC}−2.0	–	–	V	
		R0 ~ R2	$-I_{OH}$=3 mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=1.8 mA	V_{CC}−2.0	–	–	V	
Output "Low" Voltage	V_{OL}	D_4~D_{15} R0~R2	V_{disp} = V_{CC}−40V	–	–	V_{CC}−37	V	1
		D_4~D_{15} R0~R2	150kΩ to V_{CC}−40V	–	–	V_{CC}−37	V	2
Input/Output Leakage Current	$\|I_{IL}\|$	D_4~D_{15} R0~R2 R_{A0}, R_{A1}	V_{in} = V_{CC}−40V to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	D_4~D_{15} R0~R2 R_{A0}, R_{A1}	V_{disp} = V_{CC}−35V V_{in} = V_{CC}	125	250	500	μA	4

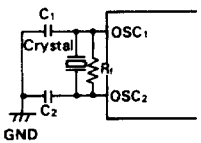
(Note 1) Applied to I/O pins with "with Pull-down MOS" selected by mask option.
(Note 2) Applied to I/O pins with "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
(Note 3) Pull-down MOS current and output buffer current are excluded.
(Note 4) Applied to I/O pins with "with Pull-down MOS" selected by mask option.

● **AC CHARACTERISTICS** (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

	Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Crystal or Ceramic Filter Oscillator	Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	4	4.5	MHz	
	Instruction Cycle Time	t_{cyc}			1.78	2	20	µs	
	Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	20	ms	1
Resistor Oscillator	Oscillation Frequency	f_{osc}	OSC_1, OSC_2	R_f=20kΩ±2%	1.8	3.0	4.2	MHz	
	Instruction Cycle Time	t_{cyc}		R_f=20kΩ±2%	1.9	2.66	4.44	µs	
	Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2	R_f=20kΩ±2%	–	–	0.5	ms	1
External Clock	External Clock Frequency	f_{CP}	OSC_1		0.4	–	4.5	MHz	2
	External Clock "High" Level Width	t_{CPH}	OSC_1		100	–	–	ns	2
	External Clock "Low" Level Width	t_{CPL}	OSC_1		100	–	–	ns	2
	External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
	External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
	Instruction Cycle Time	t_{cyc}			1.78	–	20	µs	2
$\overline{INT_0}$ "High" Level Width		t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width		t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width		t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width		t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width		t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance		C_{in}	all pins	f=1MHz V_{in} = 0V	–	–	15	pF	
RESET Fall Time		t_{RSTf}			–	–	20	ms	4

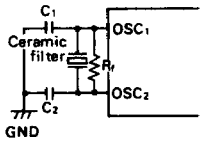
(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.0V at "Power-on", or after RESET input level goes to "High" by resetting to quit the stop mode by MCU reset on the circuits below. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



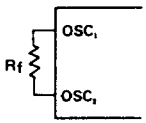
Crystal: 4.194304MHz NC-18C(Nihon Denpa Kogyo)
Rf : 1MΩ ±2%
C_1 : 22pF±20%
C_2 : 22pF±20%

Ceramic filter oscillator



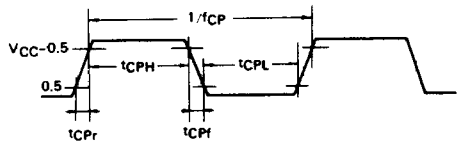
Ceramic filter: CSA4.00MG (Murata)
Rf : 1MΩ±2%
C_1 : 30pF±20%
C_2 : 30pF±20%

Resistor oscillator

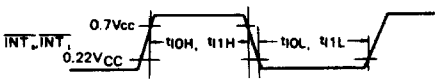


Rf : 20kΩ±2%

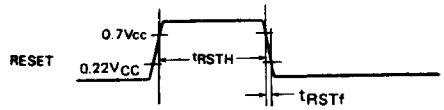
(Note 2)



(Note 3)



(Note 4)



• SERIAL INTERFACE TIMING CHARACTERISTICS

(V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

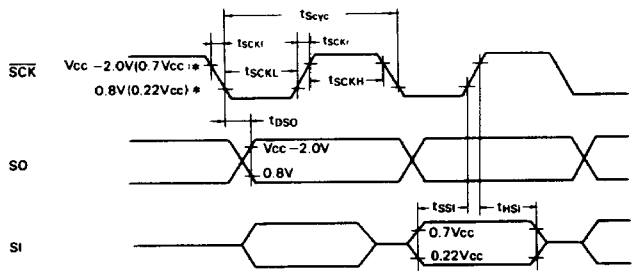
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		500	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

- At Transfer Clock Input

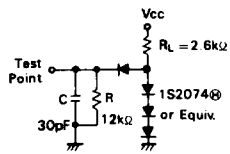
Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		500	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

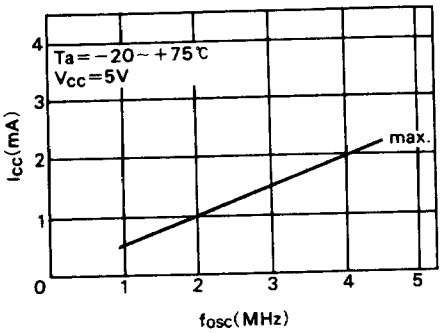


* V_{CC} − 2.0V and 0.8V are the threshold voltage for transfer clock output.
0.7 V_{CC} and 0.22 V_{CC} are the threshold voltage for transfer clock input.

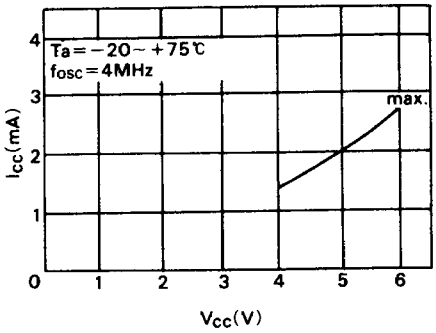
(Note 2) Timing Load Circuit



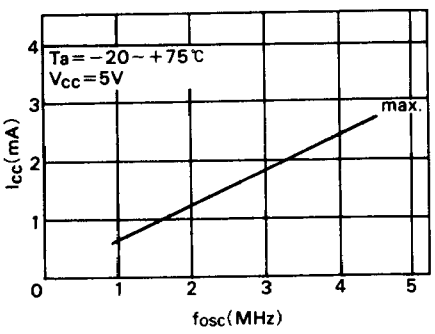
- **CHARACTERISTICS CURVE (REFERENCE DATA)**



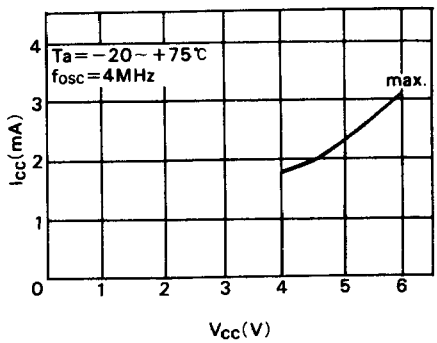
I_{CC} vs. f_{osc} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



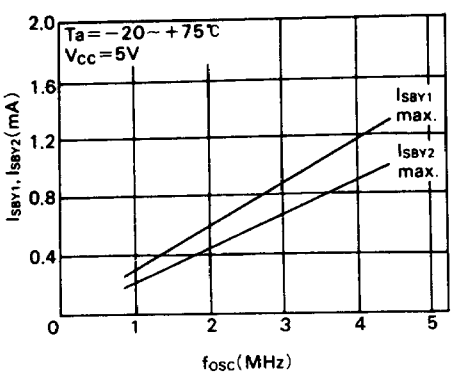
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



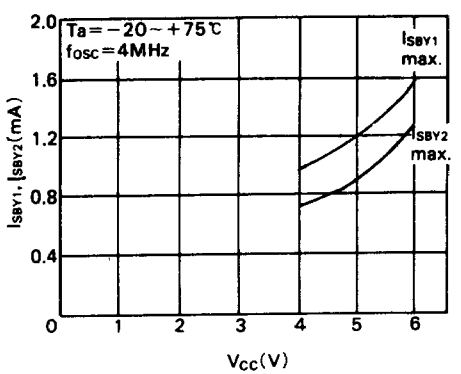
I_{CC} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



I_{CC} vs. V_{CC} Characteristics
(Resistor Oscillator Option)

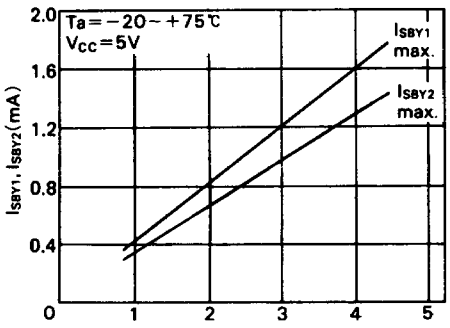


I_{SBY} vs. f_{osc} Characteristics
(Crystal, Ceramic Filter Oscillator Option)

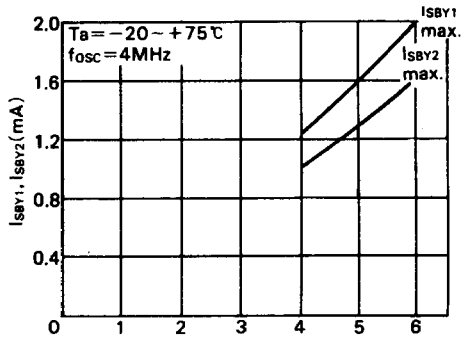


I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)

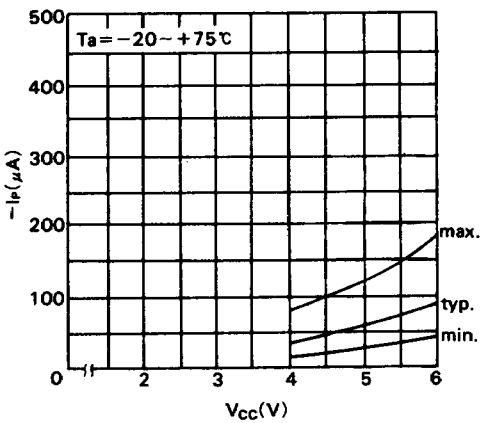
4



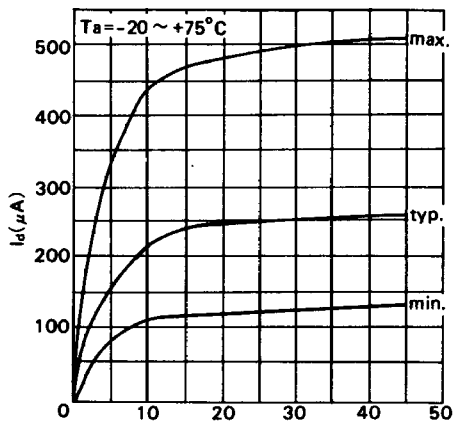
I_{SBY} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



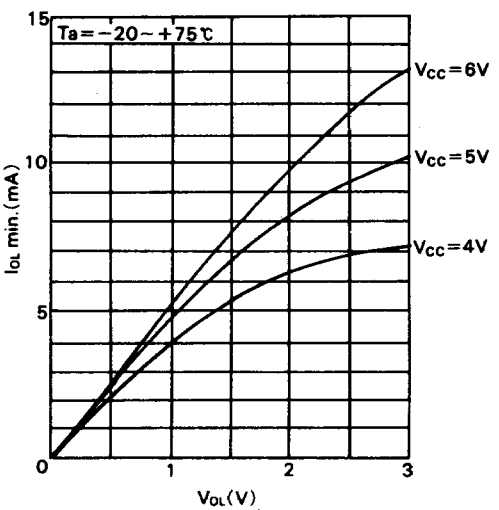
I_{SBY} vs. V_{CC} Characteristics
(Resistor Oscillator Option)



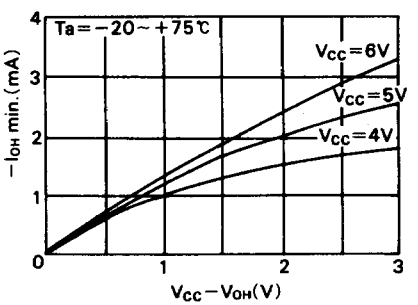
$-I_P$ (Pull-up MOS Current) vs.
V_{CC} Characteristics



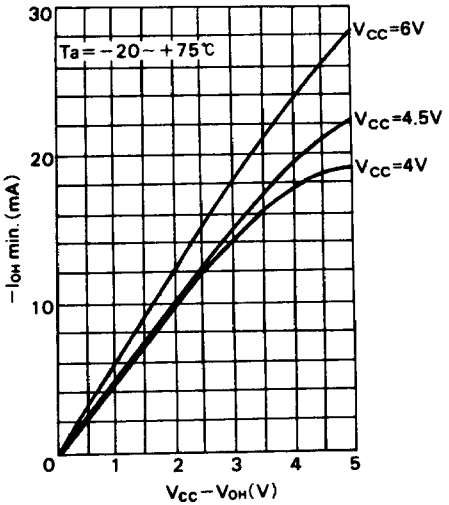
I_d (Pull-down MOS Current) vs.
(V_{CC} − V_{disp}) Characteristics



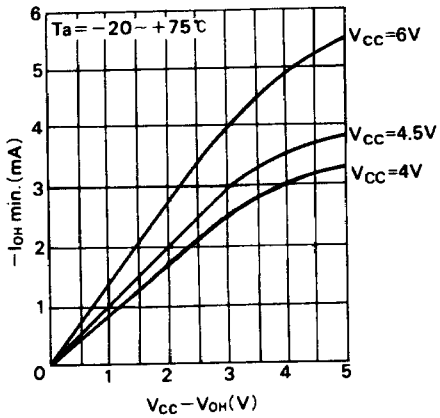
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OH}$ min vs. (V_{CC} − V_{OH}) Characteristics
(Standard Pin "CMOS")



$-I_{OH}$ min. vs. (V_{CC} − V_{OH}) Characteristics
(D_4 ~ D_{15} Pins)



$-I_{OH}$ min. vs. (V_{CC} − V_{OH}) Characteristics
(RO ~ R2 Pins)

4

- **HMCS404CL ELECTRICAL CHARACTERISTICS**
- **DC CHARACTERISTICS** (V_{CC}=2.7V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		0.85V_{CC}	–	V_{CC}+0.3	V	
		SI		0.85V_{CC}	–	V_{CC}+0.3	V	
		OSC_1		V_{CC}−0.3	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		-0.3	–	0.15V_{CC}	V	
		SI		-0.3	–	0.15V_{CC}	V	
		OSC_1		-0.3	–	0.3	V	
Output "High" Voltage	V_{OH}	$\overline{SCK}$, SO	$-I_{OH}$ = 0.1 mA	V_{CC}−0.5	–	–	V	
Output "Low" Voltage	V_{OL}	$\overline{SCK}$, SO	I_{OL} = 0.4mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	V_{in} = 0 V to V_{CC}	–	–	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	V_{CC} = 3 V f_{osc} = 2 MHz	–	–	0.6	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 3 V f_{osc} = 2 MHz	–	–	0.5	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 3 V f_{osc} = 2MHz	–	–	0.4	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	V_{in} ($\overline{TEST}$) = V_{CC}-0.2V to V_{CC} V_{in} (RESET) = 0V to 0.2 V	–	–	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	–	–	V	

(Note 1) Pull-up MOS current and output buffer current are excluded.
(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage

(Note 5) Pull-down MOS current is excluded.
(Note 6) When f_{osc}=x [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:
[When Divide-by-8 (D-8) option is selected.] max. value (f_{osc}=x [MHz]) = $\frac{x}{2}$ x max. value (f_{osc}=2 [MHz])

4

• INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN

(V_{CC} = 2.7V to 6V, GND = 0V, V_{disp} = V_{CC} –40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3$, R3 ~ R5, R9		0.85V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3$, R3 ~ R5, R9		-0.3	–	0.15 V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 0.1 mA	V_{CC}–0.5	–	–	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3$, R3 ~ R8	I_{OL} = 0.4 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$D_0 \sim D_3$, R3 ~ R9	V_{in}= 0V to V_{CC}	–	–	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 3V, V_{in}= 0V	3	15	40	μA	3
		$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 5V, V_{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" output selected by mask option.
(Note 2) Pull-up MOS current and output buffer current are excluded.
(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
  (V_{CC} = 2.7V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		0.85V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		V_{CC}−40	–	0.15V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_4 \sim D_{15}$	$-I_{OH}$=15mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=2.5mA	V_{CC}−1.0	–	–	V	
		R0 ~ R2	$-I_{OH}$=3 mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=0.5 mA	V_{CC}−1.0	–	–	V	
Output "Low" Voltage	V_{OL}	$D_4 \sim D_{15}$ R0~R2	V_{disp} = V_{CC}−40V	–	–	V_{CC}−37	V	1
		$D_4 \sim D_{15}$ R0~R2	150kΩ to V_{CC}−40V	–	–	V_{CC}−37	V	2
Input/Output Leakage Current	$\|I_{IL}\|$	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{in} = V_{CC}−40V to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{disp} = V_{CC}−35V V_{in} = V_{CC}	125	250	500	μA	4

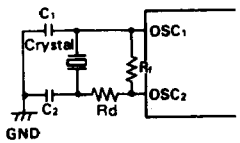
(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.
(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
(Note 3) Pull-down MOS current and output buffer current are excluded.
(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

- AC CHARACTERISTICS (V_{CC}=2.7V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

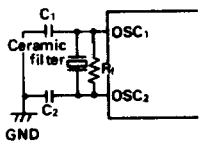
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	2	2.25	MHz	
Instruction Cycle Time	t_{cyc}			3.55	4	20	µs	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	60	ms	1
External Clock "High" Level Width	t_{CPH}	OSC_1		205	–	–	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC_1		205	–	–	ns	2
External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
$\overline{INT_0}$ "High" Level Width	t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width	t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width	t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width	t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance	C_{in}	all pins	f = 1 MHz V_{in} = 0 V	–	–	15	pF	
RESET Fall Time	t_{RSTf}			–	–	15	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. The circuits used to meesure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



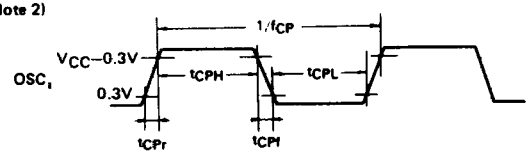
Ceramic filter oscillator



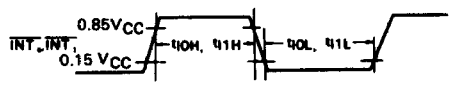
Crystal: 2.097152MHz DS-MGQ308 (Seiko Denshi)
Rf = 2MΩ ± 2%, Rd = 2.2kΩ ± 2%
C_1 = 10pF ± 20%
C_2 = 10pF ± 20%

Ceramic filter: CSA2.000MK (Murata)
Rf = 1MΩ ± 2%, C_1=C_2 = 30pF ±20%

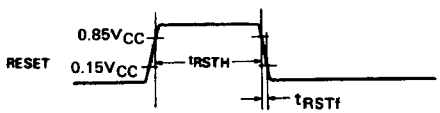
(Note 2)



(Note 3)



(Note 4)



- **SERIAL INTERFACE TIMING CHARACTERISTICS**
  (V_{CC}=2.7V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −40 to +85°C, if not specified.)

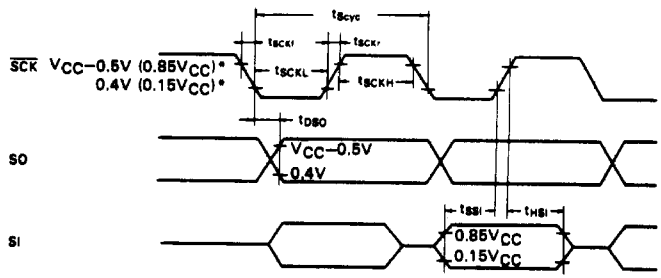
• At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	300	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	300	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	–	–	ns	1

• At Transfer Clock Input

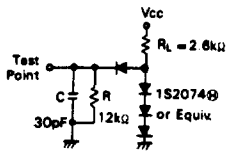
Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	300	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	300	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

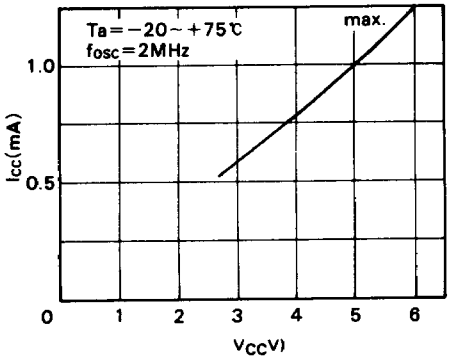


*V_{CC}−0.5V and 0.4V are the threshold voltage for transfer clock output.
0.85V_{CC} and 0.15V_{CC} are the threshold voltage for transfer clock input.

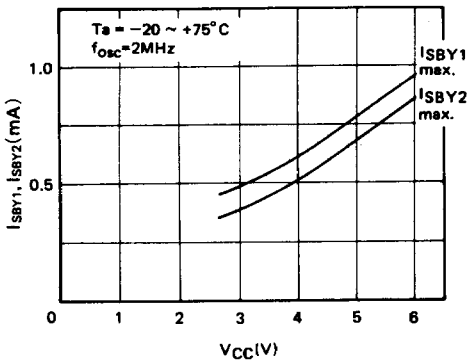
(Note 2) Timing Load Circuit



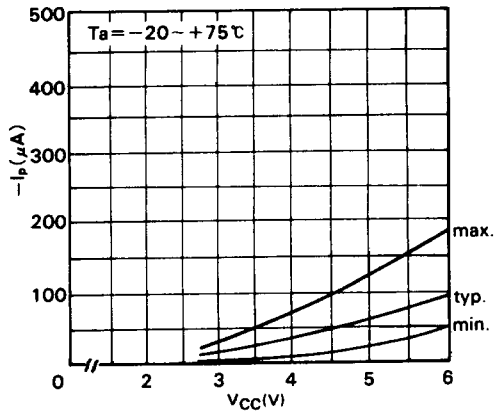
• CHARACTERISTICS CURVE (REFERENCE DATA)



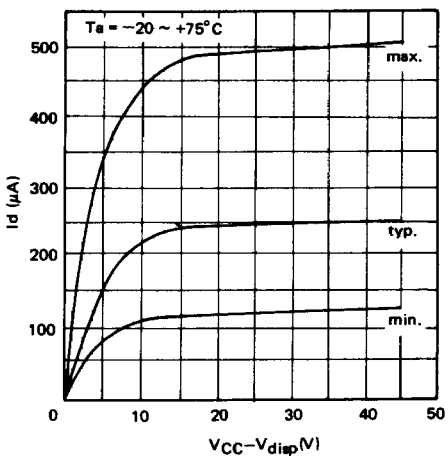
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



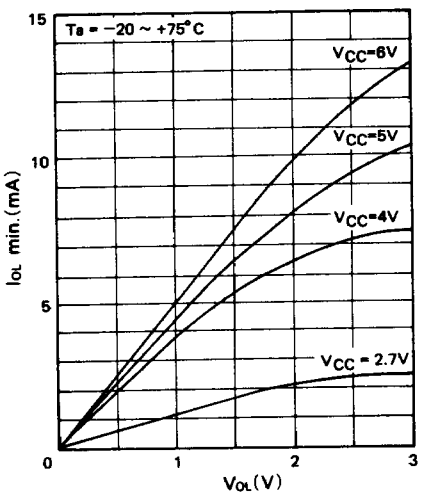
I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



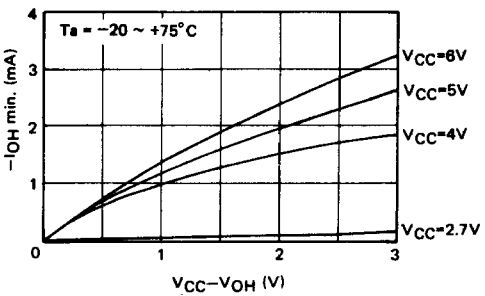
$-I_p$ (Pull-up MOS Current) vs.
V_{CC} Characteristics



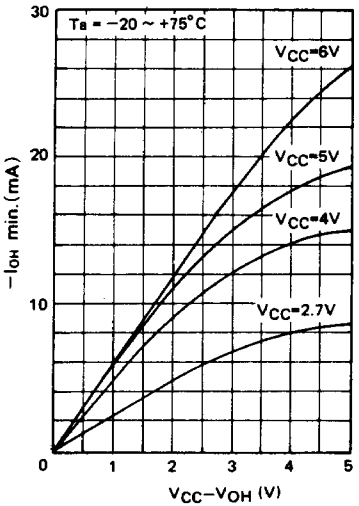
I_d (Pull-down MOS Current) vs.
($V_{CC}-V_{disp}$) Characteristics



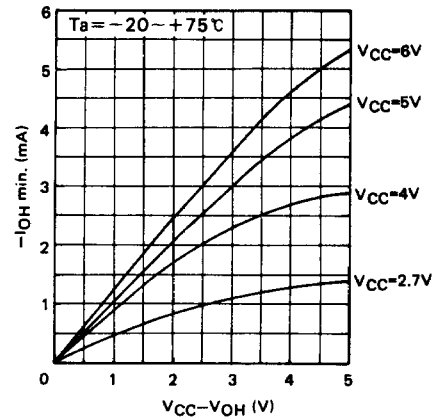
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) Characteristics
(Standard Pin "CMOS")



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) Characteristics
($D_4 \sim D_{15}$ Pins)



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) Characteristics
(R0 ~ R2 Pins)

■ HMCS404AC ELECTRICAL CHARACTERISTICS

• **DC CHARACTERISTICS** (V_{CC} = 4.5V to 6V, GND = 0V, V_{disp} = V_{CC}–40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		0.7V_{CC}	–	V_{CC}+0.3	V	
		SI		0.7V_{CC}	–	V_{CC}+0.3	V	
		OSC_1		V_{CC}–0.5	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		-0.3	–	0.22V_{CC}	V	
		SI		-0.3	–	0.22V_{CC}	V	
		OSC_1		-0.3	–	0.5	V	
Output "High" Voltage	V_{OH}	$\overline{SCK}$, SO	$-I_{OH}$ = 1.0 mA	V_{CC}–1.0	–	–	V	
			$-I_{OH}$ = 0.01 mA	V_{CC}–0.3	–	–	V	
Output "Low" Voltage	V_{OL}	$\overline{SCK}$, SO	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$ SI, SO, OSC_1	V_{in} = 0 V to V_{CC}	–	–	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	V_{CC} = 5 V f_{osc} = 6 MHz	–	–	3.0	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 5 V f_{osc} = 6 MHz	–	–	1.8	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 5 V f_{osc} = 6MHz	–	–	1.35	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	V_{in} ($\overline{TEST}$) = V_{CC} –0.3 V to V_{CC} V_{in} (RESET) = 0V to 0.3 V	–	–	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	–	–	V	

4

(Note 1) Pull-up MOS current and output buffer current are excluded.
(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3~R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0~R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3~R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0~R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3~R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0~R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 5) Pull-down MOS current is excluded.
(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value } (f_{osc}=x\text{[MHz]}) = \frac{x}{6} \times \text{max. value } (f_{osc}=6\text{[MHz]})$$

- **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
  (V_{CC} = 4.5V to 6V, GND = 0V, V_{disp} = V_{CC} – 40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3$, R3 ~ R5, R9		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3$, R3 ~ R5, R9		–0.3	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 1.0 mA	V_{CC}–1.0	–	–	V	1
		$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 0.01 mA	V_{CC}–0.3	–	–	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3$, R3 ~ R8	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$D_0 \sim D_3$, R3 ~ R9	V_{in} = 0V to V_{CC}	–	–	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 5V, V_{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.
(Note 2) Pull-up MOS current and output buffer current are excluded.
(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**

(V_{CC} = 4.5V to 6V, GND = 0V, V_{disp} = V_{CC} – 40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		V_{CC}–40	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_4 \sim D_{15}$	$-I_{OH}$=15mA, V_{CC}=5V ± 10%	V_{CC}–3.0	–	–	V	
			$-I_{OH}$=9mA	V_{CC}–2.0	–	–	V	
		R0 ~ R2	$-I_{OH}$=3mA, V_{CC}=5V ± 10%	V_{CC}–3.0	–	–	V	
			$-I_{OH}$=1.8 mA	V_{CC}–2.0	–	–	V	
Output "Low" Voltage	V_{OL}	$D_4 \sim D_{15}$ R0~R2	V_{disp} = V_{CC}–40V	–	–	V_{CC}–37	V	1
		$D_4 \sim D_{15}$ R0~R2	150kΩ to V_{CC}–40V	–	–	V_{CC}–37	V	2
Input/Output Leakage Current	$\|I_{IL}\|$	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{in} = V_{CC}–40V to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{disp} = V_{CC}–35V V_{in} = V_{CC}	125	250	500	μA	4

(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.
(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
(Note 3) Pull-down MOS current and output buffer current are excluded.
(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

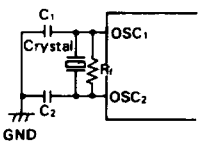
4

- **AC CHARACTERISTICS** (V_{CC}=4.5V to 6V, GND = 0V, V_{disp} = V_{CC} – 40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

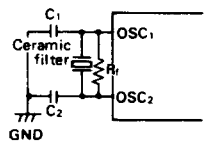
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	6	6.2	MHz	
Instruction Cycle Time	t_{cyc}			1.29	1.33	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	20	ms	1
External Clock "High" Level Width	t_{CPH}	OSC_1		70	–	–	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC_1		70	–	–	ns	2
External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
$\overline{INT_0}$ "High" Level Width	t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width	t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width	t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width	t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance	C_{in}	all pins	f = 1 MHz V_{in} = 0 V	–	–	15	pF	
RESET Fall Time	t_{RSTf}			–	–	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



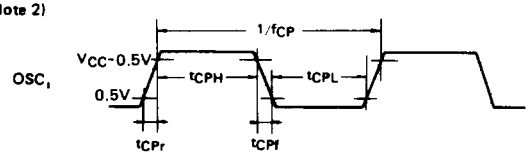
Ceramic filter oscillator



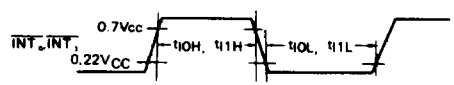
Crystal: 6.0MHz NC-18C (Nihon Denpa Kogyo)
Rf : 1MΩ ±2%
C_1 : 20pF ±20%
C_2 : 20pF ±20%

Ceramic filter : CSA6.00MG (Murata)
Rf : 1MΩ ±2%
C_1 : 30pF ±20%
C_2 : 30pF ±20%

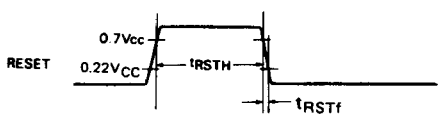
(Note 2)



(Note 3)



(Note 4)



- **SERIAL INTERFACE TIMING CHARACTERISTICS**
  (V_{CC}=4.5V to 6V, GND = 0V, V_{disp} = V_{CC} – 40V to V_{CC}, Ta = –40 to +85°C, if not specified.)

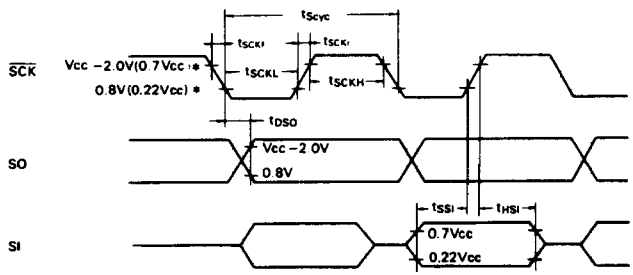
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

- At Transfer Clock Input

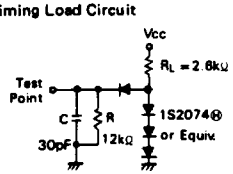
Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

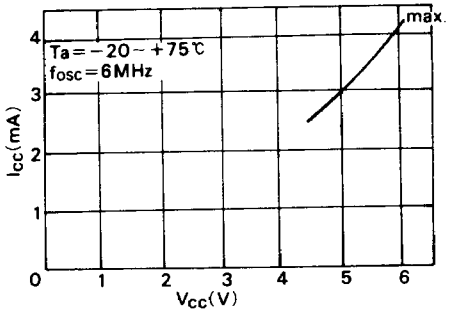


* V_{CC} – 2.0V and 0.8V are the threshold voltage for transfer clock output.
0.7 V_{CC} and 0.22 V_{CC} are the threshold voltage for transfer clock input.

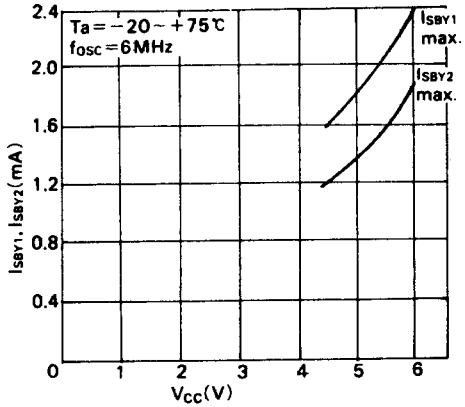
(Note 2) Timing Load Circuit



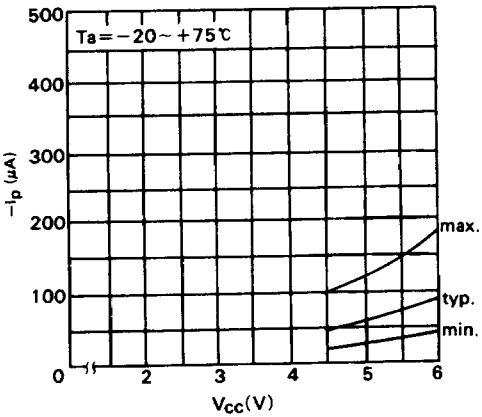
- **CHARACTERISTICS CURVE (REFERENCE DATA)**



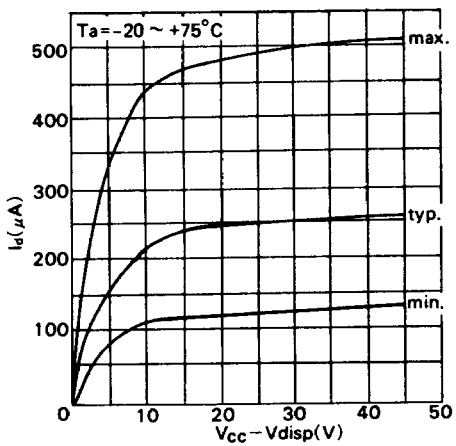
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



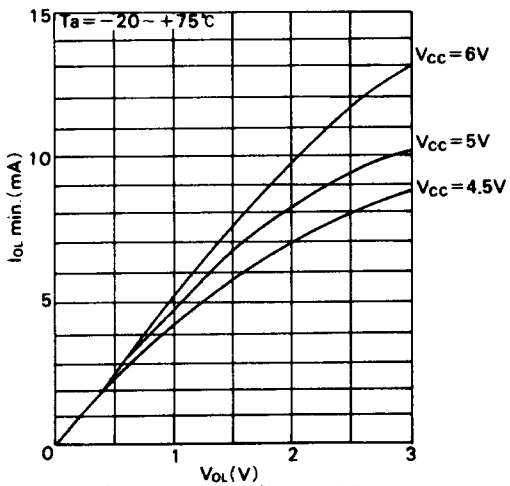
I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



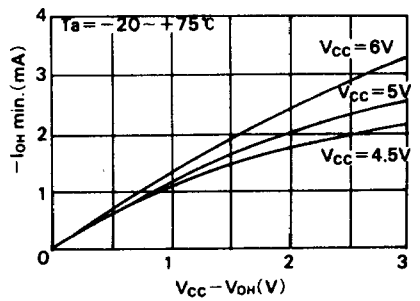
$-I_p$ (Pull-up MOS Current) vs.
V_{CC} Characteristics



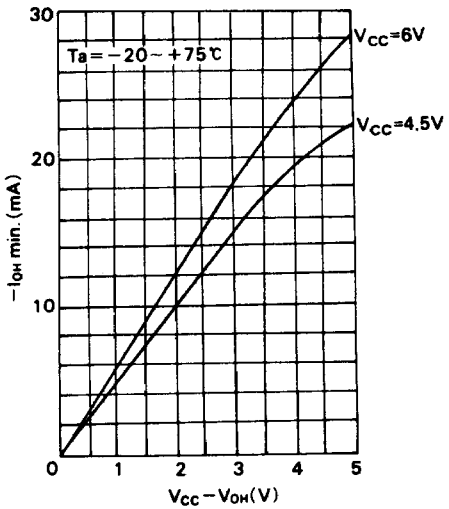
I_d (Pull-down MOS Current) vs.
(V_{CC} − V_{disp}) Characteristics



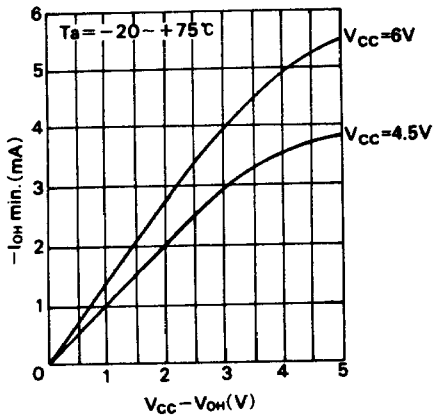
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OH}$ min vs. (V_{CC} − V_{OH}) Characteristics
(Standard Pin "CMOS")



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) Characteristics
($D_4 \sim D_{15}$ Pins)



$-I_{OH}$ min. vs. ($V_{CC} - V_{OH}$) Characteristics
(R0 ~ R2 Pins)

4

■ DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

• GND, V_{CC}, V_{disp}

These are Power Supply Pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. V_{disp} is an power supply for high voltage Input/Output pins with maximum voltage of V_{CC}-40V. V_{disp} pin can be also used as R_{A1} pin by mask option. For details, see "INPUT/OUTPUT".

• $\overline{TEST}$

$\overline{TEST}$ pin is not for user's application. $\overline{TEST}$ must be connected to V_{CC}.

• RESET

RESET pin is used to reset MCU. For details, see "RESET".

• OSC_1, OSC_2

These are Input pins to the internal oscillator circuit. They can be connected to crystal resonator, ceramic filter resonator, R_f oscillator (applicable only to the HMCS404C), or external oscillator circuit. Select the circuit of MCU by mask option corresponding to the oscillator type. For details, see "INTERNAL OSCILLATOR CIRCUIT."

• D-port (D_0 to D_{15})

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. Each pin has the mask option to select its circuit type. For details, See "INPUT/OUTPUT".

• R-port (R0 to RA)

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) R0 and R6 to R8 are output ports, R9 to RA are input ports, and R1 to R5 are Input/Output common ports. R0 to R2 and RA are the high voltage ports, R3 to R9 are the standard ports. Each pin has the mask option to select its circuit type. R_{32}, R_{33}, R_{40}, R_{41} and R_{42} are also available as $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO respectively. For details, see "INPUT/OUTPUT".

• $\overline{INT_0}$, $\overline{INT_1}$

These are the input pins to interrupt MCU operation externally. $\overline{INT_1}$ can be used as an external event input pin for TIMER-B. $\overline{INT_0}$ and $\overline{INT_1}$ are also available as R_{32}, and R_{33} respectively. For details, See "INTERRUPT".

• $\overline{SCK}$, SI, SO

These are Transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI) and serial data output pin (SO) used for serial interface. $\overline{SCK}$, SI, and SO are also available as R_{40}, R_{41} and R_{42} respectively. For details, see "SERIAL INTERFACE".

■ ROM MEMORY MAP

MCU includes 4096 words × 10 bits ROM. ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

• Vector Address Area ..... $0000 to $000F

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

• Zero-Page Subroutine Area ..... $0000 to $003F

CAL instruction allows to branch to the subroutines in $0000 to $003F.

• Pattern Area ..... $0000 to $0FFF

P instruction allows referring to the ROM data in $0000 to $0FFF as a pattern.

• Program Area ..... $0000 to $0FFF