NCS12802

12-Channel I²C Programmable Gamma Voltage Reference Generator with Integrated Auto-read

The NCS12802 is a 12− channel programmable voltage reference generator providing the gamma correction references to the TFT−LCD panel through the source driver circuit.

The twelve output voltage references are programmed through an I²C interface which can operate at standard and high speed. The output buffers can be finely tuned due to the 10 bit DAC precision (1024 steps). In addition, the NCS12802 features an auto−read function which allows uploading binary data from an external EEPROM. To support this capability, the device can act as both slave and master I²C.

In order to accelerate the dynamic correction process, the NCS12802 has two separate register banks. It can simultaneously store two different curves.

The NCS12802 is proposed in a QFN24 package and an operating temperature range from −40°C to +95°C.

Features

- 12−Channel Gamma Generator
- 1024−step Resolution (10 bits)
- Dual Bank
- Rail−to−Rail Outputs
- Auto−read Function to Communicate with External EEPROM
- Two Wire Digital Programming Interface
- Low Power Supply Current of 800 μA per Channel
- Digital Power Supply from 2.3 V to 5.0 V
- Operating Voltage from 9 V to 17.5 V
- I²C Programming Interface (Standard and Fast−Speed)
- ESD Human Body Model Protection 2 kV, Machine Model 300 V
- Operating Temperature Range: −40°C to +95°C
- Available in a QFN−24 Package with Exposed Pad
- This is a Pb−Free Device*

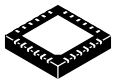
Typical Application

- TFT−LCD TV Panels
- LCD Monitor Panels

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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http://onsemi.com



24 PIN QFN, 4x4
MN SUFFIX
CASE 485L

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCS12802MNTXG	QFN−24 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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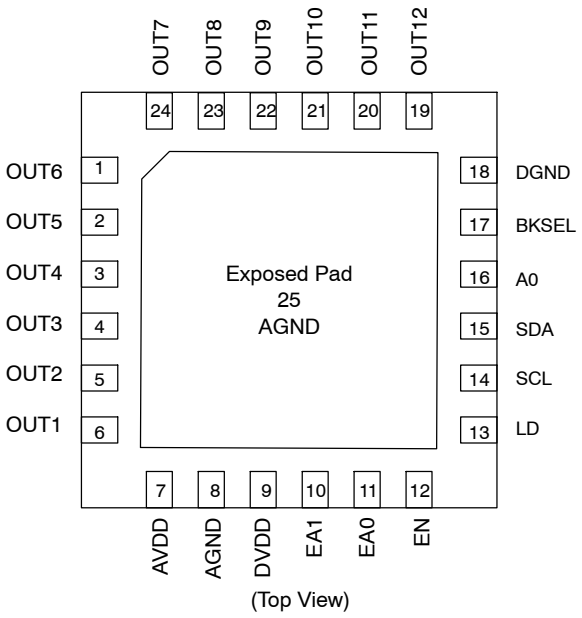


Figure 1. QFN−24 Pinout (Top View)

PIN FUNCTION AND DESCRIPTION

Pin	Name	Type	Description
1	OUT6	Output	Gamma Correction Reference Voltages − Channel 6
2	OUT5	Output	Gamma Correction Reference Voltages − Channel 5
3	OUT4	Output	Gamma Correction Reference Voltages − Channel 4
4	OUT3	Output	Gamma Correction Reference Voltages − Channel 3
5	OUT2	Output	Gamma Correction Reference Voltages − Channel 2
6	OUT1	Output	Gamma Correction Reference Voltages − Channel 1
7	AVDD	Power	Analog Power Supply
8	AGND	Ground	Analog ground (Note 1)
9	DVDD	Power	Digital Power Supply
10	EA1	Input	EEPROM select bit 1, Pin tied to 0 if auto−read is not used
11	EA0	Input	EEPROM select bit 0, Pin tied to 0 if auto−read is not used
12	EN	Input	EEPROM enable, Pin tied to 0 if auto−read is not used
13	LD	Input	Latch Pin
14	SCL	Clock	I^2C Clock
15	SDA	Input	I^2C Data
16	A0	Input	Slave Address
17	BKSEL	Input	Bank Select
18	DGND	Ground	Digital Ground (Note 1)
19	OUT12	Output	Gamma Correction Reference Voltages − Channel 12
20	OUT11	Output	Gamma Correction Reference Voltages − Channel 11
21	OUT10	Output	Gamma Correction Reference Voltages − Channel 10
22	OUT9	Output	Gamma Correction Reference Voltages − Channel 9
23	OUT8	Output	Gamma Correction Reference Voltages − Channel 8
24	OUT7	Output	Gamma Correction Reference Voltages − Channel 7

1. Exposed Pad AGND and DGND pins must be electrically connected to the same potential

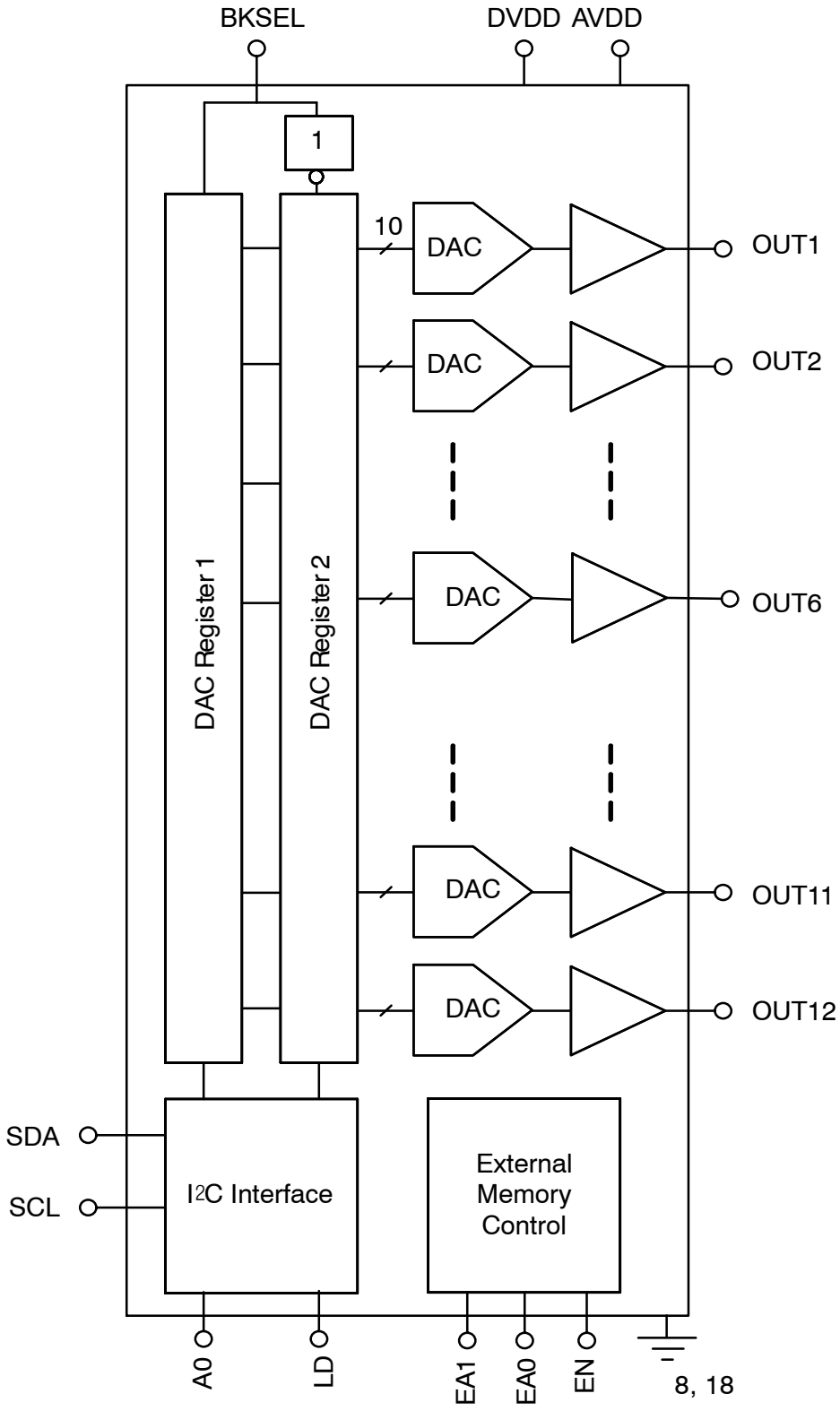


Figure 2. Application Schematic (example)

ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model (HBM) (Note 2) Machine Model (MM)	 2 kV 300 V
Moisture sensitivity (Note 3)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test	

2. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
3. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages	AVDD	22	Vdc
Power Supply Voltages referenced to GND	DVDD	6	Vdc
Signal Input Terminals (SCL, SDA, AO, LD, EN, EA0, EA1, BKSEL) Voltage Current	 V_I I_I	 $-0.5 \le V_I \le 6$ ±10	 Vdc mA
Output Short Circuit (Note 4)	I_{sc}	Continuous	mA
Maximum Junction Temperature (Note 4)	T_J	+125	°C
Operating Ambient Temperature	T_A	−40 to +95	°C
Storage temperature	T_{stg}	−65 to +150	°C
Thermal Resistance QFN−24 with Thermal Pad, Junction−to−Ambient	$R_{\theta JA}$	30	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

THERMAL RATINGS

Parameters	Symbol	Rating	Unit
Junction−to−Ambient Thermal Resistance (Note 6)	θ_{JA}	35	°C/W
Junction−to−Case (top) Thermal Resistance	θ_{JCtop}	20.6	°C/W
Junction−to−Board Thermal Resistance	θ_{JB}	9.0	°C/W
Junction−to−Top Characterization Parameter	Ψ_{JT}	0.3	°C/W
Junction−to−Board Characterization Parameter	Ψ_{JB}	8.9	°C/W
Junction−to−Case (bottom) Thermal Resistance	$\theta_{JCbottom}$	1.2	°C/W
Operating Ambient Temperature	T_A	−40 to +95	°C
Storage temperature	T_{stg}	−65 to +150	°C

5. Power dissipation must be considered to ensure maximum junction temperature (θ**JA**) is not exceeded.
6. Thermal Pad attached to PCB, 0lfm airflow, and 76 mm x 76 mm copper area.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Conditions	Symbol	Min	Type	Max	Unit
Analog Power Supply		AV_{DD}	9	15	17.5	V
Digital Power Supply		DV_{DD}	2.3	3.3	5	V

ELECTRICAL CHARACTERISTICS AV_{DD} = +15 V, DV_{DD} = 3.3 V, RL = 1.5 kΩ connected to ground, T_A = 25°C, CL = 200 pF, unless otherwise specified

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
ANALOG						
V_{rst}	Reset Value	All outputs set to Code 0000h		0.015	0.12	V
V_{oh}	Buffer Output Swing – High (T_A = −40°C to + 95°C)	OUT1 to OUT12 – Code 03FFh – Sourcing 10 mA OUT1 to OUT12 – Code 03FFh – Sourcing 5 mA	14.7 14.8	 14.9		V
V_{ol}	Buffer Output Swing – Low (T_A = −40°C to + 95°C)	OUT1 to OUT12 – Code 0000h – Sinking 10 mA OUT1 to OUT12 – Code 0000h – Sinking 5 mA		0.15 0.075	0.25 0.15	V
I_o	Continuous Output Current	Code 3FFh		30		mA
INL	Integral Non−linearity	V_{out} = GND + 0.3 V to AVDD − 0.3 V		0.3		LSB
DNL	Differential Non−linearity	V_{out} = GND + 0.3 V to AVDD − 0.3 V		0.3		LSB
ΔG	Gain Error	V_{out} = GND + 0.3 V to AVDD − 0.3 V		0.12		%
L_{Reg}	Load Regulation	10 mA, All Buffers V_{out} = AVDD / 2, I_{out} = +10 mA to −10 mA 5 mA Step		0.5		mV/ mA
T_D	Program to Out Delay			2		μs
Tbksel	Bank Switching Delay	LD Pin = 0, V_{out} = 50% of Code 1023, AVDD = 9 V		1	3.5	μs
I²C ELECTRICAL CHARACTERISTICS						
F_{CLK}	Clock Frequency (−40°C to +95°C)	Standard/Fast Mode High Speed Mode			400 3.4	kHz MHz
V_{IL}	Low Level Input Voltage	SDA or SCL			0.3 x DVDD	V
VIH	High Level Input Voltage	SDA or SCL	0.7 x DVDD			V
VOL	Low Level Output Voltage (Logic 0)	I_{sink} = 3 mA		0.1	0.4	V
FMEM	EEPROM Clock Speed	Master Mode		66	100	kHz
ANALOG POWER SUPPLY						
I_{AVDD}	Analog Supply Current	Outputs at Reset Values, No load Over temperature from −40°C to 95°C		2.8	7 8	mA
PSRR	Power Supply Rejection Ratio	F = 70 kHz, Vac = 1 V_{PP} on AVDD line		−75		dB
DIGITAL POWER SUPPLY						
I_{DVDD}	Digital Supply Current	Outputs at Reset Values, No load, Two Wires Inactive Over temperature from −40°C to 95°C		95 95	250	μA
DIGITAL VOLTAGE LEVELS						
V_{IH}	High Level Input Voltage (Logic 1)		0.7 x DVDD			V
V_{IL}	Low Level Input Voltage (Logic 0)				0.3 x DVDD	V
I_{leak}	Input Leakage Current			±0.01	±10	μA
POR	Power On Reset		1.1	1.5	1.7	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Observe maximum power dissipation. Exposed thermal die is soldered to the PCB using thermal vias.

TYPICAL CHARACTERISTICS

T_A = +25°C, AV_{DD} = 15 V, DV_{DD} = 3.3 V, R_L = 1.5 kΩ connected to Ground, C_L = 200 pF, unless otherwise specified

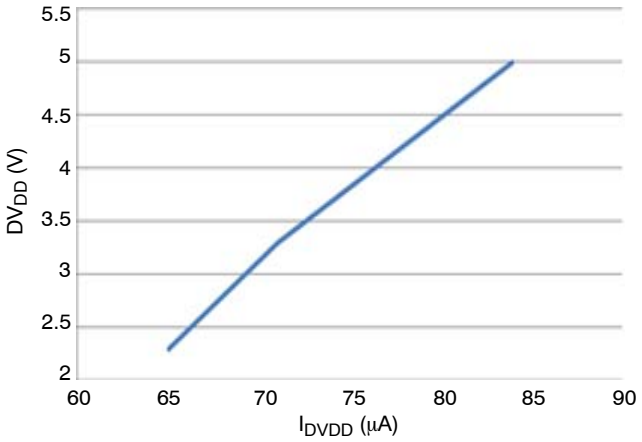


Figure 3. Digital Supply Voltage vs Supply Current

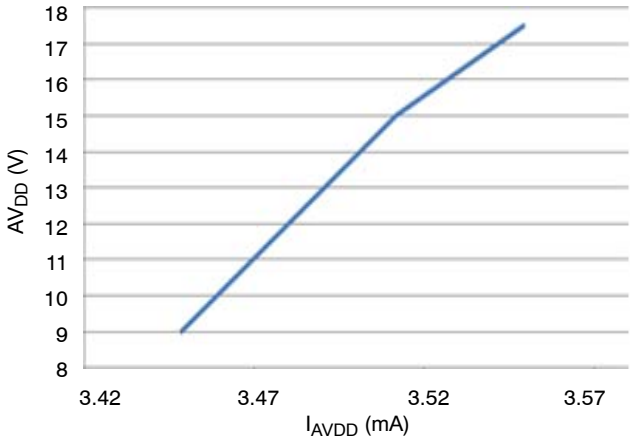


Figure 4. Analog Supply Voltage vs Analog Supply Current

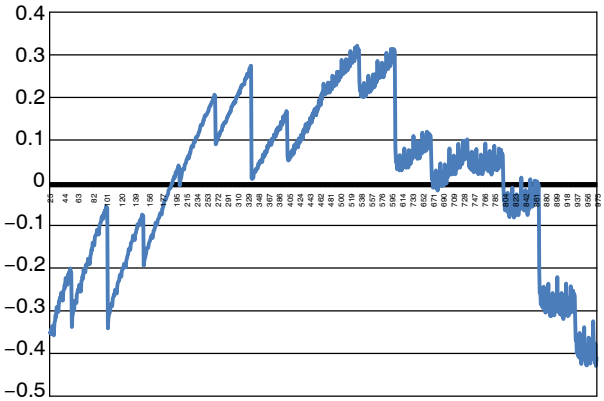


Figure 5. Integral Non Linearity Error vs Input Code

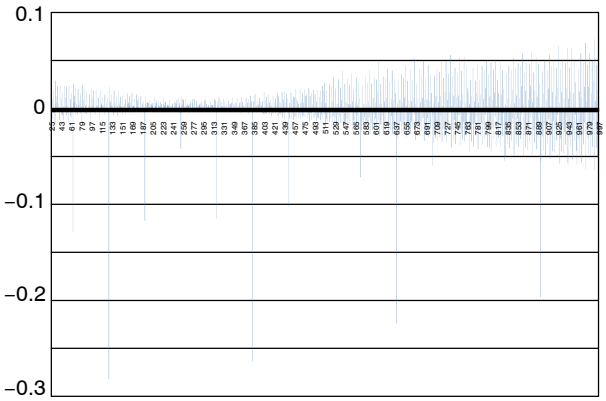


Figure 6. Differential Non Linearity Error vs Input Code

TYPICAL CHARACTERISTICS

T_A = +25°C, AV_{DD} = 15 V, DV_{DD} = 3.3 V, R_L = 1.5 kΩ connected to Ground, C_L = 200 pF, unless otherwise specified

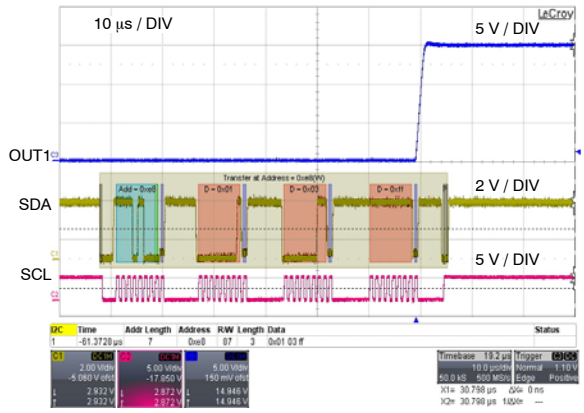


Figure 7. Large Signal Response (rising from 0 V to 15 V)

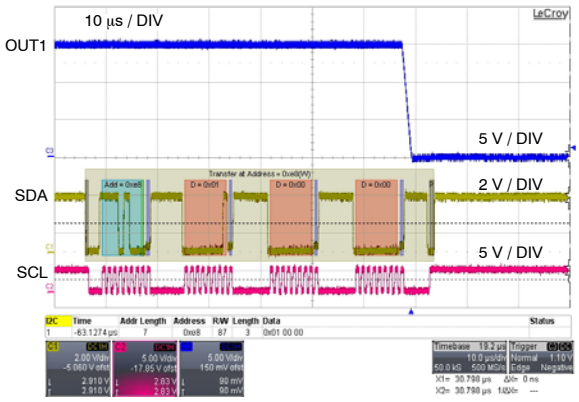


Figure 8. Large Signal Response (Falling from 15 V to 0 V)

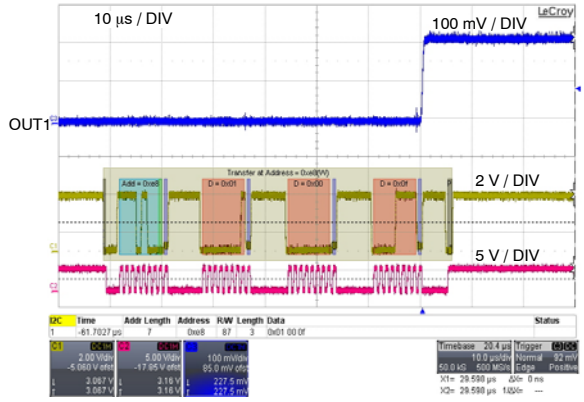


Figure 9. Small Signal Response (Rising from 0 V to 200 mV)

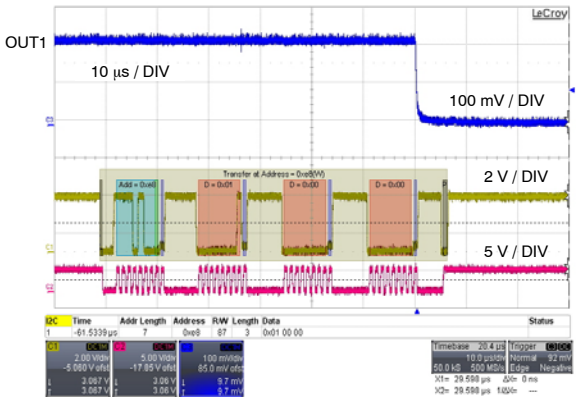


Figure 10. Small Signal Response (Falling from 200 mV to 0 V)

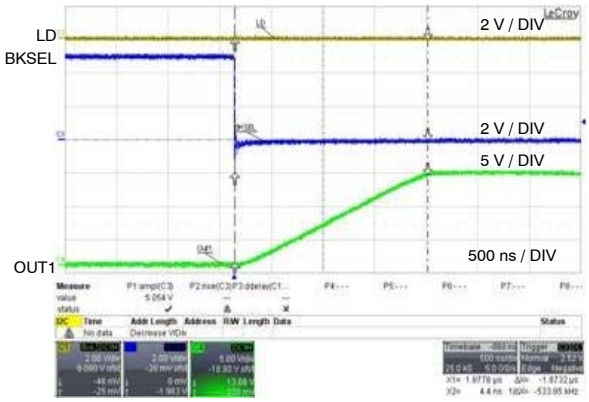


Figure 11. BKSEL Switching Time Delay Low to High

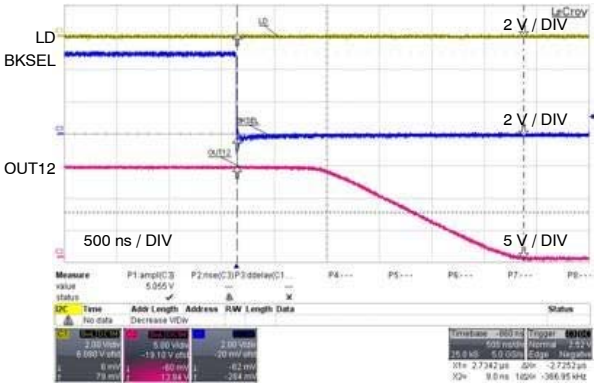


Figure 12. BKSEL Switching Time Delay High to Low

TYPICAL CHARACTERISTICS

T_A = +25°C, AV_{DD} = 15 V, DV_{DD} = 3.3 V, R_L = 1.5 kΩ connected to Ground, C_L = 200 pF, unless otherwise specified

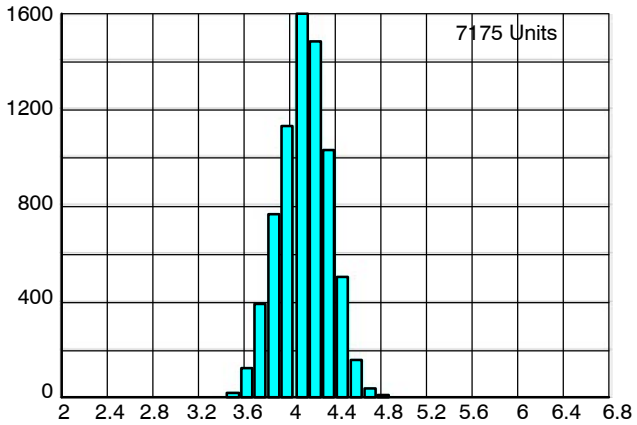


Figure 13. Analog Supply Current Histogram

APPLICATIONS INFORMATION

POWER SUPLIES

The NCS12802 has two power supplies: (AVDD, AGND) and (DVDD, DGND).

DVDD is the digital power supply ranging from 2.3 V to 5.0 V and common to the timing controller and the device control interface. It provides the power supply for the digital circuitry inside the device. AVDD is the analog power supply and ranges from 9 V to 17.5 V offering a wide dynamic voltage range to the gamma reference generator particularly suitable for medium size and big size LCD panels.

DVDD must be applied prior to or together with AVDD in order to prevent excessive power and current consumption (damage to the device may occur if AVDD left connected for an extended time without DVDD).

BUFFERS

The NCS12802 offers twelve programmable voltage references each with 10 bits resolution (1024−steps). Due to an I^2C interface, a double−register structure per channel allowing data pre−loading, the NCS12802 allows fast, easy and dynamic updating of all the voltage references alternatively. The two−wire interface can be connected to standard (100 kHz), fast mode (400 kHz) or even a High Speed mode (3.4 MHz) I^2C bus. Each buffer is capable of full−scale change in output voltage in less than 5 μs.

All buffers can be driven to within 200 mV of the positive supply rail, and to within 0.07 V of the ground rail. The output can also switch full scale monitoring LD or BSKSEL pins in 5 μs.

I^2C SERIAL CONTROL INTERFACE INTRODUCTION

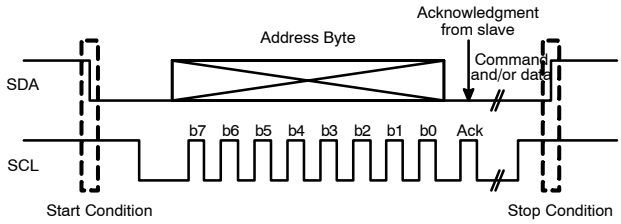


Figure 14. I^2C Bus Format

The NCS12802 communicates with the external timing controller using an I^2C communication protocol. The NCS12802 is intended to operate also as a master controller depending on logic pins configuration. It is under the control of the timing controller (master device), which controls the clock (pin SCL) and the read or write operations through SDA. Both pins require pull up resistors on their path for proper operations.

A communication is initiated by the master with a START condition toggling the SDA line from High to Low while SCL is High (Figure 14). The last bit (b0) in the slave address byte indicates if a write or read operation is intended. At the 9^{th} clock pulse the device being addressed responds to the master by performing an Acknowledge (ACK) consisting to pull SDA at a Low level (ACK = SDA LOW right at the 9^{th} clock pulse, see Figure 14). Each byte has to be followed by an acknowledge bit (Ack).

The device receiving the data provides an acknowledge (ACK) by transmitting a 0 on the SDA line during the 9th bit and provides a not−acknowledge (NACK) by transmitting a 1 on the SDA line during the 9th bit.

SDA must remain stable during communication when SCL is High. Any change in SDA, while SCL is High, will be considered as a STOP or START condition. The High or Low state of the data line SDA can only change when the clock signal SCL is Low. At the end of the communication the master provides a STOP condition by toggling SDA Low to High while SCL is High.

Every byte on the SDA line must be 8 bits long. The number of bytes is unrestricted during a communication session.

DEVICE ADDRESS:

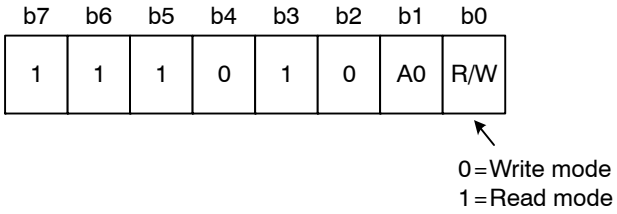


Figure 15. Address Byte Structure

In the first byte of the exchange protocol which contain the device address, the A0 pin is used to define the physical address by comparison with the bit b1 of the address byte. With only one address bit (b1) which provides two different address combinations, the master device can drive up to two NCS12802 devices using the address 111010X. b0 is setting the write or read modes (Write = 0, Read = 1). Consequently, Table 1 gives the address bit allocations considering the read mode and the write mode.

Table 1. ADDRESS BIT ALLOCATIONS

A0	Write Mode	Read Mode
0	E8h	E9h
1	EAh	EBh

NOTE: Other addresses are possible through a simple mask change. Contact ON Semiconductor local sales office or representative for detailed information.

DEVICE RESET AND POWER−ON RESET:

The device has an internal Power−On Reset (POR) Circuit which performs automatically a reset on the NCS12802 while powering up. It is also possible to reset the NCS12802 when it has already been powered up and whenever after or before a communication session. This device reset request is enabled writing the address byte 00h (0000 0000) followed by the data byte 06h (0000 0110). The NCS12802 acknowledges both bytes (00h and 06h) then a STOP will be transferred.

After reset, all the output buffers will be programmed at 0 V, their reset value (code 0000).

OUTPUT VOLTAGE

Buffer output values are determined by the analog suppy voltages and the decimal values of the programmed code using the below equation but also the amplifier performance.

$$V_{out} = \left(\frac{AVDD}{1023} * \text{decimal code}\right) \qquad \text{(eq. 1)}$$

Where decimal code varies from 0 to 1023.

Meanwhile, as no amplifier is perfect, if AVDD = 15 V, the high rail voltage would be typically 14.9 V and low rail voltage would be 0.07 V. As a consequence, the first four bytes will have the same value of 0.07 and the last 7 bytes will have the same value of 15 V (3F9 to 3FF).

NOTE: Other reset values are available as a custom modification – contact local ON Semiconductor Sales office or representative

DATA RATE:

The NCS12802 I^2C bus can operate at three different clock mode:

- The Standard Mode: the clock will run at 100 kHz
- The Fast Mode: the clock will run then at 400 kHz
- The High Speed Mode: clock running at a typical 3.4 MHz

For the Standard and Fast mode there is no need of programming. By default those are the available speed configurations. Meanwhile, it will be required from the user or the system to command the High Speed Mode by sending a special address byte 00001XXX. The undetermined bits are dedicated to the High−Speed capable master and it is noticeable the LSB of this byte is not dedicated to a Read nor a Write command. This specific addressing is called the High Speed Master Code. After the START condition, the clock is still running ≤ 400 kHz but the 12802 will not acknowledge the data. It will internally switch the appropriate filters and operate at 3.4 MHz until the next STOP command.

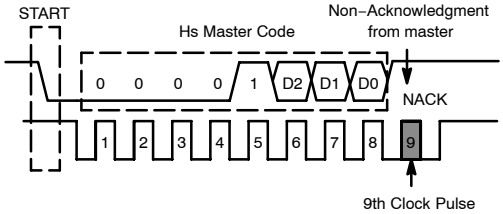


Figure 16. High Speed Master Code

EEPROM INTERFACE

EEPROM Pins EA0 and EA1:

The EA0 and EA1 pins allow the selection of the EEPROM size. The table below shows the start and stop addresses to load properly the DAC registers. Those two pins must be at a steady state before the auto−read command is ordered.

Table 2. MEMORY ADDRESSING

EA0	EA1	Register A		Register B		Tolerated EEPROM (8) and (9)
		Start Word Address	End Word Address	Start Word Address	End Word Address	
0	0	0d	23d	24d	47d	1k, 2k, 4k, 8k, 16k
0	1	361d	384d	405d	428d	2k, 4k, 8k, 16k
1	0	0d	23d	24d	47d	32k, 64k, 128k, 256k and larger
1	1	361d	384d	405d	428d	32k, 64k, 128k, 256k and larger

8. Any applicable EEPROM chip select pins (A2, A1, A0) must be hardwired to GND.
9. When EA0 = 0 and EA1 = 1, it is required that the types of EEPROM that supports Page/Block address definition with chip select pins (for example, A0 is part of the Word Address).

The EN Pin:

The status of the EN pin set the mode of operation of the NCS12802 at the Power On Reset meaning Slave or Master. If EN = 1, the device act as a master and when the data upload is completed, the NCS12802 goes back to slave mode. Reciprocally, if EN = 0, the part acts as a slave.

Table 3. AUTO−READ LOGIC

EN Pin	State	Auto−Read
Low	0	Disabled
High	1	Enabled

Note that once in slave mode and after a POR, the EN status has no effect on the device unless a general call reset (GCR) or a read again function (RA) is commanded. This EN pin is recommended to be tied to DVDD if the application allows it to allow the device enter a master mode without external monitoring. But if only the slave mode is needed, the user may keep this pin tied to GND.

THE POWER ON RESET (POR) AUTO−READ FUNCTION

The Power on Reset master mode auto−read function is illustrated with the timing diagrams Figure 19. It's 5 ms after the POR conditions (DVDD > 1.5 V) is met that the NCS12802 attempts to read the external EEPROM. It is followed with a request from the NCS12802 containing an EEPROM address followed by an acknowledge (100 μs). If the communication link with the EEPROM is well established, the download is completed in 6.7 ms (See Figure 18). Meanwhile after the five first milliseconds after Power up Condition, if the EEPROM device ID is not acknowledged, the device will go back to slave mode. The NCS12802 will remain in slave mode until another General Call Reset (GCR), Read Again (RA) or Power On Reset (POR) condition arrives.

The EN pin should be set to a high level within 5 ms of crossing the POR condition. If the EN state is not at a high steady state during this time, the NCS12802 will go back to slave mode. If the Master Mode needs to be stopped during an auto−read process, the EN pin can be set to a low logic level ('0' logic). Then, the device will go back to slave mode.

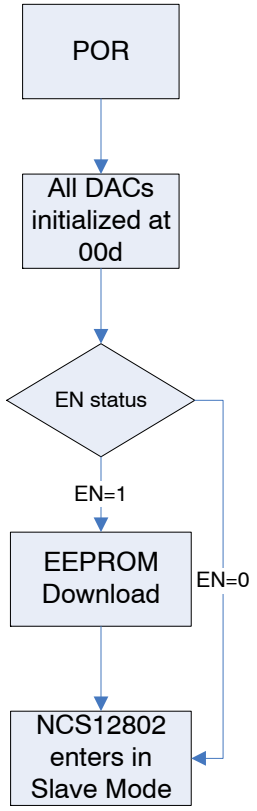


Figure 17. POR Process

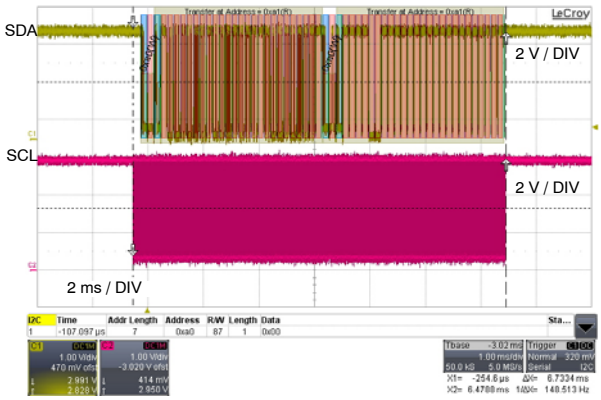


Figure 18. Duration of EEPROM Download

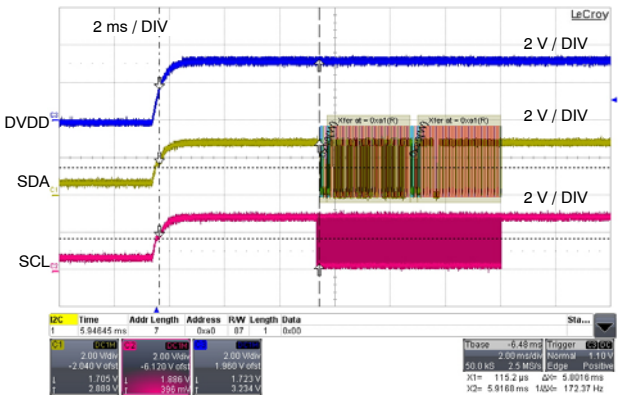


Figure 19. Power Up Sequence

THE MASTER MODE CLOCK SPEED

The NCS12802 has its own internal clock so when it goes into a master mode, it can generate its own clock on the SCL line.

This frequency is specified to be typically 66 kHz with a maximum of 100 kHz.

When the Autoread mode is activated, the communication bus needs to be available to let the NCS12802 master I^2C initiated properly for the data upload from the EEPROM.

GENRAL CALL RESET (GCR)

The answer from the device to a general call reset instruction is dependent on the status of the EN pin. The command is defined in two parts: one byte for the addressing and one byte of data for the command.

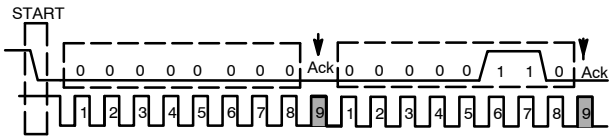


Figure 20. General Call Reset Command

If the EN = 0, when the device receives the GCR command 0006h, all the output buffers will be set to their reset value of 0.07 V (code 0000). If EN = 1 before the first ten queries or 15 ms, then the NCS12802 will download the EEPROM data as indicated previously.

READ AGAIN FUNCTION

When the NCS12802 is in slave mode, a read again function can be initiated to reload data from the EEPROM at any moment. The Read Again (RA) can be described as below in three steps:

- Send to the device address:
  - If A0 = 0 → 74h or 11101000b
  - If A0 = 1 → 75h or 11101010b

The NCS12802 will acknowledge this byte.

- Program the register address 00011100 which will be acknowledged.
- Send two byte of data xxxx xxxx and xxxx xxx1 where x are undefined bits and those bytes will be acknowledged.

DAC OUTPUT UPDATE with LD PIN:

It needs to be understood that updating the register values is very different than updating the DAC outputs because of the double registered structure. Three various methods exist to send the programmed data from the register toward the DACs in order to obtain the desired output voltage:

Method 1: Set the LD pin to a low logic level to update each DAC output voltage as soon as his corresponding register is updated.

Method 2: Set the LD pin to a high logic level to allow all the DAC output voltages to retain their respective values during the data transfer. Then, bring the LD pin voltage low to simultaneously update all the output buffer voltages to the new programmed value.

Method 3 (software mode): The LD pin is maintained at a high logic level and all 12 DACs are updated when the master writes a '1' in bit 15 of any DAC register. The update occurs after receiving the 16 bits of data on the latest register where this '1' has been written.

BKSEL PIN

The BKSEL pin allows the selection of one of the two integrated bank of register in the NCS12802. When the pin is at logic low level, the BANK0 is selected. Reciprocally, when BKSEL = 1, the BANK1 is selected.

During a software mode update of the DAC outputs (method 3 explained above), the bank to be acquired depends on the BKSEL state.

WRITE BOTH BANKS OF DAC REGISTERS

The writes executions are commanded through the I^2C–like bus in slave mode to both banks of registers. As there are different register addresses for the two banks, the BKSEL pin doesn't affect the 'write' command on each of the banks. Table 4 illustrates the non dependence of the BKSEL pin to the write commands.

The “DAC Out” voltage level update is dependent on the status of the LD pin and the BKSEL pin.

- Case 1: Bank1 is updated because LD goes low and BKSEL is high.
- Case 2:Bank0 is updated because LD is low and BKSEL goes low.
- Case 3: No update when LD is high.
- Case 4: Bank0 is updated because BKSEL is low and LD goes low.
- Case 5: Bank1 is updated because LD is low and BKSEL goes high.

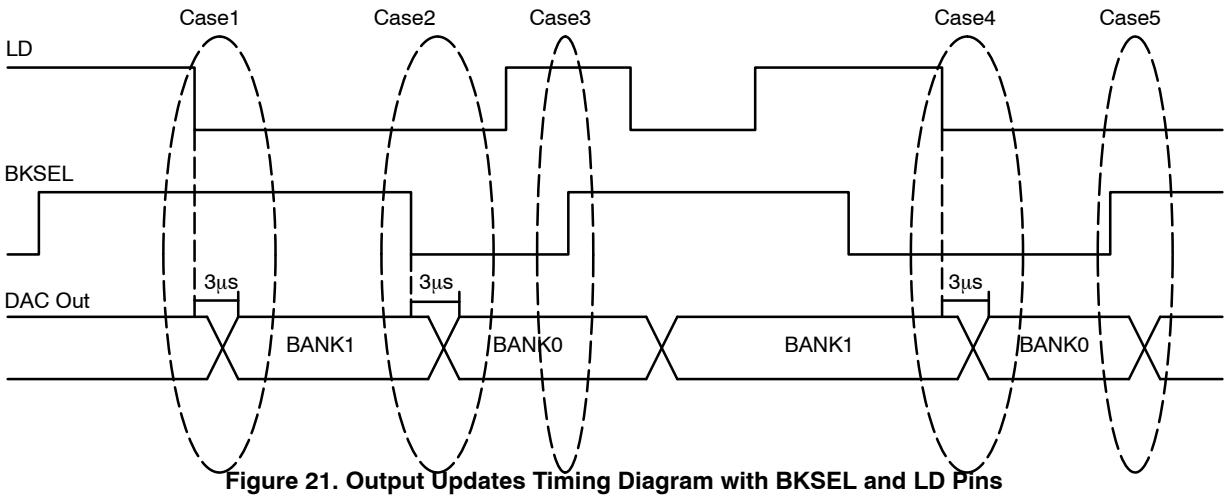


Figure 21. Output Updates Timing Diagram with BKSEL and LD Pins

Table 4. REGISTERS ADDRESSES

Gamma Buffer Output	Register	BANK0					Register	BANK1				
		R4	R3	R2	R1	R0		R4	R3	R2	R1	R0
OUT1	Register 1 BANK0	0	0	0	0	0	Register 1 BANK1	1	0	0	0	0
OUT2	Register 2 BANK0	0	0	0	0	1	Register 2 BANK1	1	0	0	0	1
OUT3	Register 3 BANK0	0	0	0	1	0	Register 3 BANK1	1	0	0	1	0
OUT4	Register 4 BANK0	0	0	0	1	1	Register 4 BANK1	1	0	0	1	1
OUT5	Register 5 BANK0	0	0	1	0	0	Register 5 BANK1	1	0	1	0	0
OUT6	Register 6 BANK0	0	0	1	0	1	Register 6 BANK1	1	0	1	0	1
OUT7	Register 7 BANK0	0	0	1	1	0	Register 7 BANK1	1	0	1	1	0
OUT8	Register 8 BANK0	0	0	1	1	1	Register 8 BANK1	1	0	1	1	1
OUT9	Register 9 BANK0	0	1	0	0	0	Register 9 BANK1	1	1	0	0	0
OUT10	Register 10 BANK0	0	1	0	0	1	Register 10 BANK1	1	1	0	0	1
OUT11	Register 11 BANK0	0	1	0	1	0	Register 11 BANK1	1	1	0	1	0
OUT12	Register 12 BANK0	0	1	0	1	1	Register 12 BANK1	1	1	0	1	1

TIMMING DIAGRAMS

Figure 22 details the timing operations on the NCS12802. The parametric Table 5 indicates all the timing values for the diagram Figure 22.

The Bus is defined as following:

- Bus Idle: Both SDA and SCL lines remain high.
- Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition.

Each data transfer is initiated with a START condition, noted with an S in the diagram below.

STOP Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition, noted with a P in the diagram below.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges data transfer.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, data transfer termination can be signaled by the master generating a Not−Acknowledge on the last byte that has been transmitted by the slave.

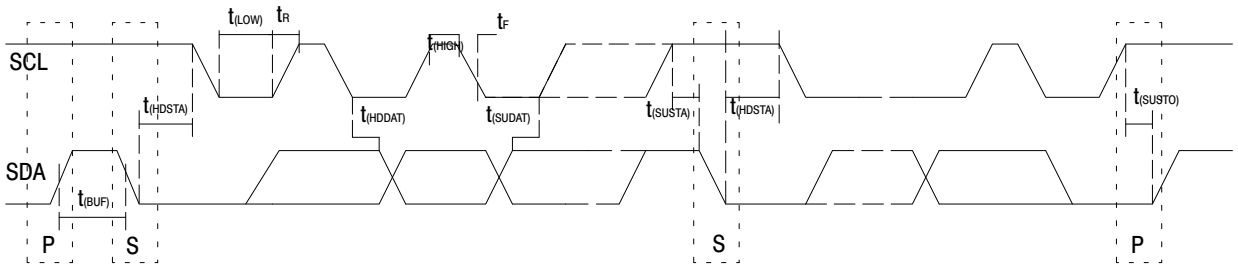


Figure 22. Two Wire timing Diagram

Table 5. TIMING CHARACTERISTICS

Parameters	Standard Mode		Fast Mode		High−Speed Mode		Unit
	Min	Max	Min	Max	Min	Max	
SCL operating frequency **f(SCL)**	0	0.1	0	0.4	0	3.4	MHz
Bus free time between STOP and START conditions **t(BUF)**	4000		600		160		ns
Hold Time after repeated START condition. After this period, the first clock is generated – **t(HDSTA)**	100		100		100		ns
Repeated START condition setup time – **t(SUSTA)**	100		100		100		ns
STOP condition setup time – **t(SUSTO)**	100		100		100		ns
Data Hold Time – **t(HDDAT)**	1 (Note 10)		0 (Note 10)		0 (Note 11)		ns
Data Setup Time – **t(SUDAT)**	250		100		10		ns
SCL clock low period – **t(LOW)**	4700		1300		160		ns
SCL clock high period – **t(HIGH)**	4000		600		60		ns
Clock/Data fall time – **tF**		300		300		160	ns
Clock/Data rise time for SCL ≤ 100 kHz – **tR**		300		300		160	ns
		1000		1000			ns

10. For cases with a fall time of SCL less than 20 ns and/or the rise time or fall time of SDA less than 20 ns, the hold time should be greater Than 20 ns
11. For cases with a fall time of SCL less than 10 ns and/or the rise or fall time of SDA less than 10 ns, the hold time should be greater than 10 ns.

SELECTION OF THE GAMMA CURVE

One of the features on the NCS12802 is to have two banks of volatile memory. It allows the device to store two different gamma reference curves. The BKSEL logic pin controls the selection of the register choice. All the twelve outputs will be programmed simultaneously after a maximum of 11.7 ms depending on the other logic pins.

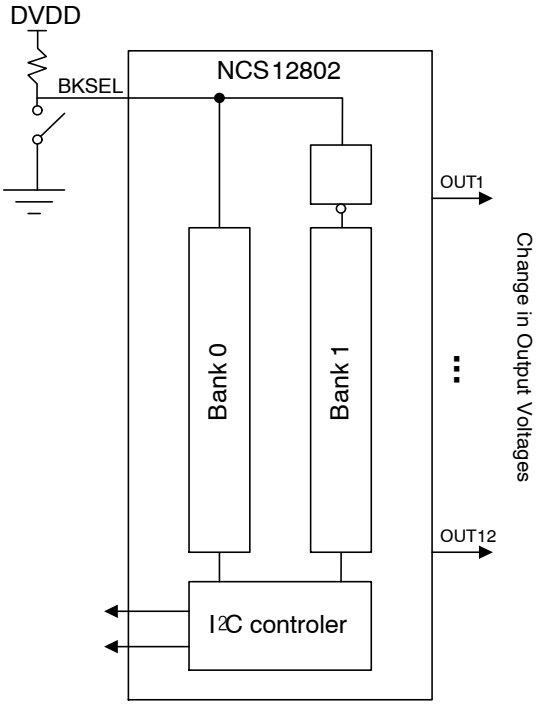


Figure 23. Gamma Control

DYNAMIC GAMMA CONTROL

Initially, the gamma correction was performed statically meaning that the correction curve was programmed only once and generally during the manufacturing phase of the flat panel TV. This second generation of gamma buffers provides a dynamic correction. It happens during the vertical synchronization of the picture. This is the non visible part of the video signal where the picture starts. So, at that particular moment, the correction is applied for every frame. As a consequence, it significantly improves the quality of the displayed movie.

Technically, this enhancement is possible thanks to feature like:

- The double−register structure.
- The High Speed interface mode
- The possible simultaneous update of all the buffers.

During the operation of the TV and after a first correction is applied on a first frame, the register is updated with new information to correct the next frame and is ready to release the references by appropriately controlling the LD pin. The whole interest is that the NCS12802 is being updated in parallel at the same time when the picture is displayed.

Example to perform a software update of the twelve channels simultaneously:

1. The LD pin needs to be set at a high logic level.
2. Write into the DACs registers from 1 to 12 keeping the bit 15 always at a low logic level ‘0’.
3. Command a second write to any DAC having this time identical data but the bit 15 set to a logic high level. Then, all DACs are updated simultaneously after receiving the 16 bits of data.

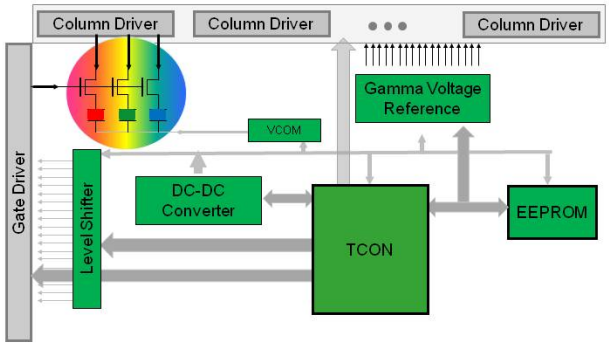


Figure 24. Application Architecture

I²C COMMUNICATION PROTOCOL

Through the I²C interface (SDA, SCL, A0), timing or system controller is able to read from or write to the register content of a single DAC or multiple DACs in a single communication session. The table below (Table 4) gives the addresses of the different DACs from VG1 to VG12.

Writing a Single or Multiple DAC Registers (Figure 25):

The master has to provide a START condition to the slave, then send the address byte with the read/write status bit (least significant bit b0) at 0 (Write status). The NCS12802 will then acknowledge this byte. The writing communication session is started.

The next byte generated will select the DAC register (VG1 to VG12) by sending the appropriate DAC address byte (Table 4). The DAC address byte is acknowledged by the NCS12802.

The DAC being selected, it can now be updated by the 10−bit code which will provide the voltage reference requested. The appropriate decimal code (integer number) ranging from 0 to 1023 is provided by Equation 1.

Because every byte on the SDA line must be 8 bits long, the 10−bit code is provided to the DAC Registers by sending 2 bytes (D15−D8 & D7−D0). On the first byte only D9 and D8 are used. The bit D15 is a specific bit used to configure by software the way the DAC output voltages are updated (see below explanations). The DAC register is actually updated after having received the second byte. These 2 bytes are acknowledged by the NCS12802.

If several DAC registers have to be updated then this is done sequentially by incrementing the DAC register pointer

or address code. There is an auto−increment function which goes over 28 addresses in order to cover the 24 required addresses (2 banks x 12 addresses). When reaching the 12th address the device will not acknowledge (NACK) every register address block until the 15th. It is only after the 16th address that the device will acknowledge (ACK) again. For example if starting with the first DAC VG1, send the address 0000 0000b first through SDA; this address will be sequentially auto−incremented to update the next DAC register VG2 (0000 0001b) then VG3 until the last one VG12, if desired, is updated as far as additional data are sent. Only one first DAC address has to be provided. This process is operated until getting updated all desired registers (actually defined by the number of 2−byte data sent) or until a STOP condition is sent.

The DAC register being updated a STOP condition can be sent through SDA to close the communication session.

In the case where the master terminates communication in the middle of a session by sending a STOP or START condition the specified register is not updated. Only DACs that have received 2 bytes will be updated.

Reading a Single or Multiple DAC Registers (Figure 25):

This communication from the slave to the master is characterized by the fact that master−receiver needs to signal the end of the transfer to the slave transmitter by a Not Acknowledge (NACK) bit.

To select the DAC register which has to be read the master has to provide a START condition to the slave, then send the address byte with the read/write status bit (least significant bit b0) at 0 (Write status). The NCS12802 will then acknowledge this byte. A writing communication session is started. The next byte generated will select the DAC register (VG1 to VG12) by sending the appropriate DAC address byte (Table 4). The DAC address byte is acknowledged by the NCS12802 (from the slave to the master). The DAC register or the first DAC register (multiple DAC register reading case) being identified, this selected register can be read or the first selected one followed by the other ones with their sequentially auto−incremented address code. The reading process is started by sending the correct device address with the read/write bit High. The NCS12802 acknowledges this byte. And the master receives the DAC register content starting by the specified one. The master acknowledges after receiving each byte. The master not−acknowledges (NACK) the last byte to indicate the end of the transfer and provides a STOP condition.

Similarly to the Write function, there is an auto−increment function which goes over 28 addresses in order to cover the 24 required addresses (2 banks x 12 addresses). When reaching the 12th address the device will not acknowledge (NACK) every register address block until the 15th. It is only after the 16th address that the device will acknowledge (ACK) again.

Communication may be terminated by sending a STOP or START condition on the bus or by sending a NACK.

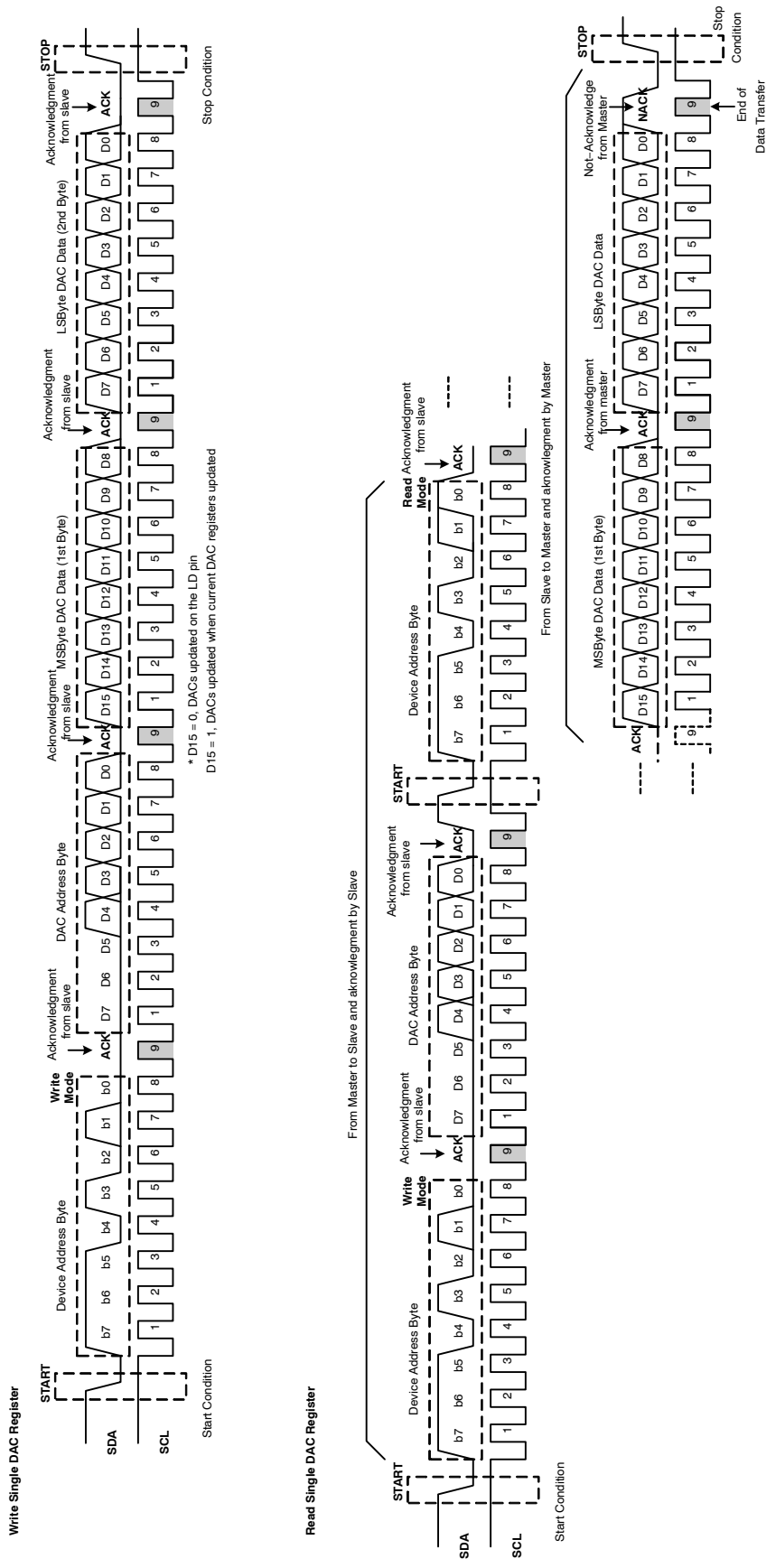


Figure 25. Write Single DAC Register / Read Single DAC Register processes / Chronograms

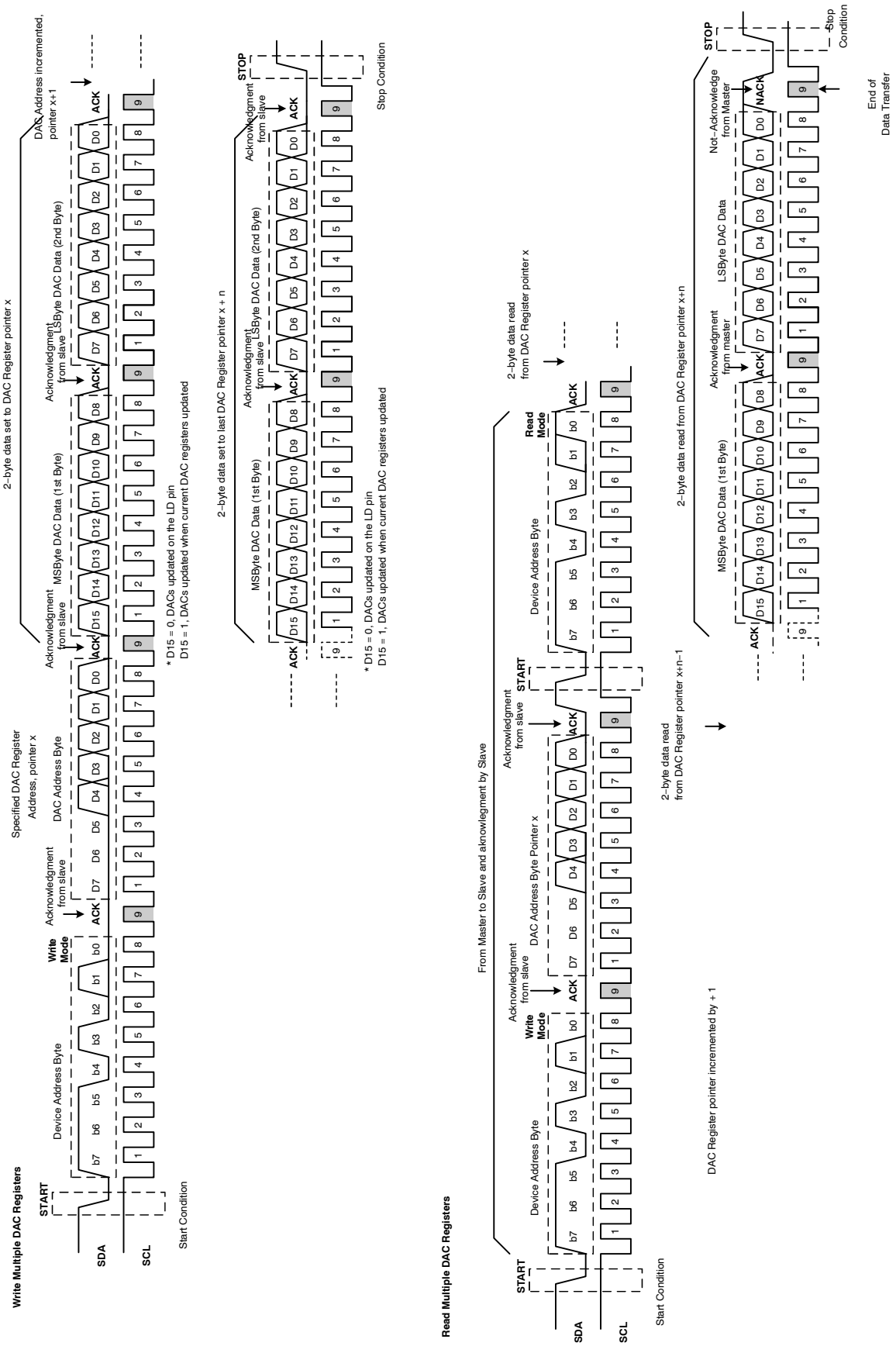


Figure 26. Write Multiple DAC Registers / Read Multiple DAC Registers processes / Chronograms

FAULT DETECTION

OUTPUT AND INPUT ESD PROTECTIONS

INPUT AND OUTPUT PROTECTION

The NCS12802 output buffers are designed to ensure a source and sink drive current according to the Figures 27 and Figure 28. Meanwhile excessive drive current can cause damages to the device, so caution is required. The output OUT1 to OUT12 have embedded ESD protection diodes as shown in Figure 27. Usually those diodes do not conduct and are passive during normal operation of the device. Irregular conditions can occur and forces the diodes to conduct high and possibly damaging current. When an output voltage becomes superior to AVDD + 0.5 V or drops below GND – 0.5 V, malfunctioning of the device can start to appear.

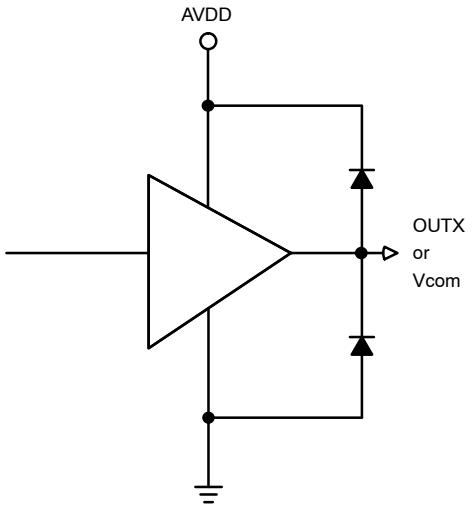


Figure 27. Output Protection Structure

One common scenario when those conditions can happen is when the output pin is connected to a large enough capacitor and the NCS12802 analog power supply AVDD is suddenly removed. Removing the power supply allows the capacitor to discharge through the current steering diodes. The energy released during the high current flow causes the power dissipation limits of the diode to be exceeded. Protection against the high current flow may be provided by placing a Schottky diode as illustrated in Figure 28. This diode has to be capable of discharging the capacitor without allowing more than 0.5 V to develop across the internal ESD diodes. It's not recommended that a large capacitor be connected to the output of the gamma buffers.

DIGITAL INPUT PROTECTIONS

The logic pins BKSEL, A0, LD, EN, EA0 and EA1 simplified schematic is illustrated Figure 29 illustrates the SCL and SDA lines.

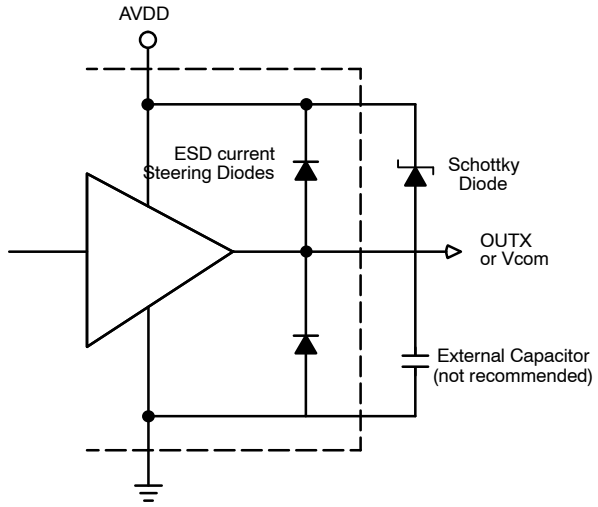


Figure 28. Output Pins ESD Protection Current Steering Diodes

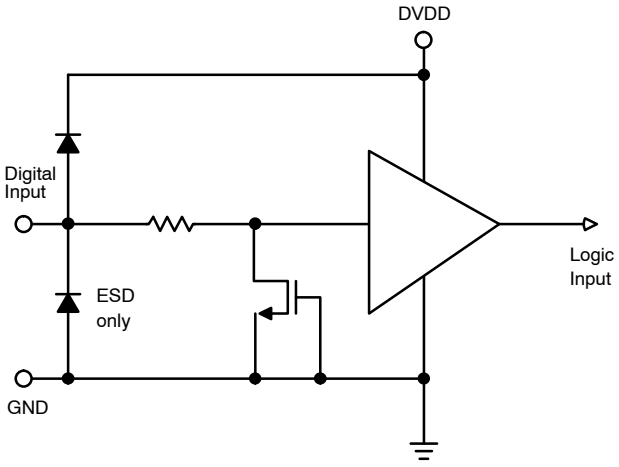


Figure 29. Digital Input Protection Scheme

APPLICATION SCHEMATIC

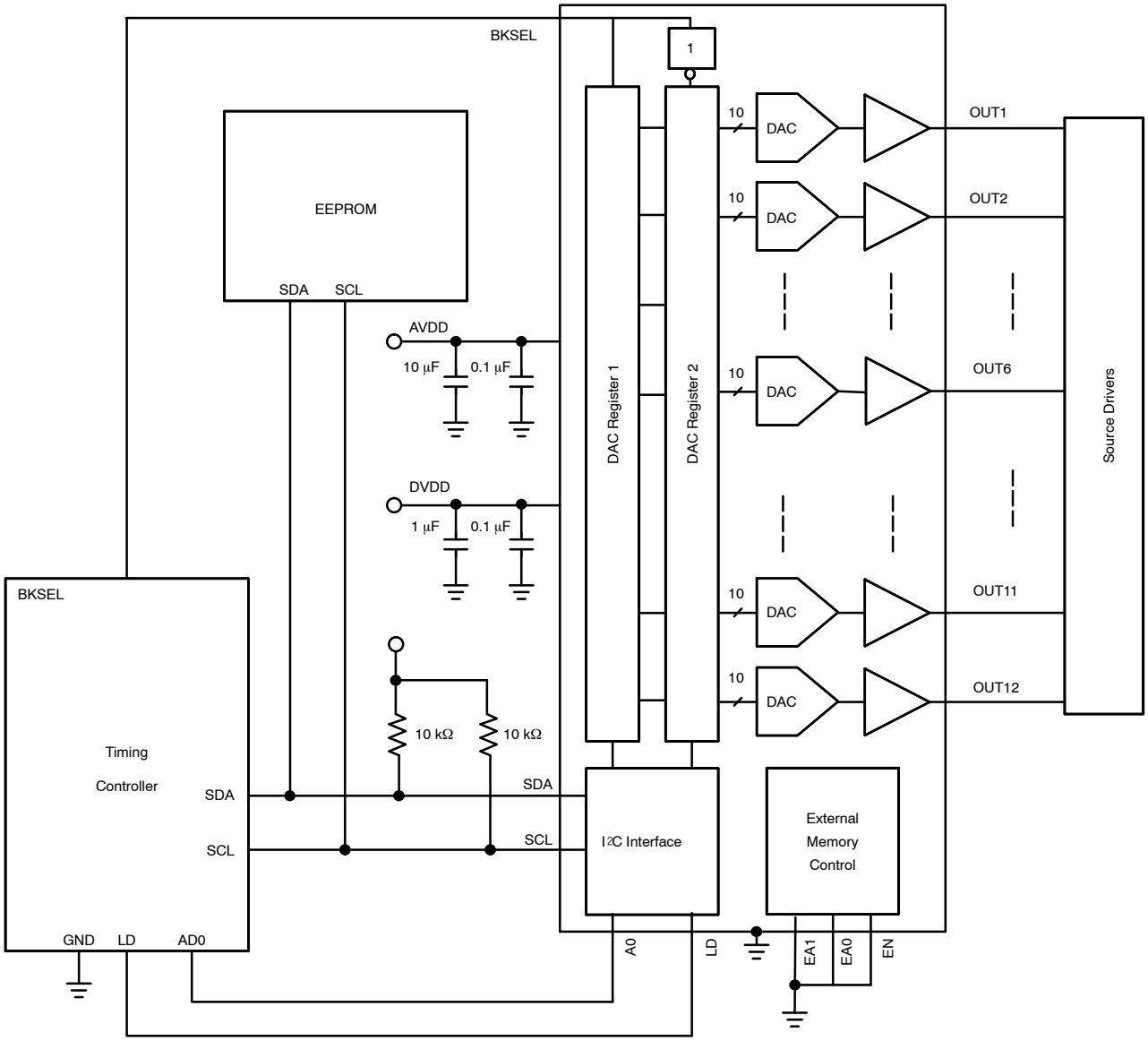


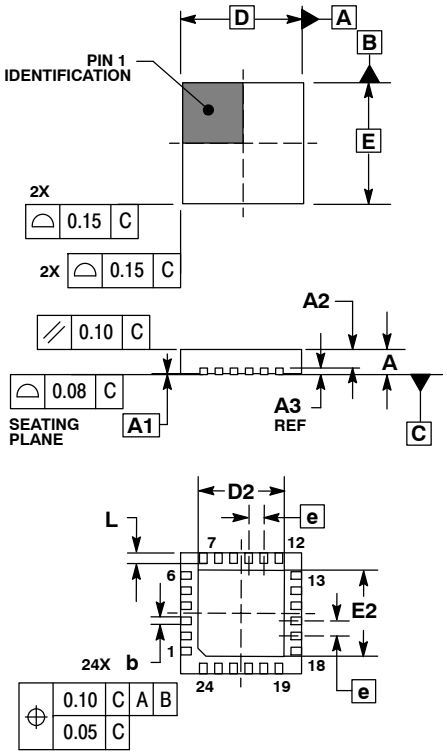
Figure 30. Application Schematic

THERMAL PAD DESIGN CONSIDERATIONS

The NCS12802 has exposed heat−sink designed to be soldered directly to metal pads on the application board. To optimize power dissipation, vias must be implemented in the exposed pad connecting the GND of the exposed pad to the GND layer of the printed circuit board. All DGND, AGND and the exposed pad must be tight together.

PACKAGE DIMENSIONS

QFN24, 4x4, 0.5P
CASE 485L−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50

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