

N-channel 600 V, 0.06 Ω typ., 42 A MDmesh™ M2 Power MOSFET in a TO247-4 package

Datasheet - production data

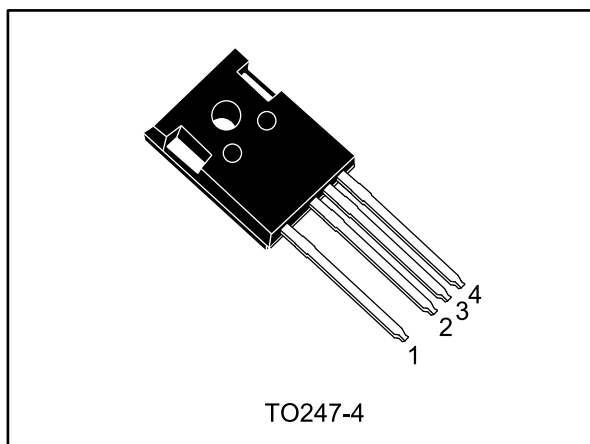
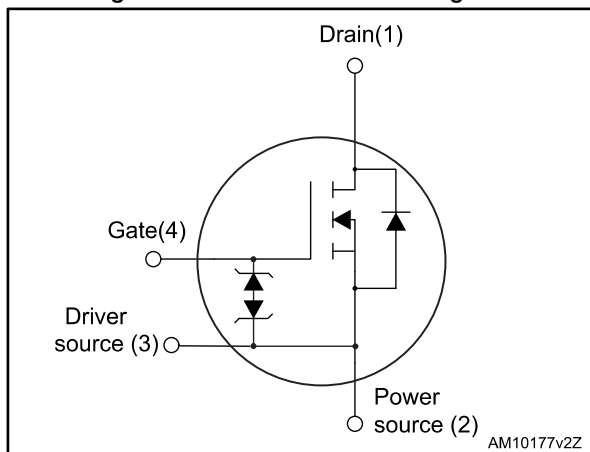


Figure 1: Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax.}$	$R_{DS(on)max.}$	I_D
STW48N60M2-4	650 V	0.07 Ω	42 A

- Excellent switching performance thanks to the extra driving source pin
- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- High efficiency switching applications:
 - Servers
 - PV inverters
 - Telecom infrastructure
 - Multi kW battery chargers

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW48N60M2-4	48N60M2	TO247-4	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	42	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	26	A
$I_{DM}^{(1)}$	Drain current (pulsed)	168	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	300	W
I_{AR}	Max. current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax.}$)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1	J
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 42\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

⁽³⁾ $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.42	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max.	50	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	600			V
I _{DSS}	Zero-gate voltage drain current (V _{GS} = 0)	V _{DS} = 600 V			1	μA
		V _{DS} = 600 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			±10	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 21 A		0.06	0.07	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	3060	-	pF
C _{oss}	Output capacitance		-	143	-	pF
C _{rss}	Reverse transfer capacitance		-	4.3	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent Output Capacitance	V _{GS} = 0, V _{DS} = 0 to 480 V	-	630	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.6	-	Ω
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 42 A, V _{GS} = 10 V See Figure 15: "Gate charge test circuit"	-	70	-	nC
Q _{gs}	Gate-source charge		-	10.5	-	nC
Q _{gd}	Gate-drain charge		-	31	-	nC

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 21 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	18.5	-	ns
t _r	Rise time		-	17	-	ns
t _{d(off)}	Turn-off-delay time	See Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform"	-	13	-	ns
t _f	Fall time		-	119	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		42	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		168	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 21\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 42\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ See Figure 16: "Test circuit for inductive load switching and diode recovery times"	-	487		ns
Q_{rr}	Reverse recovery charge		-	9.1		μC
I_{RRM}	Reverse recovery current		-	37.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 42\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ See Figure 16: "Test circuit for inductive load switching and diode recovery times"	-	605		ns
Q_{rr}	Reverse recovery charge		-	12.5		μC
I_{RRM}	Reverse recovery current		-	41.5		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

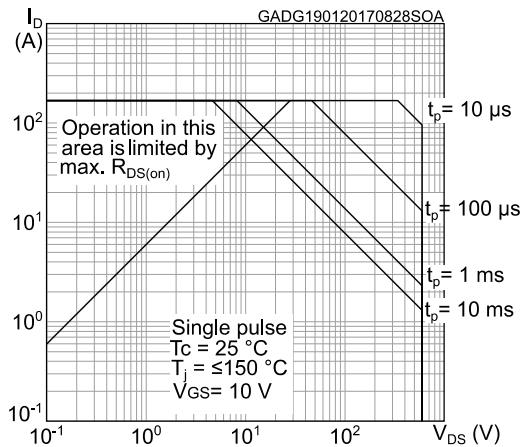


Figure 3: Thermal impedance

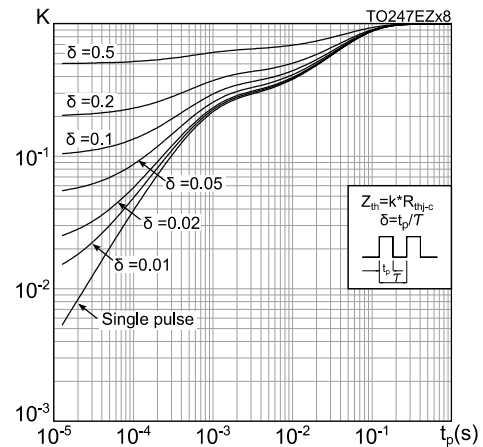


Figure 4: Output characteristics

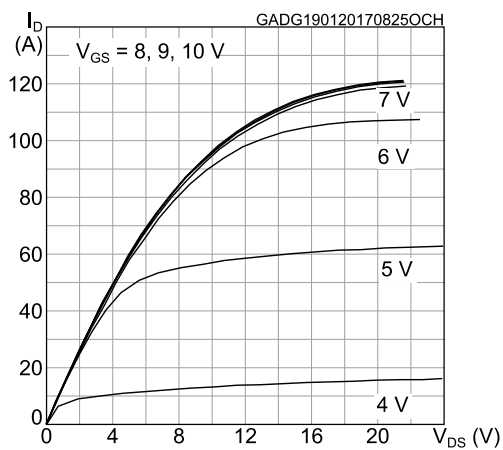


Figure 5: Transfer characteristics

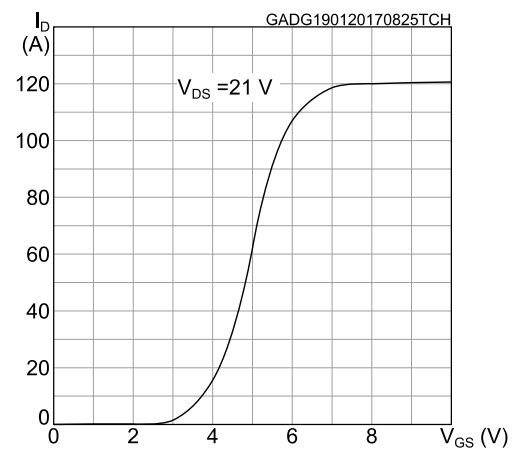


Figure 6: Gate charge vs gate-source voltage

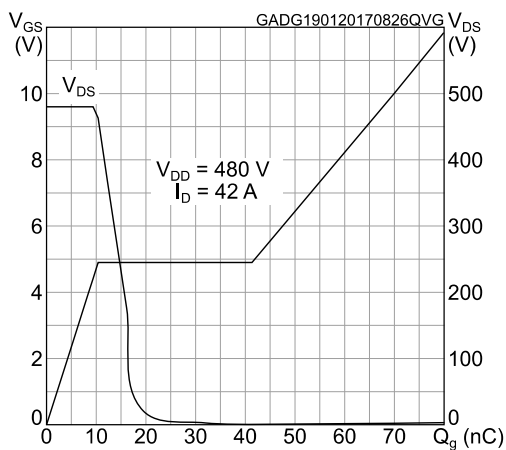


Figure 7: Static drain-source on-resistance

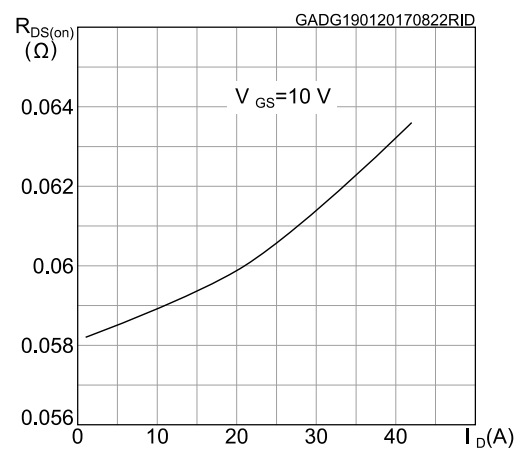


Figure 8: Capacitance variations

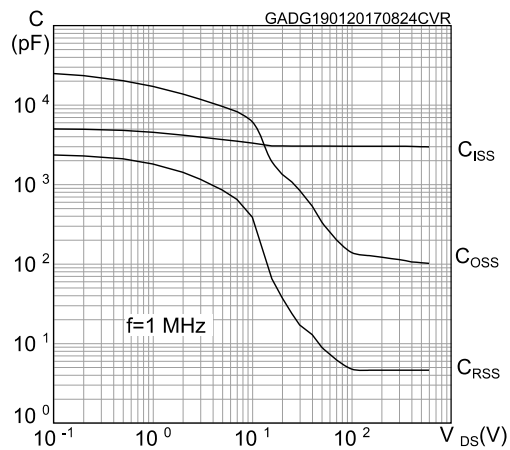


Figure 9: Output capacitance stored energy

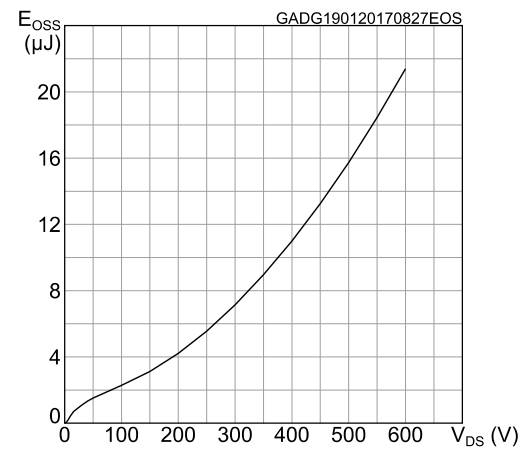


Figure 10: Normalized gate threshold voltage vs temperature

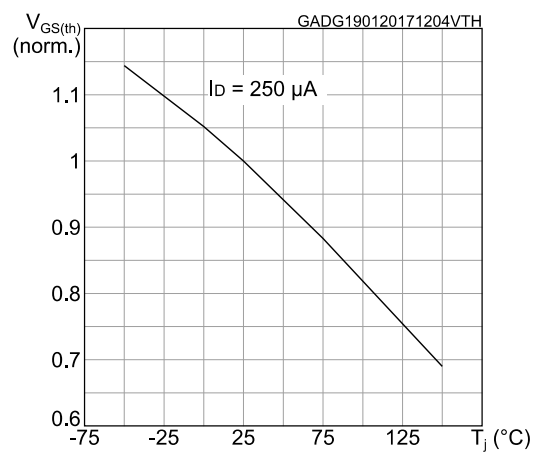


Figure 11: Normalized on-resistance vs temperature

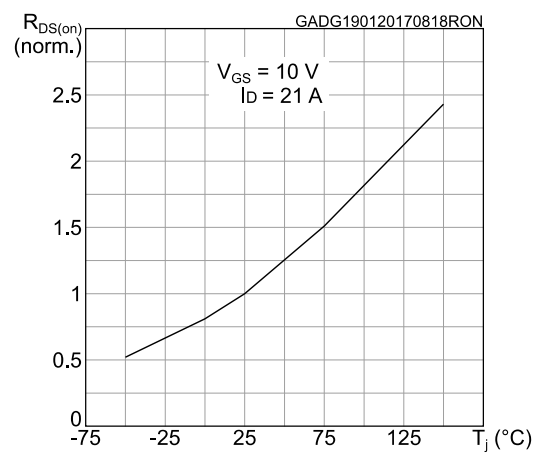
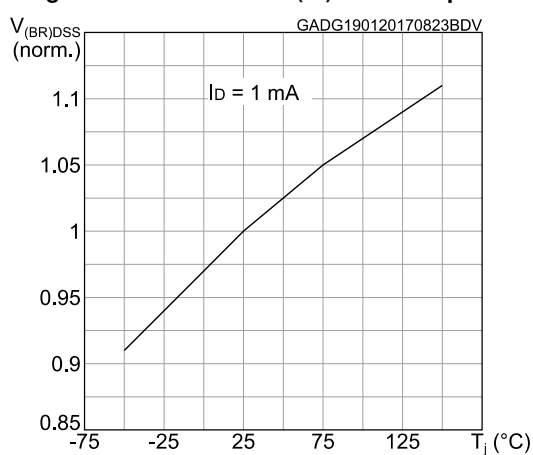
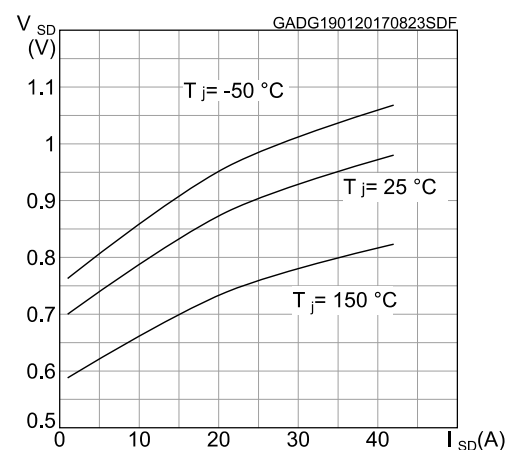
Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Switching times test circuit for resistive load



Figure 15: Gate charge test circuit



Figure 16: Test circuit for inductive load switching and diode recovery times



Figure 17: Unclamped inductive load test circuit



Figure 18: Unclamped inductive waveform



Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO247-4 package information

Figure 20: TO247-4 package outline

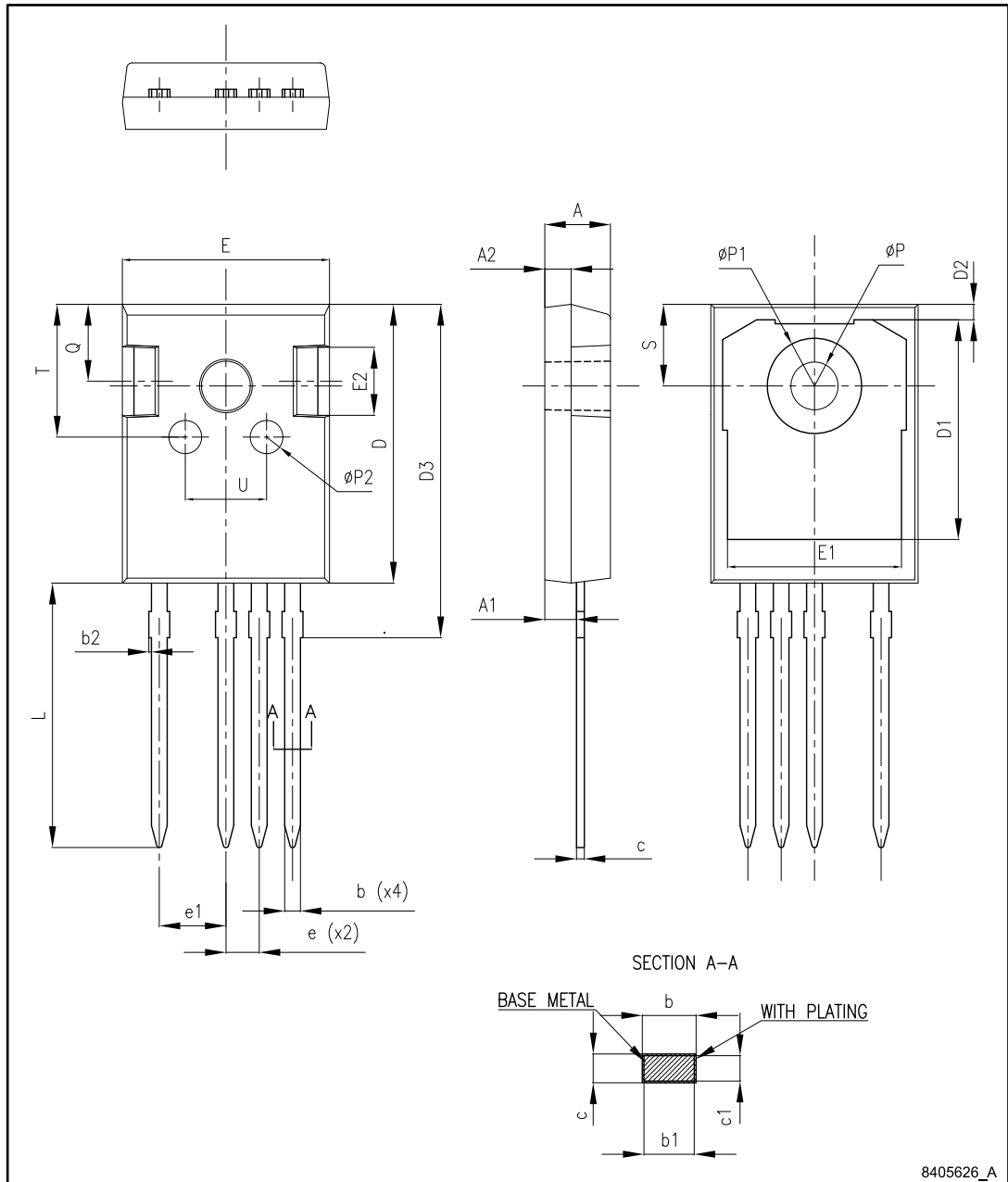


Table 8: TO247-4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
25-Jul-2014	1	Initial release.
30-Jan-2015	2	Added section <i>Electrical characteristics (curves)</i> .
20-Jan-2017	3	Updated Table 2: "Absolute maximum ratings" , Table 4: "On /off-states" , Table 5: "Dynamic" , Table 6: "Switching times" and Table 7: "Source-drain diode" . Updated Section 2.2: "Electrical characteristics (curves)" .

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