PLETRONICS
www.pletronics.com 425-776-1880





SM77G Series 3.3V
CMOS Clock Oscillators

Feb 2008

Lead Free

- Pletronics' SM77G Series is a quartz crystal controlled precision square wave generator with a CMOS output.
- The package is designed for high density surface mount designs.
- This is a low cost mass produced oscillator.
- Tape and Reel or cut tape packaging is available.
- 0.8 to 70 MHz
- 5 x 7 mm LCC Ceramic Package
- Enable/Disable
- Disable function includes low standby power mode
- Low Jitter
- Optimized for larger load applications

Pletronics Inc. certifies this device is in accordance with the RoHS 6/6 (2002/95/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following:
Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.17 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020C
Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V_{CC} Supply Voltage	-0.5V to +7.0V
Vi Input Voltage	-0.5V to V_{CC} + 0.5V
Vo Output Voltage	-0.5V to V_{CC} + 0.5V
Io Output Current	+25 mA to -25 mA

Thermal Characteristics

The maximum die or junction temperature is 155°C
The thermal resistance junction to board is 30 to 50°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Product information is current as of publication date. The product conforms to specifications per the terms of the Pletronics standard warranty. Production processsing does not necessarily include testing of all parameters.

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PART NUMBER:

SM77	45	G	E	V	- 50.0M	-XX

Packaging code or blank
T250 = 250 per Tape and Reel
T500 = 500 per Tape and Reel
T1K = 1000 per Tape and Reel

Frequency in MHz

Supply Voltage V_{cc}
V = 3.3V ± 10%

Optional Enhanced OTR
Blank = Temp. range -10 to +70°C
E = Temp. range -40 to +85°C

Series Model

Frequency Stability
45 = ± 50 ppm
44 = ± 25 ppm
20 = ± 20 ppm

Series Model

Part Marking:

PLE SM77
***FF.FFF* M**
• ***YMDXX***

or

PLE SM77
***FF.FFF* M**
• ***YYWWXX***

or

7XYWWXX
***FF.FFF* M**
• **PLE *XXX***

Marking Legend:
PLE = Pletronics
FF.FFF M = Frequency in MHz
YYWW or YWW or *YMD* = Date of Manufacture (year and week, or year-month-day)
All other marking is internal factory codes

Specifications such as frequency stability, supply voltage and operating temperature range, etc. are not identified from the marking. External packaging labels and packing list will correctly identify the ordered Pletronics part number.

Codes for Date Code YMD

Code	6	7	8	9	0	1	2
Year	2006	2007	2008	2009	2010	2011	2012

Code	A	B	C	D	E	F	G	H	J	K	L	M
Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

Code	1	2	3	4	5	6	7	8	9	A	B	C
Day	1	2	3	4	5	6	7	8	9	10	11	12
Code	D	E	F	G	H	J	K	L	M	N	P	R
Day	13	14	15	16	17	18	19	20	21	22	23	24
Code	T	U	V	W	X	Y	Z					
Day	25	26	27	28	29	30	31					

Electrical Specification for 3.30V ±10% over the specified temperature range

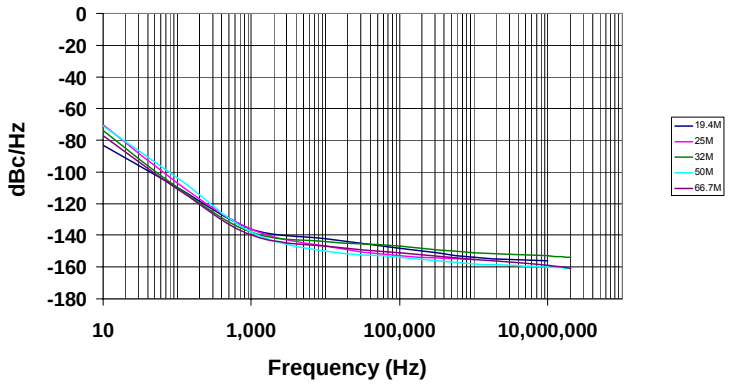
Item	Min	Max	Unit	Condition
Frequency Range	0.8	69.9	MHz	
Frequency Accuracy "45"	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures
"44"	-25	+25		
"20"	-20	+20		
Output Waveform	CMOS			
Output High Level	90	-	%	of V_{CC} (See load circuit)
Output Low Level	-	10	%	
Output Symmetry	45	55	%	at 50% point of V_{CC} (See load circuit)
Jitter	-	0.6	pS RMS	12 KHz to 20 MHz from the output frequency
	-	2.5	pS RMS	10 Hz to 1 MHz from the output frequency
E/D Internal Pull-up	50	-	Kohm	to V_{CC}
V disable	-	30	%	of V_{CC} applied to pad 1
V enable	70	-	%	
Output leakage $V_{OUT} = V_{CC}$	-10	+10	uA	Pin 1 low, device disabled
$V_{OUT} = 0V$	-10	+10	uA	
Standby Current I_{CC}	-	3	uA	
Enable time	-	100	nS	Time for output to reach a logic state
Disable time	-	100	nS	Time for output to reach a high Z state
Start up time	-	3	mS	Time for output to reach specified frequency
Operating Temperature Range	-10	+70	°C	Standard Temperature Range
	-40	+85	°C	Extended Temperature Range "E" Option
Storage Temperature Range	-55	+125	°C	

Electrical Specification for 3.30V ±10% over the specified temperature range

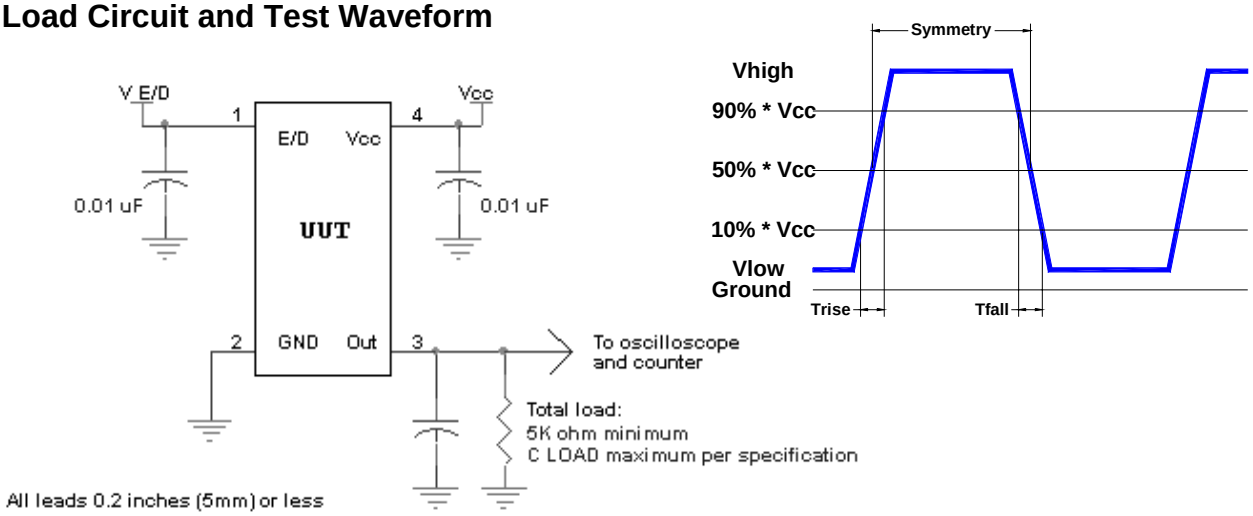
Item	Typ	Max	Unit	Condition	
Output T_{RISE} and T_{FALL}	1.5	2.5	nS	< 35 MHz	C_{LOAD} = 15 pF 10% to 90% of V_{CC} See Load Circuit
	1.8	4.0	nS	≥ 35 MHz	
	3.0	5.0	nS	< 35 MHz	C_{LOAD} =30 pF 10% to 90% of V_{CC} See Load Circuit
	2.5	5.0	nS	≥ 35 MHz	
	5.0	8.0	nS	< 35 MHz	C_{LOAD} =50 pF 10% to 90% of V_{CC} See Load Circuit
	4.0	8.0	nS	≥ 35 MHz	
V_{CC} Supply Current (I_{CC})	4.5	8	mA	< 8 MHz	C_{LOAD} = 15 pF
	5	9	mA	≥ 8 MHz and < 16 MHz	
	5.5	10	mA	≥ 16 MHz and < 35 MHz	
	13	26	mA	≥ 35 MHz	
	5	9	mA	< 8 MHz	C_{LOAD} = 30 pF
	6	10	mA	≥ 8 MHz and < 16 MHz	
	8	13	mA	≥ 16 MHz and < 35 MHz	
	14	28	mA	≥ 35 MHz	
	6	10	mA	< 8 MHz	C_{LOAD} = 50 pF
	7	12	mA	≥ 8 MHz and < 16 MHz	
	10	15	mA	≥ 16 MHz and < 35 MHz	
	18	31	mA	≥ 35 MHz	

Specifications with Pad 1 E/D open circuit

Typical phase noise plot for 5 oscillators at different output frequencies.



Load Circuit and Test Waveform



Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

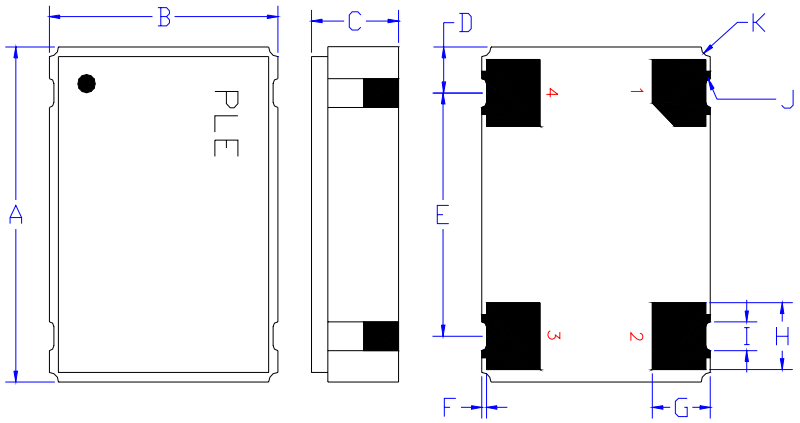
Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII



Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

RoHS Compliant
2nd LvL Interconnect
Category=e4
Max Safe Temp=260C for 10s 2X Max

Mechanical:



Not to Scale

[1] Typical dimensions

	Inches	mm
A	0.276 ±0.006	7.00 ±0.15
B	0.197 ±0.006	5.00 ±0.15
C	0.68±0.018	1.73 ±0.44
D[1]	0.038	0.96
E[1]	0.200	5.08
F[1]	0.004	0.10
G[1]	0.050	1.27
H[1]	0.055	1.40
I[1]	0.024	0.60
J[1]	0.004	0.10R
K[1]	0.008	0.020R

Contacts :
Gold 11.8 µinches 0.3 µm minimum over Nickel 50 to 350 µinches 1.27 to 8.89 µm

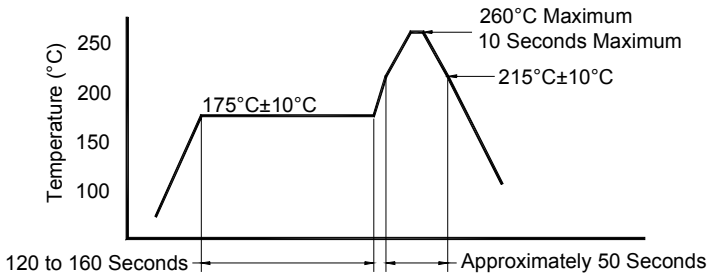
Pad	Function	Note
1	Output Enable/Disable	When this pin is not connected the oscillator shall operate. When this pin is logic low the output will be inhibited (high impedance state.) Recommend connecting this pin to V_{CC} if the oscillator is to be always on.
2	Ground (GND)	
3	Output	
4	Supply Voltage (V_{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

Lead Free

Layout and application information

For Optimum Jitter Performance, Pletronics recommends:
- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.

Reflow Cycle (typical for lead free processing)



The part may be reflowed 2 times without degradation.

Allowed rate of temperature change
Maximum 4°C per second

Tape and Reel: available for quantities of 250 to 1000 per reel, cut tape for < 250

Constant Dimensions Table 1

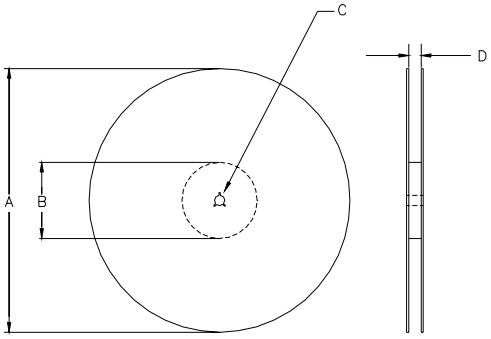
Tape Size	D0	D1 Min	E1	P0	P2	S1 Min	T Max	T1 Max
8mm	1.5 +0.1 -0.0	1.0	1.75 ±0.1	4.0 ±0.1	2.0 ±0.05	0.6	0.6	0.1
12mm		1.5						
16mm		1.5			2.0 ±0.1			
24mm		1.5						

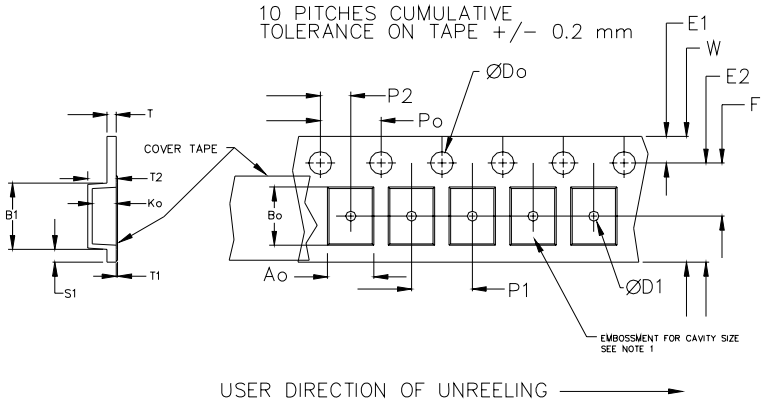
Variable Dimensions Table 2

Tape Size	B1 Max	E2 Min	F	P1	T2 Max	W Max	Ao, Bo & Ko
16 mm	12.1	14.25	7.5 ±0.1	8.0 ±0.1	8.0	16.3	Note 1

Note 1: Embossed cavity to conform to EIA-481-B

Not to scale





		REEL DIMENSIONS			
A	inches	7.0	10.0	13.0	
	mm	177.8	254.0	330.2	
B	inches	2.50	4.00	3.75	
	mm	63.5	101.6	95.3	Tape Width
C	mm	13.0 +0.5 / -0.2			
D	mm	16.4 +2.0 -0.0	16.4 +2.0 -0.0	16.4 +2.0 -0.0	16.0

Reel dimensions may vary from the above

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