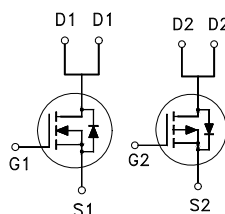
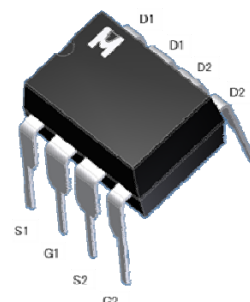


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	30V	-30V
$R_{DS(on)} (MAX.)$	21m Ω	35m Ω
I_D	7.5A	-6A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	7.5	-6	A
	$T_C = 100\text{ }^{\circ}\text{C}$		5.5	-5	
Pulsed Drain Current ¹		I_{DM}	30	-24	
Avalanche Current		I_{AS}	10	-10	
Avalanche Energy	L = 0.1mH, ID=7.5A, RG=25Ω (N) L = 0.1mH, ID=-6A, RG=25Ω (P)	E_{AS}	2.8	1.8	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E_{AR}	1.4	0.9	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	5		W
	$T_C = 100\text{ }^{\circ}\text{C}$		2		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

100% UIS testing in condition of $V_D = 15\text{V}$, $L = 0.1\text{mH}$, $V_G = 10\text{V}$, $I_L = 7.5\text{A}$, Rated $V_{DS} = 30\text{V}$ N-CH

100% UIS testing in condition of $V_D = 15\text{V}$, $L = 0.1\text{mH}$, $V_G = -10\text{V}$, $I_L = -6\text{A}$, Rated $V_{DS} = -30\text{V}$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	N-CH	30			V
		V _{GS} = 0V, I _D = -250μA	P-CH	-30			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	N-CH	1	1.5	3	
		V _{DS} = V _{GS} , I _D = -250μA	P-CH	-1	-1.5	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	N-CH			±100	nA
		V _{DS} = 0V, V _{GS} = ±20V	P-CH			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V	N-CH			1	μA
		V _{DS} = -24V, V _{GS} = 0V	P-CH			-1	
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C	N-CH			25	
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C	P-CH			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	N-CH	7.5			A
		V _{DS} = -5V, V _{GS} = -10V	P-CH	-6			
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 7.5A	N-CH		18	21	mΩ
		V _{GS} = -10V, I _D = -6A	P-CH		26	35	
		V _{GS} = 4.5V, I _D = 5.5A	N-CH		34	42	
		V _{GS} = -4.5V, I _D = -5A	P-CH		45	60	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 7.5A	N-CH		16		S
		V _{DS} = -5V, I _D = -6A	P-CH		12		
DYNAMIC							
Input Capacitance	C _{iss}	N-CH V _{GS} = 0V, V _{DS} = 15V, f = 1MHz P=CH V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	N-CH		520		pF
			P-CH		910		
Output Capacitance	C _{oss}		N-CH		88		
			P-CH		143		
Reverse Transfer Capacitance	C _{rss}		N-CH		62		
			P-CH		108		

Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz	N-CH		2.0		Ω
			P-CH		4.0		
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V) Q _g (V _{GS} =-10V) Q _g (V _{GS} =4.5V) Q _g (V _{GS} =-4.5V)	N-CH V _{DS} = 15V, V _{GS} = 10V, I _D = 7.5A P-CH V _{DS} = -15V, V _{GS} = -10V, I _D = -6A	N-CH		11.5		nC
			P-CH		13.3		
			N-CH		5		
			P-CH		7		
Gate-Source Charge ^{1,2}	Q _{gs}		N-CH		1.6		nC
			P-CH		2.1		
Gate-Drain Charge ^{1,2}	Q _{gd}		N-CH		2.8		
			P-CH		3.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}	N-CH V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω P-CH	N-CH		11		nS
			P-CH		12		
Rise Time ^{1,2}	t _r		N-CH		16		
			P-CH		18		
Turn-Off Delay Time ^{1,2}	t _{d(off)}	V _{DS} = -15V, I _D = -1A, V _{GS} = -10V, R _{GS} = 6Ω	N-CH		36		
			P-CH		38		
Fall Time ^{1,2}	t _f		N-CH		20		nS
			P-CH		22		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)							
Continuous Current	I _S		N-CH			2.3	A
			P-CH			-2.3	
Pulsed Current ³	I _{SM}		N-CH			9.2	A
			P-CH			-9.2	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V	N-CH			1.2	V
			P-CH			-1.2	
Reverse Recovery Time	t _{rr}		N-CH		50		nS
			P-CH		55		
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = I _S , dI _F /dt = 100A / μS	N-CH		30		A
			P-CH		-24		
Reverse Recovery Charge	Q _{rr}		N-CH		2		nC
			P-CH		2.2		

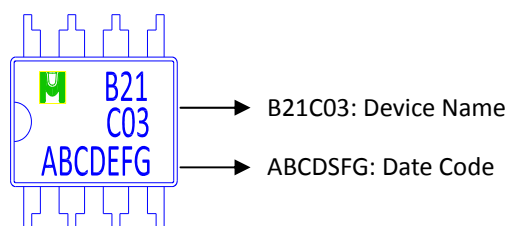
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

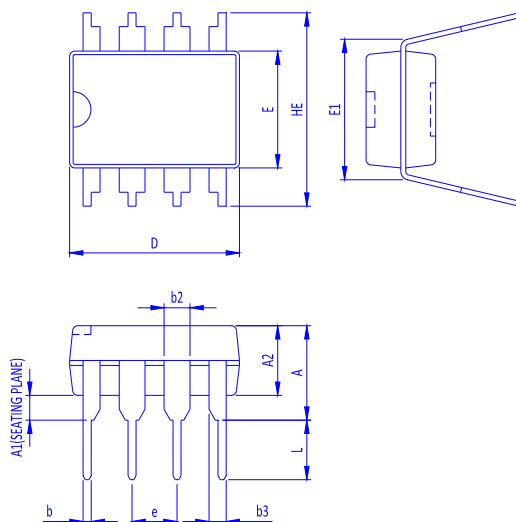
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB21C03S for DIP-8



Outline Drawing

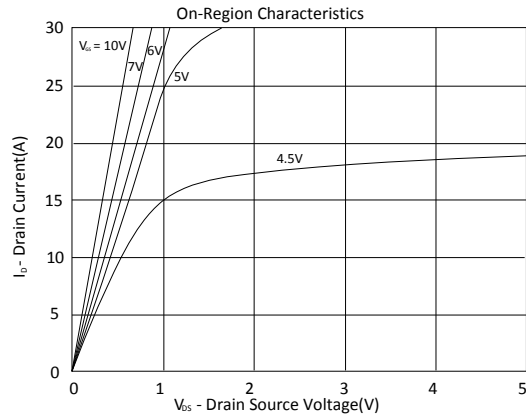
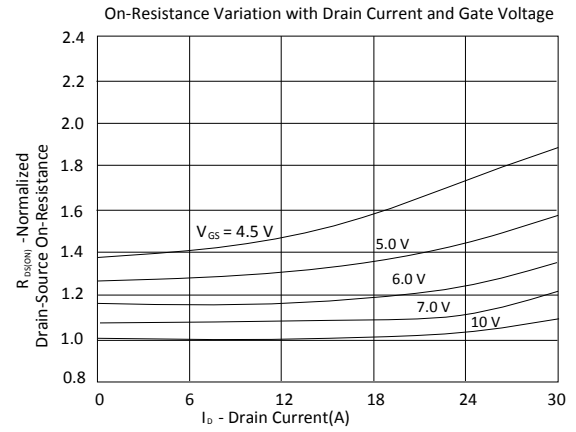
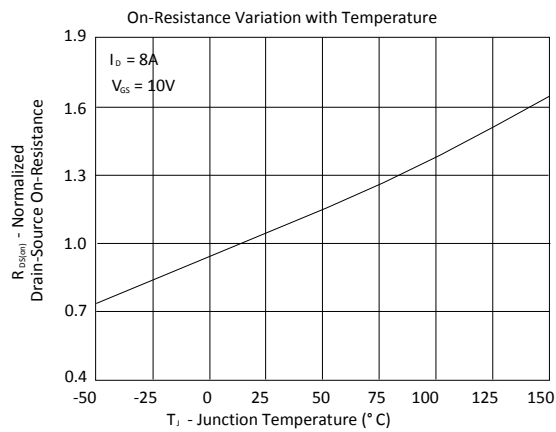
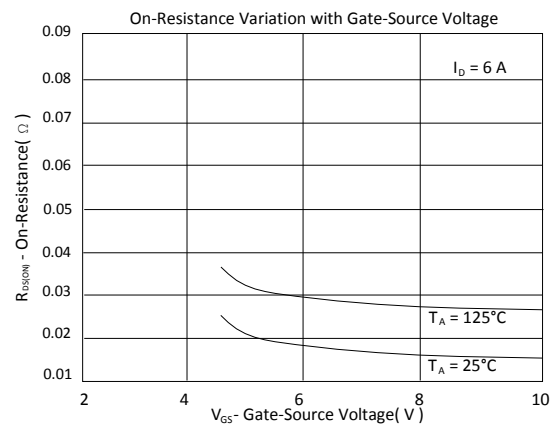
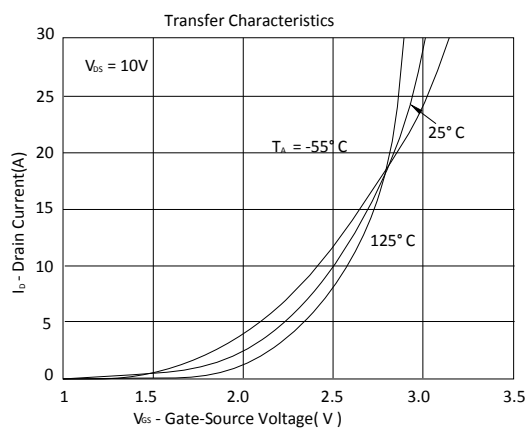
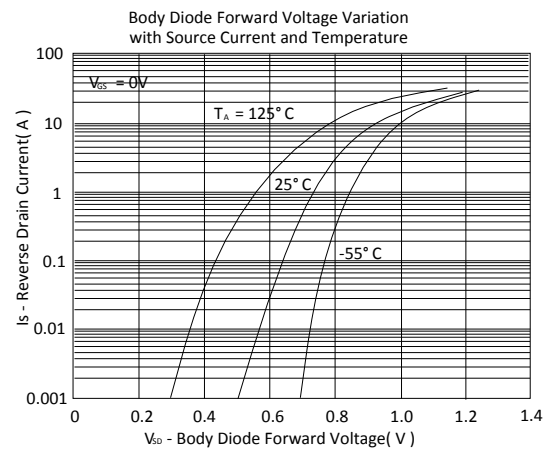


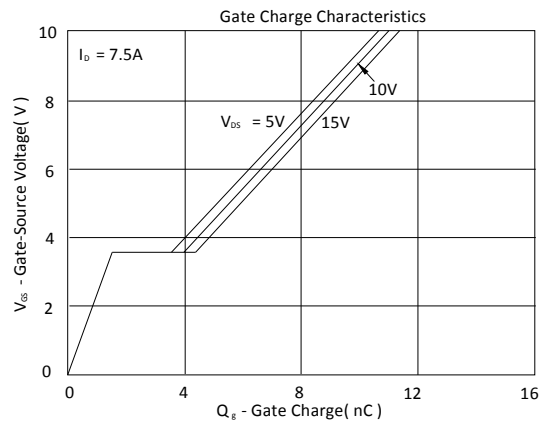
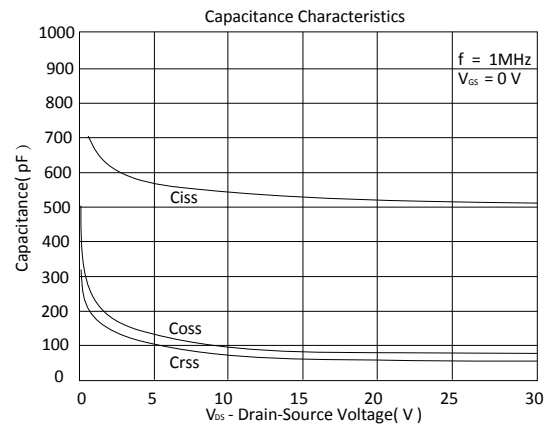
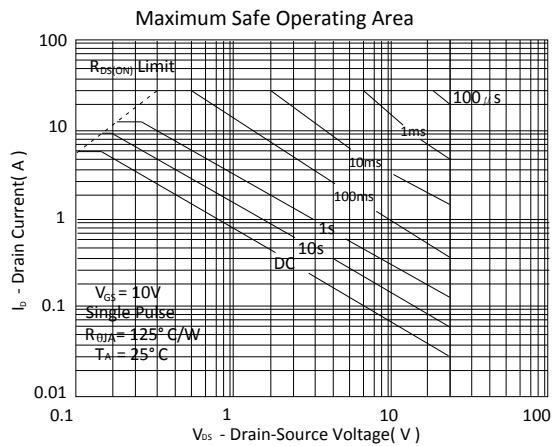
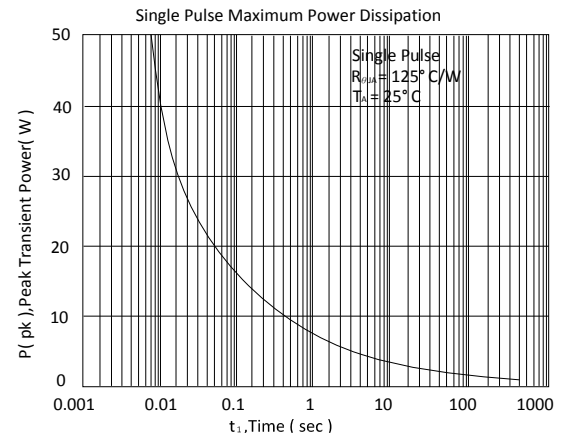
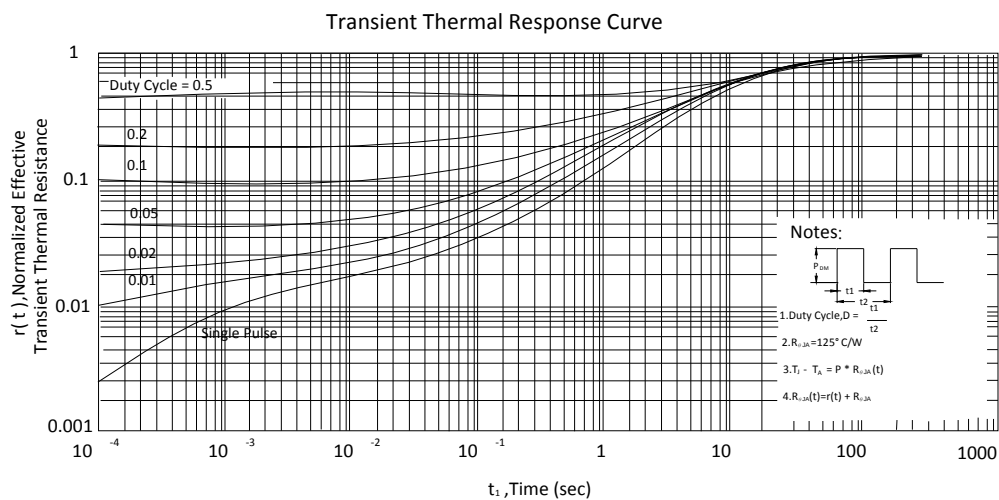
Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°



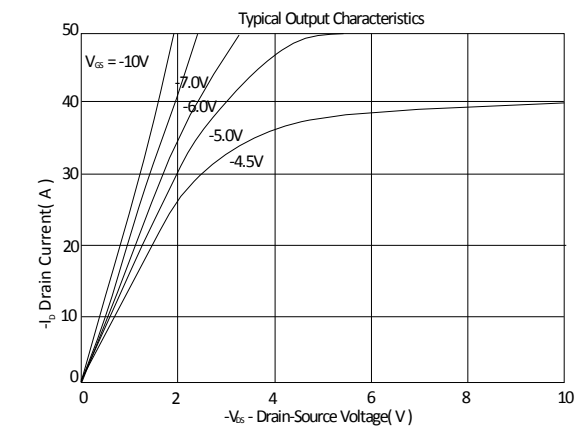
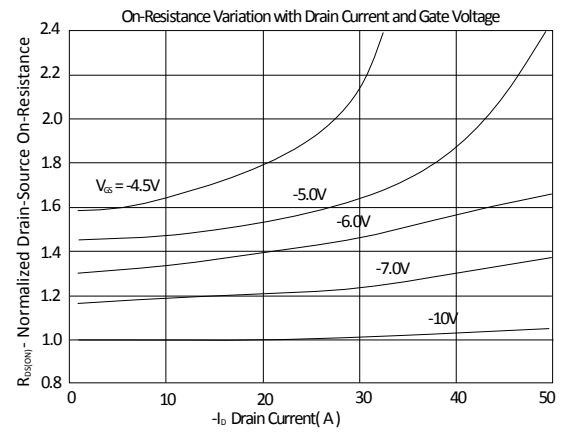
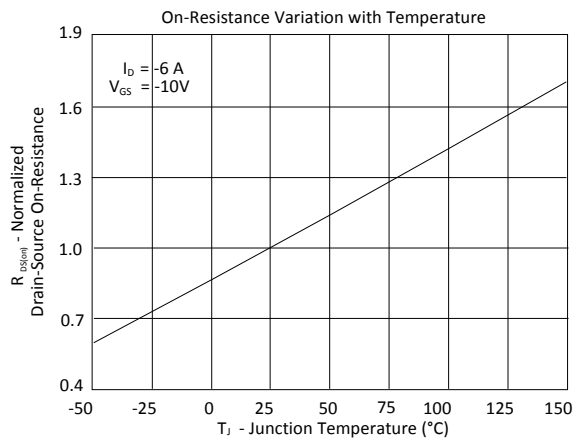
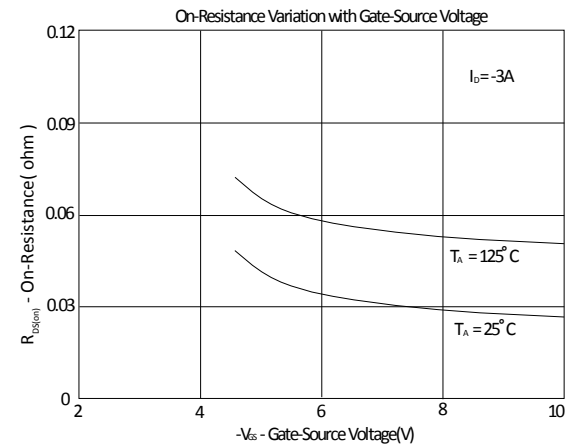
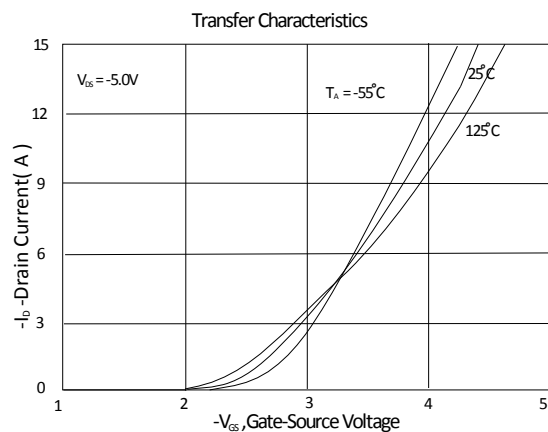
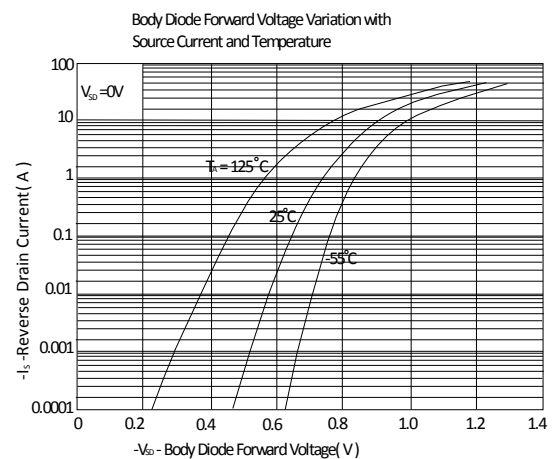
N-Channel

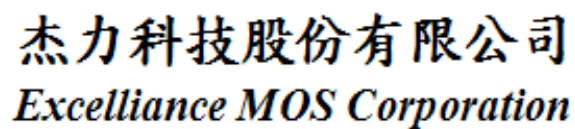






P-Channel





Gate Charge Characteristics

$I_D = -6A$

$V_{DS} = -5V$

$-10V$

$-15V$

$-V_{GS}, \text{ Gate-Source Voltage (V)}$

$Q_g, \text{ Gate Charge (nC)}$

