DP7110, DP7118, DP7119, DP7123, DP7124, DP7125

COPAL ELECTRONICS

32-Tap Digital Potentiometers with 2-Wire Interface

Description

DP7110/18/19/23/24/25 linear−taper digital potentiometers perform the same function as a mechanical potentiometer or a variable resistor. These devices consist of a fixed resistor and a wiper contact with 32−tap points that are digitally controlled through a 2−wire up/down serial interface.

The DP7110 and DP7125 are configured as potentiometers. The DP7118/19/23/24 are configured as variable resistors.

Three resistance values are available: 10 kΩ, 50 kΩ and 100 kΩ. All devices are available in space−saving 5−pin and 6−pin SOT−23 packages. The DP7110/18/19 are also available in the SC−70 package.

Features

- 0.3 μA Ultra−low Standby Current
- Single−supply Operation: 2.7 V to 5.5 V
- Glitchless Switching between Resistor Taps
- Power−on Reset to Midscale
- 2−wire Up/Down Serial Interface
- Resistance Values: 10 kΩ, 50 kΩ and 100 kΩ
- Low Wiper Resistance: 80 Ω for DP7123, DP7124, DP7125
- DP7110, DP7118, DP7119 Available in SC−70
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- LCD Screen Adjustment
- Volume Control
- Mechanical Potentiometer Replacement
- Gain Adjustment
- Line Impedance Matching

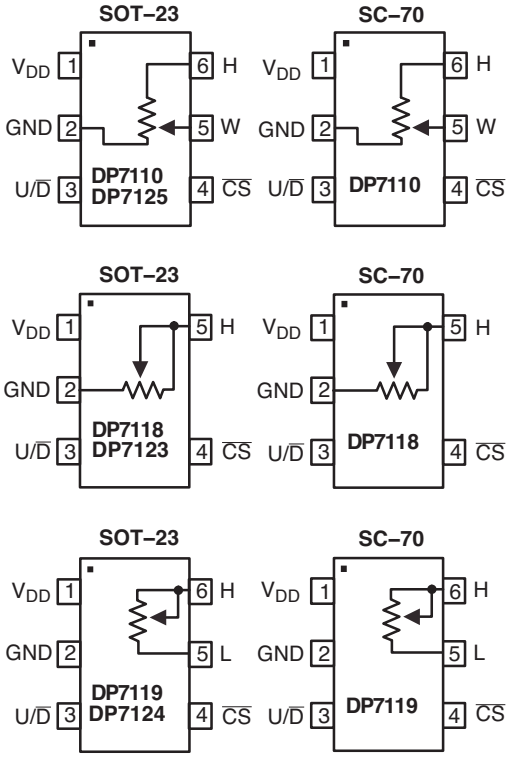


SC−70



SOT−23

PIN CONNECTIONS



(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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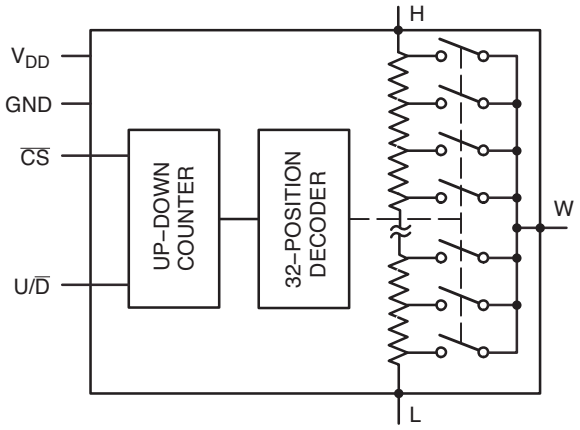


Figure 1. Functional Diagram

Table 1. PIN DESCRIPTIONS

Pin Number			Pin Name	Description
DP7110/ DP7125	DP7118/ DP7123	DP7119/ DP7124		
1	1	1	V_{DD}	Power Supply
2	2	2	GND	Ground
3	3	3	U/$\overline{D}$	Up/$\overline{Down}$ Control Input. With $\overline{CS}$ low, a low–to–high transition increments or decrements the wiper position.
4	4	4	$\overline{CS}$	Chip Select Input. A high–to–low $\overline{CS}$ transition determines the mode: increment if U/$\overline{D}$ is high, or decrement if U/$\overline{D}$ is low.
–	–	5	L	Low Terminal of Resistor
5	–	–	W	Wiper Terminal of Resistor
6	6	6	H	High Terminal of Resistor

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{DD} to GND	–0.3 to +6	V
All Other Pins to GND	–0.3 to (V_{DD} + 0.3)	V
Input and Output Latch–Up Immunity	±200	mA
Maximum Continuous Current into H, L and W 100 kΩ 50 kΩ 10 kΩ	 ±0.6 ±1.3 ±1.3	mA
Continuous Power Dissipation (T_A = +70°C) 5–pin SC–70 (Note 1) 6–pin SC–70 (Note 1)	 247 245	mW
Operating Temperature Range	–40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature Range	–65 to +150	°C
Soldering Temperature (soldering, 10 sec)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Derate 3.1 mW/°C above T_A = +70°C

Table 3. ELECTRICAL CHARACTERISTICS
(V_{DD} = 2.7 V to 5.5 V, $V_H = V_{DD}$, V_L = 0, T_A = –40°C to +85°C. Typical values are at V_{DD} = 2.7 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC PERFORMANCE						
Resolution			32			Taps
End–to–End Resistance (–00)			80	100	120	kΩ
End–to–End Resistance (–50)			40	50	60	
End–to–End Resistance (–10)			8	10	12	
End–to–End Resistance Tempco	TC_R	DP7110/18/19		200		ppm/°C
		DP7123/24/25		30	300	
Ratiometric Resistance Tempco				5		ppm/°C
Integral Nonlinearity	INL			±0.5	±1	LSB
Differential Nonlinearity	DNL				±1	LSB
Full–Scale Error				±0.1		LSB
Zero–Scale Error					1	LSB
Wiper Resistance	R_W	DP7110/18/19		200	600	Ω
		DP7123/24/25		80	200	
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
TIMING CHARACTERISTICS (Figures 7, 8)						
U/$\overline{D}$ Mode to $\overline{CS}$ Setup	t_{CU}		25			ns
$\overline{CS}$ to U/$\overline{D}$ Step Setup	t_{CI}		50			ns
$\overline{CS}$ to U/$\overline{D}$ Step Hold	t_{IC}		25			ns
U/$\overline{D}$ Step Low Period	t_{IL}		25			ns
U/$\overline{D}$ Step High Period	t_{IH}		25			ns
Up/$\overline{Down}$ Toggle Rate (Note 2)	f_{TOGGLE}			1		MHz
Output Settling Time (Note 3)	t_{SETTLE}	100 kΩ variable resistor configuration, C_L = 10 pF		1		μs
		100 kΩ potentiometer configuration, C_L = 10 pF		0.25		
POWER SUPPLY						
Supply Voltage	V_{DD}		2.7		5.5	V
Active Supply Current (Note 4)	I_{DD}				25	μA
Standby Supply Current (Note 5)	I_{SB}	V_{DD} = +5 V		0.3	1	μA

2. Up/Down Toggle Rate: $f_{TOGGLE} = 1 / t_{SETTLE}$
3. Typical settling times are dependent on end–to–end resistance.
4. Supply current measureed while changing wiper tap, f_{TOGGLE} = 1 MHz.
5. Supply current measureed while wiper position is fixed.

TYPICAL OPERATING CHARACTERISTICS

(T_A = 25°C, unless otherwise noted.)

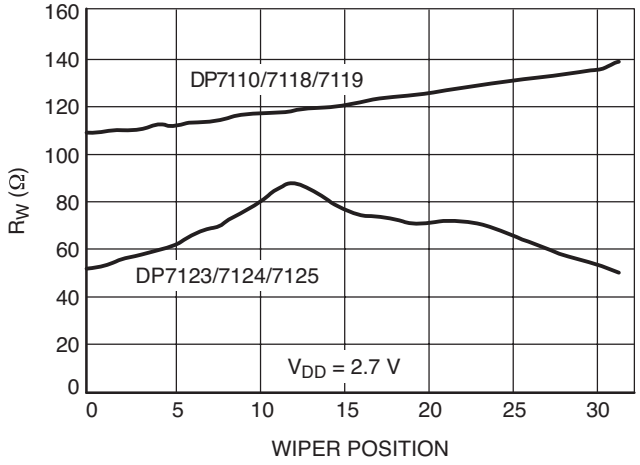


Figure 2. Wiper Resistance vs. Wiper Position

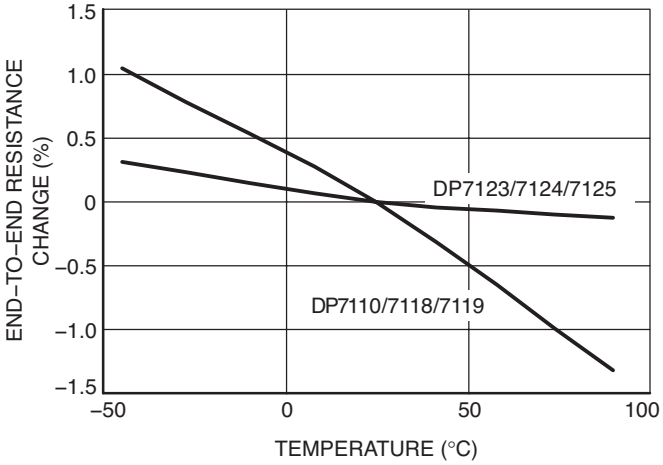


Figure 3. Change in End−to−End Resistance vs. Temperature

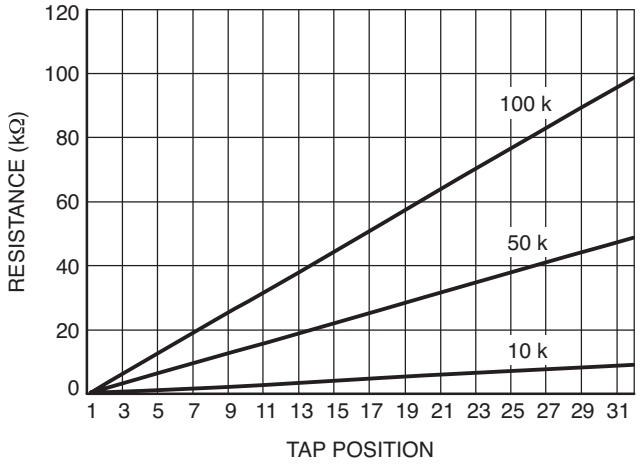


Figure 4. W−to−L Resistance vs. Tap Position

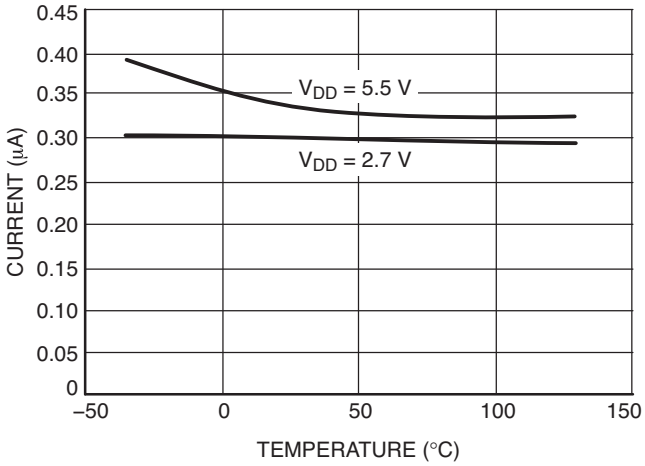


Figure 5. Supply Current vs. Temperature

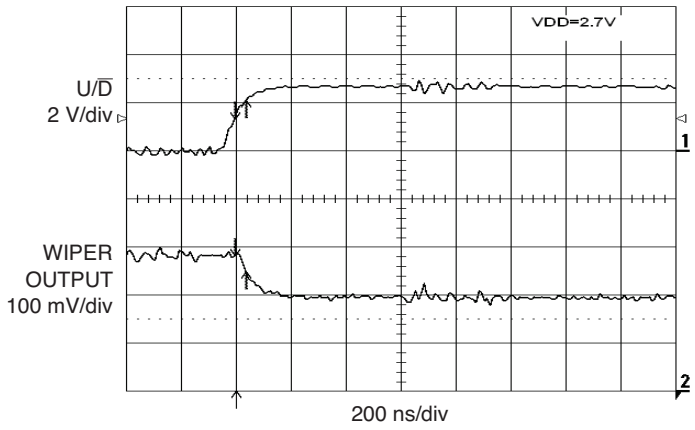


Figure 6. Tap−to−Tap Switching Transient

Functional Description

The DP7110/7118/7119/7123/7124/7125 consist of a fixed resistor and a wiper contact with 32−tap points that are digitally controlled through a 2−wire up/down serial interface. Three end−to−end resistance values are available: 10 kΩ, 50 kΩ and 100 kΩ.

The DP7110/7125 is designed to operate as a potentiometer. In this configuration, the low terminal of the resistor array is connected to ground (pin 2).

The DP7118/7123 performs as a variable resistor. In this device, the wiper terminal and high terminal of the resistor array are connected at pin 5. The DP7119/7124 is a similar variable resistor, except the low terminal is connected to pin 5.

Digital Interface Operation

The devices have two modes of operation when the serial interface is active: increment and decrement mode. The serial interface is only active when $\overline{CS}$ is low.

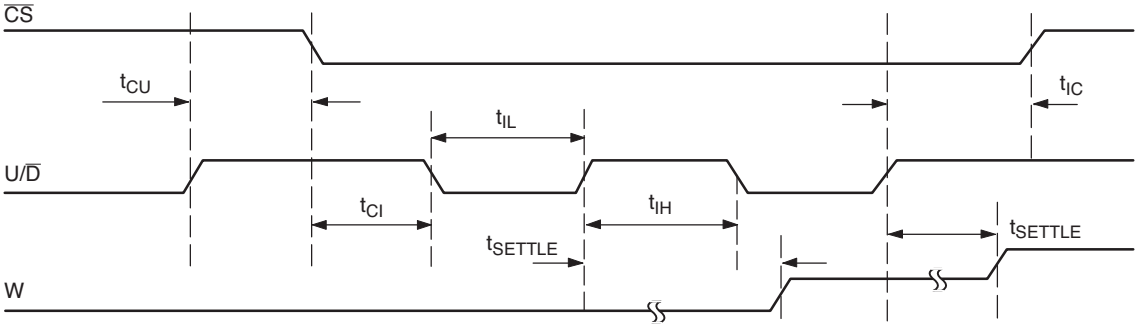
The $\overline{CS}$ and U/$\overline{D}$ inputs control the position of the wiper along the resistor array. When $\overline{CS}$ transitions from high to low, the part will go into increment mode if U/$\overline{D}$ input is high, and into decrement mode when U/$\overline{D}$ input is low. Once the mode is set, the device will remain in that mode until $\overline{CS}$ goes high again. A low−to−high transition at the U/$\overline{D}$ pin will increment or decrement the wiper position depending on the current mode (Figures 7 and 8).

When the $\overline{CS}$ input transitions to high (serial interface inactive), the value of the counter is stored and the wiper position is maintained.

Note that when the wiper reaches the maximum (or minimum) tap position, the wiper will not wrap around to the minimum (or maximum) position.

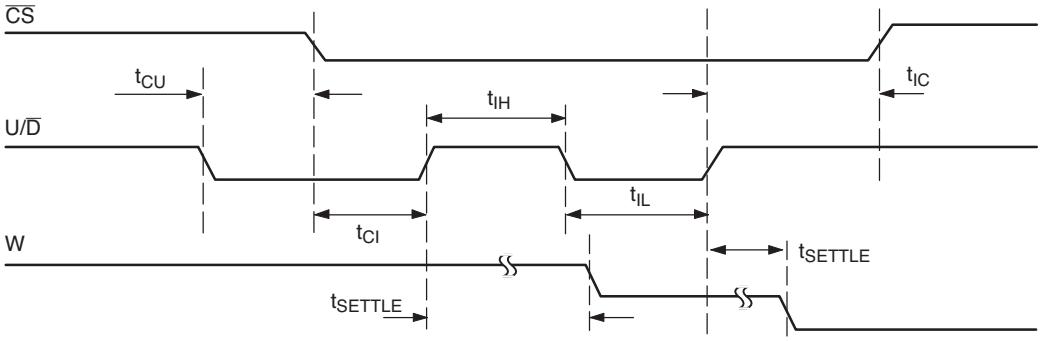
Power−On Reset

All parts in this family feature power−on reset (POR) circuitry that sets the wiper position to midscale at power−up. By default, the chip is in the increment mode.



Note: “W” is not a digital signal. It represents wiper transitions.

Figure 7. Serial Interface Timing Diagram, Increment Mode



Note: “W” is not a digital signal. It represents wiper transitions.

Figure 8. Serial Interface Timing Diagram, Decrement Mode

Applications Information

The devices are intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control, where voltage biasing adjusts the display contrast.

Alternative Positive LCD Bias Control

An op amp can be used to provide buffering and gain on the output of the DP7110/DP7125. This can be done by connecting the wiper output to the positive input of a noninverting op amp as shown in Figure 9. Figure 10 shows a similar circuit for the DP7119/DP7124.

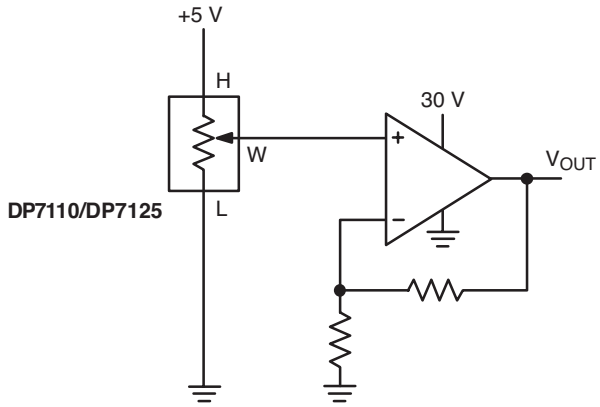


Figure 9. Positive LCD Bias Control

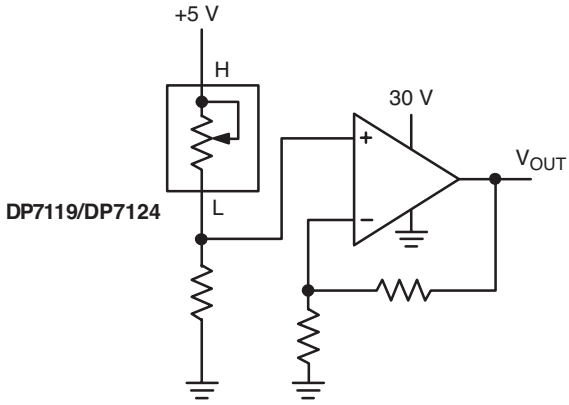


Figure 10. Positive LCD Bias Control

Adjustable Gain

Figures 11 and 12 show how to use either a variable resistor or a potentiometer to digitally adjust the gain of a noninverting op amp configuration, by connecting the device in series with a resistor to ground. The devices have a low 5 ppm/°C ratiometric tempco that allows for a very stable adjustable gain configuration over temperature.

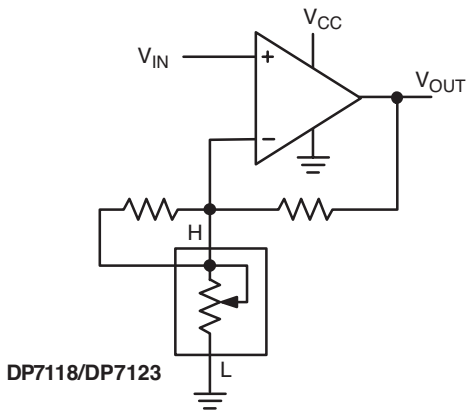


Figure 11. Adjustable Gain Circuit

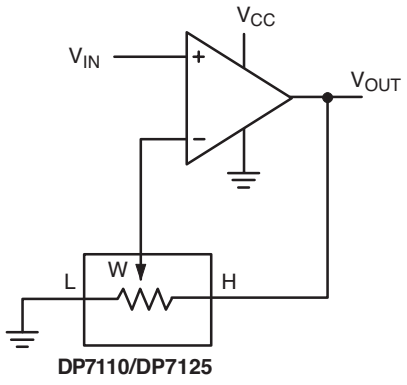
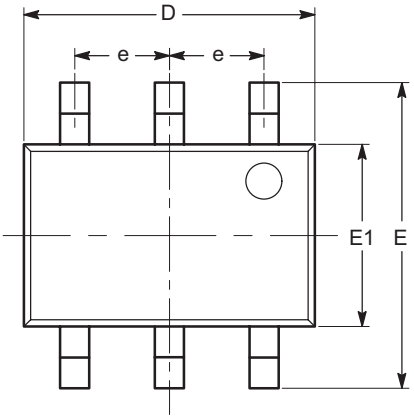


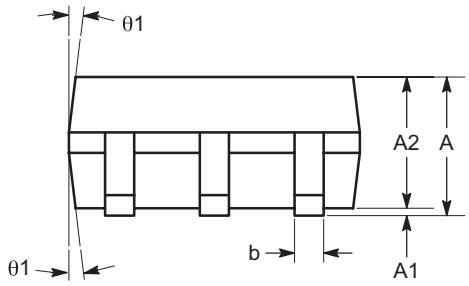
Figure 12. Adjustable Gain Circuit

PACKAGE DIMENSIONS

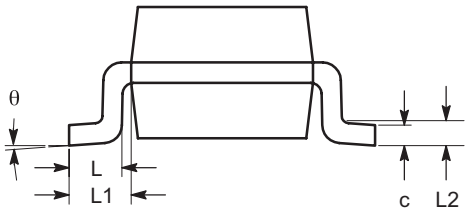
SC–70, 6 Lead, 1.25x2



TOP VIEW



SIDE VIEW



END VIEW

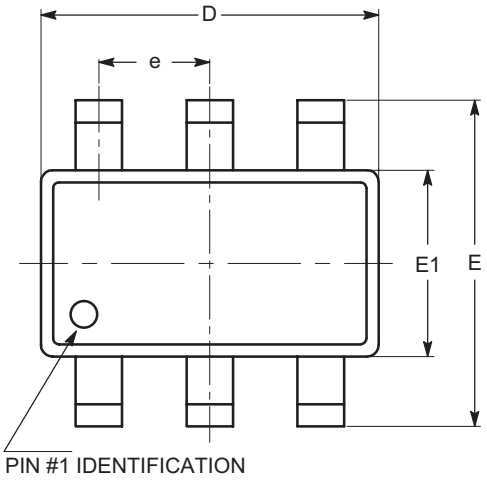
SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

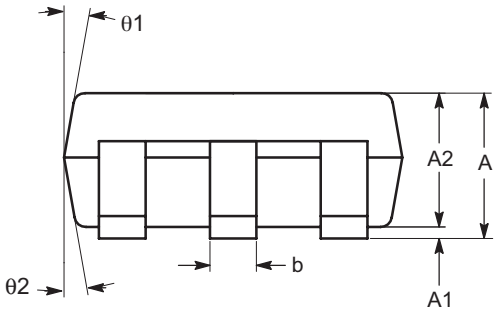
PACKAGE DIMENSIONS

SOT−23, 6 Lead

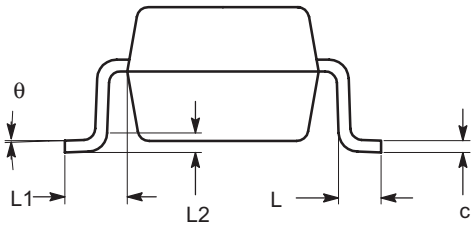


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW

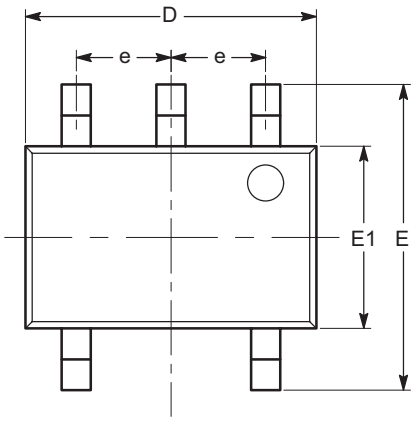


END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

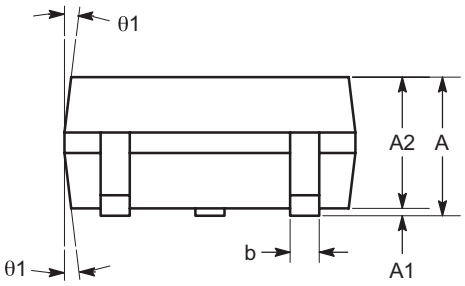
PACKAGE DIMENSIONS

SC–70, 5 Lead, 1.25x2

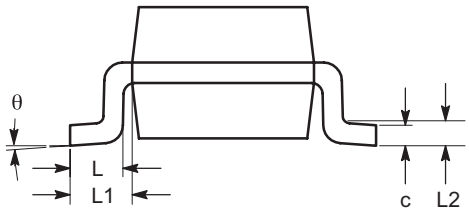


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



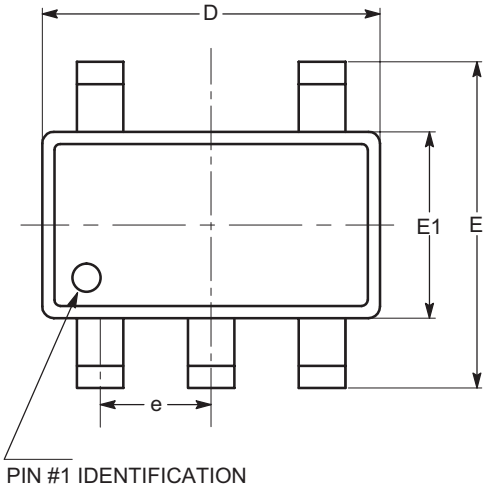
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

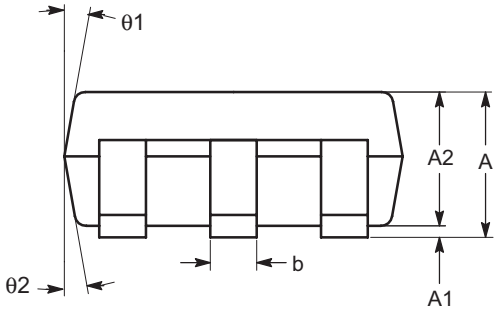
PACKAGE DIMENSIONS

SOT−23, 5 Lead

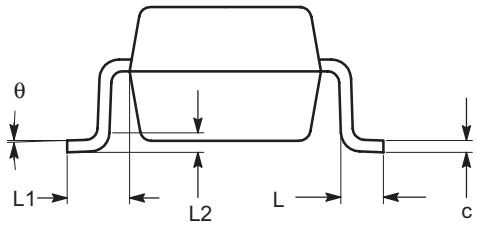


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW



END VIEW

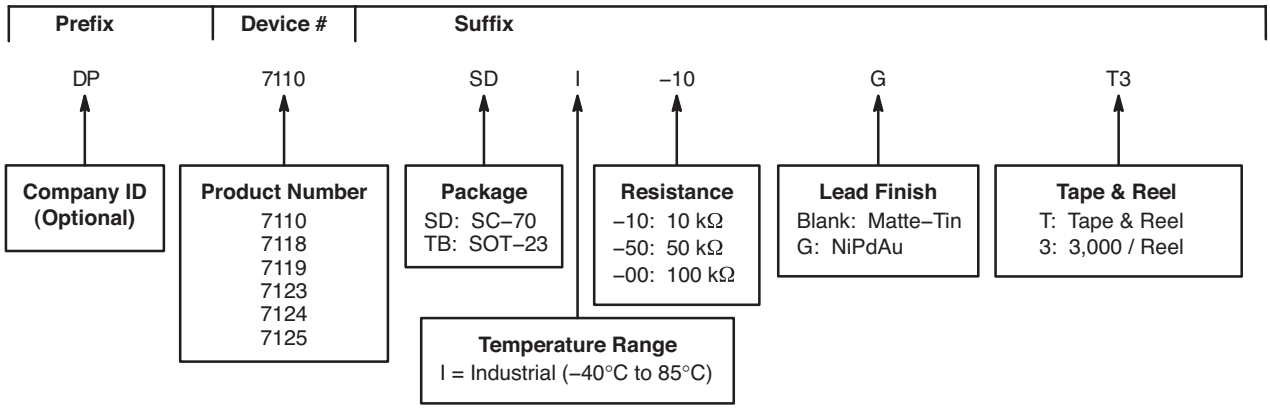
Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

Table 4. ORDERING INFORMATION

Device	Orderable Part Number	Resistor [kΩ]	Pin Package	Parts Per Reel
DP7110	DP7110SDI−10-GT3	10	SC70−6	3,000
	DP7110TBI−10−T3 (Note 6)	10	SOT23−6	3,000
	DP7110TBI−10-GT3	10	SOT23−6	3,000
	DP7110SDI−50-GT3	50	SC70−6	3,000
	DP7110TBI−50−T3 (Note 6)	50	SOT23−6	3,000
	DP7110TBI−50-GT3	50	SOT23−6	3,000
	DP7110SDI−00-GT3	100	SC70−6	3,000
	DP7110TBI−00−T3 (Note 6)	100	SOT23−6	3,000
	DP7110TBI−00-GT3	100	SOT23−6	3,000
DP7118	DP7118SDI−10-GT3	10	SC70−5	3,000
	DP7118TBI−10−T3 (Note 6)	10	SOT23−5	3,000
	DP7118TBI−10-GT3	10	SOT23−5	3,000
	DP7118SDI−50-GT3	50	SC70−5	3,000
	DP7118TBI−50−T3 (Note 6)	50	SOT23−5	3,000
	DP7118TBI−50-GT3	50	SOT23−5	3,000
	DP7118SDI−00-GT3	100	SC70−5	3,000
	DP7118TBI−00−T3 (Note 6)	100	SOT23−5	3,000
	DP7118TBI−00-GT3	100	SOT23−5	3,000
DP7119	DP7119SDI−10-GT3	10	SC70−6	3,000
	DP7119TBI−10−T3 (Note 6)	10	SOT23−6	3,000
	DP7119TBI−10-GT3	10	SOT23−6	3,000
	DP7119SDI−50-GT3	50	SC70−6	3,000
	DP7119TBI−50−T3 (Note 6)	50	SOT23−6	3,000
	DP7119TBI−50-GT3	50	SOT23−6	3,000
	DP7119SDI−00-GT3	100	SC70−6	3,000
	DP7119TBI−00−T3 (Note 6)	100	SOT23−6	3,000
	DP7119TBI−00-GT3	100	SOT23−6	3,000
DP7123 (Note 7)	DP7123TBI−10−T3 (Note 6)	10	SOT23−5	3,000
	DP7123TBI−10-GT3	10	SOT23−5	3,000
	DP7123TBI−50−T3 (Note 6)	50	SOT23−5	3,000
	DP7123TBI−50-GT3 (Note 6)	50	SOT23−5	3,000
	DP7123TBI−00−T3 (Note 6)	100	SOT23−5	3,000
	DP7123TBI−00-GT3 (Note 6)	100	SOT23−5	3,000
DP7124 (Note 7)	DP7124TBI−10−T3 (Note 6)	10	SOT23−6	3,000
	DP7124TBI−10-GT3 (Note 6)	10	SOT23−6	3,000
	DP7124TBI−50−T3 (Note 6)	50	SOT23−6	3,000
	DP7124TBI−50-GT3	50	SOT23−6	3,000
	DP7124TBI−00−T3 (Note 6)	100	SOT23−6	3,000
	DP7124TBI−00-GT3 (Note 6)	100	SOT23−6	3,000
DP7125 (Note 7)	DP7125TBI−10−T3 (Note 6)	10	SOT23−6	3,000
	DP7125TBI−10-GT3	10	SOT23−6	3,000
	DP7125TBI−50−T3 (Note 6)	50	SOT23−6	3,000
	DP7125TBI−50-GT3 (Note 6)	50	SOT23−6	3,000
	DP7125TBI−00−T3 (Note 6)	100	SOT23−6	3,000
	DP7125TBI−00-GT3 (Note 6)	100	SOT23−6	3,000

6. Contact factory for availability.
7. For DP7123, DP7124, DP7125 now being developed, please contact factory.

Example of Ordering Information (Note 10)



8. All packages are RoHS–compliant (Lead–free, Halogen–free).
9. The standard finish is NiPdAu.
10. The device used in the above example is a DP7110SDI–10-GT3 (SC–70, Industrial Temperature, 10 kΩ, NiPdAu, Tape & Reel, 3,000/Reel).
11. For additional package and temperature options, please contact your nearest COPAL ELECTRONICS Sales office.

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