

HYNIX SEMICONDUCTOR INC.
8-BIT SINGLE-CHIP MICROCONTROLLERS

GMS90C320

User's Manual (Ver. 1.2)



REVISION HISTORY

VERSION 1.2 (Oct. 2000) This book

Correct the pin number of 44-MQFP package type on page 6.

VERSION 1.1 (Oct. 1999) Before version

Version 1.2

Published by
MCU Application Team

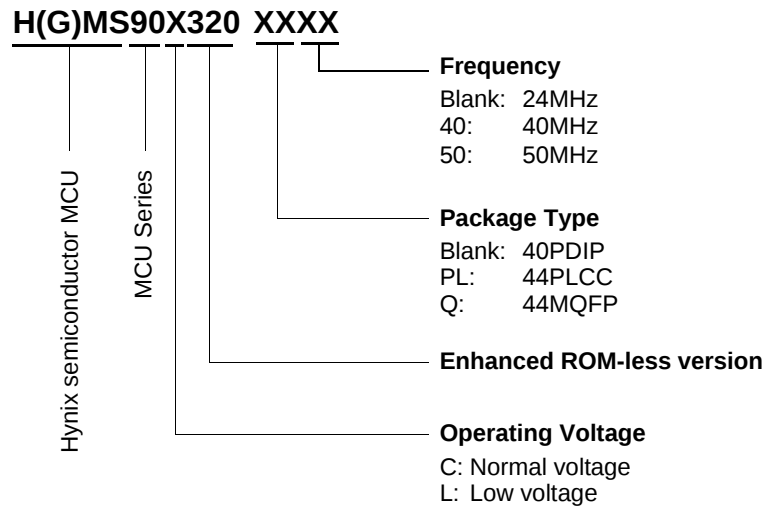
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Device Naming Structure



GMS90C320 ordering information

Operating Voltage (V)	Device Name	ROM size (bytes)	RAM size (bytes)	Operating max. Frequency (MHz)	Package Type
4.25~5.5	GMS90C320 40 GMS90C320 PL40 GMS90C320 Q40	ROM-less	256	40	40PDIP 44PLCC 44MQFP
	GMS90C320 50 GMS90C320 PL50 GMS90C320 Q50	ROM-less	256	50	40PDIP 44PLCC 44MQFP
2.7~5.5	GMS90L320 GMS90L320 PL GMS90L320 Q	ROM-less	256	24	40PDIP 44PLCC 44MQFP

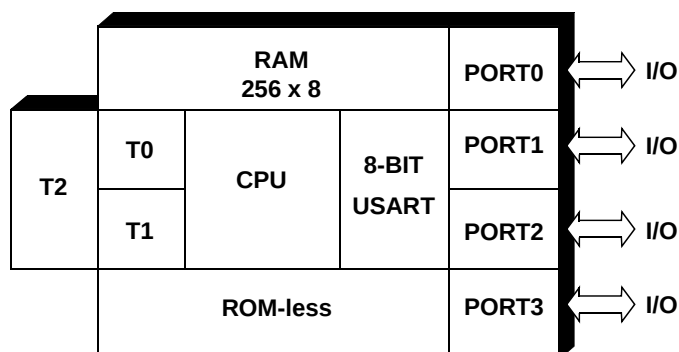
GMS90C320/L320

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER ROM-less Version for 90C52

Operating Voltage (V)	Device Name	ROM	RAM	Operating Frequency (MHz)
4.25~5.5	GMS90C320	ROM-less	256 × 8bit	40/50
2.7~5.5	GMS90L320	ROM-less	256 × 8bit	24

Features

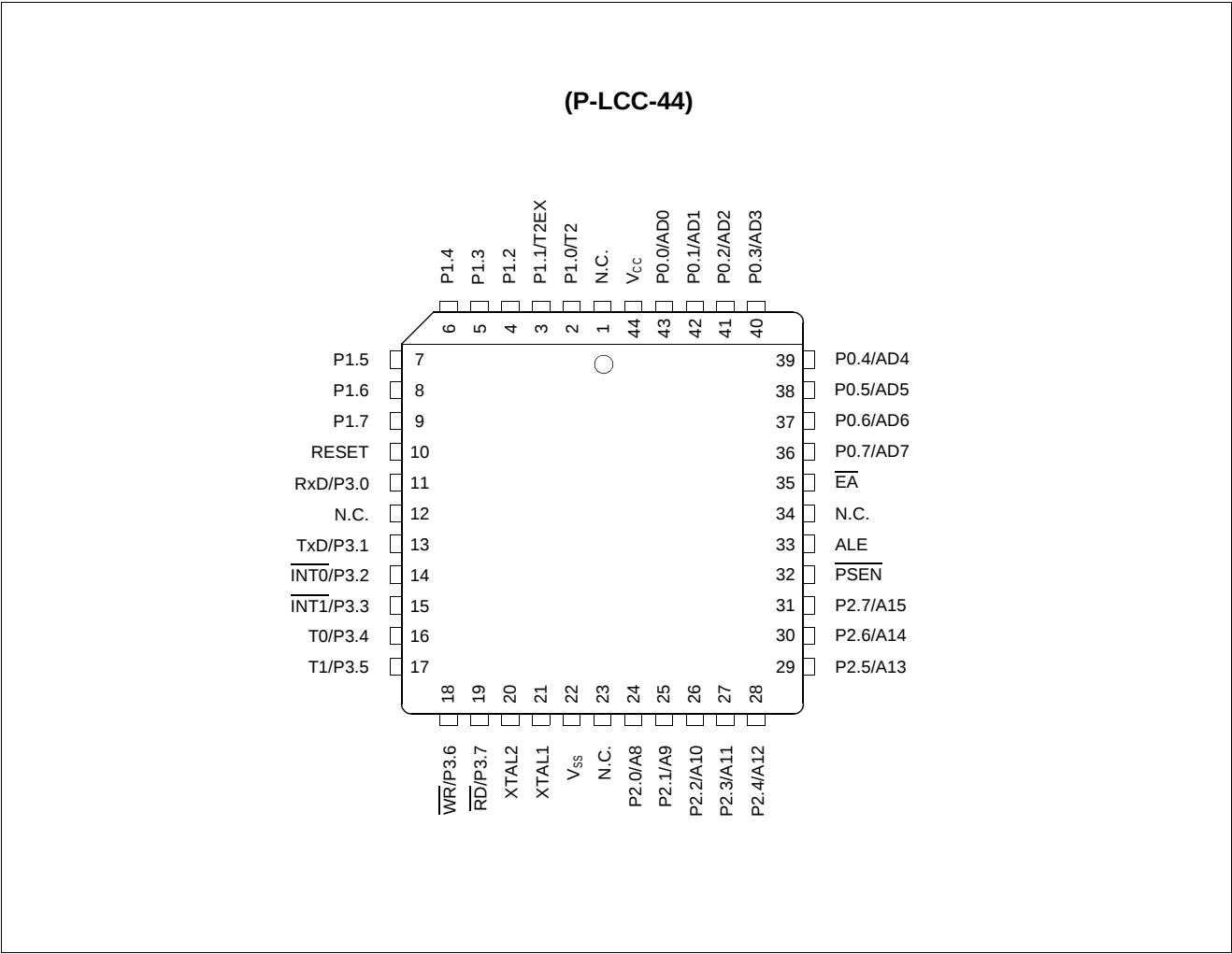
- Fully compatible to standard MCS-51 microcontroller
- Versions for 40/50 MHz operating frequency
- Low voltage version for 24MHz operating frequency
- 256 bytes of on-chip data RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers/Counters (Timer 2 with up/down counter feature)
- USART
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package



The GMS90C320 described in this document is compatible with the standard 80C32 and can be used for all present standard 80C32 applications.

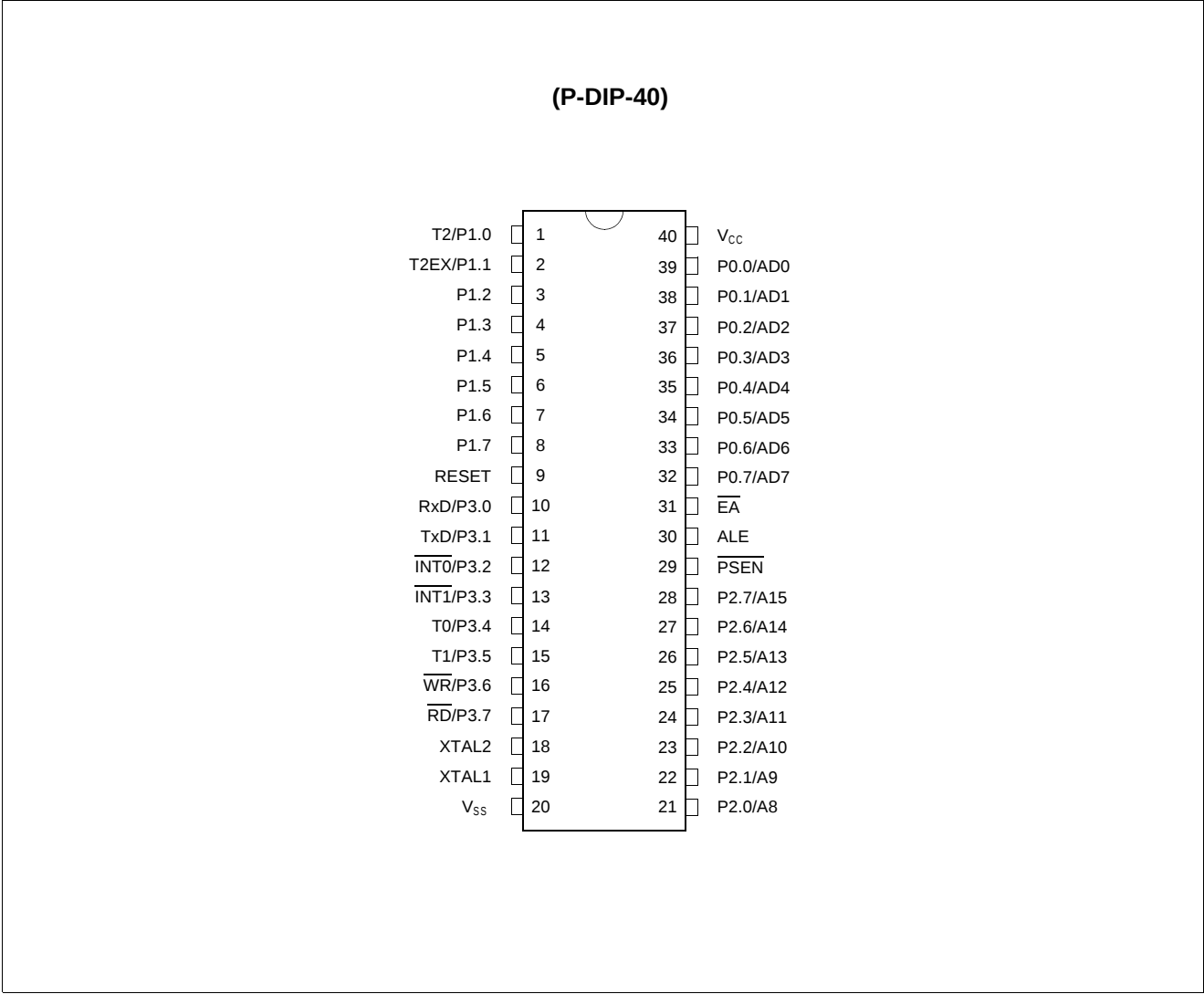
44-PLCC Pin Configuration

(top view)



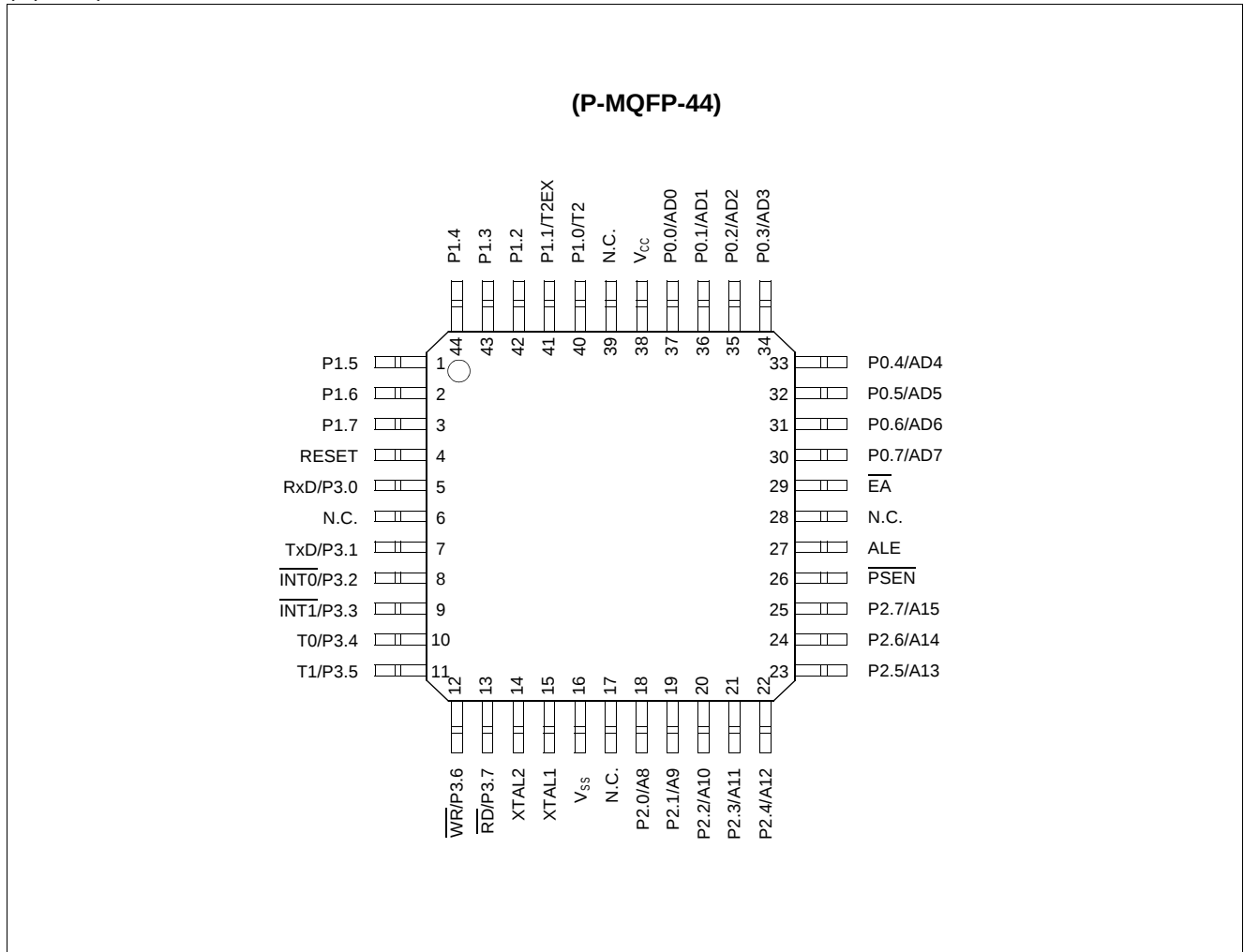
40-PDIP Pin Configuration

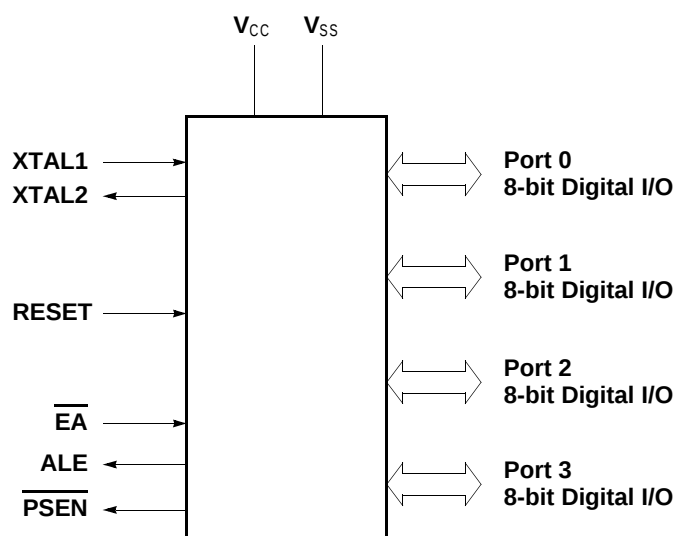
(top view)



44-PLCC Pin Configuration

(top view)





Logic Symbol

Pin Definitions and functions

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0-P1.7	2-9	1-8	40-44, 1-3	I/O	Port1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the pull-ups (I_{IL} , in the DC characteristics). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port1 also serves alternate functions of Timer 2. P1.0/T2: Timer/counter 2 external count input P1.1/T2EX: Timer/counter 2 trigger input
	2 3	1 2	40 41		
P3.0-P3.7	11,13-19	10-17	5, 7-13	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL} , in the DC characteristics) because of internal pull-up resistors. Port 3 also serves the special features of the 80C51 family, as listed below. P3.0/RxD receiver data input (asynchronous) or data input output (synchronous) of the serial interface 0 P3.1 / TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0 P3.2 / $\overline{INT0}$ interrupt 0 input / timer 0 gate control P3.3 / $\overline{INT1}$ interrupt 1 input / timer 1 gate control P3.4 / T0 counter 0 input P3.5 / T1 counter 1 input P3.6 / $\overline{WR}$ the write control signal latches the data byte from port 0 into the external data memory P3.7 / $\overline{RD}$ the read control signal enables the external data memory to port 0
	11	10	5		
	13	11	7		
	14	12	8		
	15	13	9		
	16	14	10		
	17	15	11		
	18	16	12		
	19	17	13		
XTAL2	20	18	14	O	XTAL2 Output of the inverting oscillator amplifier
XTAL1	21	19	15	I	XTAL1 Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P2.0-P2.7	24-31	21-28	18-25	I/O	Port 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the pull-ups (I_{IL} , in the DC characteristics). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	29	26	O	The Program Store Enable The read strobe to external program memory when the device is executing code from the external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activation are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
RESET	10	9	4	I	RESET A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC} .
ALE	33	30	27	O	The Address Latch Enable Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{\text{EA}}$	35	31	29	I	External Access Enable $\overline{\text{EA}}$ must be external held low to enable the device to fetch code from external program memory locations 0000 _H to FFFF _H . If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than its internal memory size.
P0.0-P0.7	43-36	39-32	37-30	I/O	Port 0 Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the GMS97C5x. External pull-up resistors are required during program verification.
V_{SS}	22	20	16	-	Circuit ground potential
V_{CC}	44	40	38	-	Supply terminal for all operating modes
N.C.	1,12, 23,34	-	6,17, 28,39	-	No connection

Function Description

The GMS90 series is fully compatible to the standard 8051 microcontroller family.

It is compatible with the standard 80C32. While maintaining all architectural and operational characteristics of the standard 80C32, the GMS90C320 incorporates some enhancements in the Timer 2 unit.

Figure 1 shows a block diagram of the GMS90C320

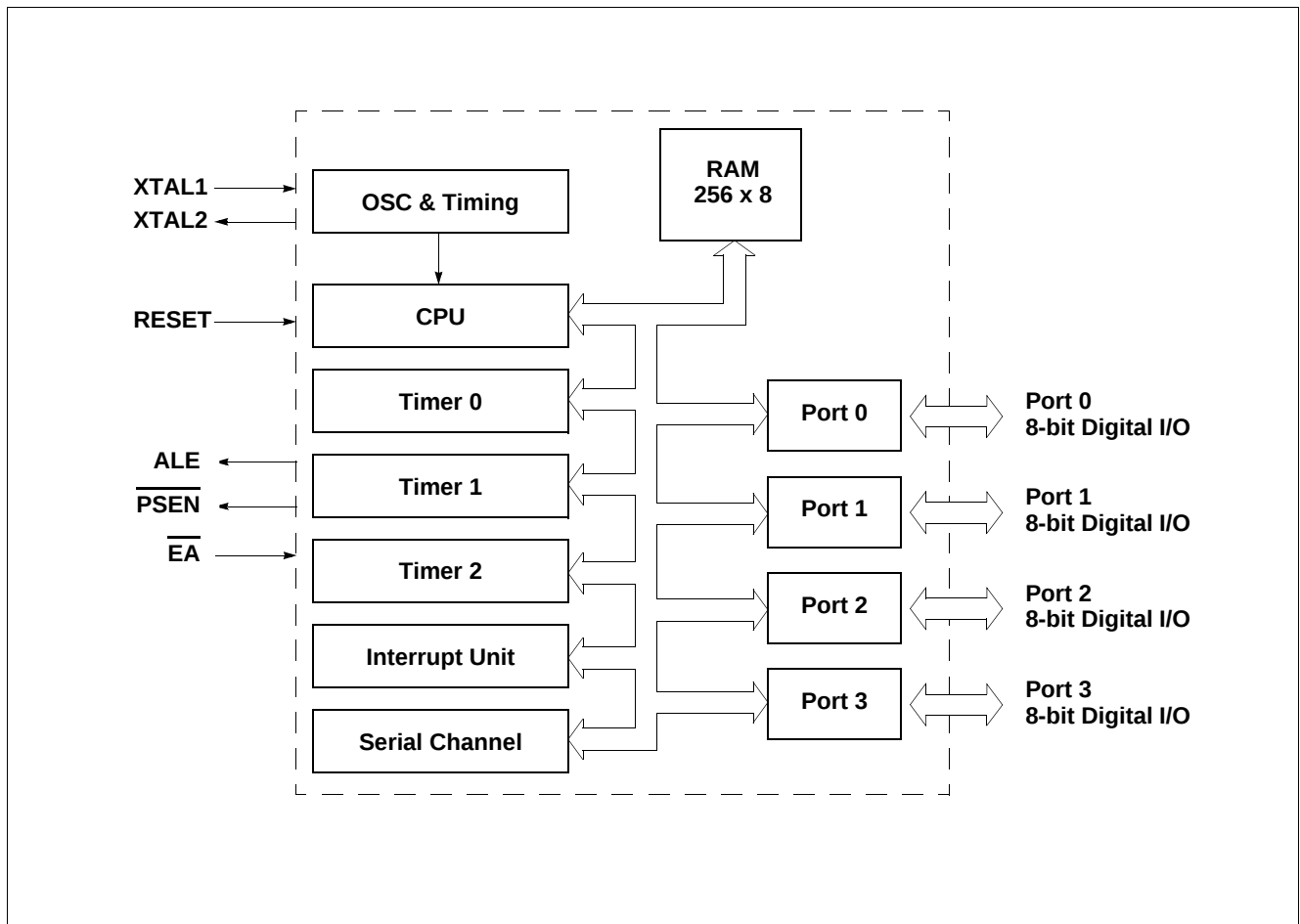


Figure 1 Block Diagram of the GMS90C320

CPU

The GMS90C320 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0μs.

Special Function Register PSW

	MSB				LSB				
Bit No.	7	6	5	4	3	2	1	0	
Addr. D0 _H	CY	AC	F0	RS1	RS2	OV	F1	P	PSW

Bit	Function
CY	Carry Flag
AC	Auxiliary Carry Flag (for BCD operation)
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits
0 0	Bank 0 selected, data address 00 _H -07 _H
0 1	Bank 1 selected, data address 08 _H -0F _H
1 0	Bank 2 selected, data address 10 _H -17 _H
1 1	Bank 3 selected, data address 18 _H -1F _H
OV	Overflow Flag
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00_H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **Table 1**, **Table 2**, and **Table 3**.

In **Table 1** they are organized in numeric order of their addresses. In **Table 2** they are organized in groups which refer to the functional blocks of the GMS90C320. **Table 3** illustrates the contents of the SFRs.

Table 1
Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80_H	P0¹⁾	FF_H	A0_H	P2¹⁾	FF_H
81 _H	SP	07 _H	A1 _H	reserved	XX _H ²⁾
82 _H	DPL	00 _H	A2 _H	reserved	XX _H ²⁾
83 _H	DPH	00 _H	A3 _H	reserved	XX _H ²⁾
84 _H	reserved	XX _H ²⁾	A4 _H	reserved	XX _H ²⁾
85 _H	reserved	XX _H ²⁾	A5 _H	reserved	XX _H ²⁾
86 _H	reserved	XX _H ²⁾	A6 _H	reserved	XX _H ²⁾
87 _H	PCON	0XXX0000 _B ²⁾	A7 _H	reserved	XX _H ²⁾
88_H	TCON¹⁾	00_H	A8_H	IE¹⁾	0X000000_B²⁾
89 _H	TMOD	00 _H	A9 _H	reserved	XX _H ²⁾
8A _H	TL0	00 _H	AA _H	reserved	XX _H ²⁾
8B _H	TL1	00 _H	AB _H	reserved	XX _H ²⁾
8C _H	TH0	00 _H	AC _H	reserved	XX _H ²⁾
8D _H	TH1	00 _H	AD _H	reserved	XX _H ²⁾
8E _H	reserved	XX _H ²⁾	AE _H	reserved	XX _H ²⁾
8F _H	reserved	XX _H ²⁾	AF _H	reserved	XX _H ²⁾
90_H	P1¹⁾	FF_H	B0_H	P3¹⁾	FF_H
91 _H	reserved	00 _H	B1 _H	reserved	XX _H ²⁾
92 _H	reserved	XX _H ²⁾	B2 _H	reserved	XX _H ²⁾
93 _H	reserved	XX _H ²⁾	B3 _H	reserved	XX _H ²⁾
94 _H	reserved	XX _H ²⁾	B4 _H	reserved	XX _H ²⁾
95 _H	reserved	XX _H ²⁾	B5 _H	reserved	XX _H ²⁾
96 _H	reserved	XX _H ²⁾	B6 _H	reserved	XX _H ²⁾
97 _H	reserved	XX _H ²⁾	B7 _H	reserved	XX _H ²⁾
98_H	SCON¹⁾	00_H	B8_H	IP¹⁾	XX000000_B²⁾
99 _H	SBUF	XX _H ²⁾	B9 _H	reserved	XX _H ²⁾
9A _H	reserved	XX _H ²⁾	BA _H	reserved	XX _H ²⁾
9B _H	reserved	XX _H ²⁾	BB _H	reserved	XX _H ²⁾
9C _H	reserved	XX _H ²⁾	BC _H	reserved	XX _H ²⁾
9D _H	reserved	XX _H ²⁾	BD _H	reserved	XX _H ²⁾
9E _H	reserved	XX _H ²⁾	BE _H	reserved	XX _H ²⁾
9F _H	reserved	XX _H ²⁾	BF _H	reserved	XX _H ²⁾

1) : Bit-addressable Special Function Register

2) : X means that the value is indeterminate and the location is reserved

Table 1
Special Function Registers in numeric order of their addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
C0_H	reserved	XX _H ²⁾	E0_H	ACC¹⁾	00_H
C1 _H	reserved	XX _H ²⁾	E1 _H	reserved	XX _H ²⁾
C2 _H	reserved	XX _H ²⁾	E2 _H	reserved	XX _H ²⁾
C3 _H	reserved	XX _H ²⁾	E3 _H	reserved	XX _H ²⁾
C4 _H	reserved	XX _H ²⁾	E4 _H	reserved	XX _H ²⁾
C5 _H	reserved	XX _H ²⁾	E5 _H	reserved	XX _H ²⁾
C6 _H	reserved	XX _H ²⁾	E6 _H	reserved	XX _H ²⁾
C7 _H	reserved	XX _H ²⁾	E7 _H	reserved	XX _H ²⁾
C8_H	T2CON¹⁾	00_H	E8_H	reserved	XX _H ²⁾
C9 _H	T2MOD	XXXXXXXX0 _B ²⁾	E9 _H	reserved	XX _H ²⁾
CA _H	RC2L	00 _H	EA _H	reserved	XX _H ²⁾
CB _H	RC2H	00 _H	EB _H	reserved	XX _H ²⁾
CC _H	TL2	00 _H	EC _H	reserved	XX _H ²⁾
CD _H	TH2	00 _H	ED _H	reserved	XX _H ²⁾
CE _H	reserved	XX _H ²⁾	EE _H	reserved	XX _H ²⁾
CF _H	reserved	XX _H ²⁾	EF _H	reserved	XX _H ²⁾
D0_H	PSW¹⁾	00_H	F0_H	B¹⁾	00_H
D1 _H	reserved	XX _H ²⁾	F1 _H	reserved	XX _H ²⁾
D2 _H	reserved	XX _H ²⁾	F2 _H	reserved	XX _H ²⁾
D3 _H	reserved	XX _H ²⁾	F3 _H	reserved	XX _H ²⁾
D4 _H	reserved	XX _H ²⁾	F4 _H	reserved	XX _H ²⁾
D5 _H	reserved	XX _H ²⁾	F5 _H	reserved	XX _H ²⁾
D6 _H	reserved	XX _H ²⁾	F6 _H	reserved	XX _H ²⁾
D7 _H	reserved	XX _H ²⁾	F7 _H	reserved	XX _H ²⁾
D8_H	reserved	XX _H ²⁾	F8_H	reserved	XX _H ²⁾
D9 _H	reserved	XX _H ²⁾	F9 _H	reserved	XX _H ²⁾
DA _H	reserved	XX _H ²⁾	FA _H	reserved	XX _H ²⁾
DB _H	reserved	XX _H ²⁾	FB _H	reserved	XX _H ²⁾
DC _H	reserved	XX _H ²⁾	FC _H	reserved	XX _H ²⁾
DD _H	reserved	XX _H ²⁾	FD _H	reserved	XX _H ²⁾
DE _H	reserved	XX _H ²⁾	FE _H	reserved	XX _H ²⁾
DF _H	reserved	XX _H ²⁾	FF _H	reserved	XX _H ²⁾

¹⁾ : Bit-addressable Special Function Register

²⁾ : X means that the value is indeterminate and the location is reserved

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Content after Reset
CPU	ACC	Accumulator	E0_H ¹⁾	00 _H
	B	B-Register	F0_H ¹⁾	00 _H
	DPH	Data Pointer, High Byte	83 _H	00 _H
	DPL	Data Pointer, Low Byte	82 _H	00 _H
	PSW	Program Status Word Register	D0_H ¹⁾	00 _H
	SP	Stack Pointer	81 _H	07 _H
Interrupt System	IE	Interrupt Enable Register	A8_H ¹⁾	0X000000 _B ²⁾
	IP	Interrupt Priority Register	B8_H ¹⁾	XX000000 _B ²⁾
Ports	P0	Port 0	80_H ¹⁾	FF _H
	P1	Port 1	90_H ¹⁾	FF _H
	P2	Port 2	A0_H ¹⁾	FF _H
	P3	Port 3	B0_H ¹⁾	FF _H
Serial Channels	PCON	Power Control Register	87 _H	0XXX0000 _B ²⁾
	SBUF	Serial Channel Buffer Register	99 _H	XX _H ³⁾
	SCON	Serial Channel 0 Control Register	98_H ¹⁾	00 _H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	88_H ¹⁾	00 _H
	TH0	Timer 0, High Byte	8C _H	00 _H
	TH1	Timer 1, High Byte	8D _H	00 _H
	TL0	Timer 0, Low Byte	8A _H	00 _H
	TL1	Timer 1, Low Byte	8B _H	00 _H
	TMOD	Timer Mode Register	89 _H	00 _H
Timer 2	T2CON	Timer 2 Control Register	C8_H ¹⁾	00 _H
	T2MOD	Timer 2 Mode Register	C9 _H	XXXXXXX0 _B ²⁾
	RC2H	Timer 2 Reload Capture Register, High Byte	CB _H	00 _H
	RC2L	Timer 2 Reload Capture Register, Low Byte	CA _H	00 _H
	TH2	Timer 2, High Byte	CD _H	00 _H
	TL2	Timer 2, Low Byte	CC _H	00 _H
Power Saving Modes	PCON	Power Control Register	87 _H	0XXX0000 _B ²⁾

¹⁾ Bit-addressable Special Function Registers

²⁾ This special function register is listed repeatedly since some bits of it also belong to other functional blocks

³⁾ X means that the value is indeterminate and the location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80 _H	P0								
81 _H	SP								
82 _H	DPL								
83 _H	DPH								
87 _H	PCON	SMOD	-	-	-	GF1	GF0	PDE	IDLE
88 _H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89 _H	TMOD	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0
8A _H	TL0								
8B _H	TL1								
8C _H	TH0								
8D _H	TH1								
90 _H	P1								
98 _H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99 _H	SBUF								
A0 _H	P2								
A8 _H	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0
B0 _H	P3								
B8 _H	IP	-	-	PT2	PS	PT1	PX1	PT0	PX0
C8 _H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
C9 _H	T2MOD	-	-	-	-	-	-	-	DCEN

--	--	--	--	--	--	--	--

SFR bit and byte addressable

--	--	--	--	--	--	--	--	--	--

SFR not bit addressable

-

This bit location is reserved.

Table 3
Contents of SFRs, SFRs in Numeric Order (cont'd)

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CA _H	RC2L								
CB _H	RC2H								
CC _H	TL2								
CD _H	TH2								
D0 _H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0 _H	ACC								
F0 _H	B								

--	--	--	--	--	--	--	--

SFR bit and byte addressable

--	--	--	--	--	--	--	--

SFR not bit addressable

-

This bit location is reserved.

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 4**:

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		GATE	C/ $\bar{T}$	M1	M0	Internal	External (Max.)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$\frac{f_{OSC}}{12 \times 32}$	$\frac{f_{OSC}}{24 \times 32}$
1	16-bit timer/counter	X	X	0	1	$\frac{f_{OSC}}{12}$	$\frac{f_{OSC}}{24}$
2	8-bit timer/counter with 8-bit autoreload	X	X	1	0	$\frac{f_{OSC}}{12}$	$\frac{f_{OSC}}{24}$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$\frac{f_{OSC}}{12}$	$\frac{f_{OSC}}{24}$

In the “timer” function ($C/\bar{T} = “0”$) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$. In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin ($P3.4/T0$, $P3.5/T1$). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ ($P3.2$, $P3.3$) can be programmed to function as a gate to facilitate pulse width measurements.

Figure 2 illustrates the input clock logic.

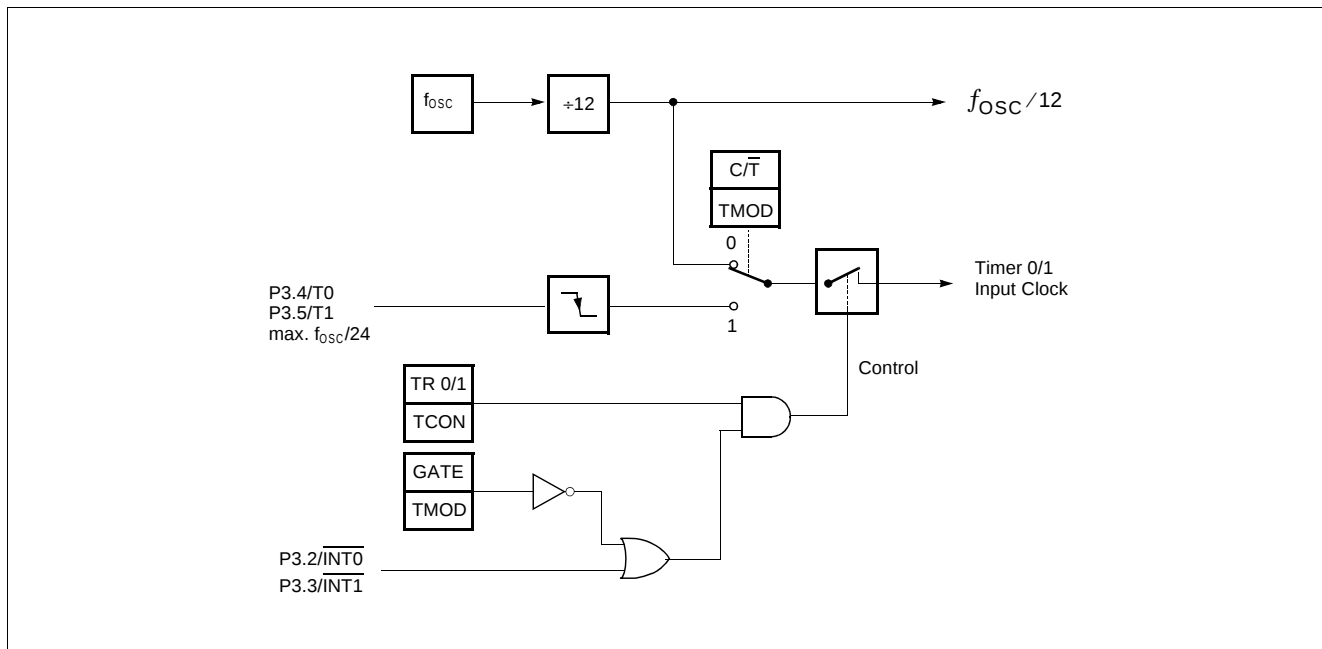


Figure 2 Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/T $\overline{2}$ (T2CON.1). It has three operating modes as shown in **Table 5**.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD DECN	T2CON EXEN	P1.1 T2EX	Remarks	Input Clock	
	RxCLK or TxCLK	CP/ RL2	TR2					Internal	External (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$\frac{f_{osc}}{12}$	max. $\frac{f_{osc}}{24}$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/Counter (only up-counting)	$\frac{f_{osc}}{12}$	max. $\frac{f_{osc}}{24}$
	0	1	1	X	1	↓	capture TH1, TL2 → RC2H, RC2L		
Baud Rate Generator	1	X	1	X	0	X	no overflow interrupt request (TF2)	$\frac{f_{osc}}{12}$	max. $\frac{f_{osc}}{24}$
	1	X	1	X	1	↓	extra external interrupt ("Timer 2")		
off	X	X	0	X	X	X	Timer 2 stops	-	-

1Note: ↓ =  falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 6**. The possible baud rates can be calculated using the formulas given in **Table 7**.

Table 6
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$\frac{f_{OSC}}{12}$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$\frac{f_{OSC}}{32}$ or $\frac{f_{OSC}}{64}$	9-bit UART 11 bits are transmitted (through TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baud rates

Baud Rate derived from	Interface Mode	Baud rate
Oscillator	0	$\frac{f_{OSC}}{12}$
	2	$\frac{2SMOD \times f_{OSC}}{64}$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autore-load)	1, 3	$\frac{2SMOD \times \text{timer 1 overflow rate}}{32}$
	1, 3	$\frac{2SMOD \times f_{OSC}}{32 \times 12 \times (256 - TH1)}$
Timer 2	1, 3	$\frac{f_{OSC}}{32 \times [65536 - (RC2H, RC2L)]}$

Interrupt System

The GMS90C320 provides 6 interrupt sources with two priority levels. Figure 3 gives a general overview of the interrupt sources and illustrates the request and control flags.

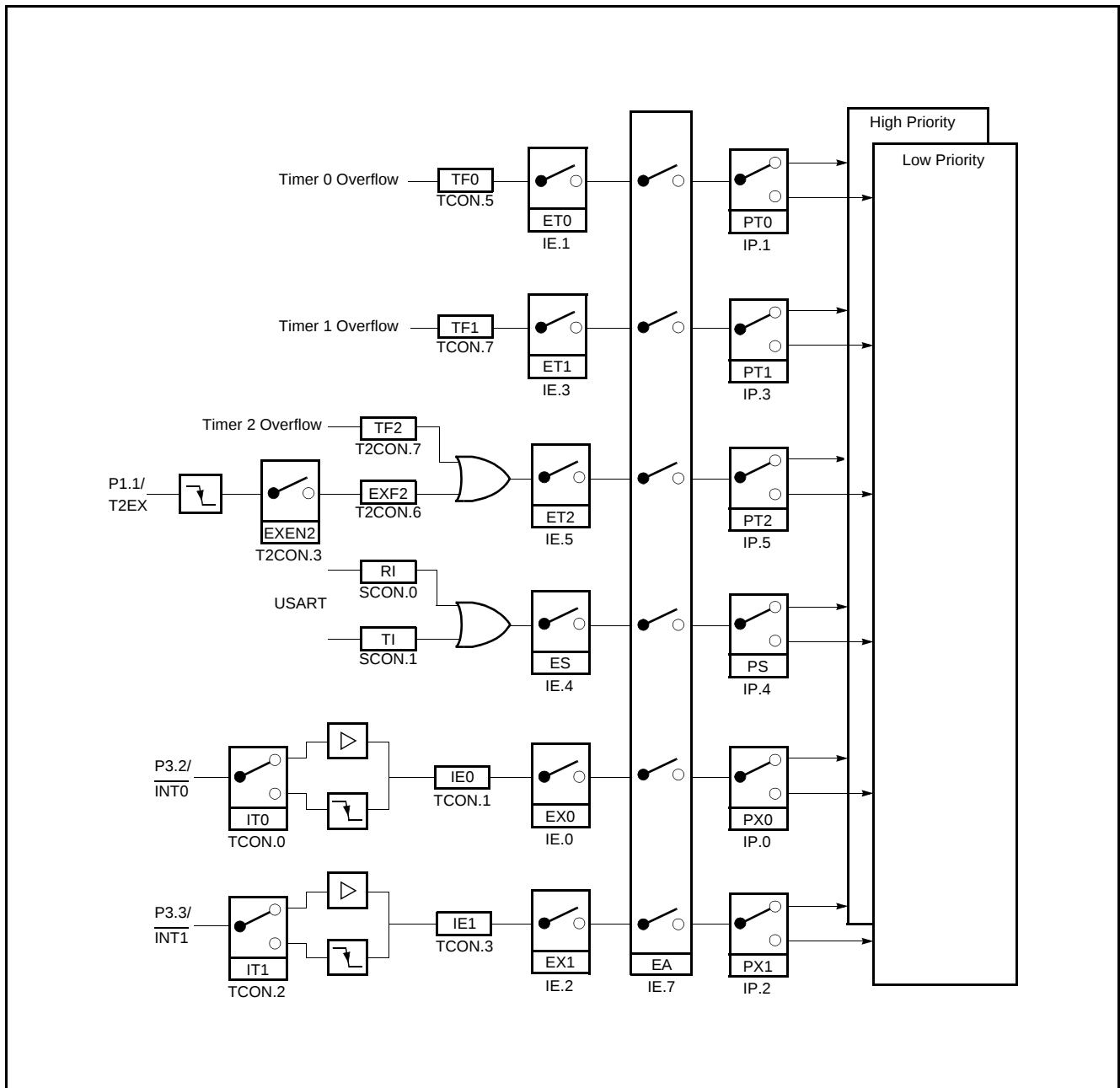


Figure 3
Interrupt Request Sources

Table 8
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003 _H
TF0	Timer 0 interrupt	000B _H
IE1	External interrupt 1	0013 _H
TF1	Timer 1 interrupt	001B _H
RI+TI	Serial port interrupt	0023 _H
TF2+EXF2	Timer 2 interrupt	002B _H

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **Table 9**.

Table 9
Interrupt Priority-Within-Level

Interrupt Source		Priority
IE0	External interrupt 0	High ↓
TF0	Timer 0 interrupt	
IE1	External interrupt 1	
TF1	Timer 1 interrupt	
RI+TI	Serial port interrupt	Low
TF2+EXF2	Timer 2 interrupt	

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON,#01H	- enabled interrupt - Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down Mode	ORL PCON,#02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down Mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T _A)	-40 to + 85°C
Storage temperature (T _{ST}).....	-65 to + 150°C
Voltage on V _{CC} pins with respect to ground (V _{SS}).....	-0.5 V to 6.5 V
Voltage on any pin with respect to ground (V _{SS}).....	-0.5 to V _{CC} + 0.5 V
Input current on any pin during overload condition	-10 mA to + 10 mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation.....	TBD

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions (V_{IN} > V_{CC} or V_{IN} < V_{SS}) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

DC Characteristics for GMS90C320

$V_{CC} = 5V \pm 10\%, -15\%$; $V_{SS} = 0V$; $T_A = 0^\circ C$ to $70^\circ C$

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	-0.5	$0.2V_{CC} - 0.1$	V	-
Input low voltage ($\overline{EA}$)	V_{IL1}	-0.5	$0.2V_{CC} - 0.3$	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2V_{CC} + 0.1$	V	-
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	$0.2V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7V_{CC}$	$V_{CC} + 0.5$	V	-
Input high voltage to $\overline{EA}$, RESET	V_{IH2}	$0.6V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.3 0.45 1.0	V	$I_{OL} = 100\mu A$ $I_{OL} = 1.6mA^{1)}$ $I_{OL} = 3.5mA$
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	-	0.3 0.45 1.0	V	$I_{OL} = 200\mu A$ $I_{OL} = 3.2mA^{1)}$ $I_{OL} = 7.0mA$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9V_{CC}$	-	V	$I_{OH} = -80\mu A$ $I_{OH} = -10\mu A$
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH1}	2.4 $0.9V_{CC}$	-	V	$I_{OH} = -800\mu A^{2)}$ $I_{OH} = -80\mu A^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	$V_{IN} = 0.45V$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	μA	$V_{IN} = 2.0V$
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_c = 1MHz$, $T_A = 25^\circ C$
Power supply current:					
Active mode, 12MHz ³⁾	I_{CC}	-	16	mA	$V_{CC} = 5V^{4)}$
Idle mode, 12MHz ³⁾	I_{CC}	-	7.5	mA	$V_{CC} = 5V^{5)}$
Active mode, 24 MHz ³⁾	I_{CC}	-	26	mA	$V_{CC} = 5V^{4)}$
Idle mode, 24MHz ³⁾	I_{CC}	-	13.5	mA	$V_{CC} = 5V^{5)}$
Active mode, 40 MHz ³⁾	I_{CC}	-	44	mA	$V_{CC} = 5V^{4)}$
Idle mode, 40 MHz ³⁾	I_{CC}	-	18	mA	$V_{CC} = 5V^{5)}$
Active mode, 50 MHz ³⁾	I_{CC}	-	55	mA	$V_{CC} = 5V^{4)}$
Idle mode, 50 MHz ³⁾	I_{CC}	-	22.5	mA	$V_{CC} = 5V^{5)}$
Power Down Mode ³⁾	I_{PD}	-	50	μA	$V_{CC} = 5.5V^{6)}$

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading: $> 50\text{pF}$ at 3.3V , $> 100\text{pF}$ at 5V), the noise pulse on ALE line may exceed 0.8V . In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the $0.9V_{CC}$ specification when the address lines are stabilizing.
- 3) $I_{CC \text{ max}}$ at other frequencies is given by:
 active mode: $I_{CC} = 1.0 \times f_{OSC} + 3.16$
 idle mode: $I_{CC} = 0.37 \times f_{OSC} + 3.63$
 where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5\text{V}$.
- 4) I_{CC} (active mode) is measured with:
 XTAL1 driven with $t_{CLCH}, t_{CHCL} = 5\text{ns}$, $V_{IL} = V_{SS} + 0.5\text{V}$, $V_{IH} = V_{CC} - 0.5\text{V}$; XTAL2 = N.C.;
 $\overline{\text{EA}} = \text{Port 0} = \text{RESET} = V_{CC}$; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1mA).
- 5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 XTAL1 driven with $t_{CLCH}, t_{CHCL} = 5\text{ns}$, $V_{IL} = V_{SS} + 0.5\text{V}$, $V_{IH} = V_{CC} - 0.5\text{V}$; XTAL2 = N.C.;
 $\text{RESET} = \overline{\text{EA}} = V_{SS}$; $\text{Port0} = V_{CC}$; all other pins are disconnected;
- 6) I_{PD} (Power Down Mode) is measured under following conditions:
 $\overline{\text{EA}} = \text{Port 0} = V_{CC}$; $\text{RESET} = V_{SS}$; XTAL2 = N.C.; XTAL1 = V_{SS} ; all other pins are disconnected.

DC Characteristics for GMS90L320

$V_{CC} = 3.3V + 0.3V, -0.6V$; $V_{SS} = 0V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45 0.30	V	$I_{OL} = 1.6mA^{1)}$ $I_{OL} = 100\mu A^{1)}$
Output low voltage (port 0, ALE, PSEN)	V_{OL1}	-	0.45 0.30	V	$I_{OL} = 3.2mA^{1)}$ $I_{OL} = 200\mu A^{1)}$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.0 $0.9V_{CC}$	-	V	$I_{OH} = -20\mu A$ $I_{OH} = -10\mu A$
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.0 $0.9V_{CC}$	-	V	$I_{OH} = -800\mu A^{2)}$ $I_{OH} = -80\mu A^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	μA	$V_{IN} = 0.45V$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	μA	$V_{IN} = 2.0V$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1MHz$ $T_A = 25^{\circ}C$
Power supply current:					
Active mode, 16 MHz ³⁾	I_{CC}	-	10	mA	$V_{CC} = 3.3V^{4)}$
Idle mode, 16MHz ³⁾	I_{CC}	-	5.25	mA	$V_{CC} = 3.3V^{5)}$
Active mode, 24MHz ³⁾	I_{CC}	-	16		$V_{CC} = 3.3V^{4)}$
Idle mode, 24MHz ³⁾	I_{CC}	-	8.25		$V_{CC} = 3.3V^{5)}$
Power Down Mode ³⁾	I_{PD}	-	10	μA	$V_{CC} = 3.6V^{6)}$

AC Characteristics

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a 't' (stand for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address

C: Clock

D: Input Data

H: Logic level HIGH

I: Instruction (program memory contents)

L: Logic level LOW, or ALE

P: $\overline{\text{PSEN}}$

Q: Output Data

R: $\overline{\text{RD}}$ signal

T: Time

V: Valid

W: $\overline{\text{WR}}$ signal

X: No longer a valid logic level

Z: Float

For example,

t_{AVLL} = Time from Address Valid to ALE Low

t_{LLPL} = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC Characteristics for 12MHz version

V_{CC} = 5V:	V _{CC} = 5V + 10%, -15%; V _{SS} = 0V; T _A = 0°C to 70°C (C _L for port 0. ALE and PSEN outputs = 100pF; C _L for all other outputs = 80pF)
V_{CC} = 3.3V:	V _{CC} = 3.3V + 0.3V, -0.6V; V _{SS} = 0V; T _A = 0°C to 70°C (C _L for port 0. ALE and PSEN outputs = 50pF; C _L for all other outputs = 50pF)
Variable clock:	V _{CC} = 5V: 1/t _{CLCL} = 3.5 MHz to 12 MHz V _{CC} = 3.3V: 1/t _{CLCL} = 1 MHz to 12 MHz

External Program Memory Characteristics

Parameter	Symbol	12 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 12MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t _{LHLL}	127	-	2t _{CLCL} -40	-	ns
Address setup to ALE	t _{AVLL}	43	-	t _{CLCL} -40	-	ns
Address hold after ALE	t _{LLAX}	43	-	t _{CLCL} -40	-	ns
ALE low to valid instruction in	t _{LLIV}	-	233	-	4t _{CLCL} -100	ns
ALE to PSEN	t _{LLPL}	58	-	t _{CLCL} -25	-	ns
PSEN pulse width	t _{PLPH}	215	-	3t _{CLCL} -35	-	ns
PSEN to valid instruction in	t _{PLIV}	-	150	-	3t _{CLCL} -100	ns
Input instruction hold after PSEN	t _{PXIX}	0	-	0	-	ns
Input instruction float after PSEN	t _{PXIZ} ¹⁾	-	63	-	t _{CLCL} -20	ns
Address valid after PSEN	t _{PXAV} ¹⁾	75	-	t _{CLCL} -8	-	ns
Address to valid instruction in	t _{AVIV}	-	302	-	5t _{CLCL} -115	ns
Address float to PSEN	t _{AZPL}	-10	-	-10	-	ns

¹⁾ Interfacing the GMS90C320 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for 12MHz version

External Data Memory Characteristics

Parameter	Symbol	12 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 12MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	400	-	6t _{CLCL} -100	-	ns
$\overline{\text{WR}}$ pulse width	t _{WLWH}	400	-	6t _{CLCL} -100	-	ns
Address hold after ALE	t _{LLAX2}	127	-	2t _{CLCL} -40	-	ns
$\overline{\text{RD}}$ to valid data in	t _{RLDV}	-	252	-	5t _{CLCL} -165	ns
Data hold after $\overline{\text{RD}}$	t _{RHDX}	0	-	0	-	ns
Data float after $\overline{\text{RD}}$	t _{RHDZ}	-	97	-	2t _{CLCL} -70	ns
ALE to valid data in	t _{LLDV}	-	517	-	8t _{CLCL} -150	ns
Address to valid data in	t _{AVDV}	-	585	-	9t _{CLCL} -165	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{LLWL}	200	300	3t _{CLCL} -50	3t _{CLCL} +50	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{AVWL}	203	-	4t _{CLCL} -130	-	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t _{WHLH}	43	123	t _{CLCL} -40	t _{CLCL} +40	ns
Data valid to $\overline{\text{WR}}$ transition	t _{QVWX}	33	-	t _{CLCL} -50	-	ns
Data setup before $\overline{\text{WR}}$	t _{QVWH}	433	-	7t _{CLCL} -150	-	ns
Data hold after $\overline{\text{WR}}$	t _{WHQX}	33	-	t _{CLCL} -50	-	ns
Address float after $\overline{\text{RD}}$	t _{RLAZ}	-	0	-	0	ns

Advance Information (12MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 12MHz)		Unit
		Min.	Max.	
Oscillator period (V _{CC} =5V)	t _{CLCL}	83.3	285.7	ns
Oscillator period (V _{CC} =3.3V)	t _{CLCL}	83.3	1	
High time	t _{CHCX}	20	t _{CLCL} - t _{CLCX}	ns
Low time	t _{CLCX}	20	t _{CLCL} - t _{CHCX}	ns
Rise time	t _{CLCH}	-	20	ns
Fall time	t _{CHCL}	-	20	ns

AC Characteristics for 16MHz version

- V_{CC} = 5V:** V_{CC} = 5V + 10%, -15%; V_{SS} = 0V; T_A = 0°C to 70°C
(C_L for port 0. ALE and PSEN outputs = 100pF; C_L for all other outputs = 80pF)
- V_{CC} = 3.3V:** V_{CC} = 3.3V + 0.3V, -0.6V; V_{SS} = 0V; T_A = 0°C to 70°C
(C_L for port 0. ALE and PSEN outputs = 50pF; C_L for all other outputs = 50pF)
- Variable clock:** V_{CC} = 5V: 1/t_{CLCL} = 3.5 MHz to 16 MHz
V_{CC} = 3.3V: 1/t_{CLCL} = 1 MHz to 16 MHz

External Program Memory Characteristics

Parameter	Symbol	16 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 16MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t _{LHLL}	85	-	2t _{CLCL} -40	-	ns
Address setup to ALE	t _{AVLL}	23	-	t _{CLCL} -40	-	ns
Address hold after ALE	t _{LLAX}	43	-	t _{CLCL} -40	-	ns
ALE low to valid instruction in	t _{LLIV}	-	150	-	4t _{CLCL} -100	ns
ALE to PSEN	t _{LLPL}	38	-	t _{CLCL} -25	-	ns
PSEN pulse width	t _{PLPH}	153	-	3t _{CLCL} -35	-	ns
PSEN to valid instruction in	t _{PLIV}	-	88	-	3t _{CLCL} -100	ns
Input instruction hold after PSEN	t _{PXIX}	0	-	0	-	ns
Input instruction float after PSEN	t _{PXIZ} ¹⁾	-	43	-	t _{CLCL} -20	ns
Address valid after PSEN	t _{PXAV} ¹⁾	55	-	t _{CLCL} -8	-	ns
Address to valid instruction in	t _{AVIV}	-	198	-	5t _{CLCL} -115	ns
Address float to PSEN	t _{AZPL}	-10	-	-10	-	ns

¹⁾ Interfacing the GMS90C320 to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for 16MHz

External Data Memory Characteristics

Parameter	Symbol	16 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 16MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	275	-	6t _{CLCL} -100	-	ns
$\overline{\text{WR}}$ pulse width	t _{WLWH}	275	-	6t _{CLCL} -100	-	ns
Address hold after ALE	t _{LLAX2}	127	-	2t _{CLCL} -40	-	ns
$\overline{\text{RD}}$ to valid data in	t _{RLDV}	-	183	-	5t _{CLCL} -130	ns
Data hold after $\overline{\text{RD}}$	t _{RHDX}	0	-	0	-	ns
Data float after $\overline{\text{RD}}$	t _{RHDZ}	-	75	-	2t _{CLCL} -50	ns
ALE to valid data in	t _{LLDV}	-	350	-	8t _{CLCL} -150	ns
Address to valid data in	t _{AVDV}	-	398	-	9t _{CLCL} -165	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{LLWL}	138	238	3t _{CLCL} -50	3t _{CLCL} +50	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{AVWL}	120	-	4t _{CLCL} -130	-	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t _{WHLH}	28	97	t _{CLCL} -35	t _{CLCL} +35	ns
Data valid to $\overline{\text{WR}}$ transition	t _{QVWX}	13	-	t _{CLCL} -50	-	ns
Data setup before $\overline{\text{WR}}$	t _{QVWH}	288	-	7t _{CLCL} -150	-	ns
Data hold after $\overline{\text{WR}}$	t _{WHQX}	23	-	t _{CLCL} -40	-	ns
Address float after $\overline{\text{RD}}$	t _{RLAZ}	-	0	-	0	ns

Advance Information (16MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 16MHz)		Unit
		Min.	Max.	
Oscillator period	t _{CLCL}	62.5	285.7	ns
High time	t _{CHCX}	17	t _{CLCL} - t _{CLCX}	ns
Low time	t _{CLCX}	17	t _{CLCL} - t _{CHCX}	ns
Rise time	t _{CLCH}	-	17	ns
Fall time	t _{CHCL}	-	17	ns

AC Characteristics for 24MHz version

- V_{CC} = 5V:** V_{CC} = 5V + 10%, -15%; V_{SS} = 0V; T_A = 0°C to 70°C
(C_L for port 0. ALE and PSEN outputs = 100pF; C_L for all other outputs = 80pF)
- V_{CC} = 3.3V:** V_{CC} = 3.3V + 0.3V, -0.6V; V_{SS} = 0V; T_A = 0°C to 70°C
(C_L for port 0. ALE and PSEN outputs = 50pF; C_L for all other outputs = 50pF)
- Variable clock:** V_{CC} = 5V: 1/t_{CLCL} = 3.5 MHz to 24 MHz
V_{CC} = 3.3V: 1/t_{CLCL} = 1 MHz to 24 MHz

External Program Memory Characteristics

Parameter	Symbol	24 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 24MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t _{LHLL}	43	-	2t _{CLCL} -40	-	ns
Address setup to ALE	t _{AVLL}	17	-	t _{CLCL} -25	-	ns
Address hold after ALE	t _{LLAX}	17	-	t _{CLCL} -25	-	ns
ALE low to valid instruction in	t _{LLIV}	-	80	-	4t _{CLCL} -87	ns
ALE to PSEN	t _{LLPL}	22	-	t _{CLCL} -20	-	ns
PSEN pulse width	t _{PLPH}	95	-	3t _{CLCL} -30	-	ns
PSEN to valid instruction in	t _{PLIV}	-	60	-	3t _{CLCL} -65	ns
Input instruction hold after PSEN	t _{PXIX}	0	-	0	-	ns
Input instruction float after PSEN	t _{PXIZ} ¹⁾	-	32	-	t _{CLCL} -10	ns
Address valid after PSEN	t _{PXAV} ¹⁾	37	-	t _{CLCL} -5	-	ns
Address to valid instruction in	t _{AVIV}	-	148	-	5t _{CLCL} -60	ns
Address float to PSEN	t _{AZPL}	-10	-	-10	-	ns

¹⁾ Interfacing the GMS90C320 to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for 24MHz

External Data Memory Characteristics

Parameter	Symbol	24 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 24MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	180	-	6t _{CLCL} -70	-	ns
$\overline{\text{WR}}$ pulse width	t _{WLWH}	180	-	6t _{CLCL} -70	-	ns
Address hold after ALE	t _{LLAX2}	56	-	2t _{CLCL} -27	-	ns
$\overline{\text{RD}}$ to valid data in	t _{RLDV}	-	118	-	5t _{CLCL} -90	ns
Data hold after $\overline{\text{RD}}$	t _{RHDX}	0	-	0	-	ns
Data float after $\overline{\text{RD}}$	t _{RHDZ}	-	63	-	2t _{CLCL} -20	ns
ALE to valid data in	t _{LLDV}	-	200	-	8t _{CLCL} -133	ns
Address to valid data in	t _{AVDV}	-	220	-	9t _{CLCL} -155	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{LLWL}	75	175	3t _{CLCL} -50	3t _{CLCL} +50	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{AVWL}	67	-	4t _{CLCL} -97	-	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t _{WHLH}	17	67	t _{CLCL} -25	t _{CLCL} +25	ns
Data valid to $\overline{\text{WR}}$ transition	t _{QVWX}	5	-	t _{CLCL} -37	-	ns
Data setup before $\overline{\text{WR}}$	t _{QVWH}	170	-	7t _{CLCL} -122	-	ns
Data hold after $\overline{\text{WR}}$	t _{WHQX}	15	-	t _{CLCL} -27	-	ns
Address float after $\overline{\text{RD}}$	t _{RLAZ}	-	0	-	0	ns

Advance Information (24MHz)

External Clock Drive

Table 11.

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 24MHz)		Unit
		Min.	Max.	
Oscillator period	t _{CLCL}	41.7	285.7	ns
High time	t _{CHCX}	12	t _{CLCL} - t _{CLCX}	ns
Low time	t _{CLCX}	12	t _{CLCL} - t _{CHCX}	ns
Rise time	t _{CLCH}	-	12	ns
Fall time	t _{CHCL}	-	12	ns

AC Characteristics for 40MHz version

$V_{CC} = 5V + 10\%, -15\%$; $V_{SS} = 0V$; $T_A = 0^\circ C$ to $70^\circ C$

(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80pF)

External Program Memory Characteristics

Parameter	Symbol	40 MHz Oscillator		Variable Oscillator 1/t _{CLCL} = 3.5 to 40MHz		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t _{LHLL}	35	-	2t _{CLCL} -15	-	ns
Address setup to ALE	t _{AVLL}	10	-	t _{CLCL} -15	-	ns
Address hold after ALE	t _{LLAX}	10	-	t _{CLCL} -15	-	ns
ALE low to valid instruction in	t _{LLIV}	-	55	-	4t _{CLCL} -45	ns
ALE to $\overline{PSEN}$	t _{LLPL}	10	-	t _{CLCL} -15	-	ns
$\overline{PSEN}$ pulse width	t _{PLPH}	60	-	3t _{CLCL} -15	-	ns
$\overline{PSEN}$ to valid instruction in	t _{PLIV}	-	25	-	3t _{CLCL} -50	ns
Input instruction hold after $\overline{PSEN}$	t _{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t _{PXIZ} ¹⁾	-	15	-	t _{CLCL} -10	ns
Address valid after $\overline{PSEN}$	t _{PXAV} ¹⁾	20	-	t _{CLCL} -5	-	ns
Address to valid instruction in	t _{AVIV}	-	65	-	5t _{CLCL} -60	ns
Address float to $\overline{PSEN}$	t _{AZPL}	-5	-	-5	-	ns

¹⁾ Interfacing the GMS90C320 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for 40MHz

External Data Memory Characteristics

Parameter	Symbol	at 40 MHz Clock		Variable Clock 1/t _{CLCL} = 3.5 to 40MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	120	-	6t _{CLCL} -30	-	ns
$\overline{\text{WR}}$ pulse width	t _{WLWH}	120	-	6t _{CLCL} -30	-	ns
Address hold after ALE	t _{LLAX2}	10	-	t _{CLCL} -15	-	ns
$\overline{\text{RD}}$ to valid data in	t _{RLDV}	-	75	-	5t _{CLCL} -50	ns
Data hold after $\overline{\text{RD}}$	t _{RHDX}	0	-	0	-	ns
Data float after $\overline{\text{RD}}$	t _{RHDZ}	-	38	-	2t _{CLCL} -12	ns
ALE to valid data in	t _{LLDV}	-	150	-	8t _{CLCL} -50	ns
Address to valid data in	t _{AVDV}	-	150	-	9t _{CLCL} -75	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{LLWL}	60	90	3t _{CLCL} -15	3t _{CLCL} +15	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{AVWL}	70	-	4t _{CLCL} -30	-	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t _{WHLH}	10	40	t _{CLCL} -15	t _{CLCL} +15	ns
Data valid to $\overline{\text{WR}}$ transition	t _{QVWX}	5	-	t _{CLCL} -20	-	ns
Data setup before $\overline{\text{WR}}$	t _{QVWH}	125	-	7t _{CLCL} -50	-	ns
Data hold after $\overline{\text{WR}}$	t _{WHQX}	5	-	t _{CLCL} -20	-	ns
Address float after $\overline{\text{RD}}$	t _{RLAZ}	-	0	-	0	ns

Advance Information (40MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 40MHz)		Unit
		Min.	Max.	
Oscillator period	t _{CLCL}	25	285.7	ns
High time	t _{CHCX}	10	t _{CLCL} - t _{CLCX}	ns
Low time	t _{CLCX}	10	t _{CLCL} - t _{CHCX}	ns
Rise time	t _{CLCH}	-	10	ns
Fall time	t _{CHCL}	-	10	ns

AC Characteristics for 50MHz version

$V_{CC} = 5V + 10\%, -15\%$; $V_{SS} = 0V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$

(C_L for port 0. ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80pF)

Variable Clock : $V_{CC} = 5V$, $1/t_{CLCL} = 3.5MHz$ to $50MHz$

External Program Memory Characteristics

Parameter	Symbol	50 MHz Oscillator		Variable Oscillator 1/ $t_{CLCL} = 3.5$ to $50MHz$		Unit
		Min.	Max.	Min.	Max.	
ALE pulse width	t_{LHLL}	25	-	$2t_{CLCL}-15$	-	ns
Address setup to ALE	t_{AVLL}	5	-	$t_{CLCL}-15$	-	ns
Address hold after ALE	t_{LLAX}	5	-	$t_{CLCL}-15$	-	ns
ALE low to valid instruction in	t_{LLIV}	-	40	-	$4t_{CLCL}-40$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	5	-	$t_{CLCL}-15$	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	45	-	$3t_{CLCL}-15$	-	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	-	20	-	$3t_{CLCL}-40$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	$t_{PXIZ}^{1)}$	-	10	-	$t_{CLCL}-10$	ns
Address valid after $\overline{PSEN}$	$t_{PXAV}^{1)}$	15	-	$t_{CLCL}-5$	-	ns
Address to valid instruction in	t_{AVIV}	-	45	-	$5t_{CLCL}-55$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	-5	-	-5	-	ns

¹⁾ Interfacing the GMS90C320 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for 50MHz

External Data Memory Characteristics

Parameter	Symbol	at 50 MHz Clock		Variable Clock 1/t _{CLCL} = 3.5 to 50MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	90	-	6t _{CLCL} -30	-	ns
$\overline{\text{WR}}$ pulse width	t _{WLWH}	90	-	6t _{CLCL} -30	-	ns
Address hold after ALE	t _{LLAX2}	25	-	2t _{CLCL} -15	-	ns
$\overline{\text{RD}}$ to valid data in	t _{RLDV}	-	60	-	5t _{CLCL} -40	ns
Data hold after $\overline{\text{RD}}$	t _{RHDX}	0	-	0	-	ns
Data float after $\overline{\text{RD}}$	t _{RHDZ}	-	28	-	2t _{CLCL} -12	ns
ALE to valid data in	t _{LLDV}	-	120	-	8t _{CLCL} -40	ns
Address to valid data in	t _{AVDV}	-	125	-	9t _{CLCL} -55	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{LLWL}	45	75	3t _{CLCL} -15	3t _{CLCL} +15	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	t _{AVWL}	50	-	4t _{CLCL} -30	-	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	t _{WHLH}	5	35	t _{CLCL} -15	t _{CLCL} +15	ns
Data valid to $\overline{\text{WR}}$ transition	t _{QVWX}	5	-	t _{CLCL} -15	-	ns
Data setup before $\overline{\text{WR}}$	t _{QVWH}	100	-	7t _{CLCL} -40	-	ns
Data hold after $\overline{\text{WR}}$	t _{WHQX}	5	-	t _{CLCL} -15	-	ns
Address float after $\overline{\text{RD}}$	t _{RLAZ}	-	0	-	0	ns

Advance Information (50MHz)

External Clock Drive

Parameter	Symbol	Variable Oscillator (Freq. = 3.5 to 50MHz)		Unit
		Min.	Max.	
Oscillator period	t _{CLCL}	20	285.7	ns
High time	t _{CHCX}	10	t _{CLCL} - t _{CLCX}	ns
Low time	t _{CLCX}	10	t _{CLCL} - t _{CHCX}	ns
Rise time	t _{CLCH}	-	10	ns
Fall time	t _{CHCL}	-	10	ns

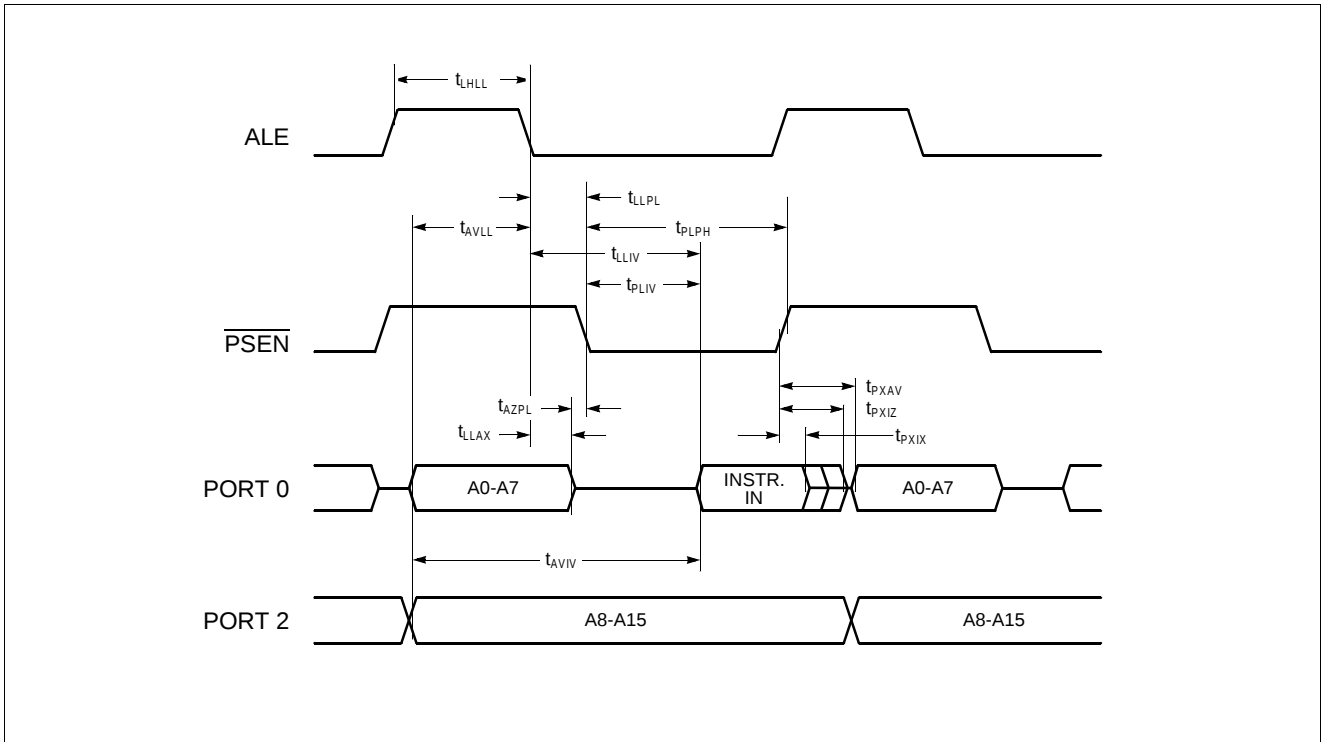


Figure 4 External Program Memory Read Cycle

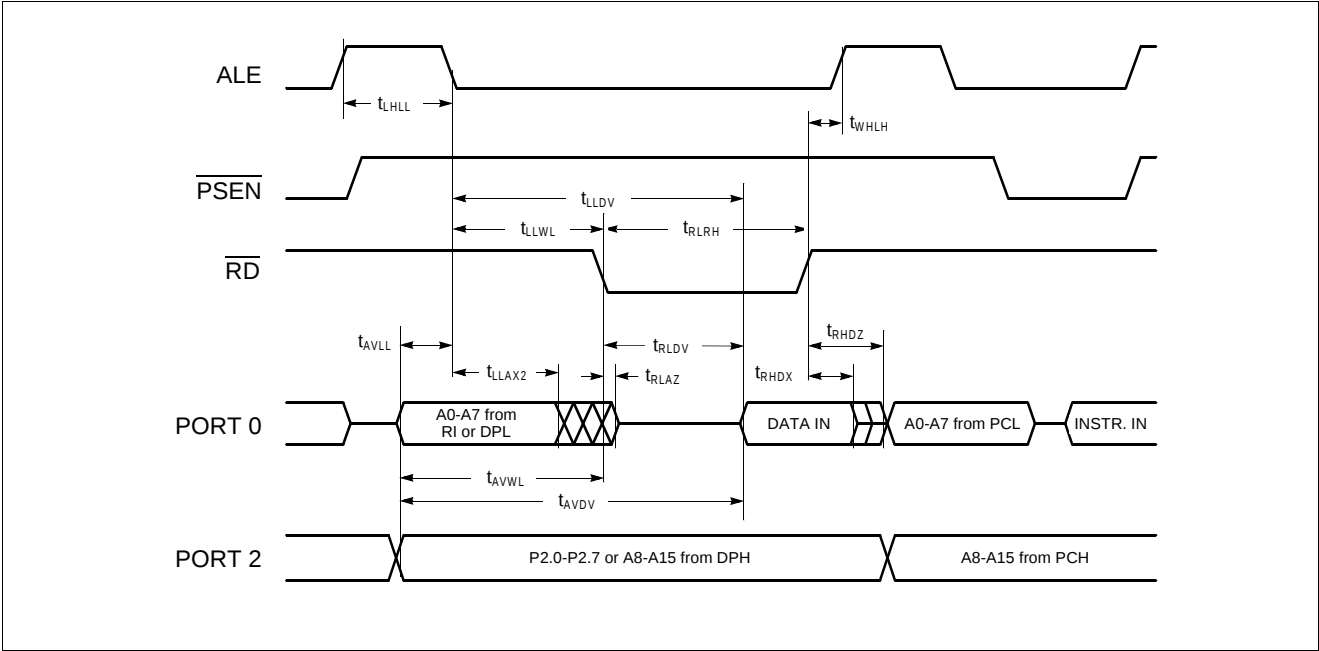


Figure 5 External Data Memory Read Cycle

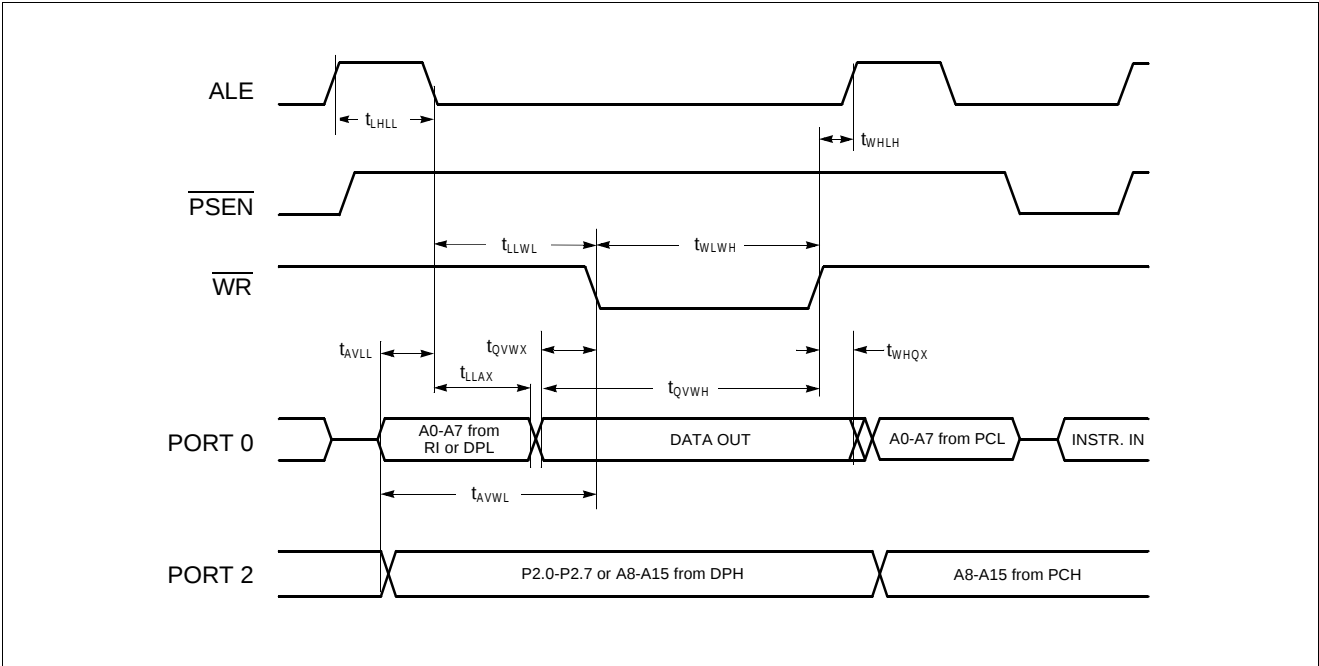
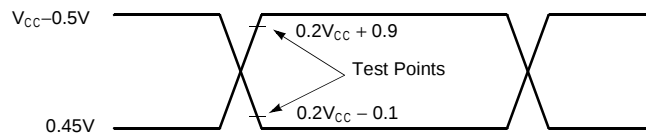
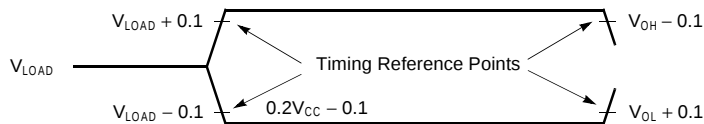


Figure 6 External Data Memory Write Cycle



AC Inputs during testing are driven at $V_{CC}-0.5V$ for a logic '1' and $0.45V$ for a logic '0'.
Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 7 AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs and begins to float when a 100mV change from the loaded V_{OH} / V_{OL} level occurs.

$I_{OL} / I_{OH} \geq 20mA$.

Figure 8 Float Waveforms

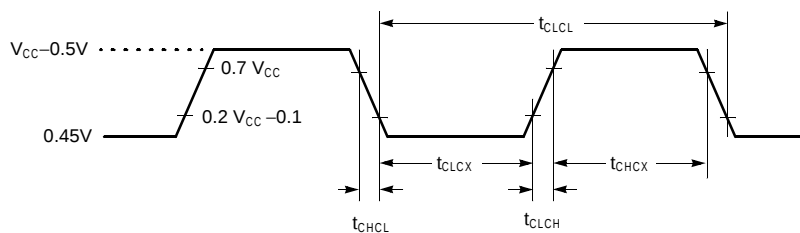


Figure 9 External Clock Cycle

OSCILLATOR CIRCUIT

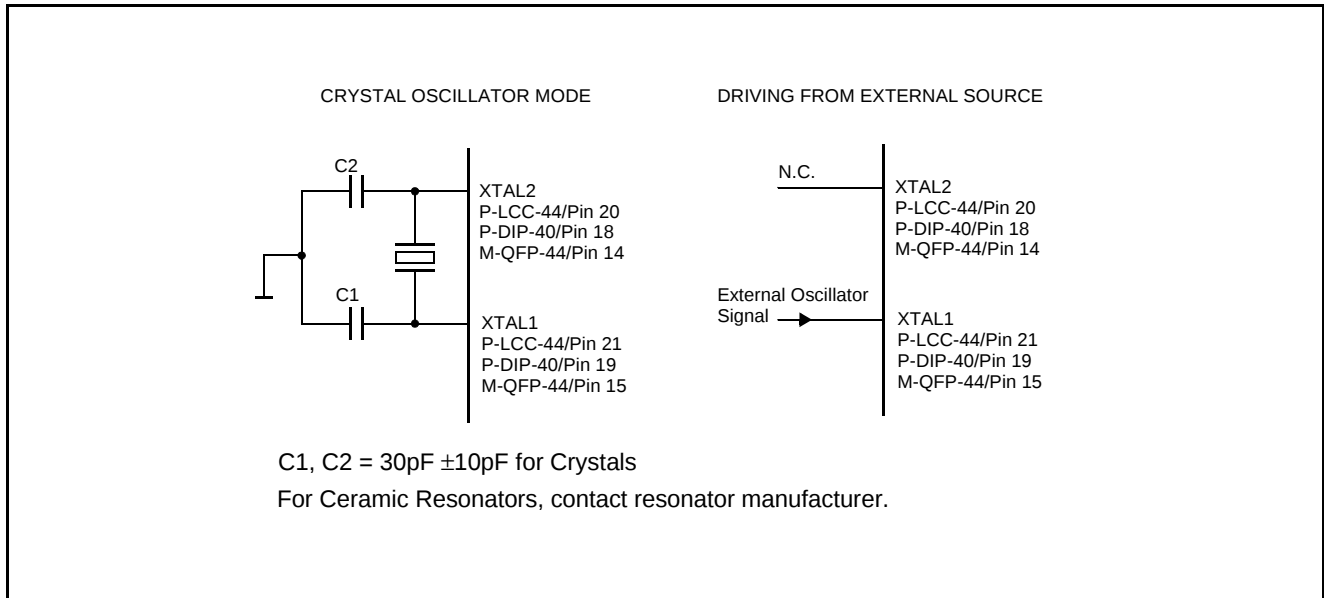


Figure 10 Recommended Oscillator Circuits

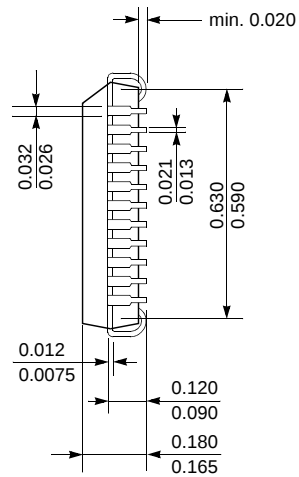
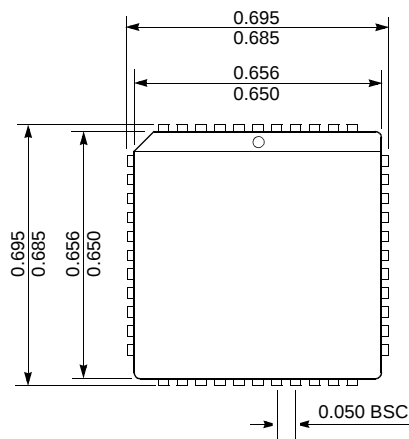
Oscillation circuit is designed to be used either with a ceramic resonator or crystal oscillator. Since each crystal and ceramic resonator have their own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Plastic Package P-LCC-44

(Plastic Leaded Chip-Carrier)

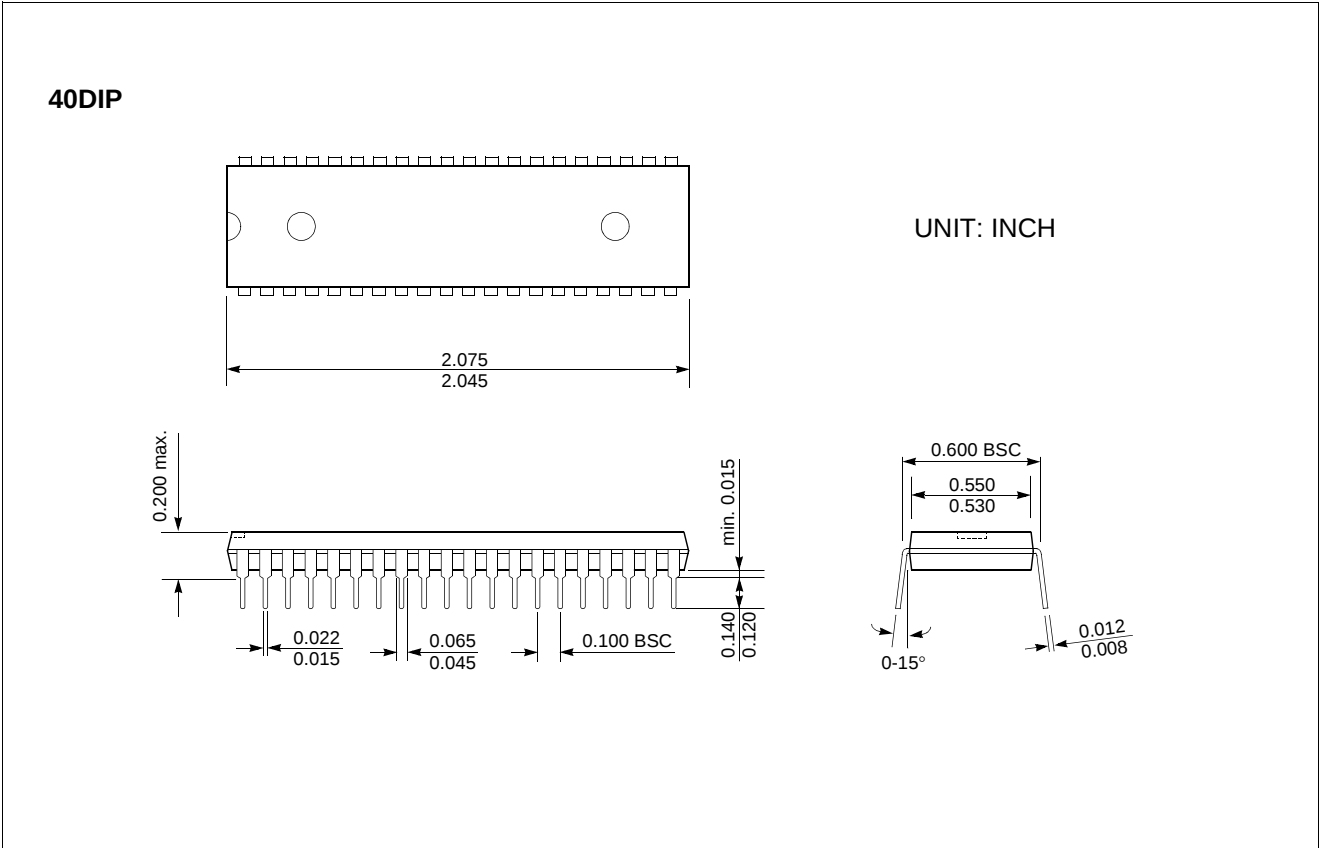
44PLCC

UNIT: INCH



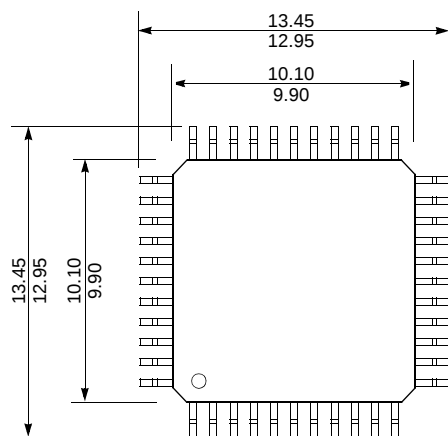
Plastic Package P-DIP-40

(Plastic Dual in-Line Package)

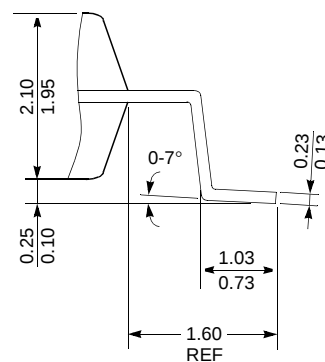
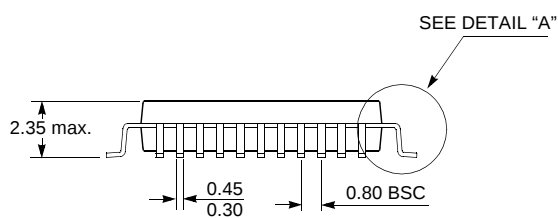


Plastic Package P-MQFP-44

(Plastic Metric Quad Flat Package)

P-MQFP-44

UNIT: MM

DETAIL "A"