Integrated Device Technology, Inc.

HIGH-SPEED 4K x 9 SYNCHRONOUS DUAL-PORT RAM

IDT7099S

FEATURES:

- High-speed clock-to-data output times
  - — Military: 20/25/30ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7099S
    Active: 900 mW (typ.)
    Standby: 50 mW (typ.)
- Architecture based on Dual-Port RAM cells
  - — Allows full simultaneous access from both ports
  - — Independent bit/byte Read and Write inputs for control functions
- Synchronous operation
  - — 4ns setup to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 15ns clock to data out
  - — 20ns cycle times, 50MHz operation
- Clock enable feature
- Guaranteed data output hold times
- Available in 68-pin PGA, 68-pin PLCC, and 80-pin TQFP
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

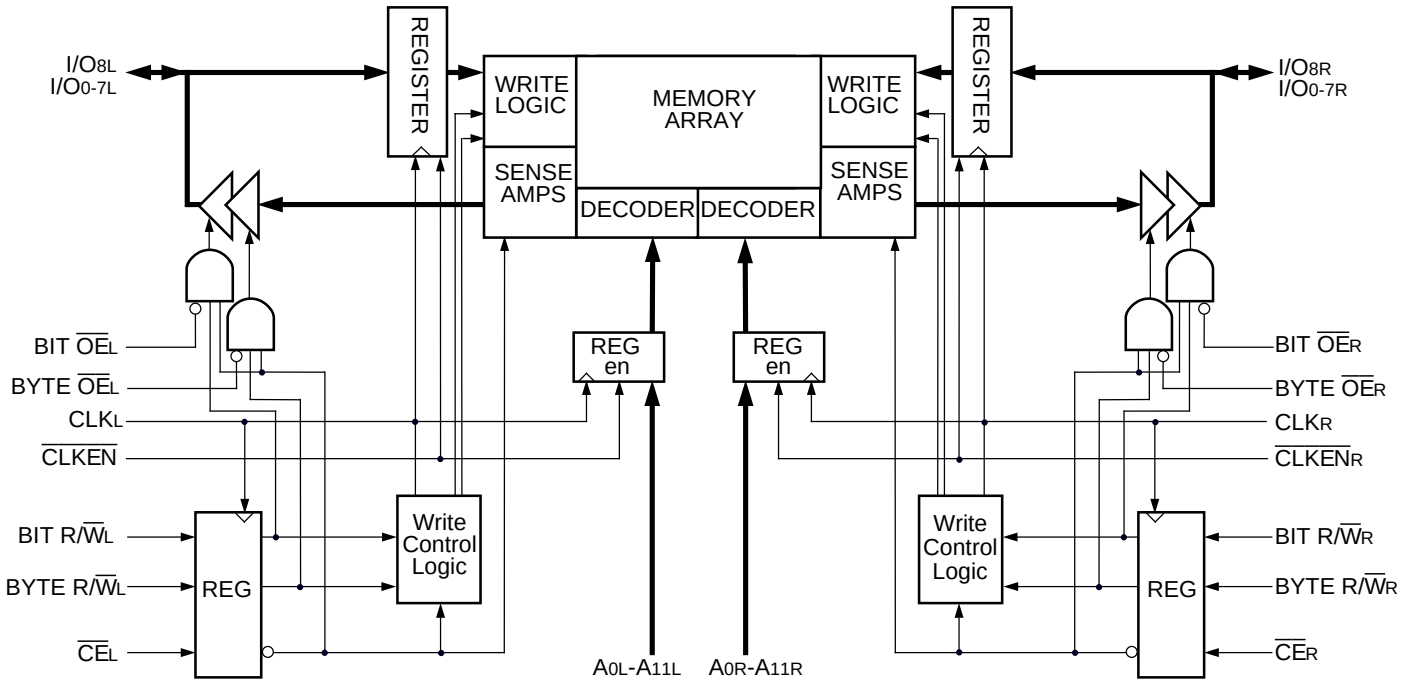
DESCRIPTION:

The IDT7099 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts. Changing data direction from reading to writing normally requires one dead cycle.

These Dual-Ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 15ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT7099 is packaged in a 68-pin PGA, 68-pin PLCC, and a 80-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

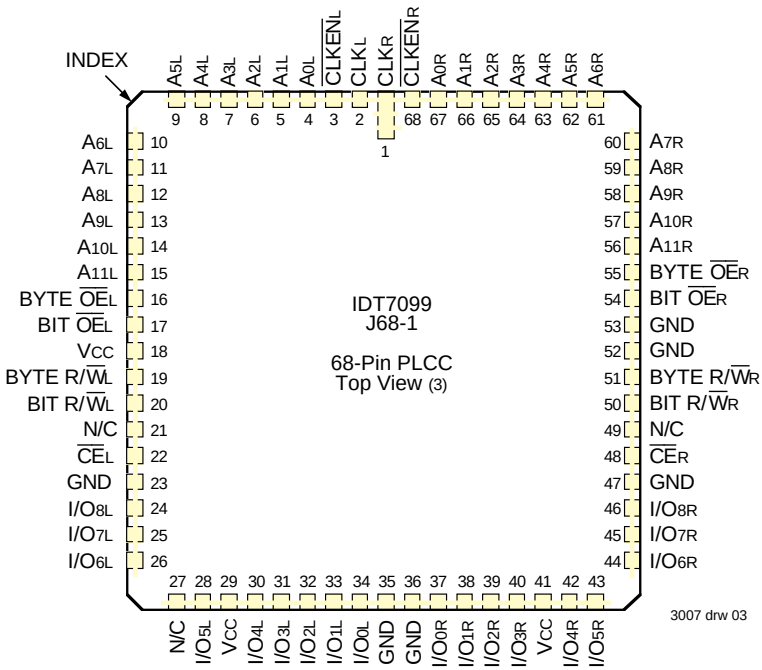


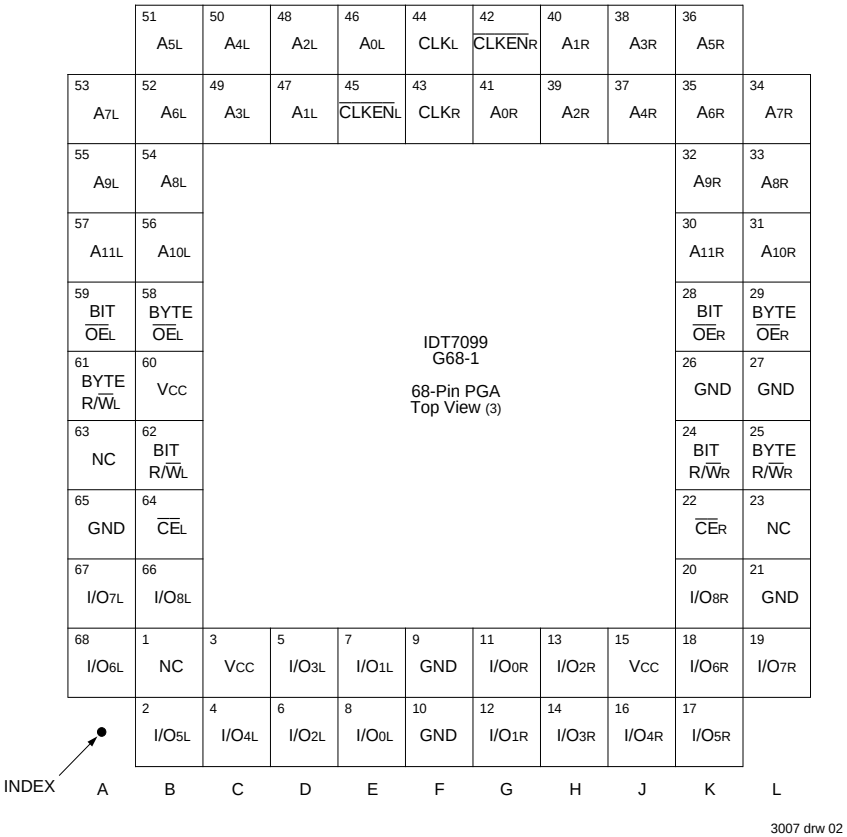
3007 drw 01

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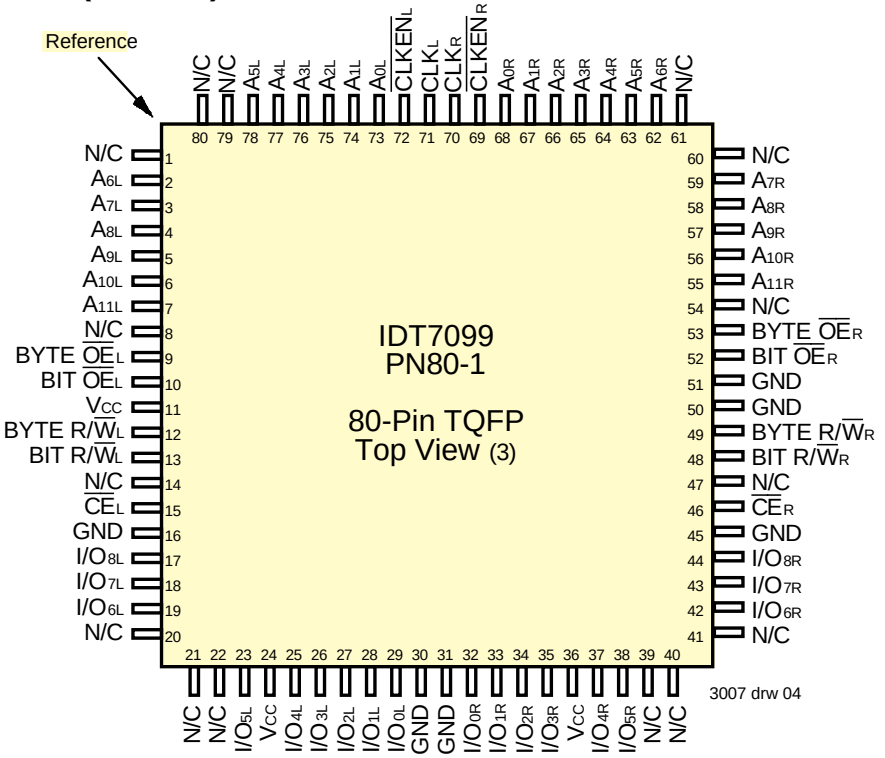
PIN CONFIGURATIONS (1,2)





NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONT'D) (1,2)



NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate the orientaion of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	–0.5 to VCC	–0.5 to VCC	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

3007 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3007 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0 (2)	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

3007 tbl 03

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE(1)

(T_A = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Condition(2)	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

3007 tbl 04

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7099S Min.	IDT7099S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, VOUT = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4mA	2.4	—	V

NOTE:
1. Input leakages are undefined at V_{CC} ≤ 2.0V.

3007 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4) (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Version	IDT7099S15 Com'l. Only Typ.	IDT7099S15 Com'l. Only Max.	IDT7099S20 Typ.	IDT7099S20 Max.	IDT7099S25 Typ.	IDT7099S25 Max.	IDT7099S30 Mil Only Typ.	IDT7099S30 Mil Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}(1)	Mil.	—	—	170	310	160	290	160	270	mA
			Com'l.	180	300	170	290	160	270	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}$L and $\overline{CE}$R = V_{IH} f = f_{MAX}(1)	Mil.	—	—	85	140	80	130	80	110	mA
			Com'l.	90	140	85	130	80	110	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_{'A'}$ = V_{IL} and $\overline{CE}_{'B'}$ = V_{IH} (3) Active Port Outputs Open, f = f_{MAX}(1)	Mil.	—	—	150	210	140	200	140	180	mA
			Com'l.	160	210	150	200	140	180	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}$R and $\overline{CE}$L ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0(2)	Mil.	—	—	10	20	10	20	10	20	mA
			Com'l.	10	15	10	—	10	—	—		
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	$\overline{CE}_{'A'}$≤0.2V and $\overline{CE}_{'B'}$ ≥ V_{CC} -0.2V(3), V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}(1)	Mil.	—	—	145	200	135	190	135	170	mA
			Com'l.	155	200	145	190	135	170	—	—	

NOTES:
1. At f = fmax, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of the 1/t_{CLK}, using "AC TEST CONDITIONS" of input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. Vcc = 5V, TA = 25°C for Typ, and are not production tested. $I_{CC\,DC}$ = 150mA (Typ).

3007 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

3007 tbl 07

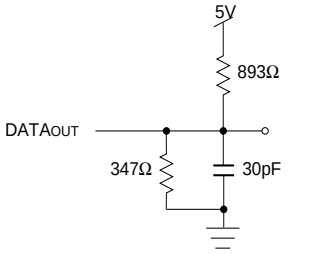


Figure 1. AC Output Test load.

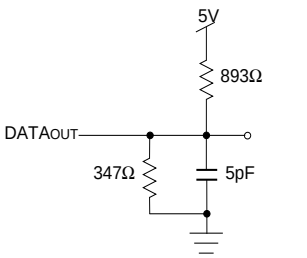


Figure 2. Output Test Load (For t_{CLZ}, t_{CHZ}, t_{OLZ}, and t_{OHZ}).
Including scope and jig.

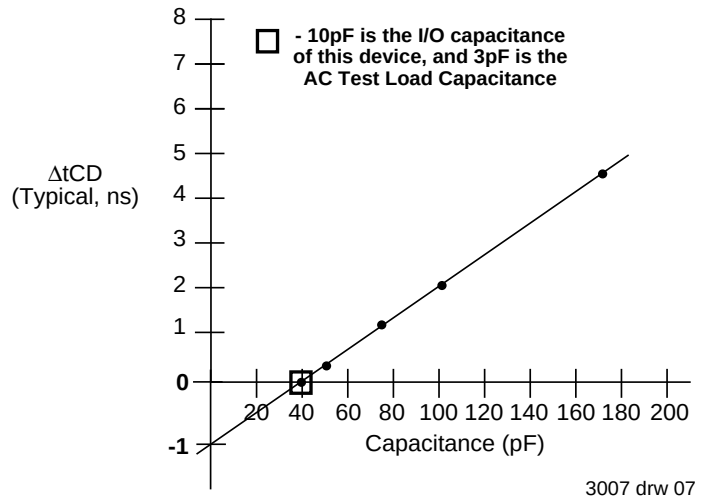


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

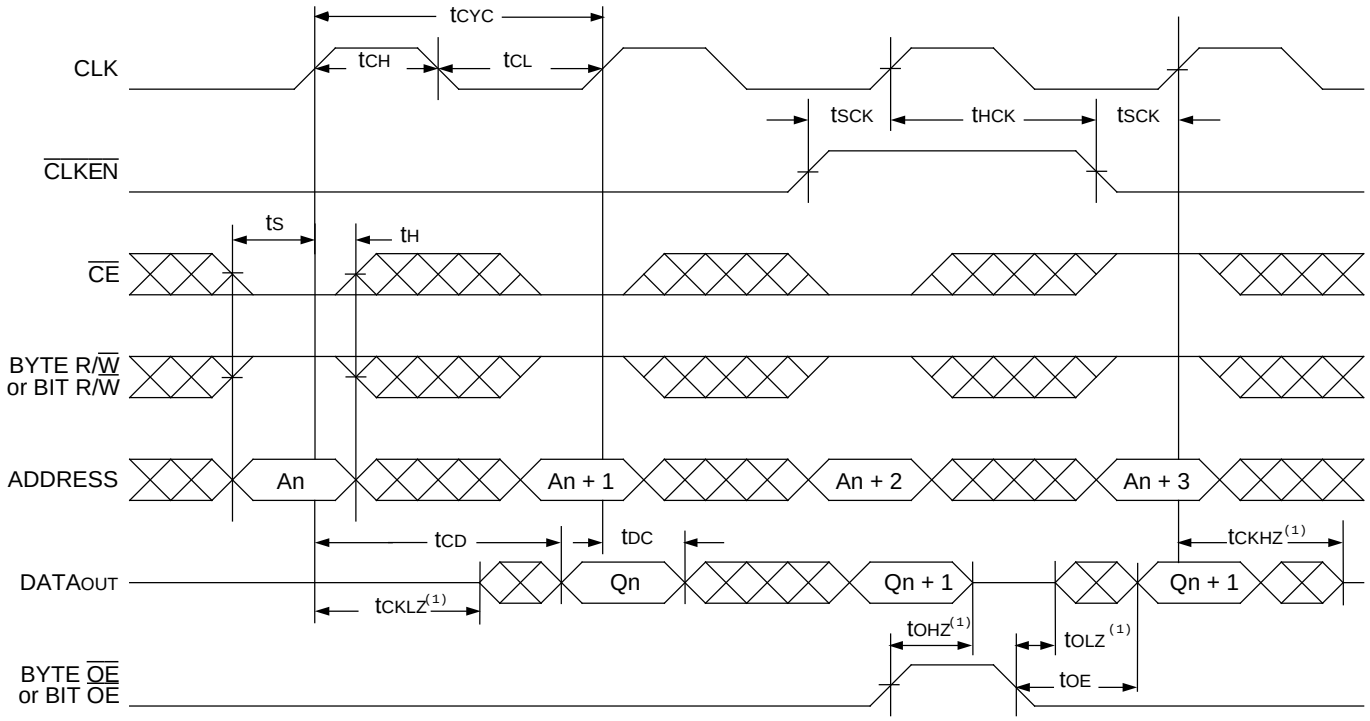
(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

		Commercial						Military						
		7099S15		7099S20		7099S25		7099S20		7099S25		7099S30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Clock Cycle Time	20	—	20	—	25	—	20	—	25	—	30	—	ns
t_{CH}	Clock High Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
t_{CL}	Clock Low Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
t_{CD}	Clock High to Output Valid	—	15	—	20	—	25	—	20	—	25	—	30	ns
t_S	Registered Signal Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
t_H	Registered Signal Hold Time	1	—	1	—	1	—	2	—	2	—	2	—	ns
t_{DC}	Data Output Hold After Clock High	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{CKLZ}	Clock High to Output Low-Z[1,2]	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1,2]	—	7	—	9	—	12	—	9	—	12	—	15	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	10	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1,2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z[1,2]	—	7	—	9	—	11	—	9	—	11	—	14	ns
t_{SCK}	Clock Enable, Disable Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
t_{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	2	—	3	—	3	—	3	—	ns
t_{CWDD}	Write Port Clock High to Read Data Delay	—	30	—	35	—	45	—	35	—	45	—	55	ns

NOTES:
3007 tbl 08

1. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.

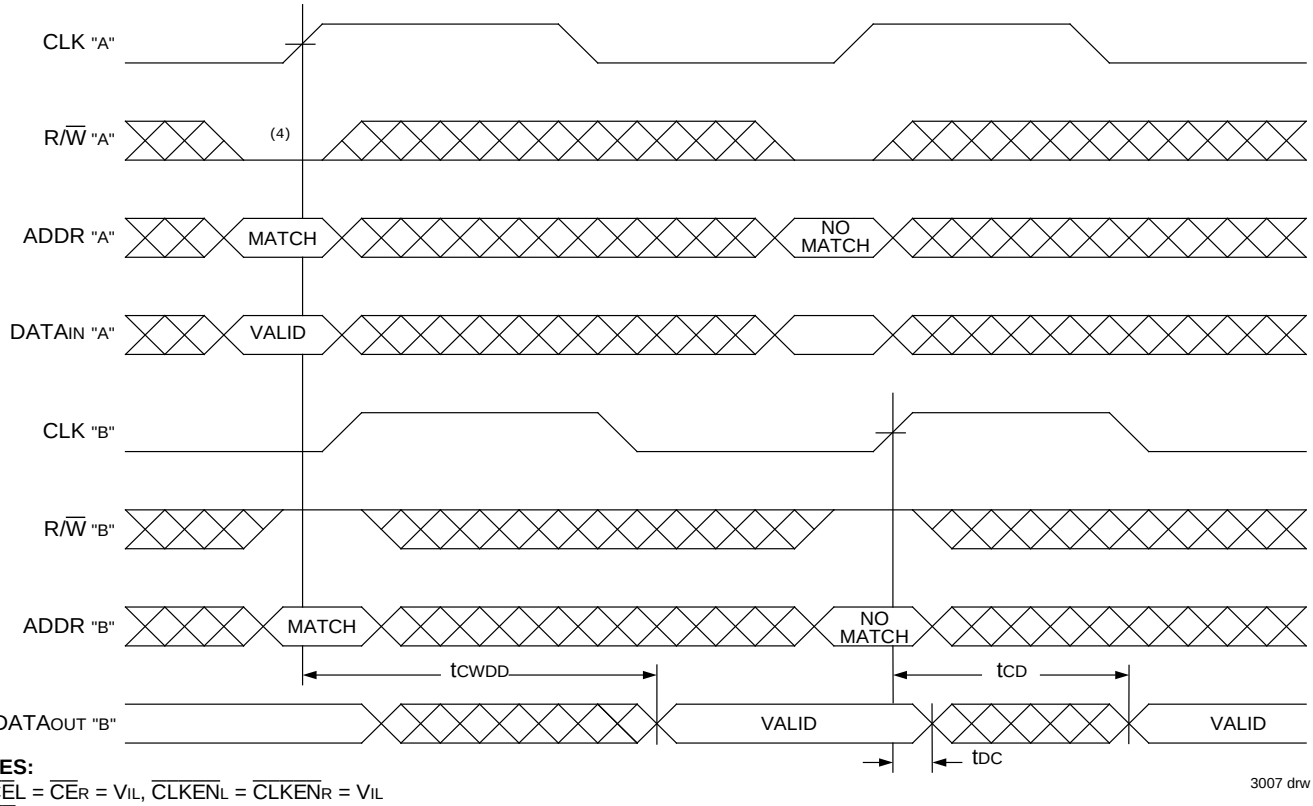
TIMING WAVEFORM OF READ CYCLE, EITHER SIDE



NOTE:
1. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

3007 drw 08

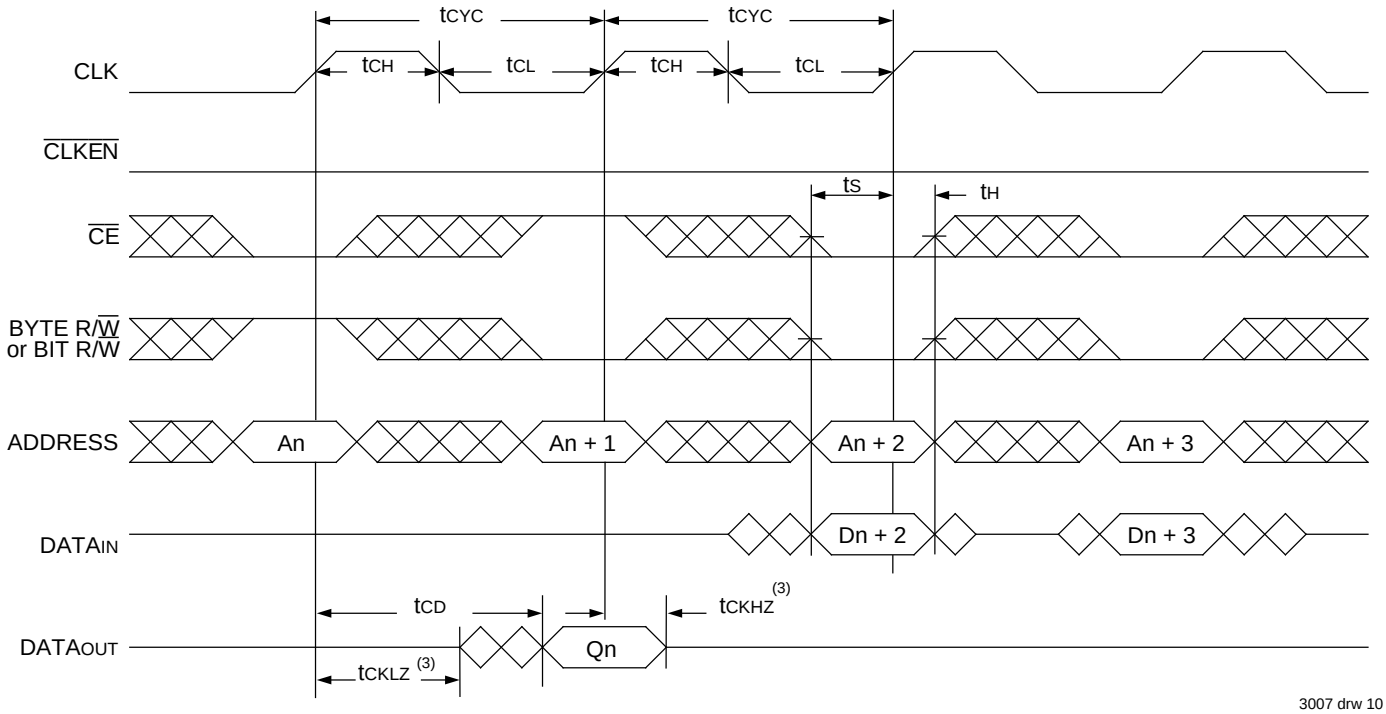
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ (1,2,3)



NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$
2. $\overline{OE}$ = V_{IL} for the reading port, port 'B'.
3. All timing is the same for left and right ports. Ports "A" may be either the left or right port. Port "B" is opposite from port "A".
4. $R/\overline{W}_{'A'}$ was active (V_{IL}) during the previous $CLK_{'A'}$, when enabled the write path.

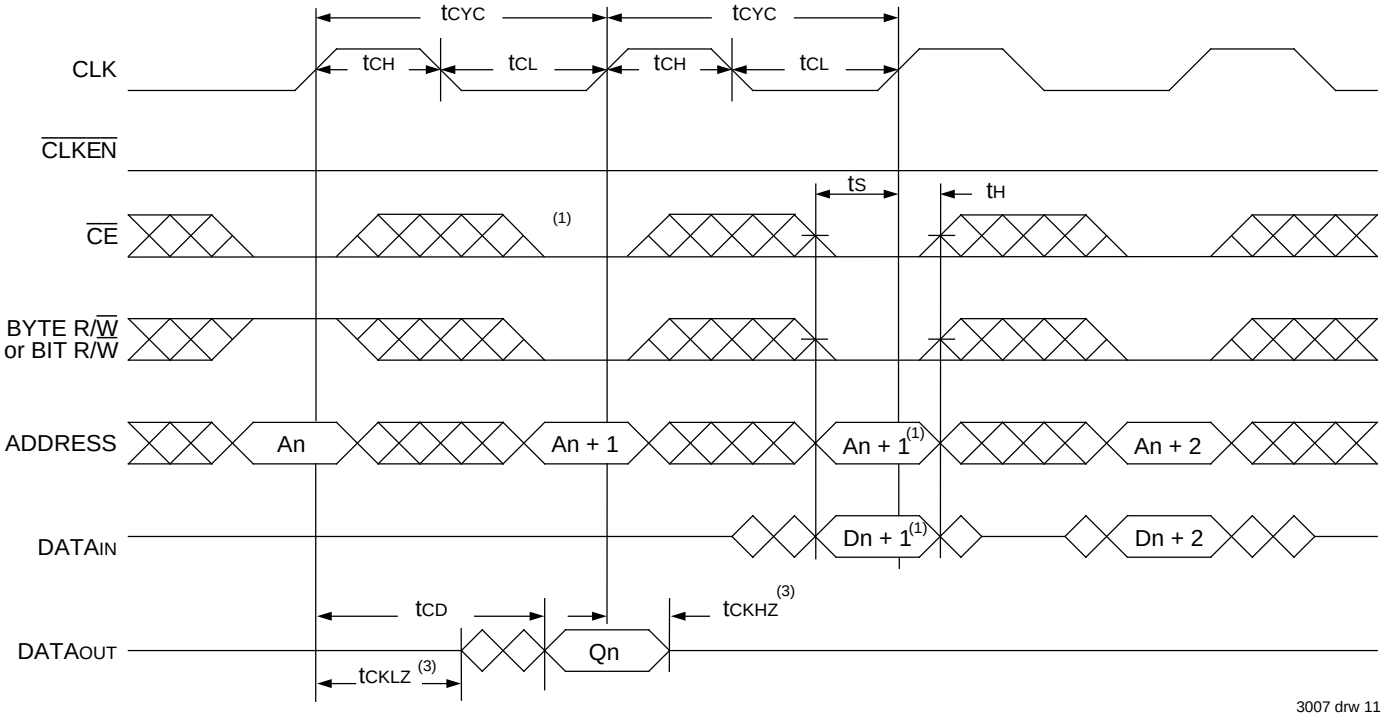
3007 drw 09

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ = V_{IH} (2)



3007 drw 10

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 2, $\overline{CE}$ = V_{IL} (2)



3007 drw 11

NOTES:
1. During dead cycle, if $\overline{CE}$ = V_{IL}, then invalid data will be written into array. The An+1 must be rewritten on the following cycle.
2. $\overline{OE}$ low throughout.
3. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

FUNCTIONAL DESCRIPTION

The IDT7099 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent on the low to high transitions of the clock signal allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the BYTE R/$\overline{W}$ and BIT R/$\overline{W}$ pins are low for at least one clock cycle before any write is attempted. A High on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The device has separate Bit Write, Byte Write, Bit Enable, and Byte Enable pins to allow for independent control.

TRUTH TABLE I – READ/WRITE CONTROL(1)

Inputs						Outputs		
Synchronous(3)				Asynchronous				
CLK	$\overline{CE}$	Byte R/$\overline{W}$	Bit R/$\overline{W}$	Byte $\overline{OE}$	Bit $\overline{OE}$	I/O0-7	I/O8	Mode
↑	h	h	h	X	X	High-Z	High-Z	Deselected, Power Down, Data I/O Disabled
↑	h	l	h	X	X	DATAIN	High-Z	Deselected, Power Down, Byte Data Input Enabled
↑	h	h	l	X	X	High-Z	DATAIN	Deselected, Power Down, Bit Data Input Enabled
↑	h	l	l	X	X	DATAIN	DATAIN	Deselected, Power Down, Data Input Enabled
↑	l	l	h	X	L	DATAIN	DATAOUT	Write Byte, Read Bit
↑	l	l	h	X	H	DATAIN	High-Z	Write Byte Only
↑	l	h	l	L	X	DATAOUT	DATAIN	Read Byte, Write Bit
↑	l	h	l	H	X	High-Z	DATAIN	Write Bit Only
↑	l	l	l	X	X	DATAIN	DATAIN	Write Byte, Write Bit
↑	l	h	h	L	L	DATAOUT	DATAOUT	Read Byte, Read Bit
↑	l	h	h	H	L	High-Z	DATAOUT	Read Bit Only
↑	l	h	h	L	H	DATAOUT	High-Z	Read Byte Only
↑	l	h	h	H	H	High-Z	High-Z	Data I/O Disabled

3007 tbl 09

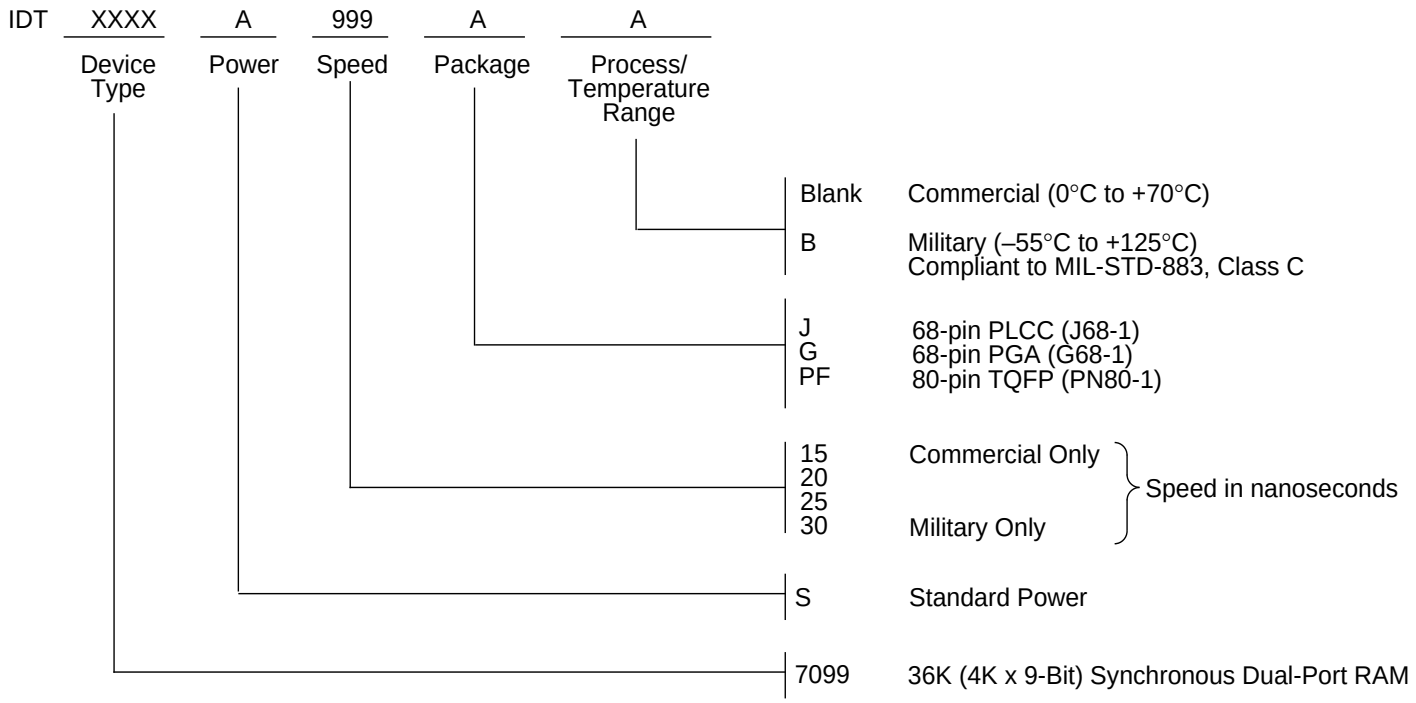
TRUTH TABLE II – CLOCK ENABLE FUNCTION TABLE(1)

	Inputs		Register Inputs		Register Outputs	
Operating Mode	CLK(3)	$\overline{CLKEN}$(2)	ADDR	DATAIN	ADDR	DATAOUT
Load "1"	↑	l	h	h	H	H
Load "0"	↑	l	l	l	L	L
Hold (do nothing)	↑	h	X	X	NC	NC
	X	H	X	X	NC	NC

NOTES: 3007 tbl 10

1. 'H' = High voltage level steady state, 'h' = High voltage level one set-up time prior to the low-to-high clock transition, 'L' = Low voltage level steady state 'l' = Low voltage level one set-up time prior to the Low-to-High clock transition, 'X' = Don't care, 'NC' = No change
2. $\overline{CLKEN}$ = VIL must be clocked in during Power-Up.
3. Control signals are initialted and terminated on the rising edge of the CLK, depending on their input level. When R/$\overline{W}$ and $\overline{CE}$ are low, a write cycle is initiated on the low-to-high transition of the CLK. Termination of a write cycle is done on the next low-to-high transistion of the CLK.

ORDERING INFORMATION



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