PRELIMINARY

8XC51FX
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLERS

Commercial/Express

87C51FA/83C51FA/80C51FA/87C51FB/83C51FB/87C51FC/83C51FC
***See Table 1 for Proliferation Options**

- **High Performance CHMOS EPROM/ROM/CPU**
- **12/24/33 MHz Operation**
- **Three 16-Bit Timer/Counters**
- **Programmable Counter Array with:**
  - **— High Speed Output,**
  - **— Compare/Capture,**
  - **— Pulse Width Modulator,**
  - **— Watchdog Timer Capabilities**
- **Up/Down Timer/Counter**
- **Three Level Program Lock System**
- **8K/16K/32K On-Chip Program Memory**
- **256 Bytes of On-Chip Data RAM**
- **Improved Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **7 Interrupt Sources**
- **Four Level Interrupt Priority**
- **Programmable Serial Channel with:**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **TTL Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Controller Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **Extended Temperature Range Except for 33 MHz Offering (−40°C to +85°C)**

MEMORY ORGANIZATION

ROM Device	EPROM Version	ROMLESS Version	ROM/ EPROM Bytes	RAM Bytes
83C51FA	87C51FA	80C51FA	8K	256
83C51FB	87C51FB	80C51FA	16K	256
83C51FC	87C51FC	80C51FA	32K	256

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 87C51FA/8XC51FB/8XC51FC is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. The Intel 83C51FA/80C51FA is fabricated on CHMOS III technology. Being a member of the MCS® 51 controller family, the 8XC51FA/8XC51FB/8XC51FC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 controller products. The 8XC51FA/8XC51FB/8XC51FC is an enhanced version of the 8XC52/8XC54/8XC58. Its added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control.

For the remainder of this document, the 8XC51FA, 8XC51FB, 8XC51FC will be referred to as the 8XC51FX, unless information applies to a specific device.

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April 1996 Order Number: 272322-004

Table 1. Proliferation Options

	Standard*1	-1	-2	-24	-33
80C51FA	X	X	X	X	X
83C51FA	X	X	X	X	X
87C51FA	X	X	X	X	X
83C51FB	X	X	X	X	X
87C51FB	X	X	X	X	X
83C51FC	X	X	X	X	X
87C51FC	X	X	X	X	X

NOTES:
*1 3.5 MHz to 12 MHz; 5V ±20%
-1 3.5 MHz to 16 MHz; 5V ±20%
-2 0.5 MHz to 12 MHz; 5V ±20%
-24 3.5 MHz to 24 MHz; 5V ±20%
-33 3.5 MHz to 33 MHz; 5V ±10%

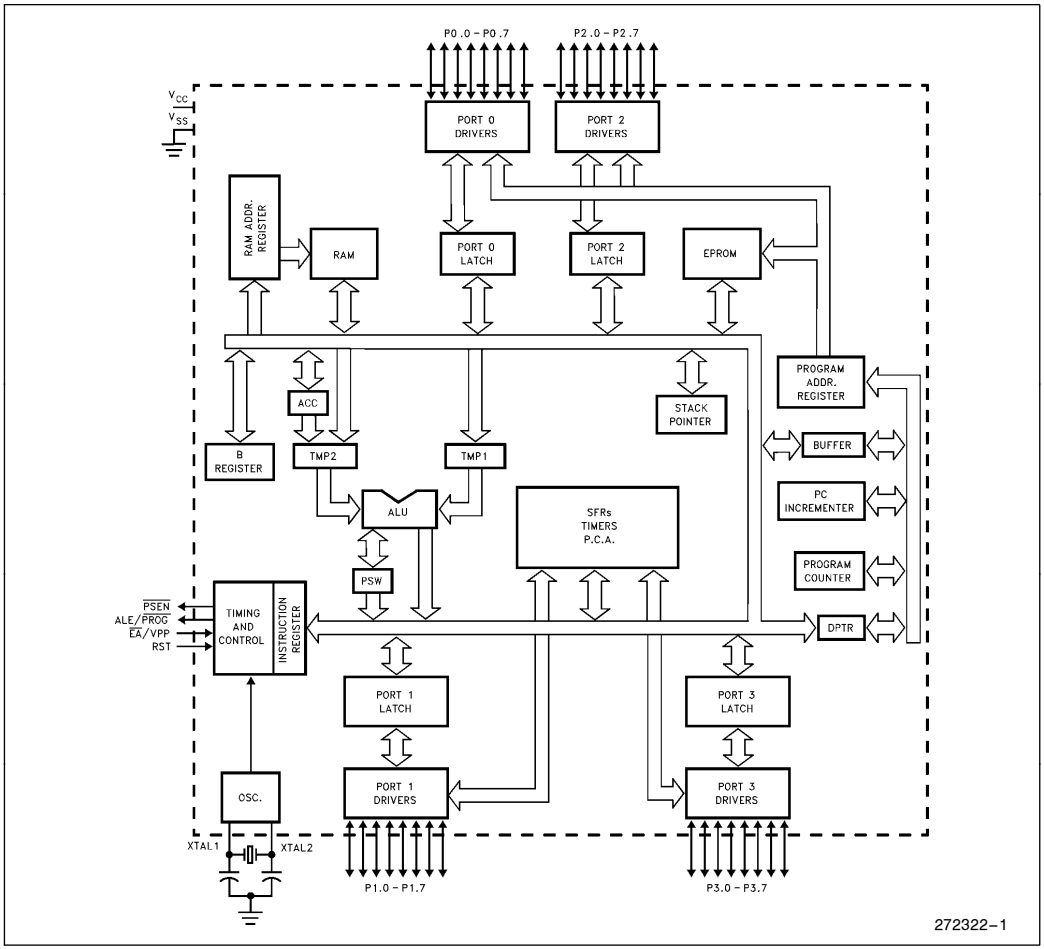


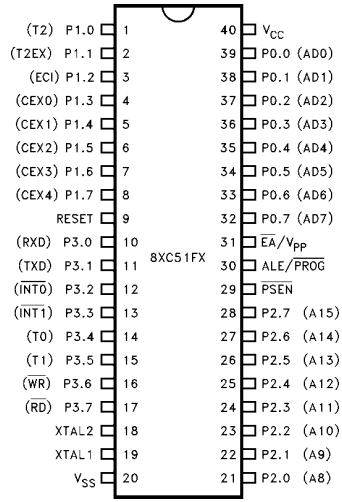
Figure 1. 8XC51FX Block Diagram

PROCESS INFORMATION

The 87C51FA/8XC51FB/8XC51FC is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order No. 210997.

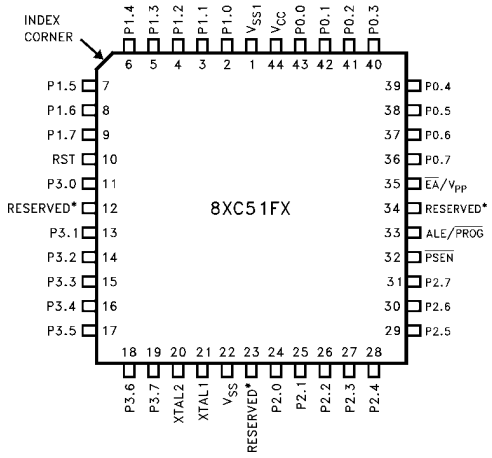
PACKAGES

Part	Prefix	Package Type
8XC51FX	P	40-Pin Plastic DIP
	D	40-Pin CERDIP
	N	44-Pin PLCC
	S	44-Pin QFP



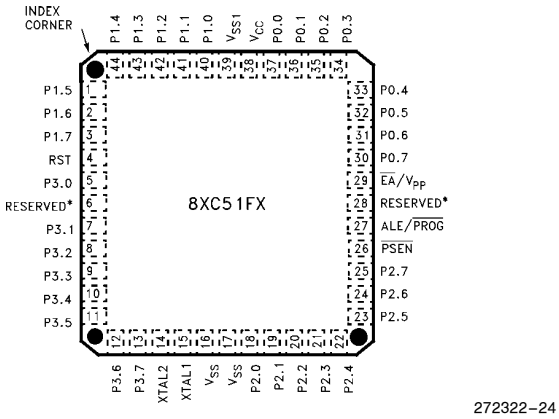
272322–2

DIP



272322–23

PLCC



272322–24

*Do not connect Reserved Pins.

QFP

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP devices or any 83C51FA/80C51FA device). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitution for the V_{SS} pin. (Connection not necessary for proper operation.)

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51FX:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FX.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51FX is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, ''Oscillators for Microcontrollers.''

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

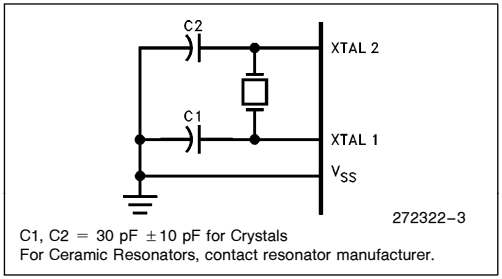


Figure 3. Oscillator Connections

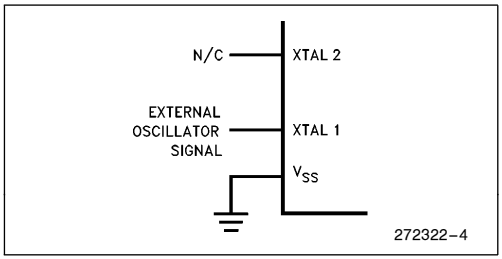


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FX either hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- Ambient light is known to affect the internal RAM contents during operation. If the 87C51FX application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), ''Designing with the 80C51BH.''

ONCE MODE

The ONCE (''On-Circuit Emulation'') Mode facilitates testing and debugging of systems using the 8XC51FX without the 8XC51FX having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FX is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

8XC51FX EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 3.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

NOTE:
Intel offers Express Temperature specifications for all 8XC51FX speed options except for 33 MHz.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
P	Plastic	Commercial	No
S	QFP	Commercial	No
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes
LP	Plastic	Extended	Yes
LS	QFP	Extended	Yes
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
TP	Plastic	Extended	No
TS	QFP	Extended	No

NOTE:
Contact distributor or local sales office to match EXPRESS prefix with proper device.

EXAMPLES:
P87C51FC indicates 87C51FC in a plastic package and specified for commercial temperature range, without burn-in.
LD87C51FC indicates 87C51FC in a cerdip package and specified for extended temperature range with burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} . . . . . 0V to +13.0V
Voltage on Any Other Pin to V_{SS} . . −0.5V to +6.5V
I_{OL} per I/O Pin . . . . . 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	°C
V_{CC}	Supply Voltage 8XC51FX-33 All Others	 4.5 4.0	 5.5 6.0	V
f_{OSC}	Oscillator Frequency 8XC51FX 8XC51FX-1 8XC51FX-2 8XC51FX-24 8XC51FX-33	 3.5 3.5 0.5 3.5 3.5	 12 16 12 24 33	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Note 5) (Ports 1, 2 and 3)			0.3 0.45 1.0	V	I_{OL} = 100 μA I_{OL} = 1.6 mA (Note 1) I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage (Note 5) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)			0.3 0.45 1.0	V	I_{OL} = 200 μA I_{OL} = 3.2 mA (Note 1) I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Ports 1, 2 and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V	I_{OH} = −10 μA I_{OH} = −30 μA (Note 2) I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) 83C51FA/80C51FA (Express)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V	I_{OH} = −200 μA I_{OH} = −3.2 mA (Note 2) I_{OH} = −7.0 mA I_{OH} = −6.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V

DC CHARACTERISTICS (Over Operating Conditions)

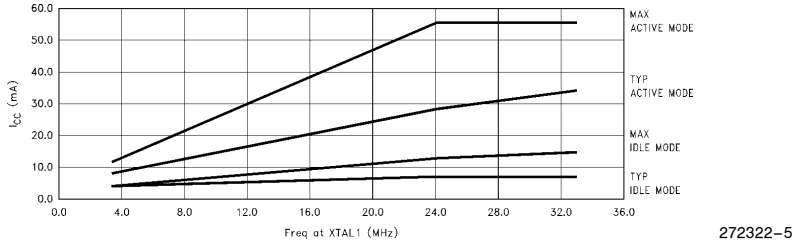
All parameter values apply to all devices unless otherwise indicated. (Continued)

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
I_{LI}	Input leakage Current (Port 0)			±10	µA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Express Commercial			 −750 −650	 µA	$V_{IN} = 2V$
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1MHz, 25°C
I_{CC}	Power Supply Current: Active Mode At 12 MHz (Figure 5) At 16 MHz At 24 MHz At 33 MHz Idle Mode At 12 MHz (Figure 5) At 16 MHz At 24 MHz At 33 MHz Power Down Mode		 15 20 28 35 5 6 7 7 5	 30 38 56 56 7.5 9.5 13.5 15 75	 mA mA mA mA mA mA mA mA µA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Typicals are based on limited number of samples, and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



Note:
I_{CC} max at 33 MHz is at 5V ±10% V_{CC}, while I_{CC} max at 24 MHz and below is at 5V ±20% V_{CC}.

Figure 5. 8XC51FA/FB/FC I_{CC} vs Frequency

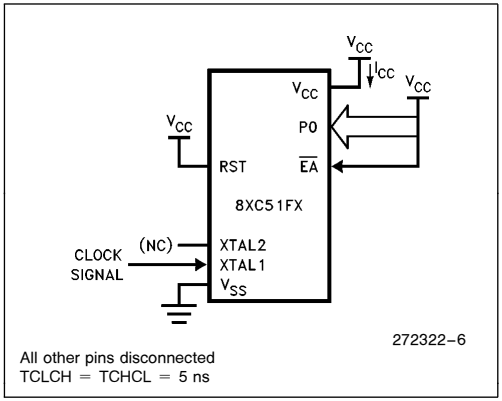


Figure 6. I_{CC} Test Condition, Active Mode

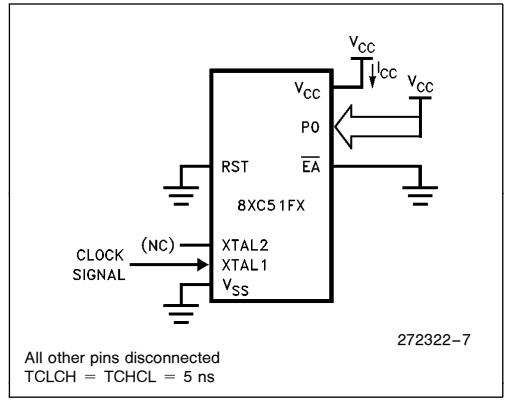


Figure 7. I_{CC} Test Condition Idle Mode

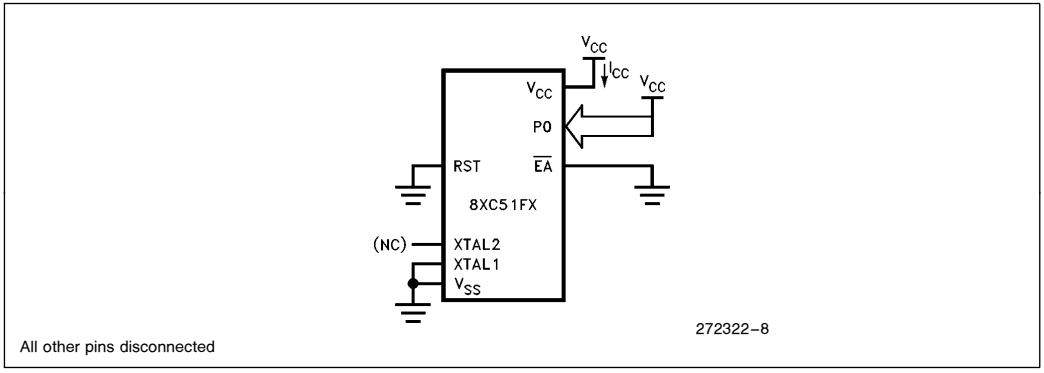


Figure 8. I_{CC} Test Condition, Power Down Mode. V_{CC} = 2.0V to 6.0V.

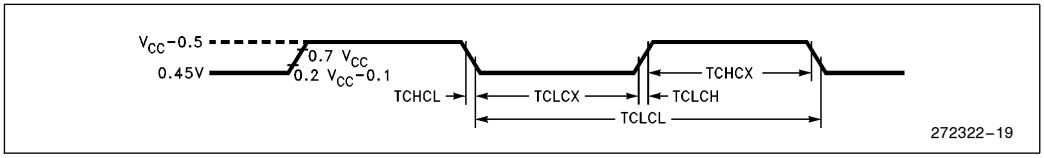


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to PSEN Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XC51FX refers to 8XC51FX, 8XC51FX-1 and 8XC51FX-2.

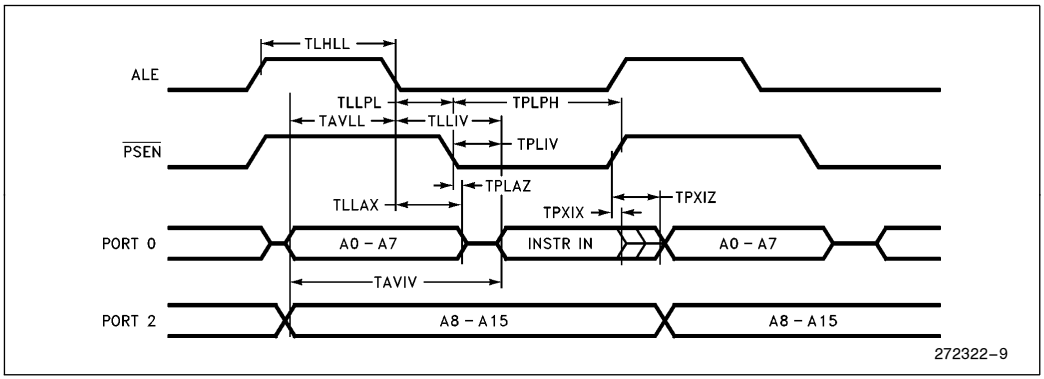
Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XC51FX 8XC51FX-1 8XC51FX-2 8XC51FX-24 8XC51FX-33							 3.5 3.5 0.5 3.5 3.5	 12 16 12 24 33	MHz
TLHLL	ALE Pulse Width	127		43		21		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low 8XC51FX 8XC51FX-24 8XC51FX-33	43		 12		 5		 TCLCL−40 TCLCL−30 TCLCL−25		 ns ns ns
TLLAX	Address Hold After ALE Low 8XC51FX/-24 8XC51FX-33	53		12		 5		 TCLCL−30 TCLCL−25		 ns ns
TLLIV	ALE Low to Valid Instr In 8XC51FX 8XC51FX-24 8XC51FX-33		234		91		 56		 4TCLCL−100 4TCLCL−75 4TCLCL−65	 ns ns ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low 8XC51FX/-24 8XC51FX-33	53		12		 5		 TCLCL−30 TCLCL−25		 ns ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		80		46		3TCLCL−45		
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instr In 8XC51FX 8XC51FX-24 8XC51FX-33		145		35		 35		 3TCLCL−105 3TCLCL−90 3TCLCL−55	 ns ns ns
TPXIX	Input Instr Hold after $\overline{\text{PSEN}}$	0		0		0		0		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

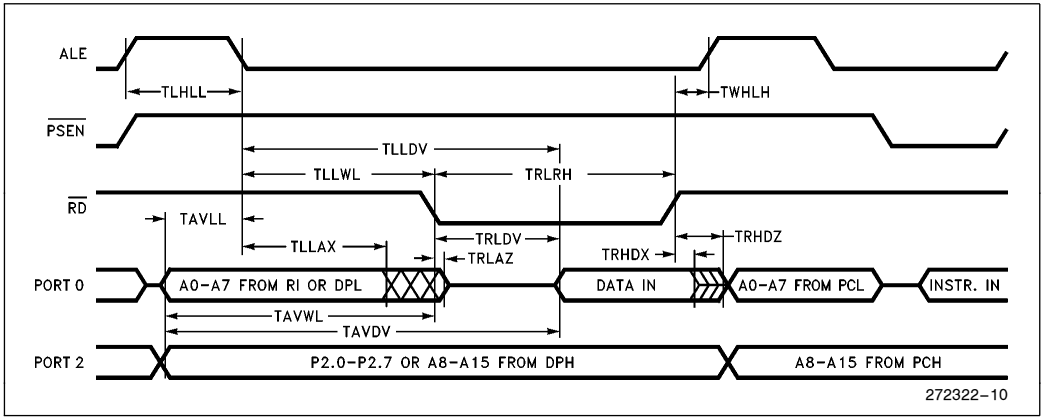
All parameter values apply to all devices unless otherwise indicated

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instr Float After $\overline{PSEN}$									
	8XC51FX		59						TCLCL-25	ns
	8XC51FX-24				21				TCLCL-20	ns
	8XC51FX-33						5		TCLCL-25	ns
TAVIV	Address to Valid Instr In									
	8XC51FX/-24		312		103				5TCLCL−105	ns
	8XC51FX-33						71		5TCLCL−80	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		150		82		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		150		82		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In									
	8XC51FX		252						5TCLCL−165	ns
	8XC51FX-24				113				5TCLCL−95	ns
	8XC51FX-33						61		5TCLCL−90	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$									
	8XC51FX/24		107		23				2TCLCL−60	ns
	8XC51FX-33						35		2TCLCL−25	ns
TLLDV	ALE Low to Valid Data In									
	8XC51FX		517						8TCLCL−150	ns
	8XC51FX-24/33				243		150		8TCLCL−90	ns
TAVDV	Address to Valid Data In									
	8XC51FX		585						9TCLCL−165	ns
	8XC51FX-24/33				285		180		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	75	175	41	140	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low									
	8XC51FX	203						4TCLCL−130		ns
	8XC51FX-24			77				4TCLCL−90		ns
	8XC51FX-33					46		4TCLCL−75		ns
TQVWX	Data Valid to $\overline{WR}$ Transition									
	8XC51FX	33						TCLCL−50		ns
	8XC51FX-24/33			12		0		TCLCL−30		ns
TWHQX	Data Hold After $\overline{WR}$									
	8XC51FX	33						TCLCL−50		ns
	8XC51FX-24			7				TCLCL−35		ns
	8XC51FX-33					3		TCLCL−27		ns
TQVWH	Data Valid to $\overline{WR}$ High									
	8XC51FX	433						7TCLCL−150		ns
	8XC51FX-24/33			222		142		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High									
	8XC51FX	43	123					TCLCL−40	TCLCL+40	ns
	8XC51FX-24			12	71			TCLCL−30	TCLCL+30	ns
	8XC51FX-33					5	55	TCLCL−25	TCLCL+25	ns

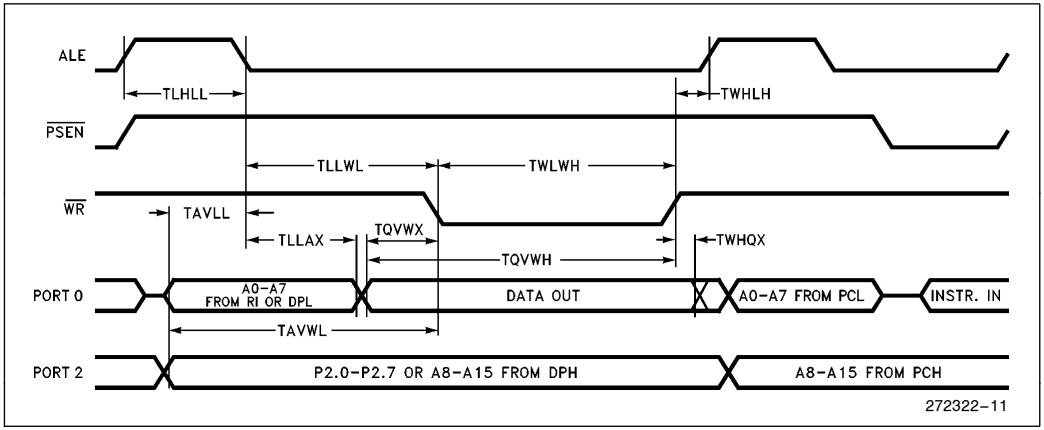
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

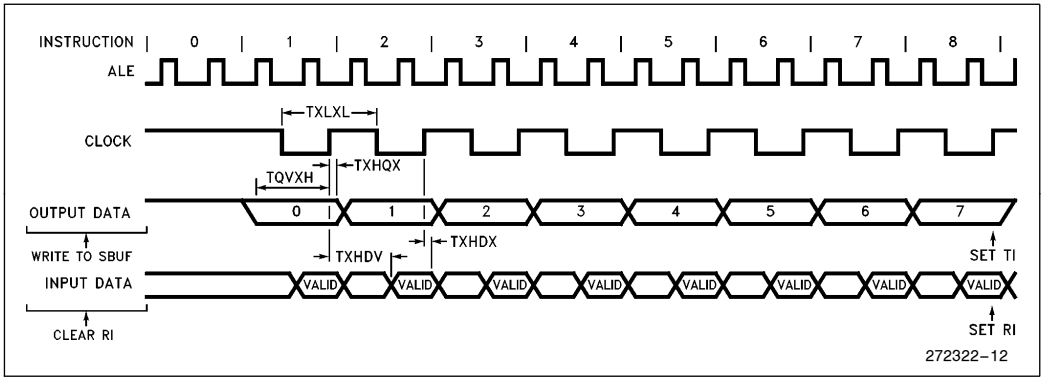


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.50		0.36		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		284		167		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge 8XC51FX 8XC51FX-24/33	50		34		10		2TCLCL−117 2TCLCL−50		ns ns
TXHDX	Input Data Hold After Clock Rising Edge	0			0		0	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		283		167		10TCLCL−133	ns

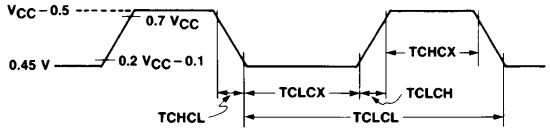
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

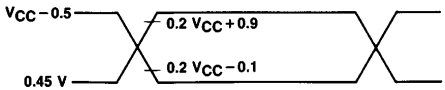
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			MHz
	8XC51FX	3.5	12	MHz
	8XC51FX-1	3.5	16	MHz
	8XC51FX-2	0.5	12	MHz
	8XC51FX-24	3.5	24	MHz
	8XC51FX-33	3.5	33	MHz
TCHCX	High Time	20		ns
	8XC51FX-24/33	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCX	Low Time	20		ns
	8XC51FX-24/33	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCH	Rise Time		20	ns
	8XC51FX-24		10	ns
	8XC51FX-33		5	ns
TCHCL	Fall Time		20	ns
	8XC51FX-24		10	ns
	8XC51FX-33		5	ns

EXTERNAL CLOCK DRIVE WAVEFORM



272322–13

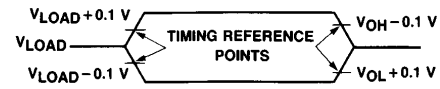
AC TESTING INPUT, OUTPUT WAVEFORMS



272322–14

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



272322–15

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA.

PROGRAMMING THE EPROM/OTP

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal EPROM locations.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 4. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 10.

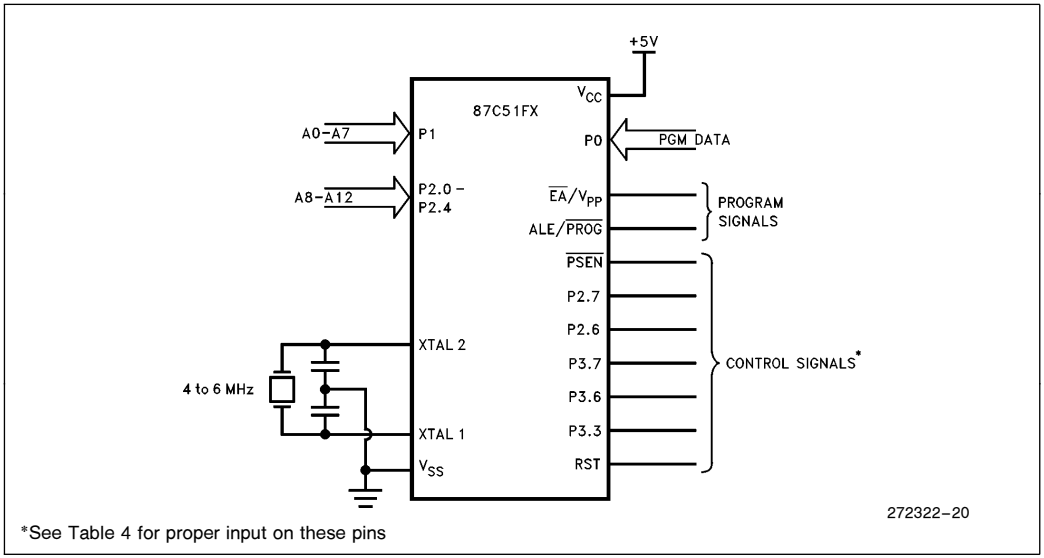
Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

NOTE:

- $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

Table 4. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⎍	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⎍	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⎍	12.75V	H	H	H	H	H
	Bit 2	H	L	⎍	12.75V	H	H	H	L	L
	Bit 3	H	L	⎍	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 4 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FX the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V $\pm$0.25V.
5. Pulse, ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C51FX.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

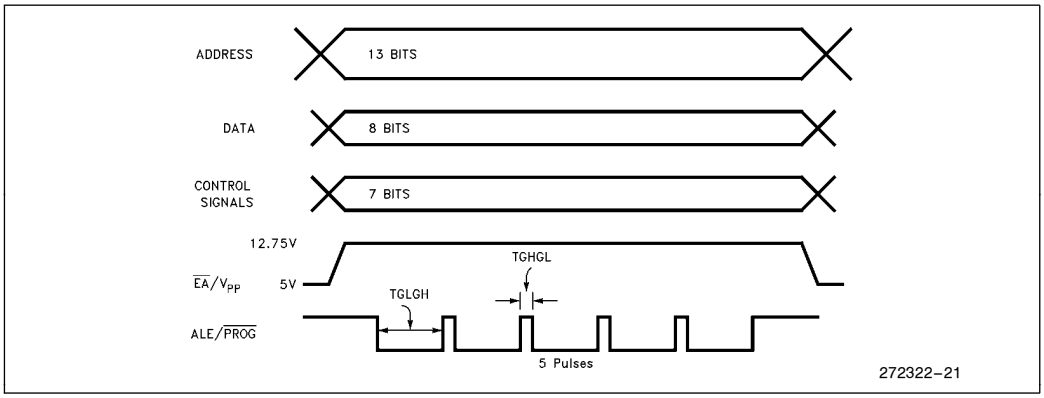


Figure 11. Programming Signals Waveforms

ROM and EPROM Lock System

The 87C51FX program lock system, when programmed, protects the onboard program against software piracy.

The 83C51FX has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 5. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table. The 83C51FA does not have protection features.

The 87C51FX has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 5.

Table 5. Program Lock Bits and the Features

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 4 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51FX has 3 programmable lock bits that when programmed according to Table 5 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 87C51FX has 3 signature bytes in locations 30H, 31H, and 60H. The 83C51FA has 2 signature bytes in locations 30H and 31H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	83C51FA	7AH/FAH
	87C51FA	FAH
	83C51FB	7BH/FBH
	87C51FB	FBH
	83C51FC	7CH/FCH
	87C51FC	FCH

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

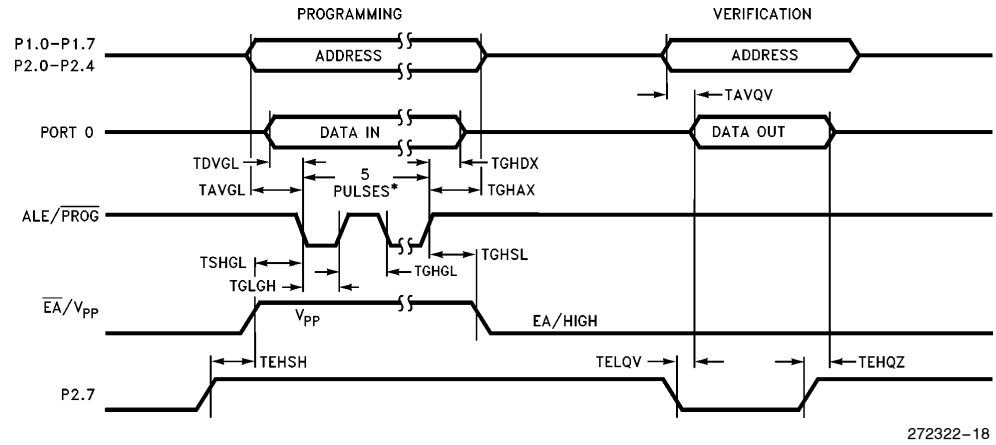
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



NOTE:
*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order No. 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
P	45°C/W	16°C/W	All
D	36°C/W	13°C/W	80C51FA, 83C51FA, 8XC51FC
	45°C/W	15°C/W	87C51FA, 8XC51FB
N	46°C/W	16°C/W	All
S	97°C/W	24°C/W	FA
	96°C/W	24°C/W	FB
	87°C/W	18°C/W	FC

DATA SHEET REVISION HISTORY

Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this datasheet (272322-003) and the previous version (272322-002):

1. Removed 8XC51FX-3 and 8XC51FX-20, replaced with 8XC51FX-24.
2. Included 8XC51FX-24 and 8XC51FX-33 devices.
3. 80C51FA and 83C51FA now have the same features as 87C51FA, 8XC51FB and 8XC51FC; same DC spec used for all devices.

The following differences exist between the ''-002'' and ''-001'' version of 8XC51FX datasheet:

1. Removed 8XC51FX-L from datasheet.
2. Include V_{OH1} for 83C51FA (Express)/80C51FA (Express).

This 8XC51FX datasheet (272322-001) replaces the following datasheets:

87C51FA/83C51FA/80C51FA	270258-007
83C51FA/80C51FA EXPRESS	270620-001
87C51FA EXPRESS	270619-001
87C51FA-20/-3	272081-002
87C51FB/83C51FB	270563-005
87C51FB-20/-3 83C51FB-20/-3	272080-002
87C51FB/83C51FB EXPRESS	270767-002
87C51FC/83C51FC	270789-004
87C51FC/83C51FC EXPRESS	270903-001
87C51FC-20/-3 83C51FC-20/-3	272028-002