F1956 Datasheet

7-Bit 0.25 dB Wideband Digital Step Attenuator *1 to 6000 MHz*

General Description

This document describes the specification for the F1956 Digital Step Attenuator. The F1956 is part of IDT's *Glitch-Free™* family of DSAs optimized for the demanding requirements of Base Station (BTS) radio cards and numerous other non-BTS applications. This device is offered in compact 5 mm x 5 mm 32-pin package with 50 Ω input and output impedance for ease of integration into the radio or RF system.

Competitive Advantage

The F1956 offers very high reliability due to its construction from a monolithic silicon die in a QFN package. The insertion loss is very low with minimal distortion. Additionally the device is designed to have extremely accurate attenuations levels. These accurate attenuation level improves system SNR and/or ACLR by ensuring system gain is as close to targeted level as possible. Also, the very fast settling time in parallel mode is ideal for fast switching systems. Finally, the device is *Glitch-Free™* with less than 2 dB of ringing across the attenuation range in stark contrast to competing DSAs that glitch as much as 10 dB during MSB state changes.

- ✓ Lowest insertion loss for best SNR
- ✓ *Glitch-Free™* technology to protect PA or ADC during transitions between attenuation states.
- ✓ Extremely accurate attenuation levels
- ✓ Ultra low distortion
- ✓ MSL1 and 2000 V HBM ESD

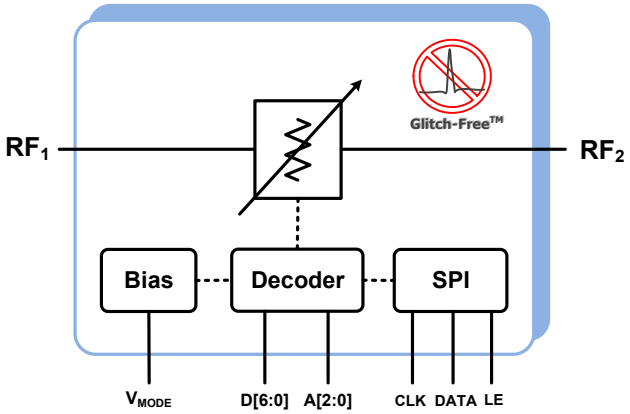
Ordering Information



Features

- Serial & 7-bit Parallel Interface
- 31.75 dB Range
- 0.25 dB steps
- *Glitch-Free™*: low transient overshoot
- 500 ns settling time
- Ultra linear > 64 dBm IIP3
- Low Insertion Loss < 1.7 dB @ 4 GHz
- Attenuation error < ±0.2 dB @ 4 GHz
- Bi-directional RF use
- 3.3 V or 5 V Supply
- 1.8 V or 3.3 V control logic
- Low Current Consumption: 350 µA typical
- -40 °C to +105 °C operating temperature
- 5 mm x 5 mm Thin QFN 32 pin package

Functional Block Diagram



Part# Details

Part#	Freq Range (MHz)	Resolution / Range (dB)	Control	IL (dB)	Pinout
F1950	150 - 4000	0.25 / 31.75	Parallel & Serial	1.3	PE43702 PE43701
F1951	100 - 4000	0.50 / 31.5	Serial Only	1.2	HMC305
F1952	100 – 4000	0.50 / 15.5	Serial Only	0.9	HMC305
F1953	400 – 4000	0.50 / 31.5	Parallel & Serial	1.3	PE4302 DAT-31R5
F1956	**1 - 4000**	**0.25 / 31.75**	**Parallel & Serial**	**1.4**	**PE43705, PE43712, RFSA3715**
F1912	1 – 4000	0.50 / 31.5	Parallel & Serial	1.6	PE4312 PE4302

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
VDD to GND	V_{DD}	-0.3	+5.5	V
D[6:0], DATA, CLK, LE, A0, A1, A2, V_{MODE}	VCNTL	-0.3	Min (V_{DD} + 0.3, 3.9)	V
RF1, RF2	V_{RF}	-0.3	+0.3	V
Maximum Input Power applied to RF1 or RF2 (>100 MHz)	P_{RF}		+34	dBm
Operating Case Temperature			105	°C
Continuous Power Dissipation			1.5	W
Maximum Junction Temperature	TJ_{max}		+150	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		1500 (Class 1C)	V
ESD Voltage – CDM (Per JESD22-C101F)	V_{ESDCDM}		500 (Class C2)	V

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	40 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	4 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

F1956 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{DD}		3.00		5.25	V
Operating Temperature Range	T_{CASE}	Case Temperature	-40		+105	°C
Frequency Range	F_{RF}		1		6000	MHz
RF CW Input Power	P_{CW}	RF1 or RF2			See Figure 1	dBm
RF Peak Input Power	P_{peak}	RF1 Port, V_{DD} = 3.3V, T_{CASE}= 85 °C, F_{RF} > 500 MHz, WCDMA, 3GPP, Downlink, 64 DPCH, Chip rate =3.84 MSPS, Avg. Pin = +22 dBm				
		1 %			28.9	dBm
		0.1 %			30.7	
		0.01 %			32.3	
		0.001 %			33.2	
RF Source Impedance	Z_{RFI}	Single Ended		50		Ω
RF Load Impedance	Z_{RFO}	Single Ended		50		Ω

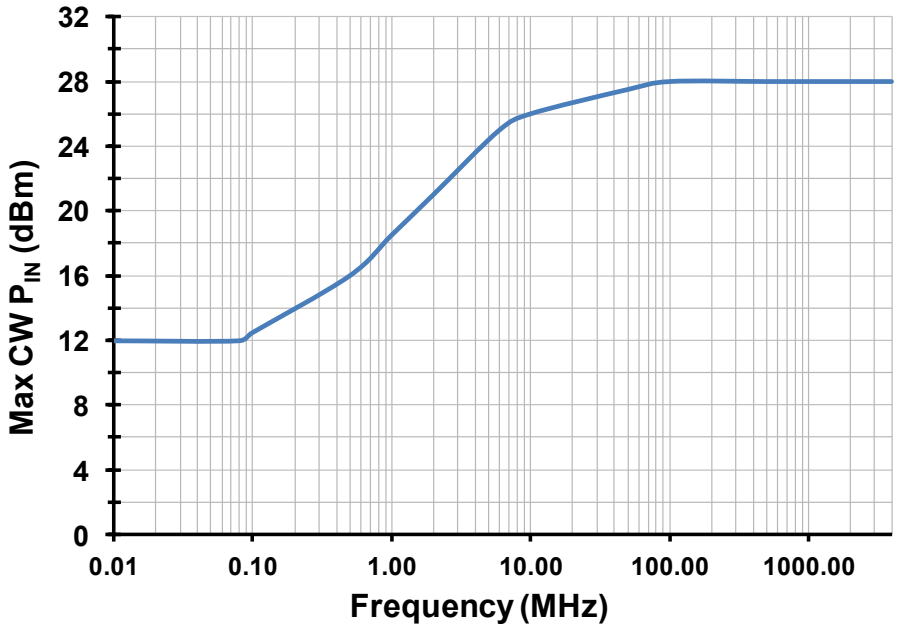


Figure 1 - Maximum Operating RF input power vs Input frequency

F1956 SPECIFICATION

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25 °C, F_{RF} = 2 GHz, 0.25 dB steps unless otherwise noted. Minimum Attenuation D[6:0] = [0000000], Maximum Attenuation D[6:0] = [1111111], EVKit losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High	V_{IH}	CLK, LE, DATA, D[6:0], A0, A1, A2, V_{MODE}				
		3.0 V ≤ V_{DD} ≤ 3.6 V	1.17[2]		V_{DD}	V
		3.6 V < V_{DD}	***1.17***[1]		3.6	
Logic Input Low	V_{IL}	CLK, LE, DATA, D[6:0], A0, A1, A2, V_{MODE}			***0.63***	V
Logic Current	I_{IH}, I_{IL}	Individual Pins	***-40***		***+20***	µA
Supply Current	I_{DD}			350	***800***	µA
Attenuation Range	ATT_{RNG}	No missing codes		31.75		dB
Minimum Gain Step	LSB	F_{RF} ≤ 4.5 GHz		0.25		dB
		F_{RF} ≤ 6.5 GHz		0.50		
		F_{RF} ≤ 8.5 GHz		1.00		
DSA Settling time	τ_{SET}	Max to Min Attenuation to settle to within 0.5 dB of final value		0.9		µs
		Min to Max Attenuation to settle to within 0.5 dB of final value		1.8		
Video Feedthrough RF1, RF2 ports	VID_{FT}	Measured at RF ports with 2.5 ns risetime, 0 to 3.3 V control pulse		10		mV_{pp}
Maximum spurious level on any RF port[4]	$Spur_{MAX}$	Spur Freq ~ 2.2 MHz		-140		dBm
Serial Clock Speed	F_{CLK}	SPI 3 wire bus			***25***	MHz
Parallel to Serial Setup	A	SPI 3 wire bus	***100***			ns
Serial Data Hold Time	B	SPI 3 wire bus	***10***			ns
LE Delay	C	SPI 3 wire bus Time from final serial clock rising edge	***10***			ns
Maximum Switching Rate	SW_{RATE}			25		kHz

Specification Notes:
Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3. The input 0.1 dB compression point is used as a linearity figure of merit. The recommended maximum input power is specified as the lesser of the two values from RF CW Power (Figure 1) and the RF Average Power (Recommended Operating Conditions Table)..
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

F1956 SPECIFICATION (CONTINUED)

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25°C, F_{RF} = 2 GHz, 0.25 dB steps unless otherwise noted. Minimum Attenuation D[6:0] = [0000000], Maximum Attenuation D[6:0] = [1111111], EVKit losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Insertion Loss	IL	1 MHz < F_{RF} ≤ 2 GHz		1.3	***1.8***	dB
		2 GHz < F_{RF} ≤ 3 GHz		1.3	1.9	
		3 GHz < F_{RF} ≤ 4 GHz		1.6	2.2	
		4 GHz < F_{RF} ≤ 5 GHz		2.1	2.6	
		5 GHz < F_{RF} ≤ 6 GHz		2.6	3.0	
Relative Phase (Amin vs. Amax)	ΦΔ	F_{RF} = 1 GHz		12		deg
		F_{RF} = 2 GHz		25		
		F_{RF} = 4 GHz		55		
		F_{RF} = 6 GHz		90		
Step Error (Differential Non-Linearity)	DNL	Max error between adjacent steps		0.10	0.19	dB
Absolute Attenuation Error (Integral Non-Linearity)	INL	Max Error for state 19.75 dB, FRF = 2 GHz	***-0.4***	0.1	***+0.5***	dB
		Max Error, over all states F_{RF} = 2 GHz	-0.8		+0.5	
Input Return Loss	S_{11}	1 MHz < F_{RF} ≤ 2 GHz		20	15	dB
		2 GHz < F_{RF} ≤ 4 GHz		20	15	
		4 GHz < F_{RF} ≤ 6 GHz		14	7	
Output Return Loss	S_{22}	1 MHz < F_{RF} ≤ 2 GHz		18	14	dB
		2 GHz < F_{RF} ≤ 4 GHz		16	12	
		4 GHz < F_{RF} ≤ 6 GHz		11	7	
Input IP3	IIP3	P_{IN} = +10 dBm per tone 50 MHz Tone Separation				
		Attn = 0.00 dB		64		dBm
		Attn = 15.75 dB		64		
		Attn = 31.75 dB		64		
		Attn = 0.00 dB P_{IN} = +22 dBm per tone 1 MHz Tone Separation				
		F_{RF} = 0.7 GHz	60	63.4		dBm
		F_{RF} = 1.8 GHz	60	63.4		
		F_{RF} = 2.2 GHz	60	64.1		
		F_{RF} = 2.6 GHz	60	63.3		
Input 0.1dB Compression[3]	$P_{0.1dB}$	F_{RF} = 2 GHz, Attn = 10 dB		34.5		dBm

Specification Notes:
Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3. The input 0.1 dB compression point is used as a linearity figure of merit. The recommended maximum input power is specified as the lesser of the two values from RF CW Power (Figure 1) and the RF Average Power (Recommended Operating Conditions Table)..
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

PROGRAMMING OPTIONS

F1956 can be programmed using either the parallel or serial interface; selectable via V_{MODE} (pin 3). Serial mode is selected by floating V_{MODE} or pulling V_{MODE} to a logic high and parallel mode is selected by setting V_{MODE} to logic low.

SERIAL CONTROL MODE

F1956 Serial mode is selected by floating V_{MODE} (pin 3) or pulling it to logic high. The serial interface is a 16-bit shift register made up of two words. The first 8-bit word is the Attenuation word, which controls the DSA state. The second word is the address word, which uses only 3 of 8-bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0 – A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common DATA, CLK and LE**.**

When serial programming is used, all the parallel control input pins 26 – 32 can be left open or grounded. If a pin is grounded then an additional 25 µA will be drawn from the voltage supply per pin.

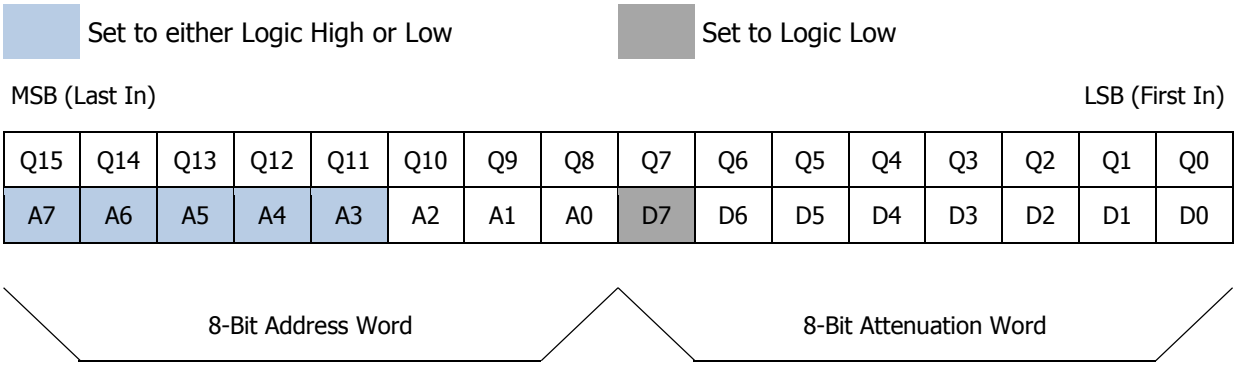


Figure 2 -Two 8-bit words are comprised of 16bit serial in, parallel out shift register

Table 1 -Truth Table for the Serial Address Word

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	Address Setting
X	X	X	X	X	0	0	0	000
X	X	X	X	X	0	0	1	001
X	X	X	X	X	0	1	0	010
X	X	X	X	X	0	1	1	011
X	X	X	X	X	1	0	0	100
X	X	X	X	X	1	0	1	101
X	X	X	X	X	1	1	0	110
X	X	X	X	X	1	1	1	111

Table 2 - Truth Table for the Serial Control Word

D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.25
0	0	0	0	0	0	1	0	0.5
0	0	0	0	0	1	0	0	1
0	0	0	0	1	0	0	0	2
0	0	0	1	0	0	0	0	4
0	0	1	0	0	0	0	0	8
0	1	0	0	0	0	0	0	16
0	1	1	1	1	1	1	1	31.75

SERIAL MODE DEFAULT CONDITION

When the device is first powered up it will default to the **Maximum Attenuation** setting as described below: Note that for the F1956 in all cases logic high (1) has the attenuation stepped IN, while logic low (0) has the attenuation stepped OUT.

MSB (Last In) LSB (First In)

Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	0	0	0	0	1	1	1	1	1	1	1

8-Bit Address Word 8-Bit Attenuation Word

Figure 3 -Default register settings set for max attenuation and 000 Address Word

REGISTER TIMING DIAGRAM: (NOTE THE TIMING SPEC INTERVALS IN BLUE)

With serial control, the F1956 can be programmed via the serial port on the rising edge of Latch Enable (LE) which loads the last 8 DATA line bits [formatted LSB (D0) first] resident in the SHIFT register followed by the Address Word into the ACTIVE register.

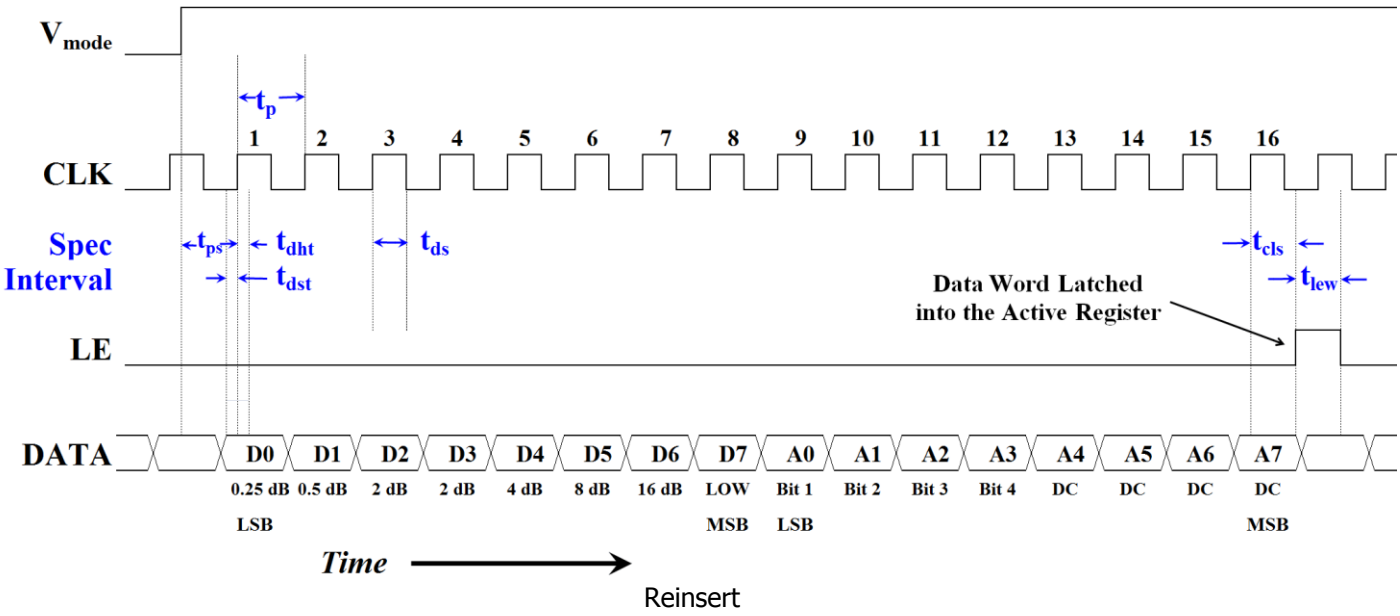


Figure 4 - Serial Timing Diagram

Note - When Latch enable is high, the shift register is disabled and DATA is NOT continuously clocked into the shift register which minimizes noise. It is recommended that Latch enable be left high when the device is not being programmed.

Table 3 - Serial Mode Timing Table

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{ps}	Parallel to Serial Setup Time - From rising edge of Vmode to rising edge of CLK for D5	***100***		ns
t_p	Clock high pulse width	***10***		ns
t_{cls}	LE Setup Time - From the rising edge of CLK pulse for D0 to LE rising edge minus half the clock period.	***10***		ns
t_{lew}	LE pulse width	***30***		ns
t_{dst}	Data Setup Time - From the starting edge of Data bit to rising edge of CLK	***10***		ns
t_{dht}	Data Hold Time - From rising edge of CLK to falling edge of the Data bit.	***10***		ns

PARALLEL CONTROL MODE

For the F1956 the user has the option of running in one of two parallel modes. Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode:

Direct Parallel Mode is selected when V_{MODE} is a logic low and LE is a logic high. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 26 – 32]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode:

Latched Parallel Mode is selected when V_{MODE} is logic low and LE is toggled from logic low to high. To utilize Latched Parallel Mode:

- Set V_{MODE} is logic low.
- Set LE to logic low.
- Adjust pins [26, 27, 28, 29, 30, 31, 32] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic low).
- Pull LE to a logic high. The device will then transition to the attenuation settings reflected by pins D6 - D0.
- IF LE is pulled to a logic low then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with V_{MODE} set for logic low and LE logic low. In this case the default setting is MAXIMUM Attenuation.

Table 4 - Truth Table for the Parallel Control Word

D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.25
0	0	0	0	0	1	0	0.5
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	2
0	0	1	0	0	0	0	4
0	1	0	0	0	0	0	8
1	0	0	0	0	0	0	16
1	1	1	1	1	1	1	31.75

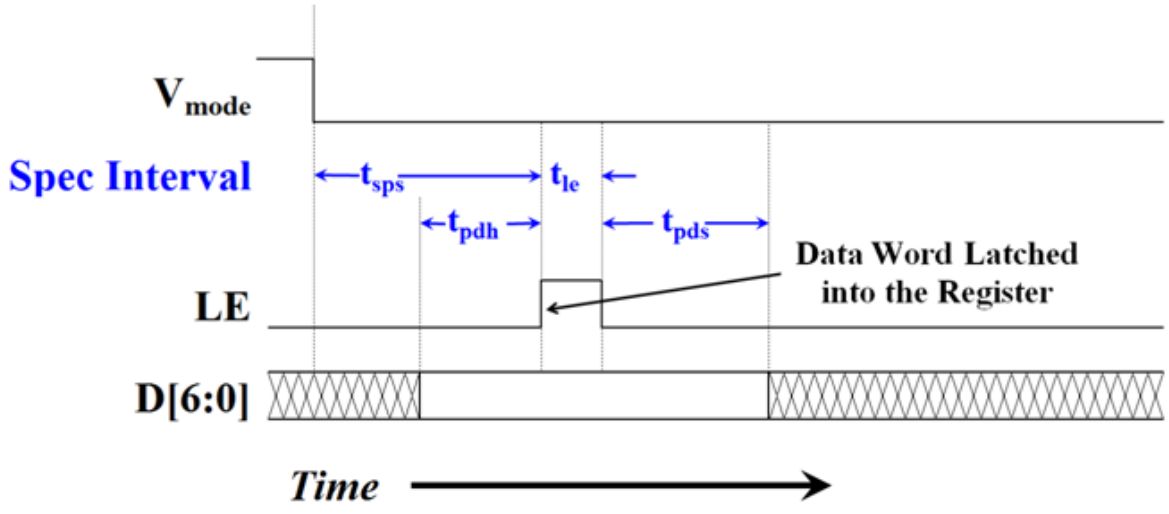


Figure 5 - Latched Parallel Mode Timing Diagram

Table 5 - Latched Parallel Mode Timing

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{sps}	Serial to Parallel Mode Setup Time	100		ns
t_{pdh}	Parallel Data Hold Time	10		ns
t_{le}	LE minimum pulse width	10		ns
t_{pds}	Parallel Data Setup Time	10		ns

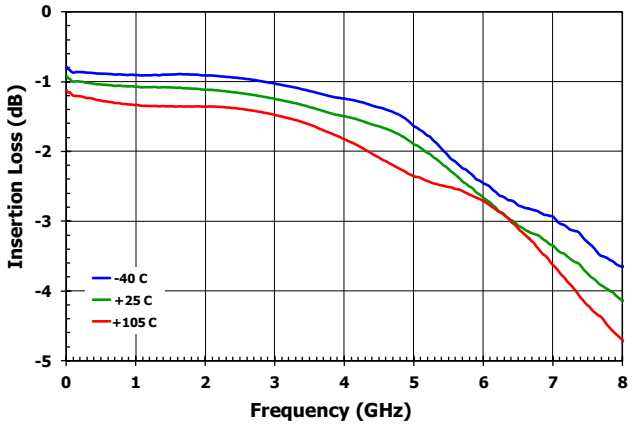
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

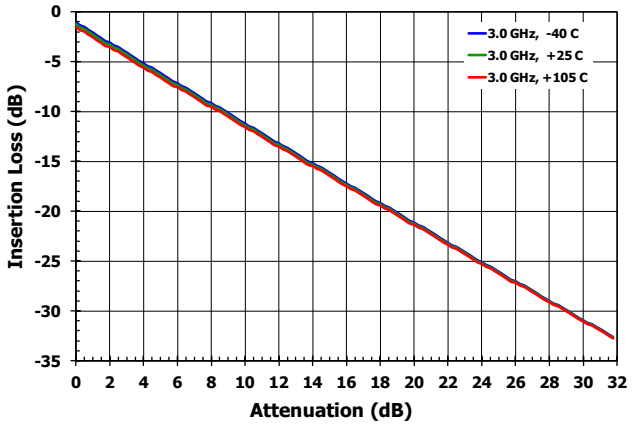
1. **V_{DD} = +3.30 V**
2. **T_{CASE} = +25 °C**
3. **50 MHz Tone Space**
4. **Serial Control**
5. **P_{IN} = 0 dBm**
6. **RF1 is the input port**
7. **Attenuation Setting = 0 dB**
8. **EVKit losses (traces and connectors) are fully de-embedded**

TYPICAL OPERATING CONDITIONS (- 1 -)

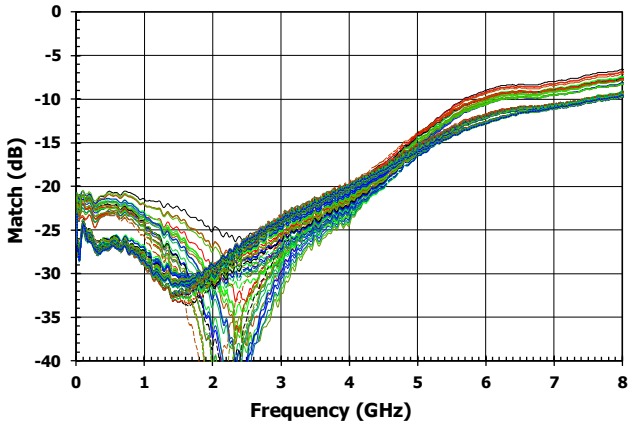
Insertion Loss vs Frequency



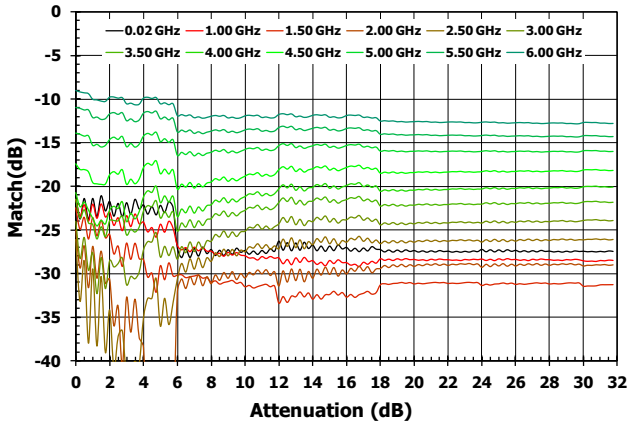
Insertion Loss vs Attenuation



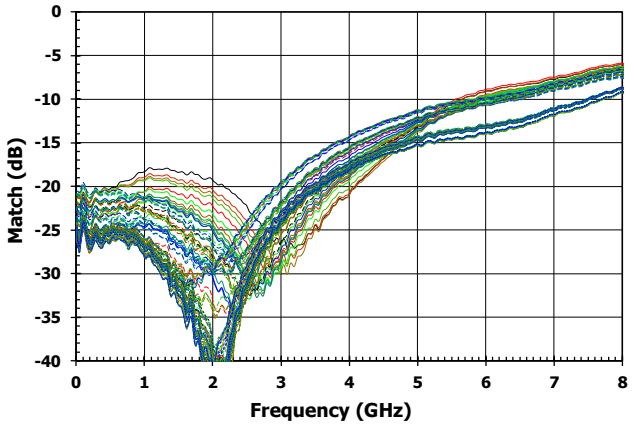
Input Return Loss vs Frequency [All States]



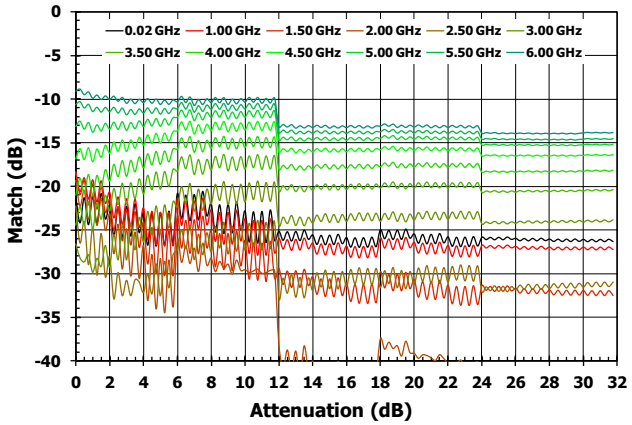
Input Return Loss vs Attenuation



Output Return Loss vs Frequency [All States]

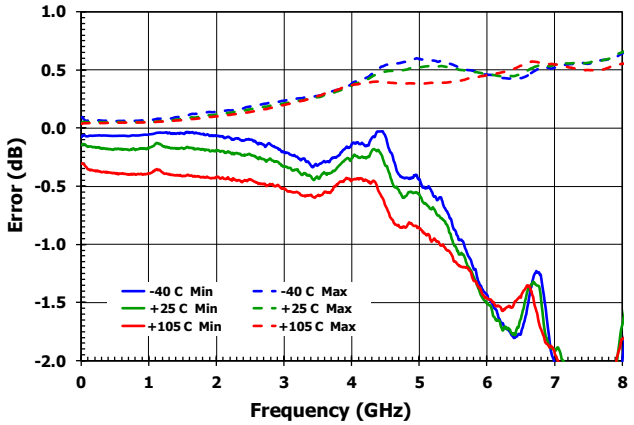


Output Return Loss vs Attenuation

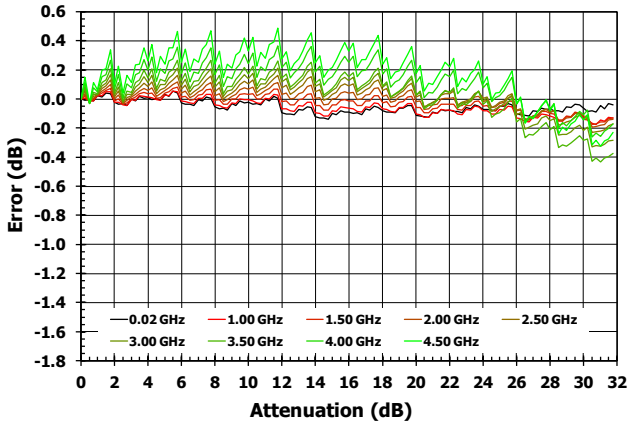


TYPICAL OPERATING CONDITIONS (- 2 -)

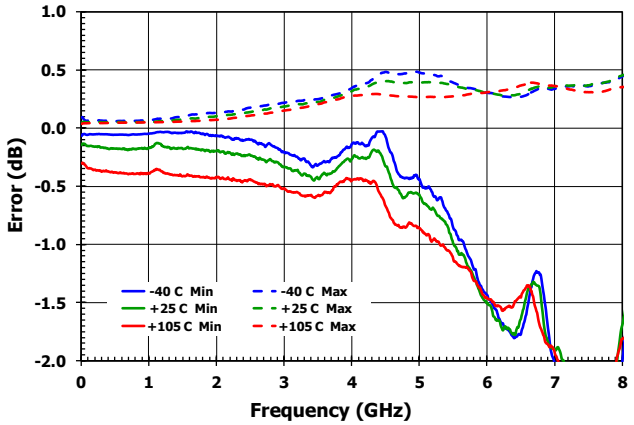
Worst Case Absolute Accuracy (LSB=0.25 dB)



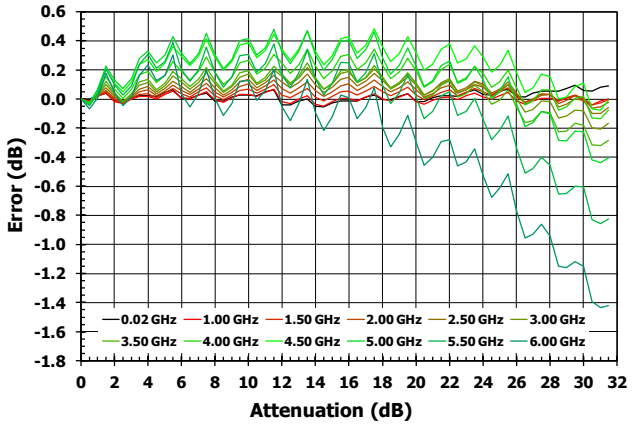
Absolute Accuracy (LSB=0.25 dB)



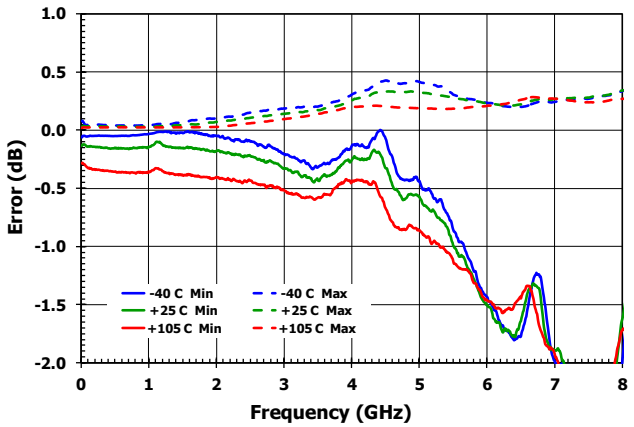
Worst Case Absolute Accuracy (LSB=0.50 dB)



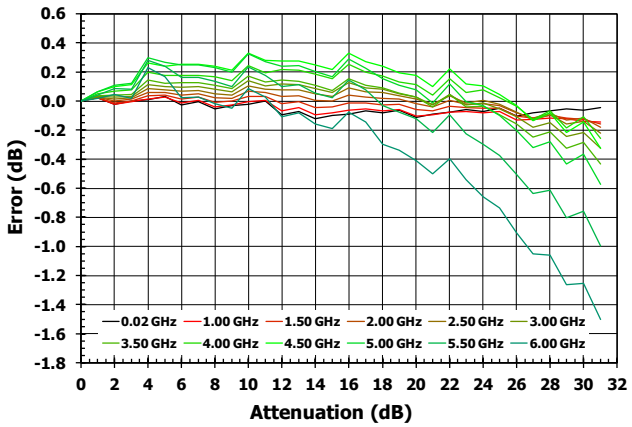
Absolute Accuracy (LSB=0.50 dB)



Worst Case Absolute Accuracy (LSB=1.00 dB)

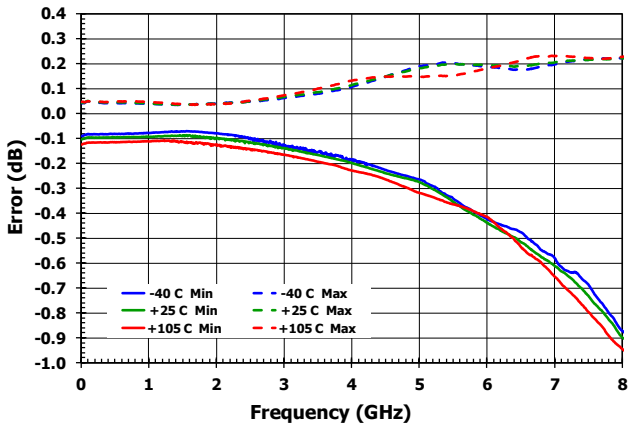


Absolute Accuracy (LSB=1.00 dB)

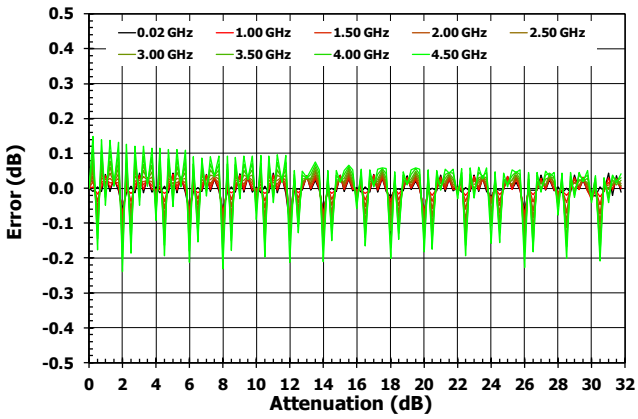


TYPICAL OPERATING CONDITIONS (- 3 -)

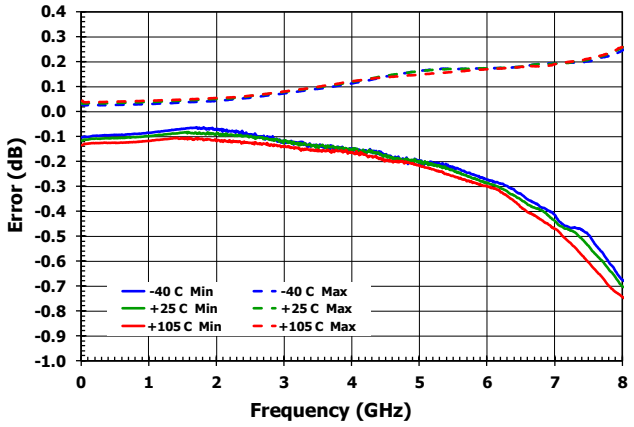
Worst Case Step Accuracy (LSB=0.25 dB)



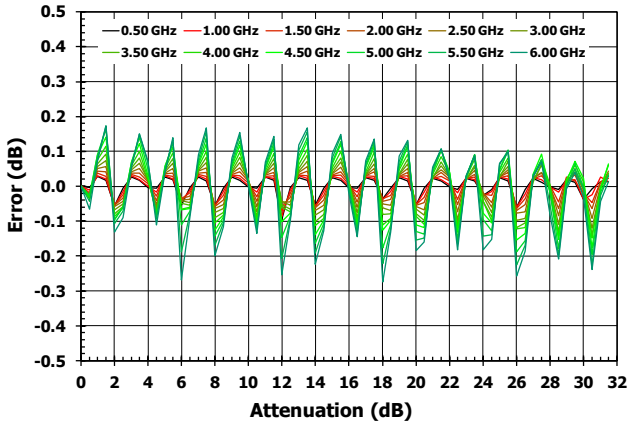
Step Accuracy (LSB=0.25 dB)



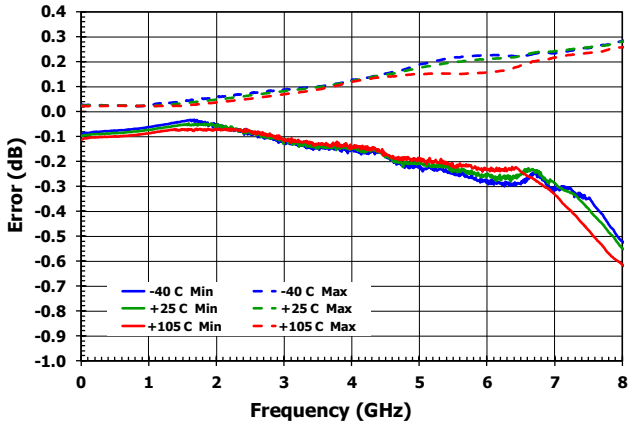
Worst Case Step Accuracy (LSB=0.50 dB)



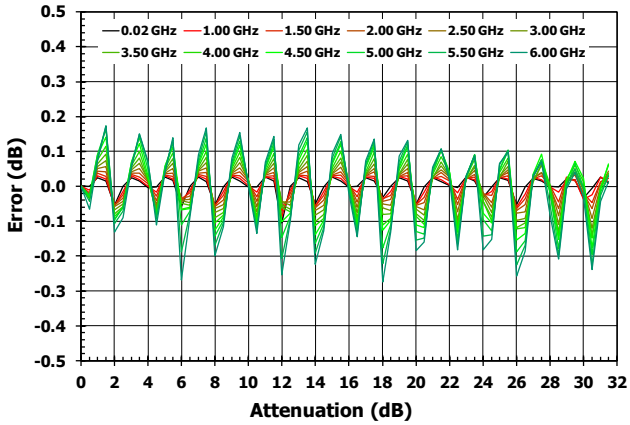
Step Accuracy (LSB=0.50 dB)



Worst Case Step Accuracy (LSB=1.00 dB)

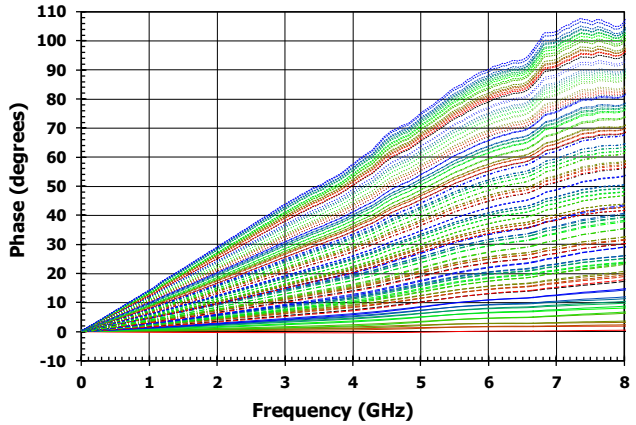


Step Accuracy (LSB=1.00 dB)

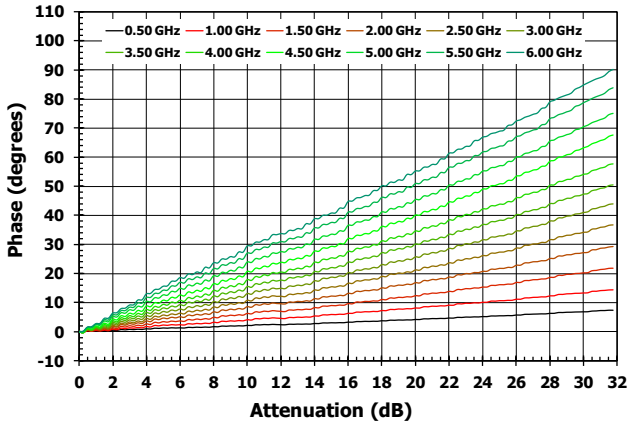


TYPICAL OPERATING CONDITIONS (- 4 -)

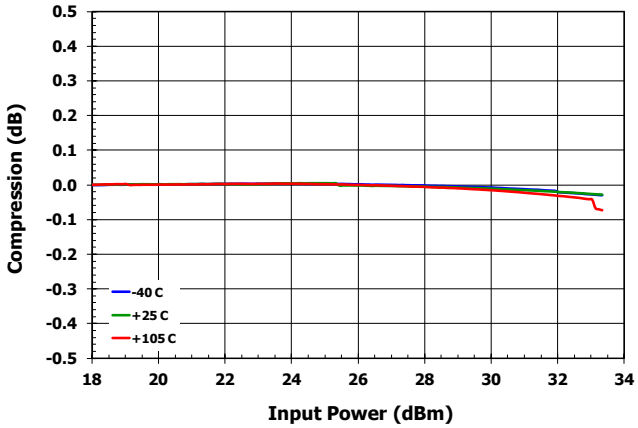
Relative Insertion Phase vs Frequency [All States]



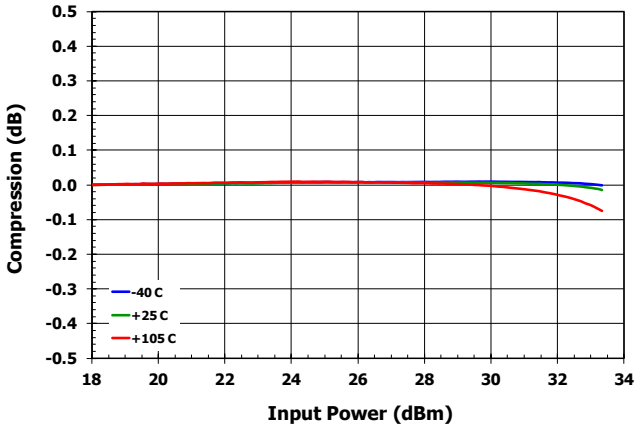
Relative Insertion Phase vs Attenuation



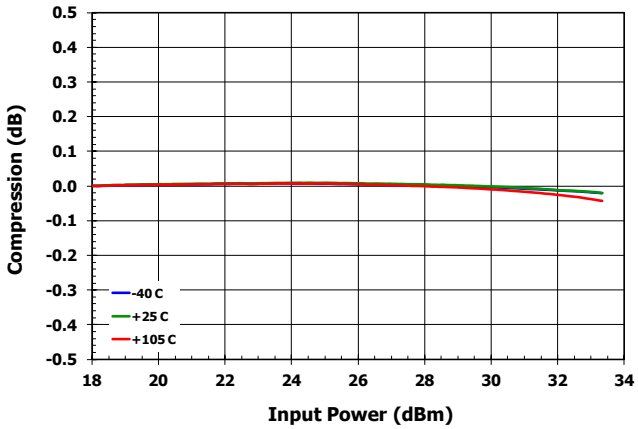
Input Compression (at 2 GHz, Attn=0 dB)



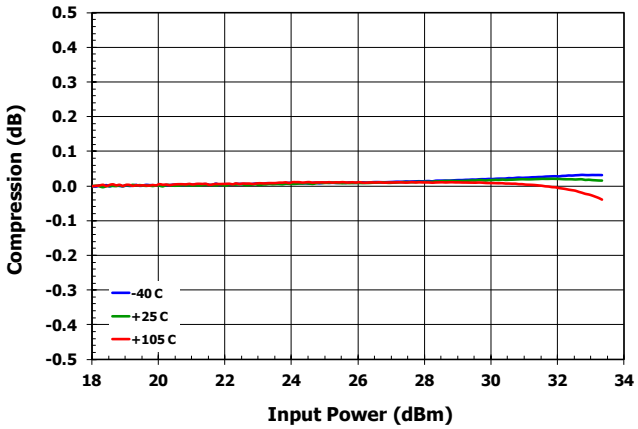
Input Compression (at 2 GHz, Attn=16 dB)



Input Compression (at 2 GHz, Attn=4 dB)

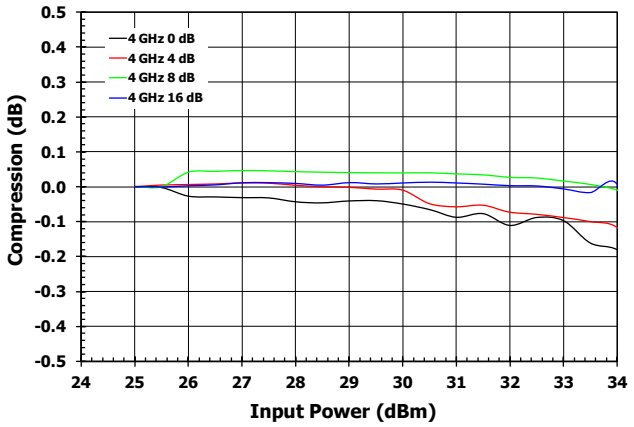


Input Compression (at 2 GHz, Attn=31.75 dB)

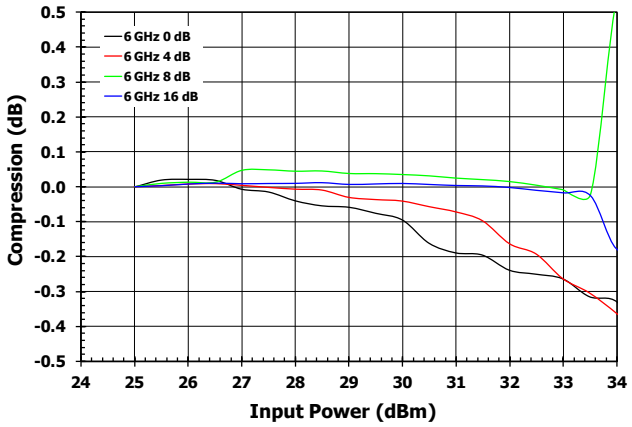


TYPICAL OPERATING CONDITIONS (- 5 -)

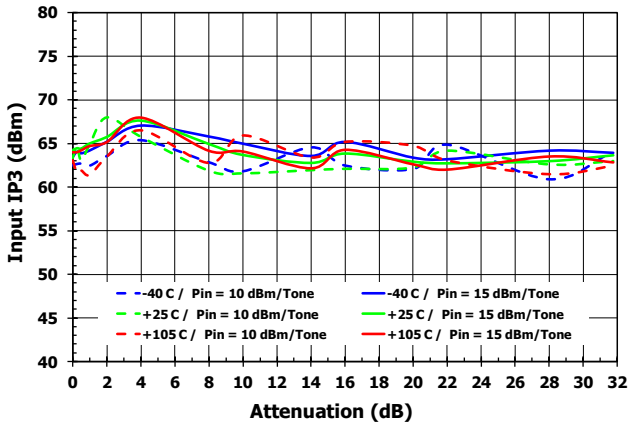
Input Compression (+25 °C, 4 GHz)



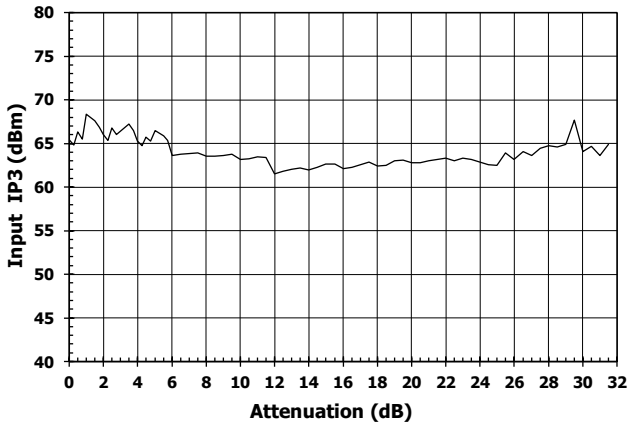
Input Compression (+25 °C, 6 GHz)



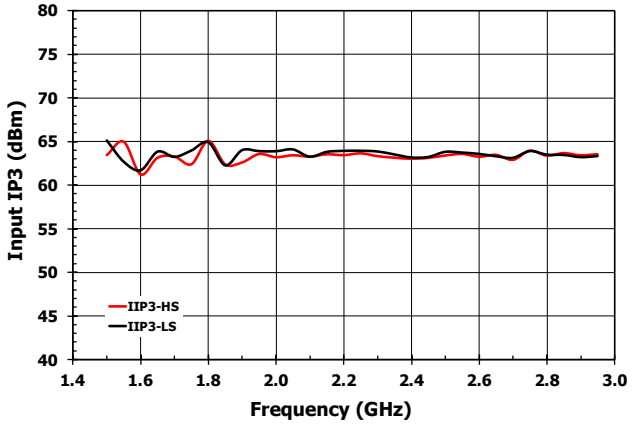
Input IP3 vs Attenuation [2 GHz]



Input IP3 vs Attenuation [3.92 GHz]

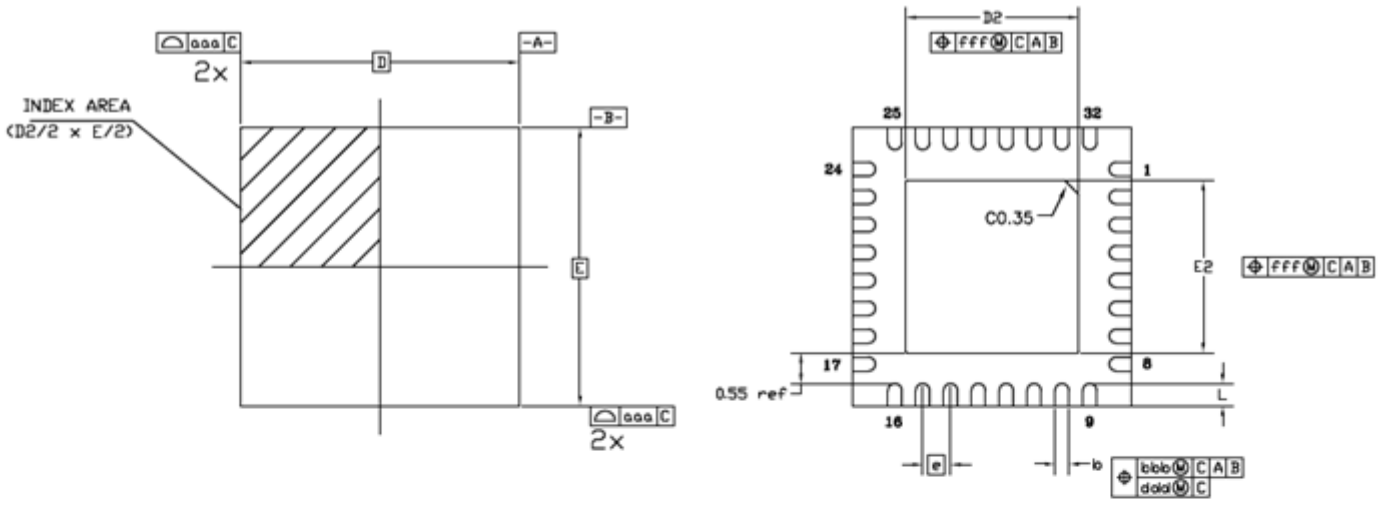


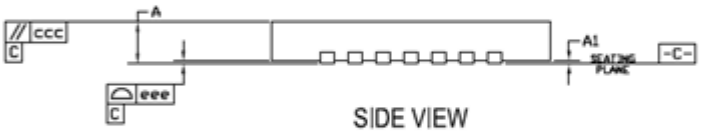
Input IP3 vs Frequency [Attn=0 dB, Pin=+22 dBm]



PACKAGE DRAWING

5mm x 5mm 32-pin TQFN), Use Exposed PAD (EPAD) ***Option P1***





SYMBOL	DIMENSION		
	MIN	NOM	MAX
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

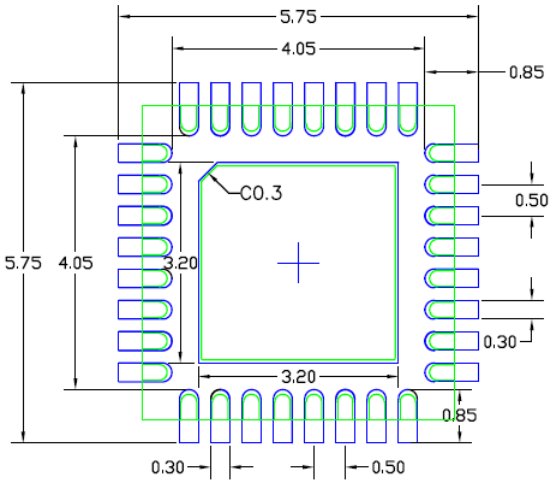
EPAD OPTION

SYMBOL	P1		
	MIN	NOM	MAX
E2	3.00	3.10	3.20
D2	3.00	3.10	3.20

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

LAND PATTERN DIMENSION

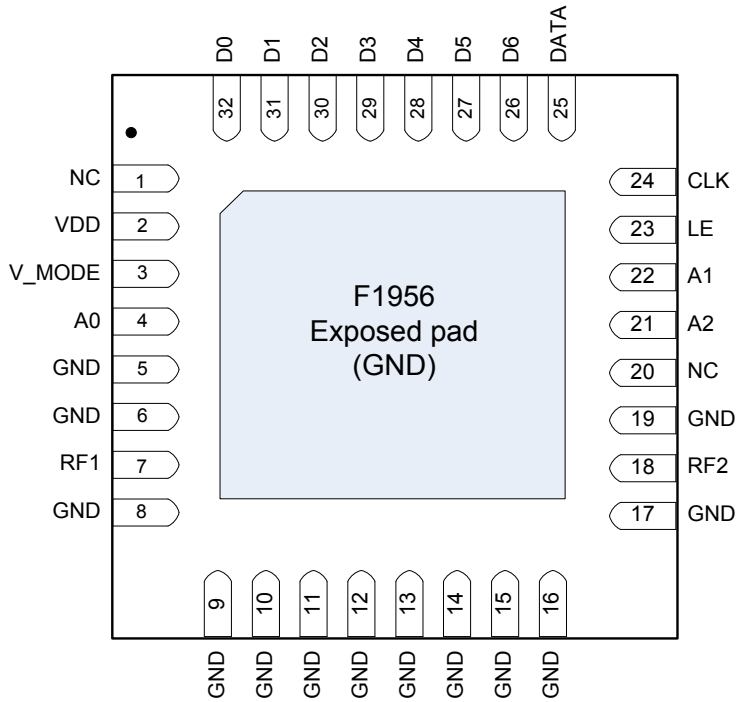


EPAD 3.1 mm SQ

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

PIN DIAGRAM

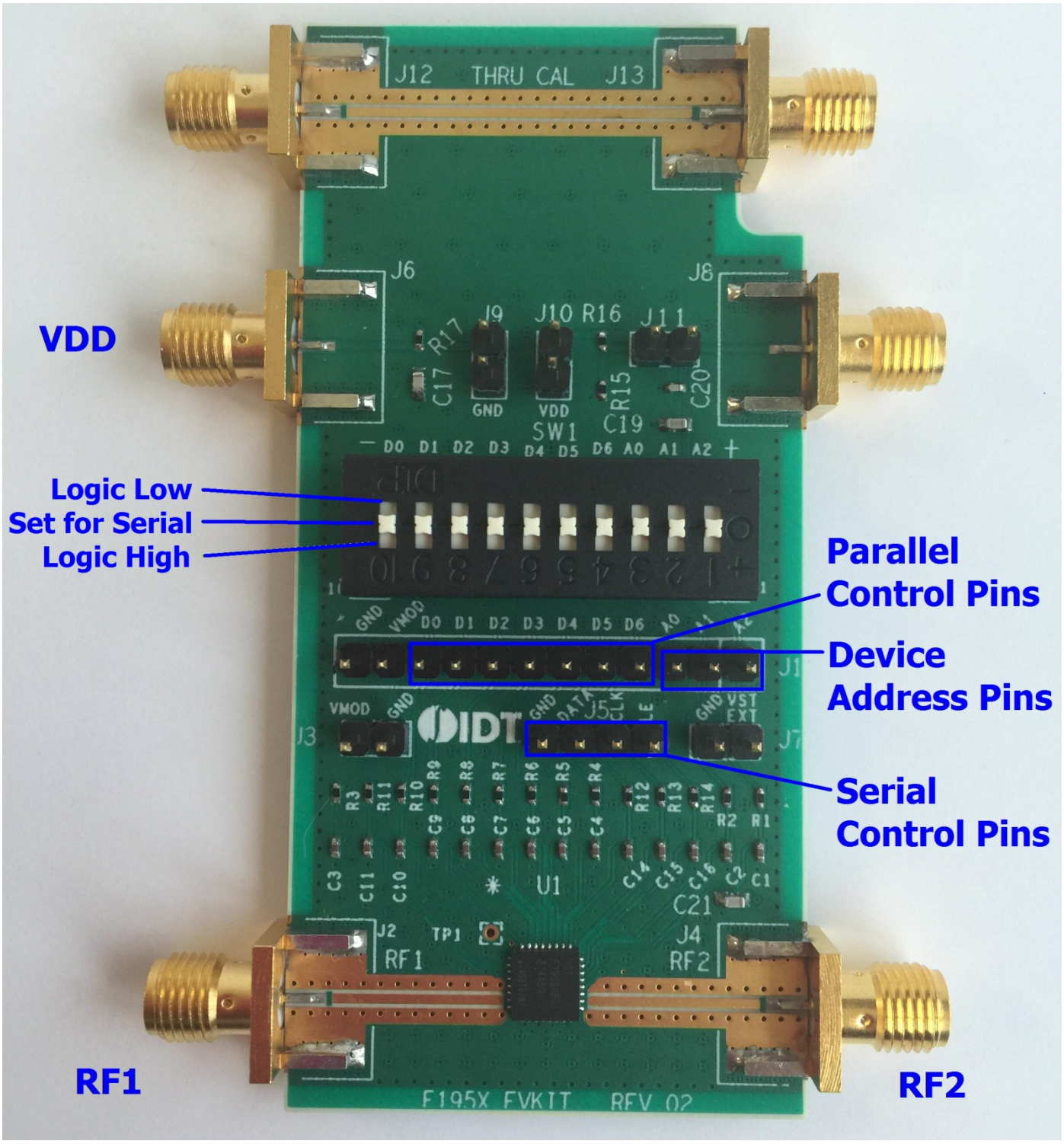
TOP View
(looking through the top of the package)



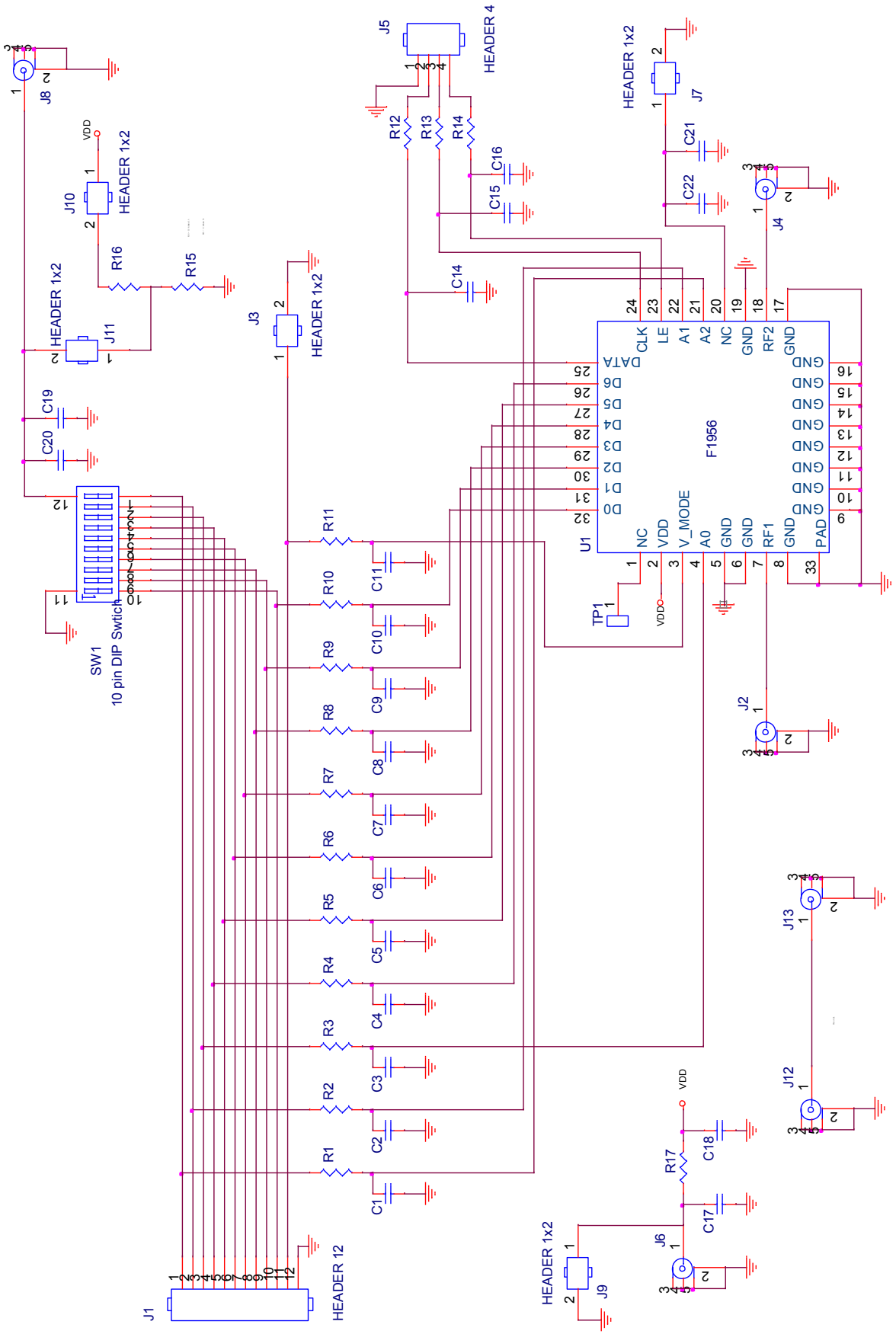
PIN DESCRIPTION

Pin	Name	Function
1	DNC	**This pin must be left open.**
2	VDD	Main Supply. Use 3.3 V or 5 V. Bypass capacitor as close to pin as possible.
3	V_{MODE}[1]	Logic low for parallel mode. Logic high or NC for serial mode.
4	A0[2]	Address bit A0 connection.
5	GND	Connect directly to paddle ground or as close as possible to pin with thru via. This pin is not internally connected
6	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
7	RF1[3]	Device RF input or output (bi-directional). AC couple to this pin unless 0V DC.
8 – 17	GND	Connect each pin directly to paddle ground or as close as possible to pin with thru vias.
18	RF2[3]	Device RF input or output (bi-directional). AC couple to this pin unless 0V DC.
19	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
20	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
21	A2[2]	Address bit A2 connection
22	A1[2]	Address bit A1 connection.
23	LE[1]	Serial interface latch enable input.
24	CLK[1]	Serial interface clock input.
25	DATA[1]	Serial interface data input.
26	D6[1]	Parallel control bit, 16 dB. Ground pin if not used.
27	D5[1]	Parallel control bit, 8 dB. Ground pin if not used.
28	D4[1]	Parallel control bit, 4 dB. Ground pin if not used.
29	D3[1]	Parallel control bit, 2 dB. Ground pin if not used.
30	D2[1]	Parallel control bit, 1 dB. Ground pin if not used.
31	D1[1]	Parallel control bit, 0.5 dB. Ground pin if not used.
32	D0[1]	Parallel control bit, 0.25 dB. Ground pin if not used.
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal and RF performance.

EVKIT PICTURE



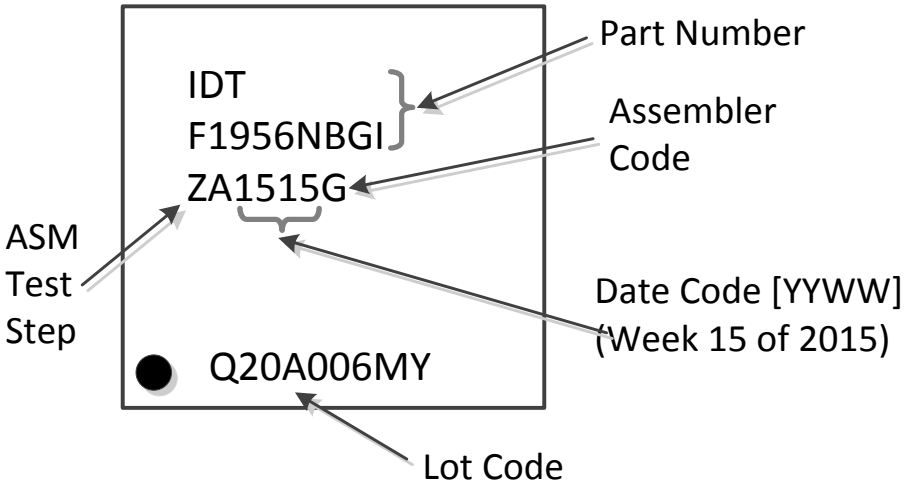
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM (REV 2)

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C1 - C11, C14, C15, C16	14	100 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
2	C18, C20, C22	3	1000 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
3	C17, C19, C21	3	10 nF ±5%, 50 V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	MURATA
4	R17	1	0 Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
5	R1 - R14	14	100 Ω ±1%, 1/10 W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
6	R15	1	6.98 kΩ ±5%, 1/10 W, Resistor (0402)	ERJ-2RKF6981X	PANASONIC
7	R16	1	10 kΩ ±1%, 1/10 W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
8	J3, J7, J9, J10, J11	5	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
9	J5	1	CONN HEADER VERT SGL 4 X 1 POS GOLD	961104-6404-AR	3M
10	J1	1	CONN HEADER VERT SGL 12 X 1 POS GOLD	961112-6404-AR	3M
11	J2, J4, J6, J8, J12, J13	6	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
12	SW1	1	SWITCH 10 POSITION DIP SWITCH	KAT1110E	E-Switch
13	U1	1	DSA	F1956	IDT
14		1	Printed Circuit Board	F1955 EVKit Rev 02	IDT

TOP MARKINGS



APPLICATIONS INFORMATION

Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Digital Pin Voltage & Resistance Values

The following table provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

Pin	Name	Open Circuit DC Voltage	Internal Connection
3	V_{MODE}	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
4, 21, 22	A0, A2, A1	0 V	100 kΩ resistor to GND
23, 24, 25	LE, CLK, DATA	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
26 – 32	D6 – D0	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V

REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
O	2015-May-22		Initial Release
1	2015-Sep-29	2	Datasheet Format Update Added Maximum Average Power Rating
2	2016-Apr-01		Maximum operating frequency changed to 6 GHz. Added curves showing performance at higher frequencies.

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