CONSTANT CURRENT LED DRIVER WITH DIGITAL AND PWM BRIGHTNESS CONTROL

FEATURES

- LED Driver With Integrated Overvoltage and Short-Circuit Protection
- 2.7-V to 6.0-V Input Voltage Range
- 500-mV/250-mV Feedback Voltage
- TPS61060 Powers Up to 3 LEDs
- TPS61061 Powers Up to 4 LEDs
- TPS61062 Powers Up to 5 LEDs
- PWM Brightness Control on Enable
- Digital Brightness Control on ILED
- 1.0-MHz Fixed Switching Frequency
- 400-mA Internal Power MOSFET Switch
- LEDs Disconnected During Shutdown
- Operates With Small-Output Capacitors Down to 220 nF
- Up to 80% Efficiency
- 8-Pin NanoFree™ Package (Chipscale, CSP)
- 3 × 3-mm QFN Package

APPLICATIONS

- White LED Driver
- Cellular Phones
- PDA, Pocket PC, and Smart Phones
- Digital Still Camera
- Handheld Devices

DESCRIPTION

The TPS61060/61/62 is a high-frequency, synchronous boost converter with constant current output to drive up to 5 white LEDs. For maximum safety, the device features integrated overvoltage and an advanced short-circuit protection when the output is shorted to ground. The device operates with 1-MHz fixed switching frequency to allow small external components and to simplify possible EMI problems. The device comes with three different overvoltage protection thresholds (14 V/18 V/23 V) to allow inexpensive and small-output capacitors with lower voltage ratings. The LED current is initially set with the external sense resistor Rs, and the feedback voltage is regulated to 500 mV or 250 mV, depending on the ILED pin configuration. Digital brightness control is implemented by applying a simple digital signal to the ILED pin. Alternatively, a PWM signal up to 1 kHz can be applied to the enable pin to control the LED brightness. During shutdown, the output is disconnected from the input to avoid leakage current through the LEDs.

TYPICAL APPLICATION

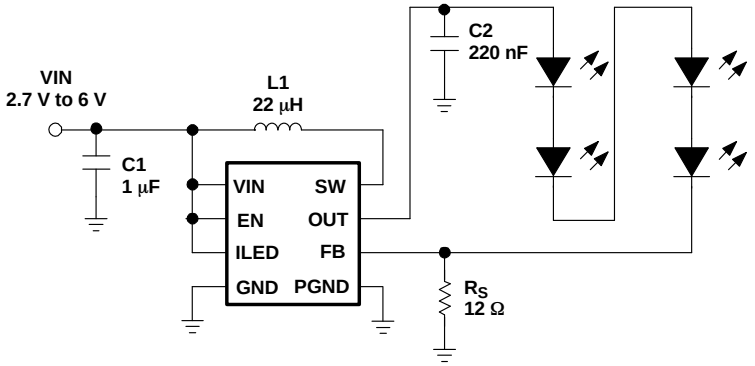


Figure 1.

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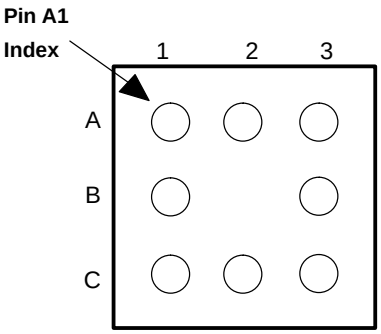
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

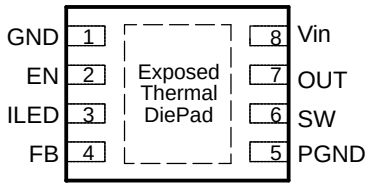
T_A	OVERVOLTAGE PROTECTION (OVP)	PACKAGE		PACKAGE MARKING	
		NanoFree	QFN	NanoFree(1)	QFN(2)
–40 to 85°C	14 V (min)	TPS61060YZF	TPS61060DRB	AKX	AQP
	18 V (min)	TPS61061YZF	TPS61061DRB	AKY	AQQ
	22.2 V (min)	TPS61062YZF	TPS61062DRB	AKZ	AQR

(1) The YZF package is available in tape and reel. Add R suffix (TPS61060YZFR) to order quantities of 3000 parts per reel or add T suffix (TPS61060YZFT) to order 250 parts per reel.
(2) The DRB package is available in tape and reel. Add R suffix (TPS61060DRBR) to order quantities of 3000 parts per reel.

8-Pin NanoFree Package
Top View



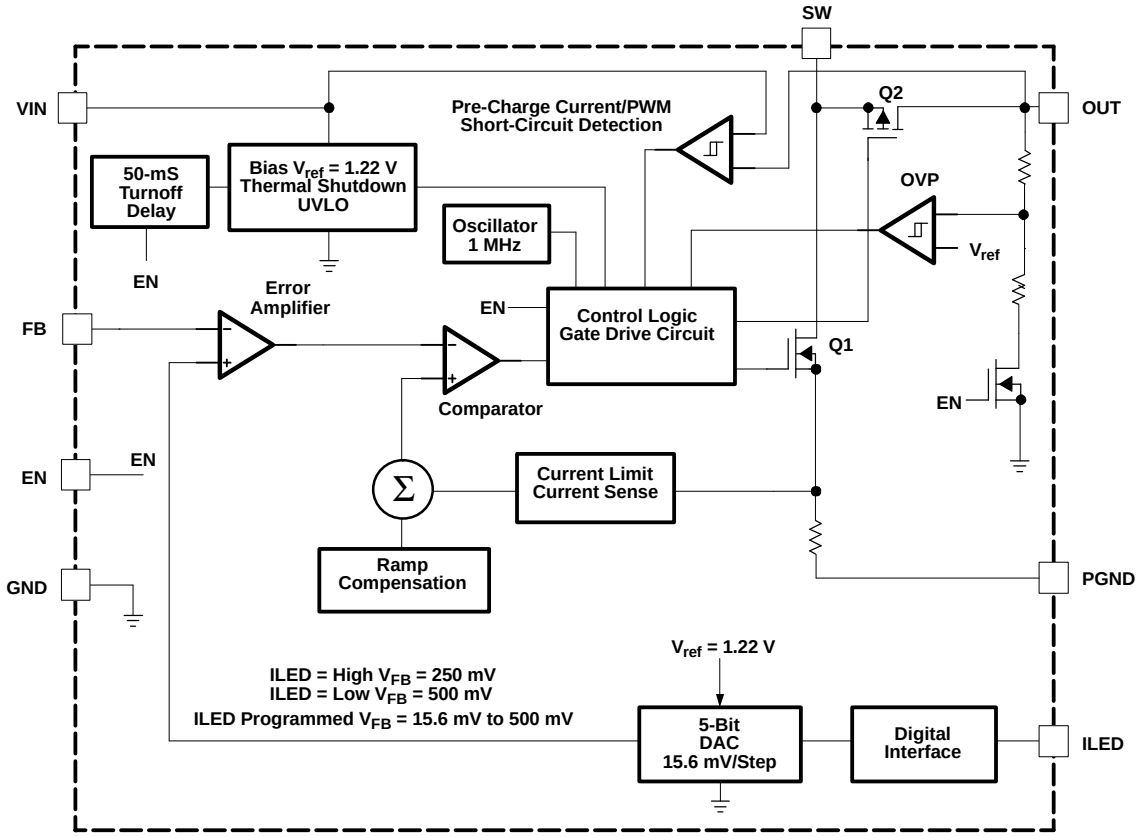
8-Pin 3x3-mm QFN Package
Top View



TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	CSP	QFN		
VIN	B1	8	I	Input supply pin of the device
EN	A2	2	I	Enable pin. This pin needs to be pulled high to enable the device. To allow brightness control of the LEDs a PWM signal up to 1 kHz can be applied. This pin has an internal pulldown resistor.
GND	A1	1		Analog ground
PGND	C3	5		Power ground
FB	B3	4	I	This is the feedback pin of the device. The feedback pin regulates the LED current through the sense resistor by regulating the voltage across Rs. The feedback voltage is set by the ILED pin. ILED=GND sets the feedback voltage to 500 mV. ILED=high sets the feedback voltage to 250 mV. Refer to digital brightness control section for more information.
OUT	C1	7	O	Output of the device
SW	C2	6	I	Switch pin of the device
ILED	A3	3	I	Digital brightness control input. When this pin is grounded the digital brightness control is disabled. When this pin is connected to high then the feedback voltage is reduced to typically 250 mV and the digital brightness control is enabled. Refer to digital brightness control section for more information.
PowerPAD™	–	–		The PowerPAD™ (exposed thermal diepad) is only available on the QFN package. The PowerPAD™ needs to be connected and soldered to analog ground (GND).

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
VIN(2)	Supply voltages on pin	–0.3 V to 7 V
EN, ILED, FB(2)	Voltages on pins	–0.3 V to 7 V
OUT(2)	Voltage on pin	33 V
SW(2)	Voltage on pin	33 V
	Continuous power dissipation	See Dissipation Rating Table
	Operating junction temperature range	–40°C to 150°C
	Storage temperature range	–55°C to 150°C
	Lead temperature (soldering, 10 sec)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \leq 25°C$ POWER RATING	$T_A = 70° C$ POWER RATING	$T_A = 85°C$ POWER RATING
QFN(1)	270°C/W	370 mW	204 mW	148 mW
QFN(2)	60°C/W	1.6W	916mW	666mW
CSP(3)	220°C/W	454 mW	250 mW	181 mW
CSP(4)	110°C/W	909 mW	500mW	363 mW

(1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad.
(2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad.
(3) R_θ is based on a 1-layer PCB according to JEDEC standard.
(4) R_θ is based on a 2-layer PCB according to JEDEC standard. Refer to application section on how to improve thermal resistance $R_{\theta JA}$.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_I	Input voltage range	2.7		6.0	V
L	Inductor(1)		22		µH
C_I	Input capacitor(1)		1		µF
C_O	Output capacitor(1)	0.22	1		µF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

(1) Refer to application section for further information

ELECTRICAL CHARACTERISTICS

V_{in} = 3.6 V, EN = V_{IN}, T_A= –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.7		6.0	V
I_Q	Operating quiescent current into Vin	Device not switching			1	mA
I_{SD}	Shutdown current	EN = GND		1	10	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		1.65	1.8	V
V_{HYS}	Undervoltage lockout hysteresis			50		mV
ENABLE AND ILED						
V_{EN}	Enable high-level voltage	V_{IN} = 2.7 V to 6.0 V	1.2			V
V_{EN}	Enable low-level voltage	V_{IN} = 2.7 V to 6.0 V			0.4	V
R_{EN}	Enable pulldown resistor		200	300		kΩ
t_{shtdn}	Enable-to-shutdown delay (1)	EN = high to low			50	ms
t_{PWML}	PWM low-level signal time (1)	PWM signal applied to EN			25	ms
V_{ILED}	ILED high-level voltage	V_{IN} = 2.7 V to 6.0 V	1.2			V
V_{ILED}	ILED low-level voltage	V_{IN} = 2.7 V to 6.0 V			0.4	V
I_{ILED}	ILED input leakage current	ILED = GND or VIN		0.1	3	µA
	DAC resolution	5 Bit		15.6		mV
tup	Increase feedback voltage one step	ILED = high to low	1		75	us
tdown	Decrease feedback voltage one step	ILED = high to low	180		300	us
tdelay	Delay time between up/down steps	ILED = low to high	1.5			us
toff	Digital programming off, VFB=500mV	ILED = high to low	720			us

(1) A PWM low signal applied to EN for a period of time (≥25 ms) could cause a device shutdown. After a period of ≥50 ms the device definitely enters shutdown mode.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK FB						
I_{FB}	Feedback input bias current	V_{FB} = 500 mV		1	1.5	uA
V_{FB}	Feedback regulation voltage	ILED = GND, after start-up	485	500	515	mV
V_{FB}	Feedback regulation voltage	ILED = High, after start-up	240	250	260	mV
POWER SWITCH SYNCHRONOUS RECTIFIER AND CURRENT LIMIT (SW)						
$r_{DS(ON)}$	P-channel MOSFET on-resistance	V_O = 10 V, Isw = 10 mA		2.5	3.7	Ω
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, Isw = 100 mA		0.6	0.9	Ω
	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 2.7 V, Isw = 100 mA		0.7	1.0	Ω
I_{swleak}	Switch leakage current	V_{IN} = V_{SW}=6.0 V, V_{OUT} = GND, EN=GND		0.1	2	µA
I_{SW}	N-Channel MOSFET current limit	V_O = 10 V	325	400	475	mA
OSCILLATOR						
f_s	Switching frequency		0.8	1.0	1.2	MHz
OUTPUT						
Vovp	Output overvoltage protection	V_O rising; TPS61060	14	14.5	16	V
Vovp	Output overvoltage protection	V_O rising; TPS61061	18	18.5	19.8	V
Vovp	Output overvoltage protection	V_O rising; TPS61062	22.2	23.5	25	V
Vovp	Output overvoltage protection hysteresis	TPS61060/61/62, V_O falling		0.7		V
Vo	Output voltage threshold for short-circuit detection	V_O falling		V_{IN}–0.7		V
Vo	Output voltage threshold for short-circuit detection	V_O rising		V_{IN}–0.3		V
Ipre	Pre-charge current and short circuit current	Start-up, EN = low to high, OUT = GND				mA
		V_{IN} = 6 V		180		
		V_{IN} = 3.6 V		95		
		V_{IN} = 2.7 V		65		
D	Maximum duty cycle			95%		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs LED current; 2 LEDs, ILED = high	2
		vs LED current; 3 LEDs, ILED = low	3
		vs LED current; 3 LEDs, ILED = high	4
		vs LED current; 4 LEDs, ILED = low	5
		vs LED current; 4 LEDs, ILED = high	6
		vs LED current; 5 LEDs, ILED = high	7
	PWM dimming		8
	Digital brightness control	Feedback voltage vs ILED programming step	9
	LED current	vs PWM duty cycle	10
	Soft-start operation		11
	Short-circuit protection		12
	Overvoltage protection		13
	Input voltage ripple		14

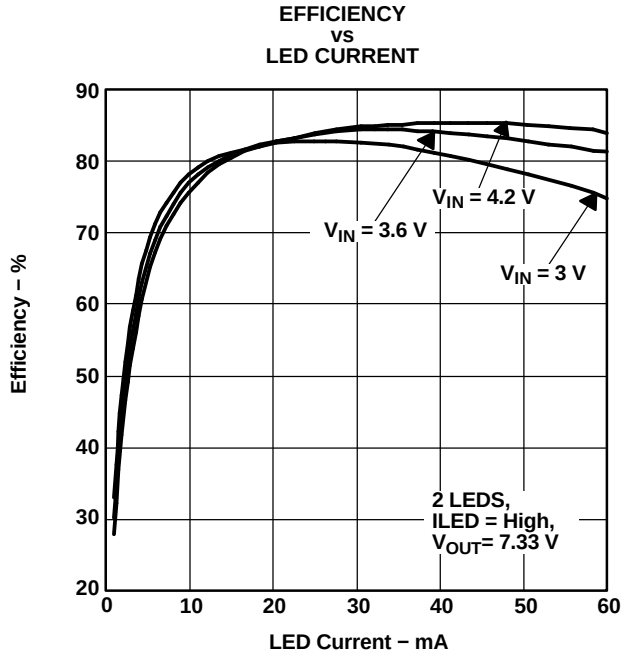


Figure 2.

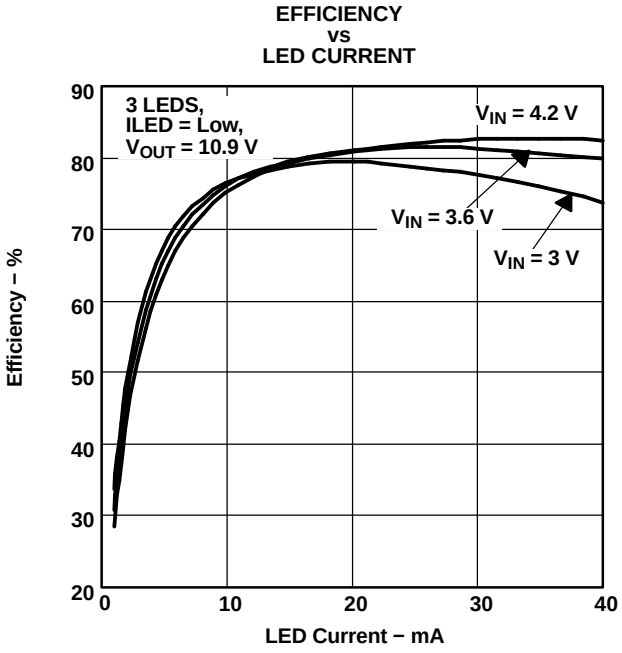


Figure 3.

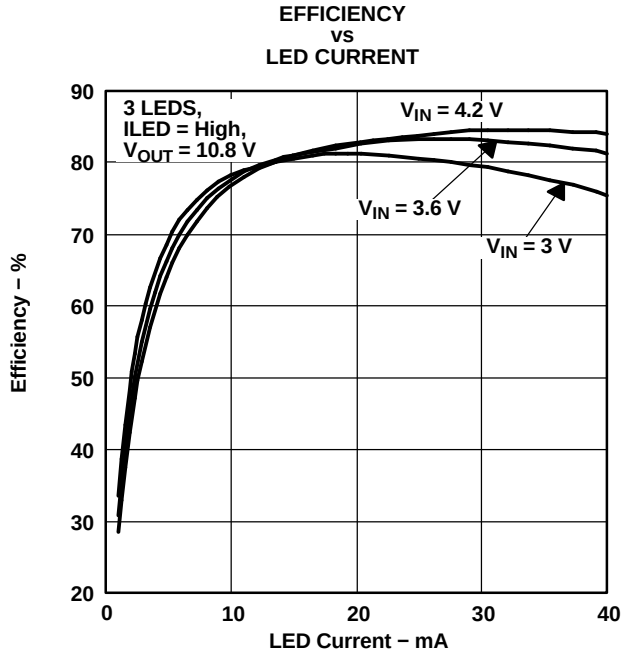


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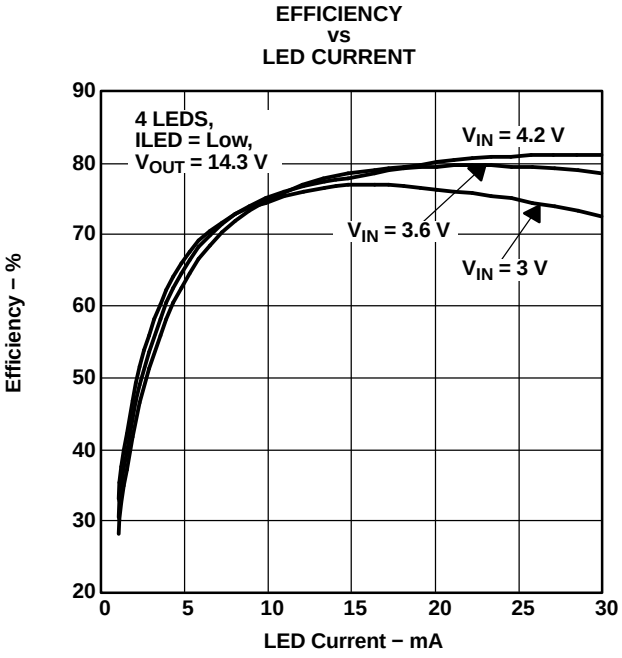


Figure 5.

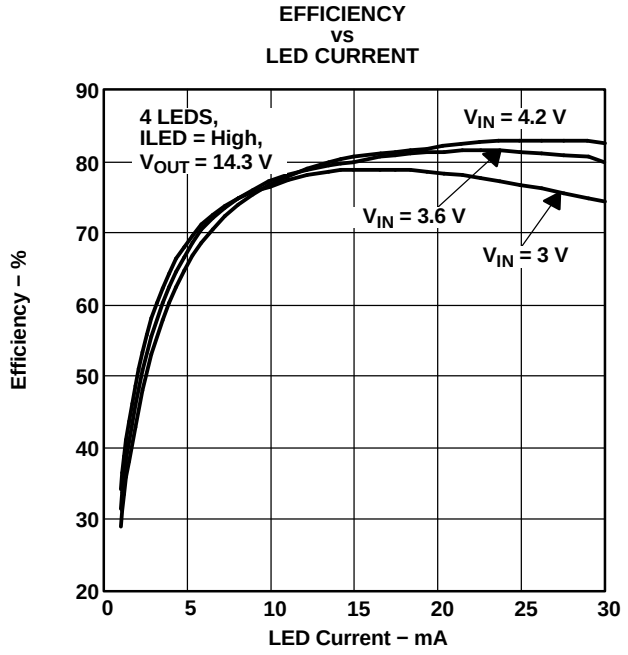


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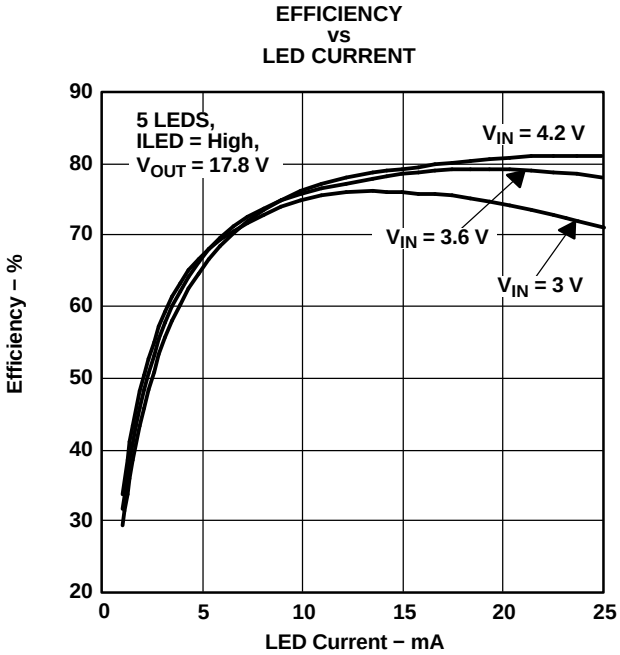


Figure 7.

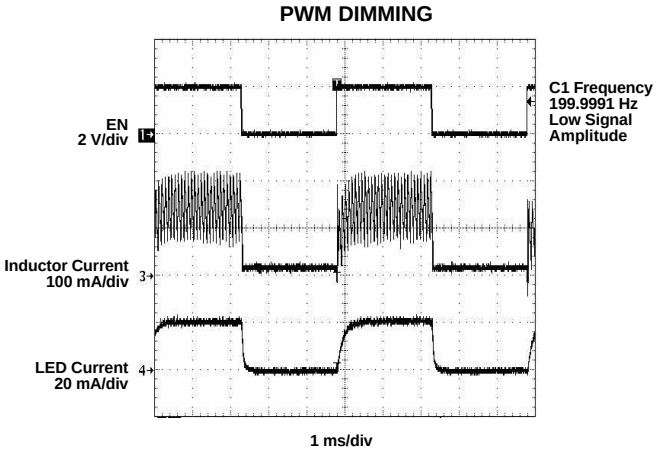


Figure 8.

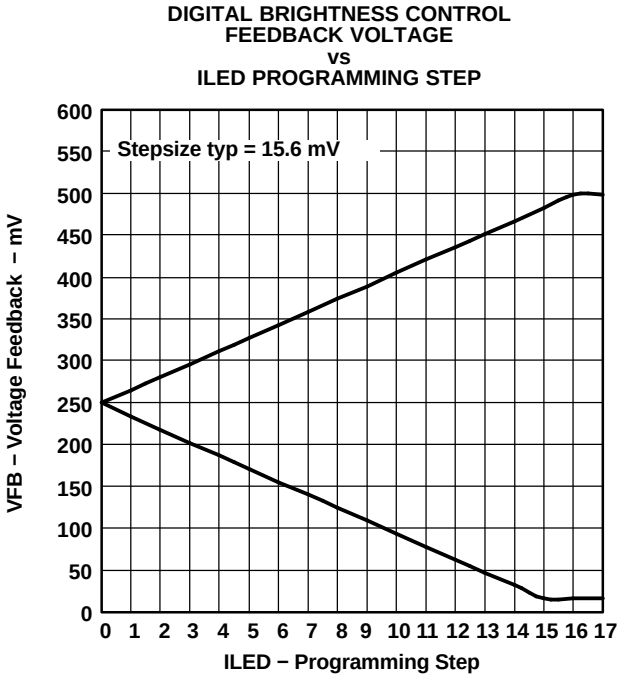


Figure 9.

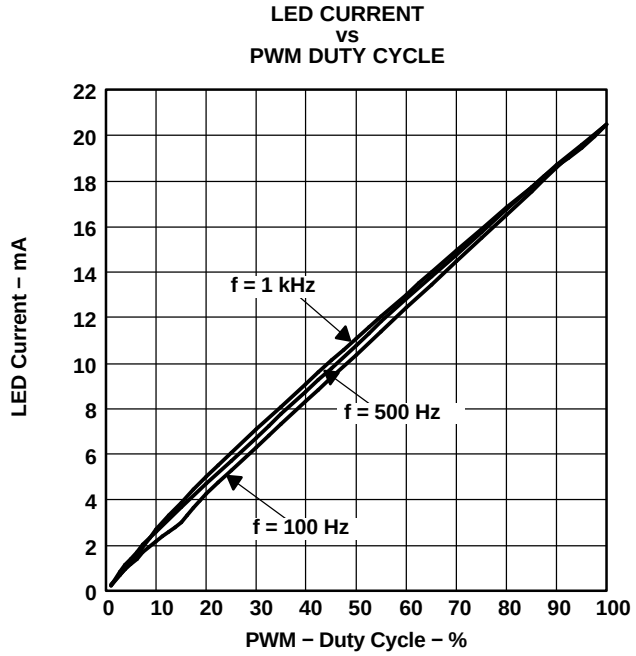


Figure 10.

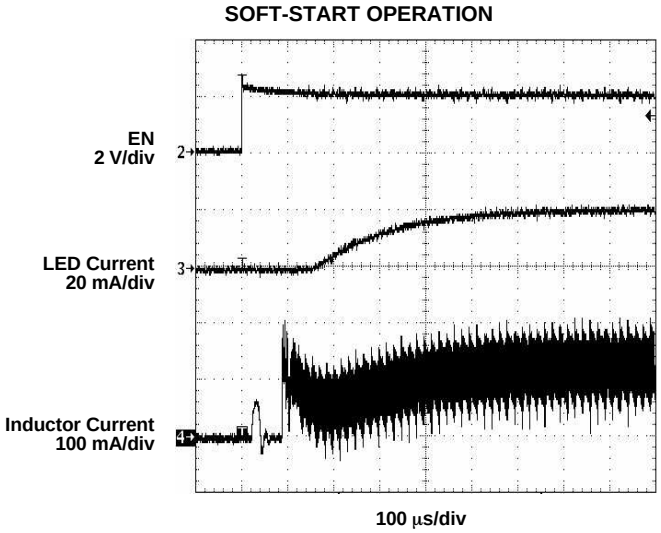


Figure 11.

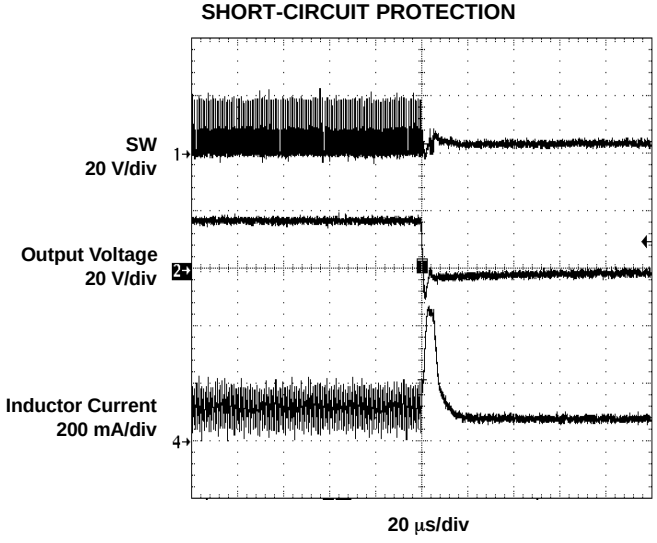


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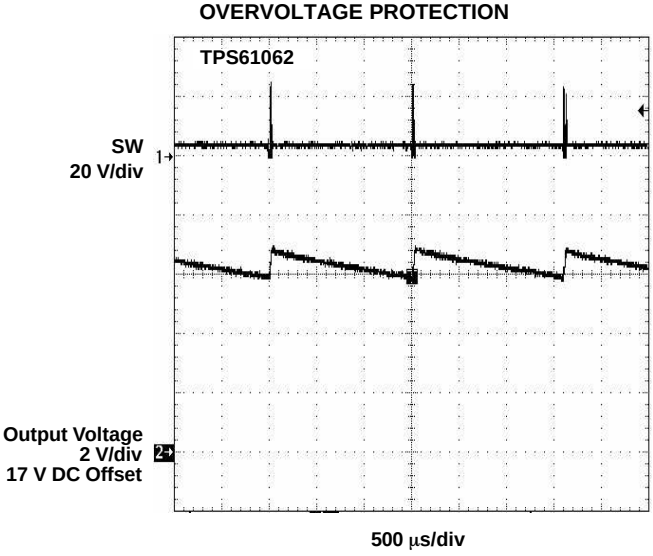


Figure 13.

INPUT VOLTAGE RIPPLE

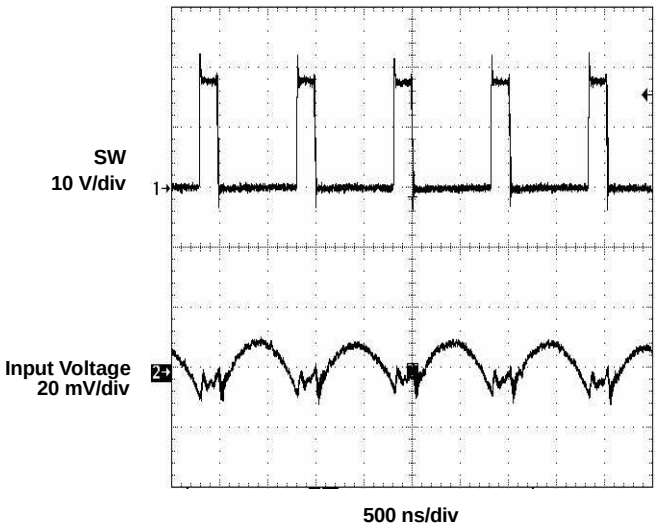


Figure 14.

DETAILED DESCRIPTION

OPERATION

The TPS61060/61/62 family is a constant-frequency, PWM current-mode converter with integrated N-channel MOSFET switch and synchronous P-channel MOSFET rectifier. The device operates in pulse width modulation (PWM) with a fixed switching frequency of 1 MHz. Operation is understood best by referring to the block diagram. The duty cycle of the converter is set by the error amplifier and the sawtooth ramp applied to the comparator. Because the control architecture is based on a current-mode control, a compensation ramp is added to allow stable operation for duty cycles larger than 50%. The converter is a fully integrated synchronous boost converter operating always in continuous conduction mode. This allows low noise operation and avoids ringing on the switch pin as it would be seen on a converter when entering discontinuous conduction mode.

START-UP

To avoid high inrush current during start-up, special care is taken to control the inrush current. When the device is first enabled, the output capacitor is charged with a constant precharge current of typically 100 mA until the output voltage is typically 0.3 V below Vin. The the device starts with a reduced analog controlled current limit for typically 40 µs. After this time period, the device enters its normal regulation with full current limit. The start-up current waveform is shown in Figure 11. The fixed precharge current during start-up allows the device to start up without problems when driving LEDs because the LED only starts to conduct current when the forward voltage is reached. If, for any reason a resistive load is driven, the maximum start-up load current needs to be smaller, or equal to, the precharge current.

SHORT-CIRCUIT PROTECTION

The TPS6106x family has an advanced short-circuit protection in case the output of the device is shorted to ground. Because the device is configured as a current source even when the LEDs are shorted, the maximum current is controlled by the sense resistor Rs. As an additional safety feature, the TPS6106x series also protects the device and inductor when the output is shorted to ground. When the output is shorted to ground, the device enters precharge mode and limits the maximum current to typically 100 mA.

DETAILED DESCRIPTION (continued)

OVERVOLTAGE PROTECTION (OVP)

As with any current source, the output voltage rises when the output gets high impedance or disconnected. To prevent the output voltage exceeding the maximum switch voltage rating (33 V) of the main switch, an overvoltage protection circuit is integrated. As soon as the output voltage exceeds the OVP threshold, the converter stops switching and the output voltage falls down. When the output voltage falls below the OVP threshold, the converter continues operation until the output voltage exceeds the OVP threshold again. To allow the use of inexpensive low-voltage output capacitors, the TPS6106x series has different OVP levels that need to be selected according to the number of external LEDs and their maximum forward voltage.

ENABLE PWM DIMMING

The enable pin allows disabling and enabling of the device as well as brightness control of the LEDs by applying a PWM signal up to typically 1 kHz. When a PWM signal is applied, the LED current is turned on when the EN is high and off when EN is pulled low. Changing the PWM duty cycle therefore changes the LED brightness. To allow higher PWM frequencies on the enable pin, the device continues operation when a PWM signal is applied. As shown in the block diagram, the EN pin needs to be pulled low for at least 50 ms to fully turn the device off. The enable input pin has an internal 300-kΩ pulldown resistor to disable the device when this pin is floating.

DIGITAL BRIGHTNESS CONTROL (ILED)

The ILED pin features a simple digital interface to allow digital brightness control. This can save processor power and battery life. Using the digital interface to control the LED brightness does not required a PWM signal all the time, and the processor can enter sleep mode if available. To save signal lines, the ILED pin can be connected to the enable pin to allow digital programming and enable/disable function at the same time with the same signal. Such a circuit is shown in Figure 22.

The ILED pin basically sets the feedback regulation voltage (V_{FB}); thus, it sets the LED current. When the ILED pin is connected to GND, the digital brightness control is disabled and the feedback is regulated to V_{FB} = 500 mV. When the ILED pin is pulled high, the digital brightness control is enabled starting at its midpoint where the feedback is regulated to V_{FB} = 250 mV. The digital brightness control is implemented by adjusting the feedback voltage in digital steps with a typical maximum voltage of V_{FB} = 500 mV. For this purpose, a 5-bit DAC is used giving 32 steps equal to a 15.6-mV change in feedback voltage per step. To increase or decrease the internal reference voltage, the ILED pin needs to be pulled low over time as outlined in Table 1 and specified in the electrical table. When the internal DAC is programmed to its highest or lowest value, it stays at this value until it gets programmed in the opposite direction again.

Table 1. Increase/Decrease Internal Reference Voltage

FEEDBACK VOLTAGE	TIME	ILED LOGIC LEVEL
Increase	1 µs to 75 µs	Low
Decrease	180 µs to 300 µs	Low
Brightness control disabled	≥550 µs	Low
Delay between steps	1.5 µs	High

Between each cycle the ILED pin needs to be pulled high for 1.5 µs.

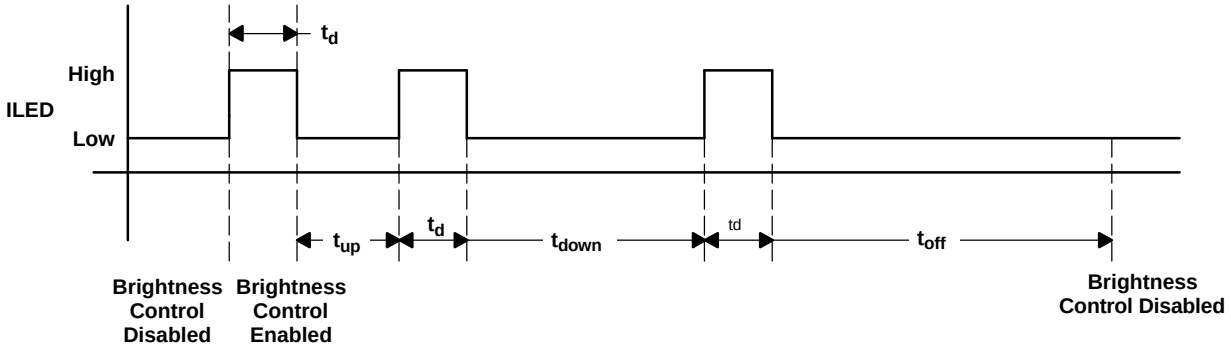


Figure 15. ILED Timing Diagram

Using the digital interface on the ILED pin allows simple implementation of a two-step brightness control by pulling the ILED either high or low. For full LED current with V_{FB} = 500 mV, the ILED needs to be pulled low and to program half the LED current with V_{FB} = 250 mV, the ILED pin needs to be pulled high.

EFFICIENCY AND FEEDBACK VOLTAGE

The feedback voltage has a direct effect on the converter efficiency. Because the voltage drop across the feedback resistor does not contribute to the output power (LED brightness), the lower the feedback voltage the higher the efficiency. Especially when powering only three or less LEDs, the feedback voltage impacts the efficiency around 2% depending on the sum of the forward voltage of the LEDs. To take advantage of this, the ILED pin can be connected to VIN, setting the feedback voltage to 250 mV.

UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents mis-operation of the device at input voltages below typical 1.65 V. When the input voltage is below the undervoltage threshold the device remains off and both internal MOSFETs are turned off providing isolation between input and output.

THERMAL SHUTDOWN

An internal thermal shutdown is implemented and turns off the internal MOSFETs when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

CHIPSCALE PACKAGE DIMENSIONS

The TPS6106x is available in Chipscale package and has the following mechanical dimensions: E=D=1.446mm (typ), E=D=1.424mm (min), E=D=1.5mm (max). Please refer to mechanical drawing of the package (YZF).

APPLICATION INFORMATION

INDUCTOR SELECTION

The device requires typically a 22-µH or 10-µH inductance. When selecting the inductor, the inductor saturation current should be rated as high as the peak inductor current at maximum load, and respectively, maximum LED current. Because of the special control loop design, the inductor saturation current does not need to be rated for the maximum switch current of the converter. The maximum converter switch current usually is not reached even when the LED current is pulsed by applying a PWM signal to the enable pin. The maximum inductor peak current, as well as LED current, is calculated as:

$$\text{Duty Cycle}: \ D = 1 - \frac{Vin}{Vout} \tag{1}$$

$$\text{Maximum LED current}: \ I_{LED} = \left(Isw - \frac{Vin \times D}{2 \times fs \times L} \right) \times (1 - D) \times \eta \tag{2}$$

$$\text{Inductor peak current}: \ i_{Lpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{LED}}{(1 - D) \times \eta} \tag{3}$$

with:

fs = Switching frequency (1 MHz typ)

L = Inductor value

η = Estimated converter efficiency (0.75)

Isw = Minimum N-channel MOSFET current limit (325 mA)

Using the expected converter efficiency is a simple approach to calculate maximum possible LED current as well as peak inductor current. The efficiency can be estimated by taking the efficiency numbers out of the provided efficiency curves or to use a worst-case assumption for the expected efficiency, e.g., 75%.

EFFICIENCY

The overall efficiency of the application depends on the specific application conditions and mainly on the selection of the inductor. A physically smaller inductor usually shows lower efficiency due to higher switching losses of the inductor (core losses, proximity losses, skin effect losses). A trade-off between physical inductor size and overall efficiency has to be made. The efficiency can typically vary around ±5% depending on the selected inductor. Figures 2 to 7 can be used as a guideline for the application efficiency. These curves show the typical efficiency with a 22 µH inductor (muRata LQH32CN220K23). Figure 23 shows a basic setup where the efficiency is taken/measured as:

$$\eta = \frac{V_{LED} \times I_{LED}}{V_{in} \times I_{in}} \tag{4}$$

Table 2. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS
10 µH	TDK VLF3012AT-100MR49	2,6 mm × 2,8 mm × 1,2 mm
10 µH	Murata LQH32CN100K53	3,2 mm × 2,5 mm × 1,55 mm
10 µH	Murata LQH32CN100K23	3,2 mm × 2,5 mm × 2,0 mm
22 µH	TDK VLF3012AT-220MR33	2,6 mm × 2,8 mm × 1,2 mm
22 µH	Murata LQH32CN220K53	3,2 mm × 2,5 mm × 1,55 mm
22 µH	Murata LQH32CN220K23	3,2 mm × 2,5 mm × 2,0 mm

OUTPUT CAPACITOR SELECTION

The device is designed to operate with a fairly wide selection of ceramic output capacitors. The selection of the output capacitor value is a trade-off between output voltage ripple and capacitor cost and form factor. In general, capacitor values of 220 nF up to 4.7 µF can be used. When using a 220-nF output capacitor, it is recommended

to use X5R or X7R dielectric material to avoid the output capacitor value falling far below 220 nF over temperature and applied voltage. For systems with wireless or RF sections, EMI is always a concern. To minimize the voltage ripple in the LED string and board traces, the output capacitor needs to be connected directly from the OUT pin of the device to ground rather than across the LEDs. A larger output capacitor value reduces the output voltage ripple. Table 3 shows possible input and/or output capacitors.

INPUT CAPACITOR SELECTION

For good input voltage filtering low ESR ceramic capacitors are recommended. A 1-µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering and EMI reduction this value can be increased. The input capacitor should be placed as close as possible to the input pin of the converter. Table 3 shows possible input and/or output capacitors.

Table 3. Capacitor Selection

CAPACITOR	VOLTAGE RATING	FORM FACTOR	COMPONENT SUPPLIER(1)	COMMENTS
INPUT CAPACITOR				
1 µF	10 V	0603	Tayo Yuden LMK107BJ105	
OUTPUT CAPACITOR				
220 nF	16 V	0603	Tayo Yuden EMK107BJ224	TPS61060
220 nF	50 V	0805	Tayo Yuden UMK212BJ224	TPS61060/61/62
470 nF	35 V	0805	Tayo Yuden GMK212BJ474	TPS61060/61/62
1 µF	16 V	0805	Tayo Yuden EMK212BJ105	TPS61060
1 µF	35 V	1206	Tayo Yuden GMK316BJ105	TPS61060/61/62
1 µF	25 V	1206	TDK C3216X7R1E105	TPS61060/61/62

(1) Similar capacitors are also available from TDK and other suppliers.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter. The input capacitor should be placed as close as possible to the input pin for good input voltage filtering. The inductor should be placed as close as possible to the switch pin to minimize the noise coupling into other circuits. The output capacitor needs to be placed directly from the OUT pin to GND rather than across the LEDs. This reduces the ripple current in the trace to the LEDs. The GND pin needs to be connected directly to the PGND pin. When doing the PCB layout, the bold traces (Figure 16) should be routed first, as well as placement of the inductor, input and output capacitors.

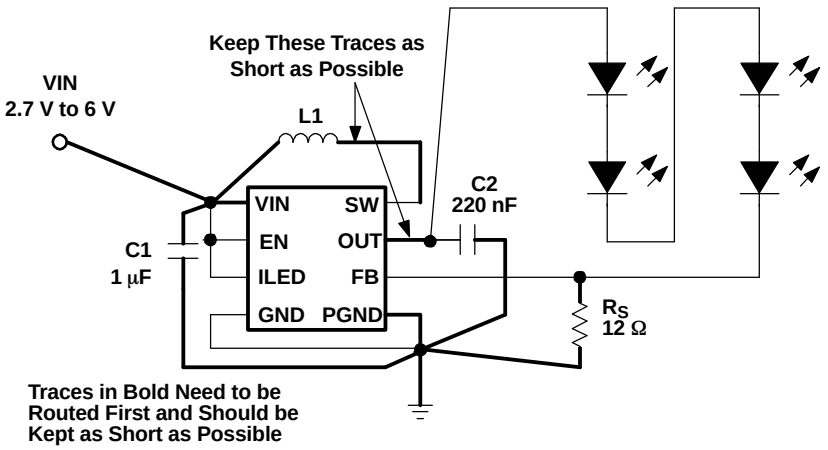


Figure 16. Layout Considerations

THERMAL CONSIDERATIONS

The TPS6106x comes in a thermally enhanced QFN package. The package includes a thermal pad that improves the thermal capabilities of the package. Also see QFN/SON PCB Attachment Application Note (SLUA271). The thermal resistance junction-to-ambient $R_{\theta JA}$ of the QFN package greatly depends on the PCB layout. Using thermal vias and wide PCB traces improves the thermal resistance $R_{\theta JA}$. The thermal pad needs to be soldered to analog ground on the PCB.

For the NanoFree package, similar guidelines apply as for the QFN package. The thermal resistance $R_{\theta JA}$ depends mainly on the PCB layout.

TYPICAL APPLICATIONS

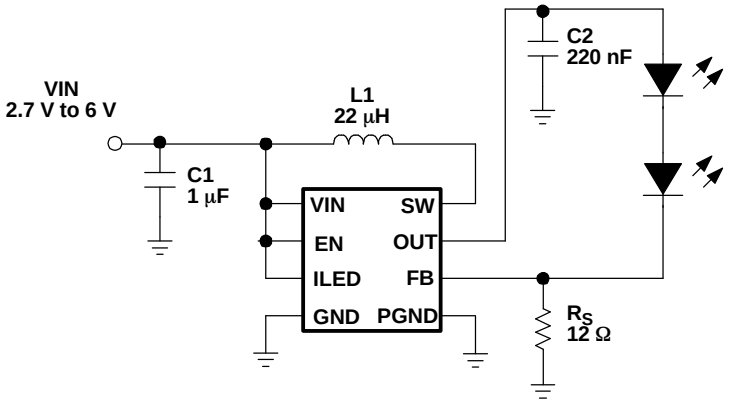


Figure 17. TPS61060 Powering Two White LEDs

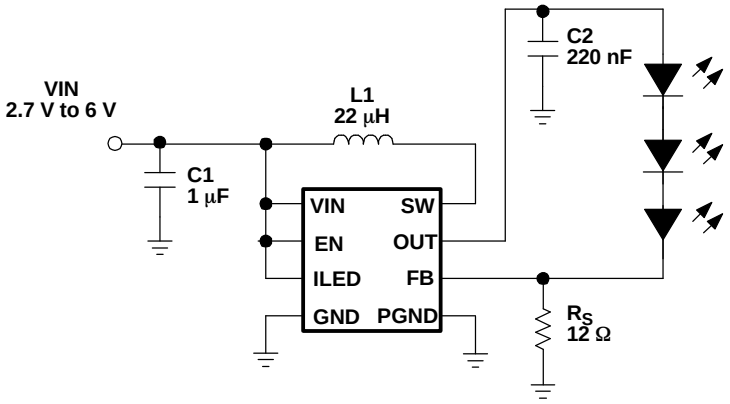


Figure 18. TPS61060 Powering Three White LEDs

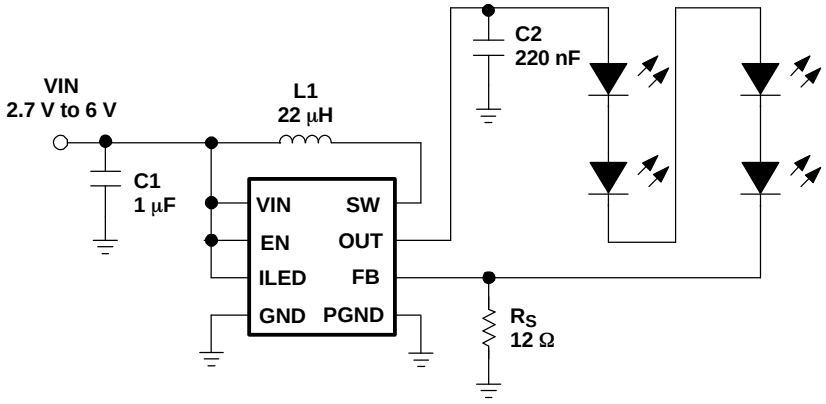


Figure 19. TPS61061 Powering Four White LEDs

TYPICAL APPLICATIONS (continued)

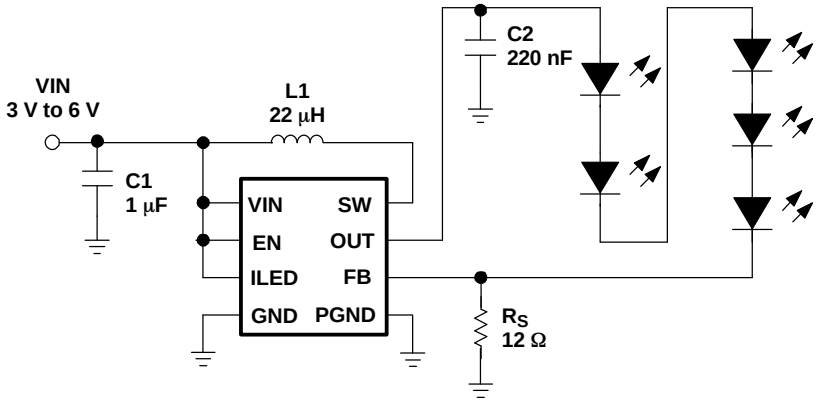


Figure 20. TPS61062 Powering Five White LEDs

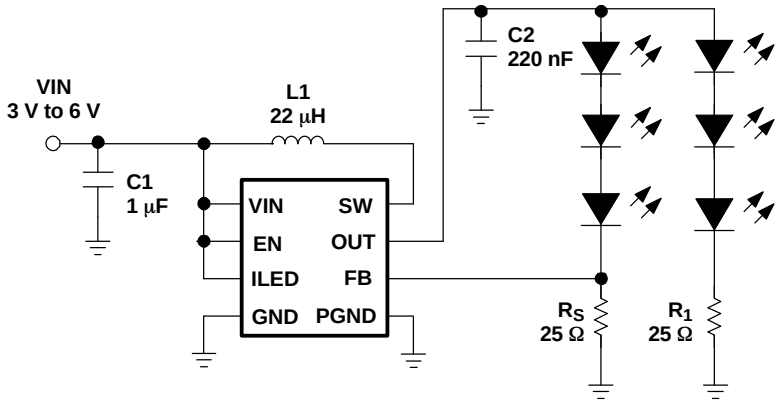


Figure 21. TPS61060 Powering Six White LEDs

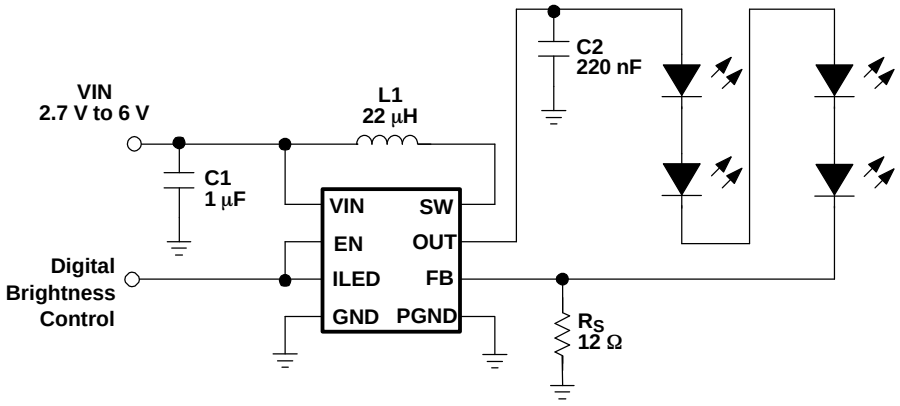


Figure 22. TPS61061 Digital Brightness Control(2)

(2) This circuit combines the enable with the digital brightness control pin, allowing the digital signal applied to ILED to also enable and disable the device.

TYPICAL APPLICATIONS (continued)

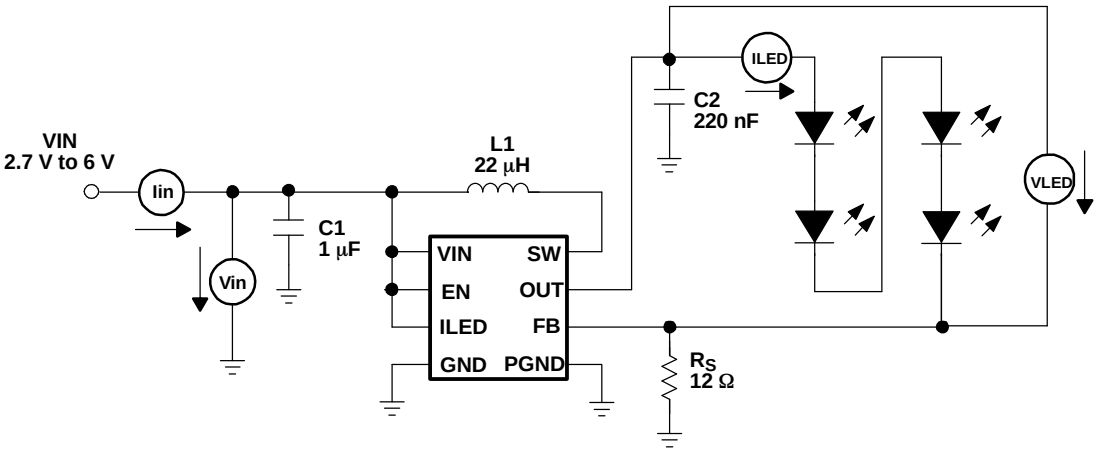


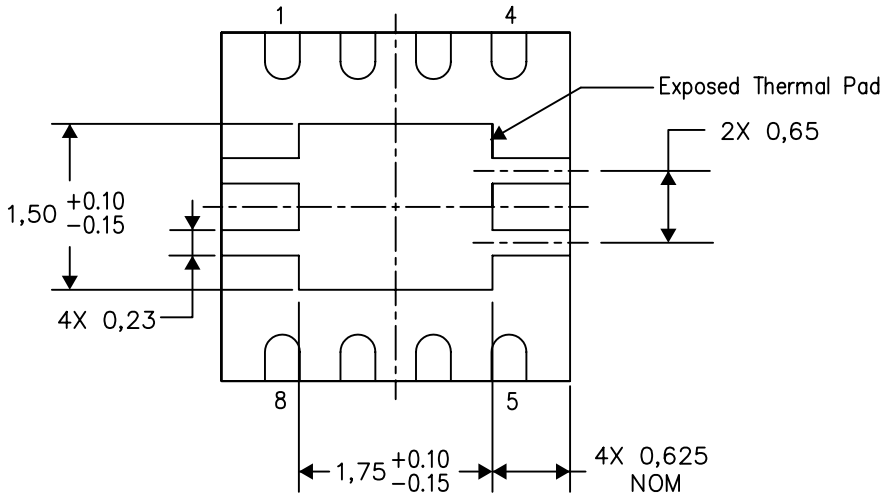
Figure 23. Efficiency Measurement Setup

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

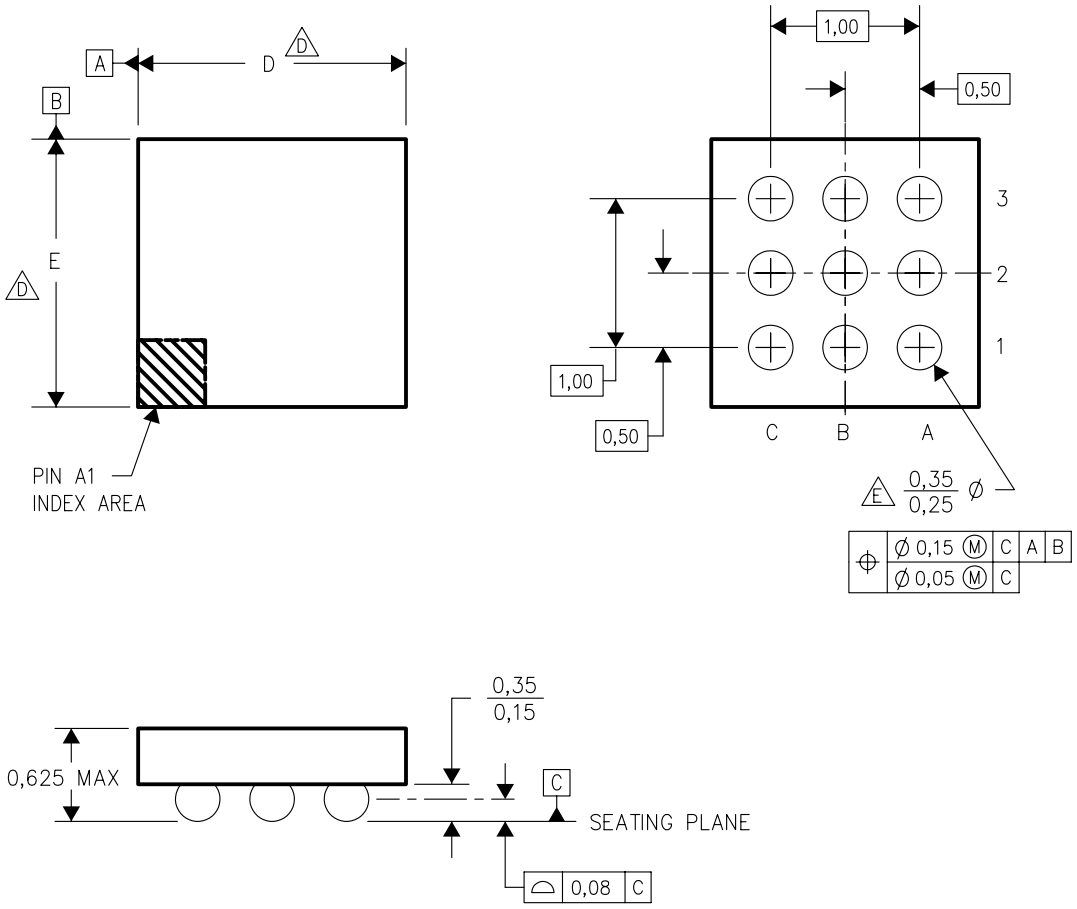


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



4205058–3/D 10/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZF package can have dimension D ranging from 1.35 to 2.15 mm and dimension E ranging from 1.35 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEF (Drawing #4204181) for tin–lead (SnPb) balls.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS61060DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61060DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61060YZFR	ACTIVE	DSBGA	YZF	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS61060YZFT	ACTIVE	DSBGA	YZF	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS61061DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61061DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61061YZFR	ACTIVE	DSBGA	YZF	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS61061YZFT	ACTIVE	DSBGA	YZF	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS61062DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61062DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61062YZFR	ACTIVE	DSBGA	YZF	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS61062YZFT	ACTIVE	DSBGA	YZF	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

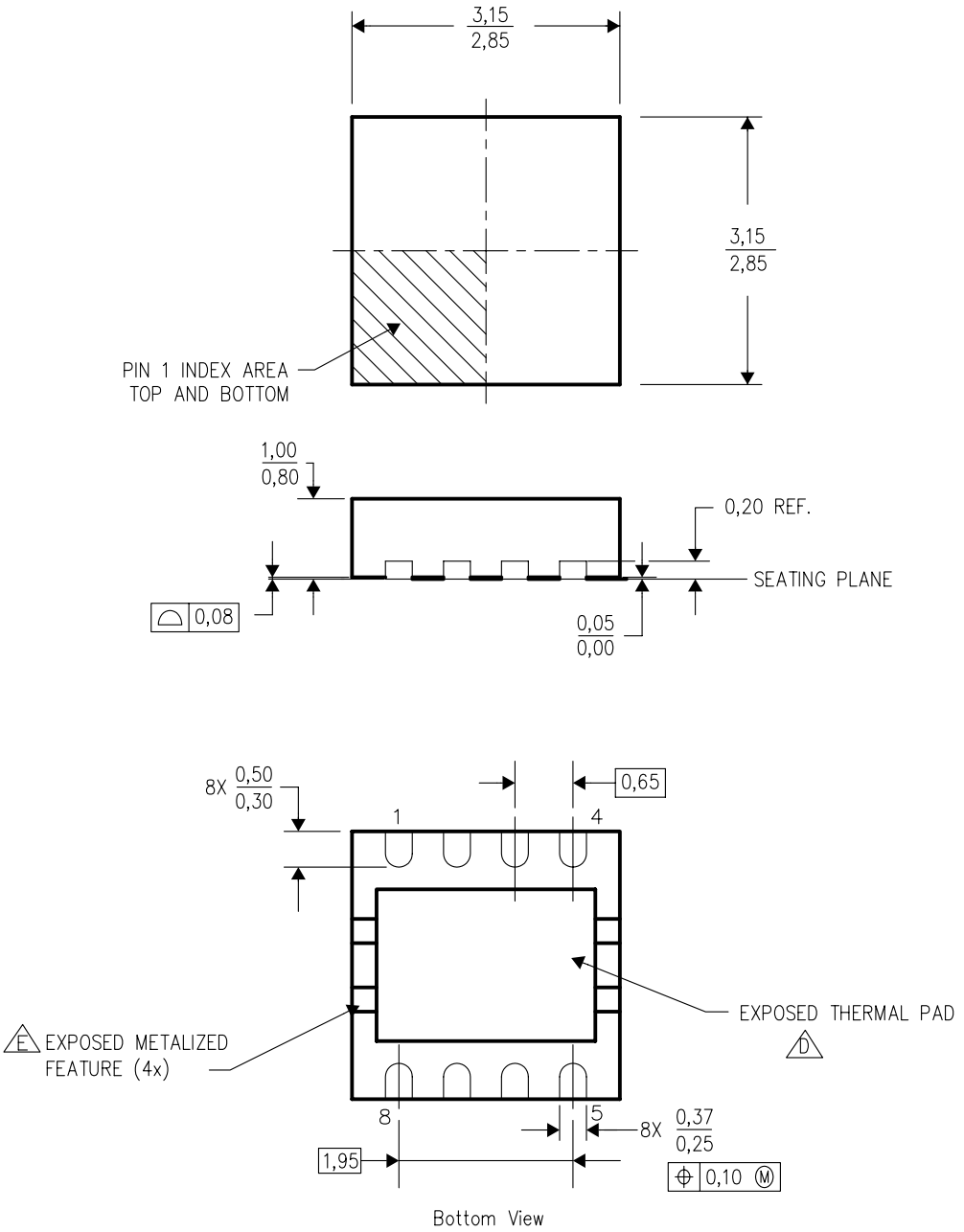
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



4203482/G 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

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