MIC23156

1.5A, 3 MHz Synchronous Buck Regulator with HyperLight Load® and I²C Control for Dynamic Voltage Scaling

Features

- Input Voltage: 2.7V to 5.5V
- Up to 1.5A Output Current
- 1 MHz I²C Controlled Adjustable Output:
  - V_{OUT} = 0.7 to 2.4V in 10 mV Steps
- High Output Voltage Accuracy (±1.5% over Temperature)
- Fast Pin-Selectable Output Voltage
- Programmable Soft-Start Using External Capacitor
- Ultra-Low Quiescent Current of 30 µA when Not Switching
- Thermal Shutdown and Current-Limit Protection
- Safe Start-Up into Pre-Biased Output
- Stable with 1 µH Output Inductor and 2.2 µF Ceramic Capacitor
- Up to 93% Peak Efficiency
- –40°C to +125°C Junction Temperature Range
- Available in 16-ball, 0.4 mm pitch, 1.81 mm x 1.71 mm Wafer Level Chip-Scale (WLCSP) and 17-pin, 2.8 mm x 2.5 mm QFN Packages

Applications

- Mobile Handsets
- Solid-State Drives (SSD)
- WiFi/WiMx/WiBro Modules
- Portable Applications

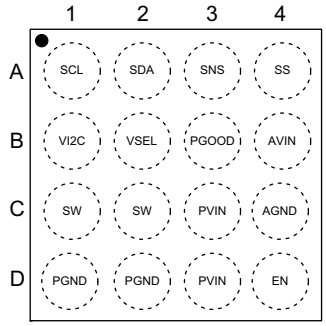
General Description

The MIC23156 is a high-efficiency, 1.5A synchronous buck regulator with HyperLight Load® mode and dynamic voltage scaling control through I²C. HyperLight Load provides very high efficiency at light loads and ultra-fast transient response. The ability to dynamically change the output voltage and maintain high output voltage accuracy make the MIC23156 perfectly suited for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage, throughout the entire load range, with the use of small output capacitors. Fast mode plus I²C provides output voltage and chip enable/disable control from a standard I²C bus with I²C clock rates of 100 kHz, 400 kHz, and 1 MHz.

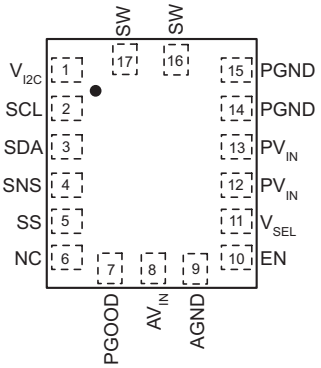
The MIC23156 is designed for use with 1 µH, and an output capacitor as small as 2.2 µF, that enables a total solution size less than 1 mm in height.

Package Types

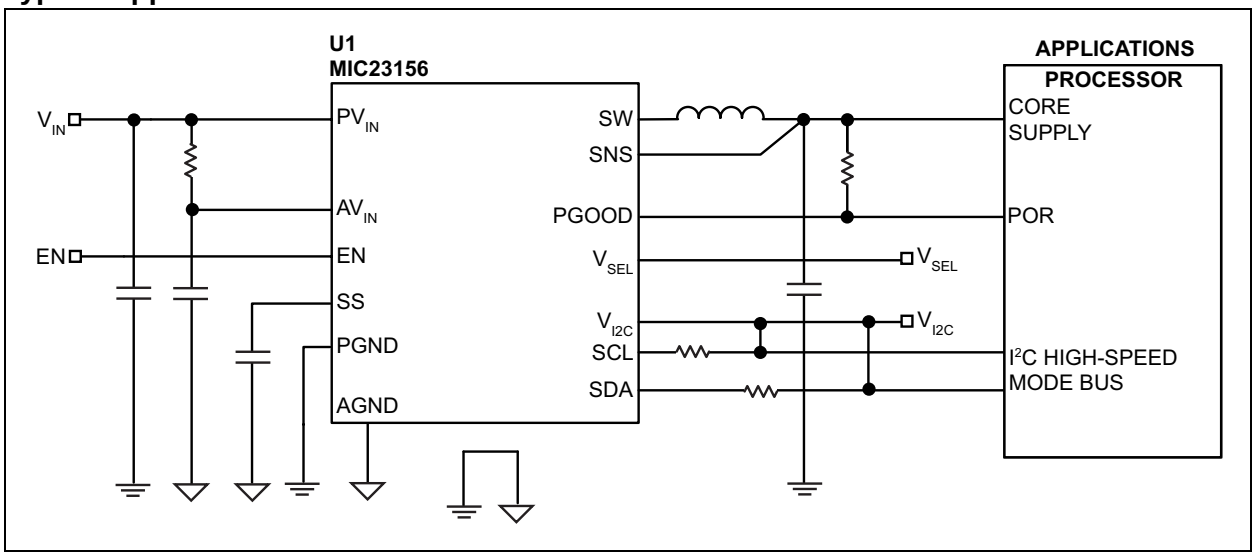
16-Ball 1.81 mm x 1.71 mm WLCSP (CS)
(Top View)



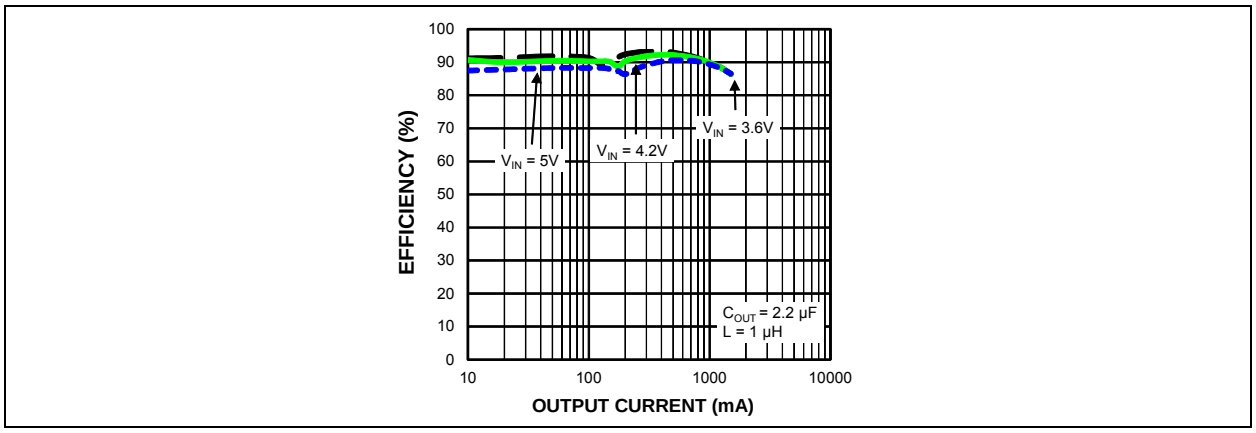
17-Pin 2.5 mm x 2.8 mm QFN (ML)
(Top View)



Typical Application Schematic



Efficiency (V_{OUT} = 2.4V) vs. Output Current



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input Supply Voltage (AV_{IN}, PV_{IN}, V_{I2C}) ..... –0.3V to +6V
Switch Voltage (SW) ..... –0.3V to AV_{IN}
Logic Voltage (EN, PGOOD) ..... –0.3V to AV_{IN}
Logic Voltage (V_{SEL}, SCL, SDA) ..... –0.3V to V_{I2C}
Analog Input Voltage (SNS, SS) ..... –0.3V to AV_{IN}
Power Dissipation (T_A = +70°C) ..... Internally Limited
ESD Rating(1) ..... 2 kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings(1)

Input Supply Voltage (AV_{IN}, PV_{IN}, V_{I2C}) ..... +2.7V to +5.5V
Switch Voltage (SW) ..... 0V to AV_{IN}
Logic Voltage (EN, PGOOD) ..... 0V to AV_{IN}
Logic Voltage (V_{SEL}, SCL, SDA) ..... 0V to V_{I2C}
Analog Input Voltage (SNS, SS) ..... 0V to AV_{IN}

Note 1: The device is not ensured to function outside the operating range.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1]

Electrical Specifications: unless otherwise specified, T_A = +25°C; AV_{IN} = PV_{IN} = V_{EN} = V_{VI2C} = 3.6V; L = 1.0 µH; C_{OUT} = 2.2 µF. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Supply Input Voltage Range	**2.7**	—	**5.5**	V	—
EN_{LOW}	Enable Logic Pin Low Threshold	—	—	**0.5**	V	Logic low
EN_{HIGH}	Enable Logic Pin High Threshold	**1.2**	—	—	V	Logic high
I_{VSEL_LO}	V_{SEL} Logic Pin Low Threshold	—	—	**0.3 x V_{I2C}**	V	Logic low
I_{VSEL_HI}	V_{SEL} Logic Pin High Threshold	**0.7 x V_{I2C}**	—	—	V	Logic high
I_{EN}	Logic Pin Input Current	—	0.1	**2**	µA	Pins: EN and V_{SEL}
UVLO	Undervoltage Lockout Threshold	**2.45**	2.55	**2.65**	V	Rising
UVLO_HYS	Undervoltage Lockout Hysteresis	—	75	—	mV	Falling
T_{SHD}	Shutdown Temperature (Threshold)	—	160	—	°C	—
T_{SHD_HYST}	Shutdown Temperature Hysteresis	—	20	—	°C	—
I_{SHDN}	Shutdown Supply Current	—	0.1	5	µA	V_{EN} = 0V
DC-to-DC Converter						
V_{OUT}	Output Voltage Accuracy	–1.5	—	+1.5	%	V_{OUT} = 1V, I_{OUT} = 10 mA
I_Q	Quiescent Supply Current	—	30	50	µA	I_{OUT} = 0 mA, V_{FB} > 1.2 * V_{OUT}
V_{OUT}	Output Voltage Range	0.7	—	2.4	V	
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Line Regulation	—	0.02	—	%/V	3.0V < V_{AVIN} < 4.5V, I_{LOAD} = 10 mA
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Load Regulation	—	0.04	—	%	20 mA < I_{OUT} < 1A
R_{SWON}	Switch-On Resistance	—	0.17	—	Ω	I_{SW} = +100 mA, high-side switch PMOS (QFN)
		—	0.15	—		I_{SW} = +100 mA, high-side switch PMOS (WLCSP)
		—	0.15	—		I_{SW} = –100 mA, low-side switch NMOS (QFN)
		—	0.13	—		I_{SW} = –100 mA, low-side switch NMOS (WLCSP)
I_{LIM}	Current Limit (DC Value)	1.7	2.9	5.1	A	V_{OUT} = 1V
f_{SW}	Oscillator Switching Frequency	—	3	—	MHz	—
D_{MAX}	Maximum Duty Cycle	80	—	—	%	Frequency = 3 MHz
—	DVS Step-Size	—	19	—	mV	—
t_{SS}	Soft Start Time	—	250	—	µs	V_{OUT} = 90%, C_{SS} = 120 pF

Note 1: Specifications are for packaged product only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, T_A = +25°C; AV_{IN} = PV_{IN} = V_{EN} = V_{VI2C} = 3.6V; L = 1.0 µH; C_{OUT} = 2.2 µF. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I²C Interface (Assuming 550 pF Total Bus Capacitance						
	I²C Address	10110111, 0xB7			—	Read (Binary, Hex)
		10110110, 0xB6				Write (Binary, Hex)
V_{IL}	Low-Level Input Voltage	—	—	**0.3 x V_{I2C}**	V	SCL, SDA
V_{IH}	High-Level Input Voltage	**0.7 x V_{I2C}**	—	—	V	SCL, SDA
R_{SDA_PD}	SDA Pull-Down Resistance	—	20	—	W	Open-drain pull-down on SDA during read back, I_{SDA} = 500 µA
Power Good (PG)						
V_{PG_LOW}	PGOOD Output Low	—	100	—	mV	V_{OUT} < 80% V_{NOM}, I_{PGOOD} = -500 µA
I_{PG_LEAK}	PGOOD Output Leakage	—	—	**5**	µA	V_{OUT} = V_{NOM}
V_{PG_TH}	PGOOD Threshold (% of V_{OUT} < V_{NOM})	86	—	96	%	V_{OUT} ramping up
V_{PG_HYS}	PGOOD Hysteresis	—	5	—	%	—

Note 1: Specifications are for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Junction Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance WLCSP 16-Ball	θ_{JA}	—	150	—	°C/W	—
Thermal Resistance QFN-17	θ_{JA}	—	89	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

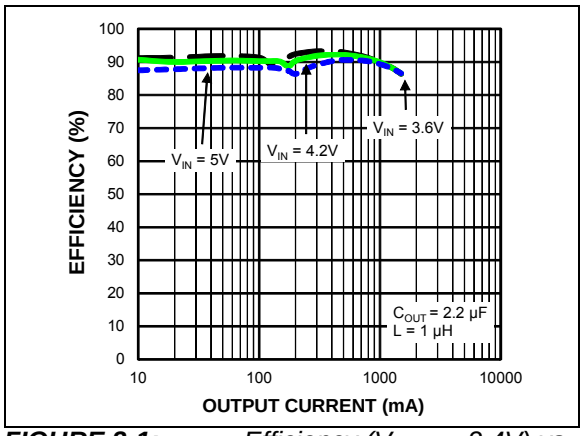


FIGURE 2-1: *Efficiency (V_{OUT} = 2.4V) vs. Output Current.*

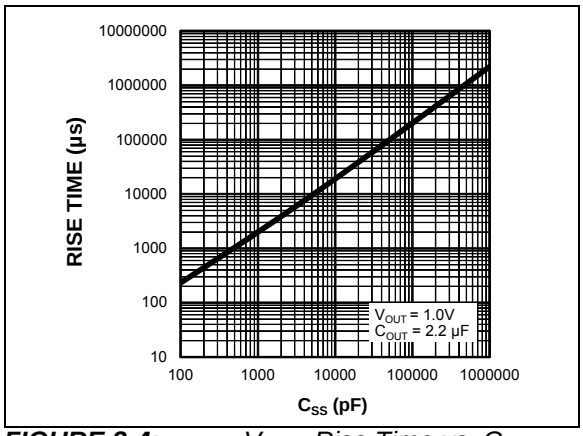


FIGURE 2-4: *V_{OUT} Rise Time vs. C_{SS}.*

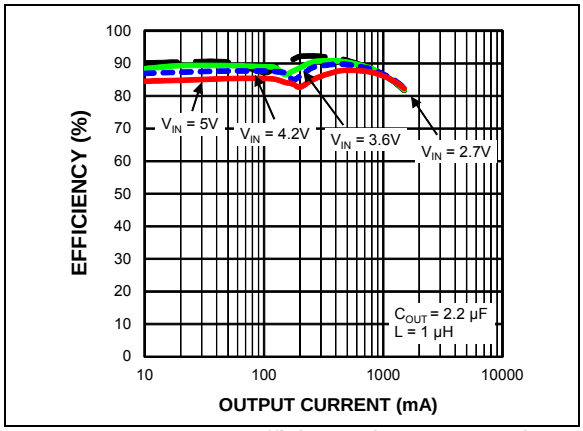


FIGURE 2-2: *Efficiency (V_{OUT} = 1.8V) vs. Output Current.*

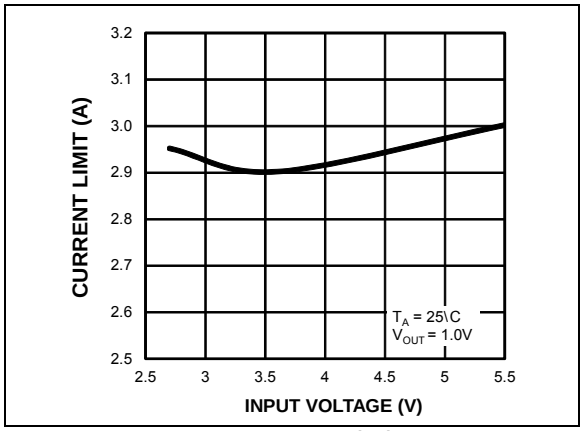


FIGURE 2-5: *Current Limit vs. Input Voltage.*

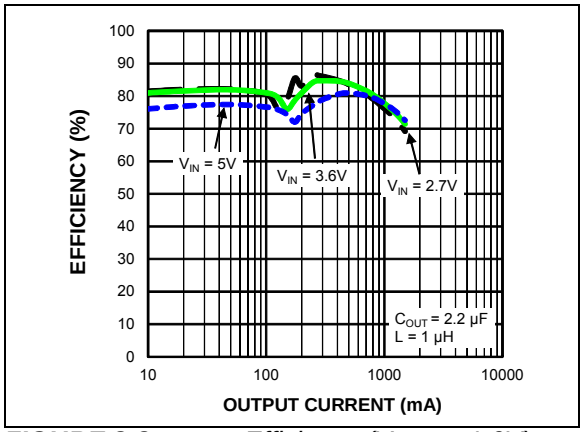


FIGURE 2-3: *Efficiency (V_{OUT} = 1.0V) vs. Output Current.*

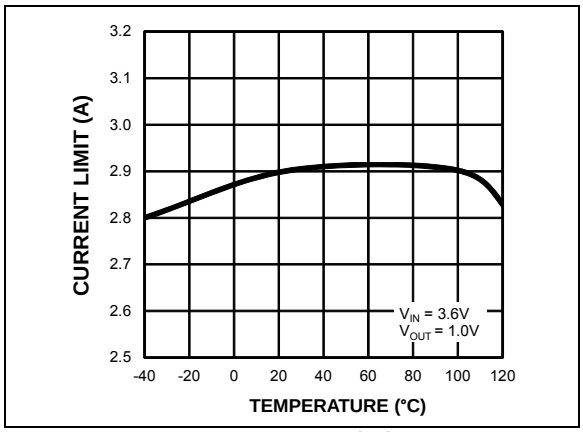


FIGURE 2-6: *Current Limit vs. Temperature.*

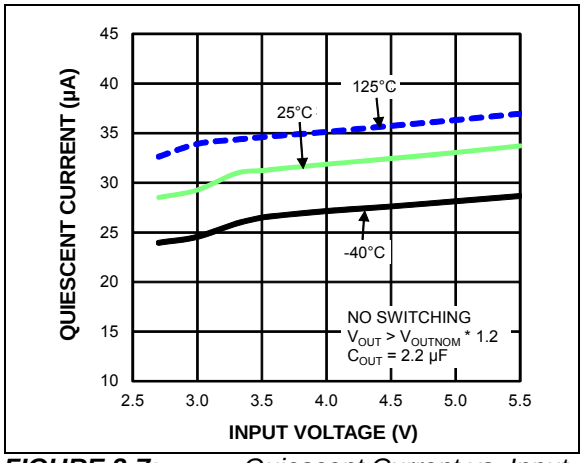


FIGURE 2-7: *Quiescent Current vs. Input Voltage.*

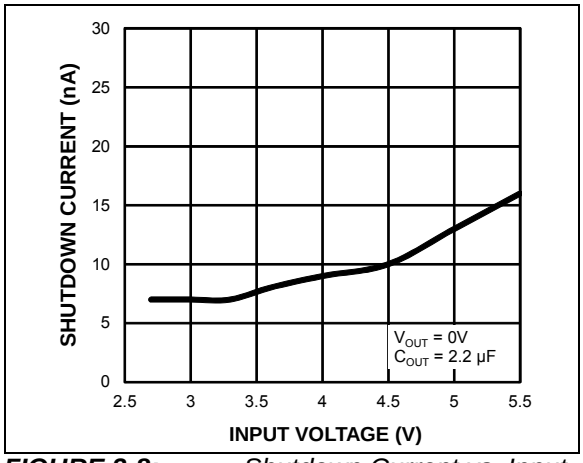


FIGURE 2-8: *Shutdown Current vs. Input Voltage.*

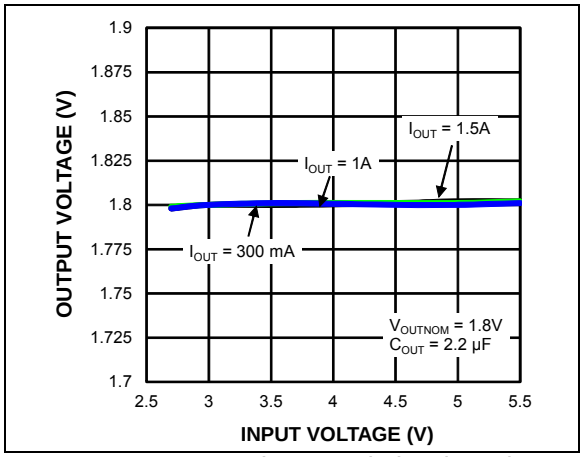


FIGURE 2-9: *Line Regulation (CCM).*

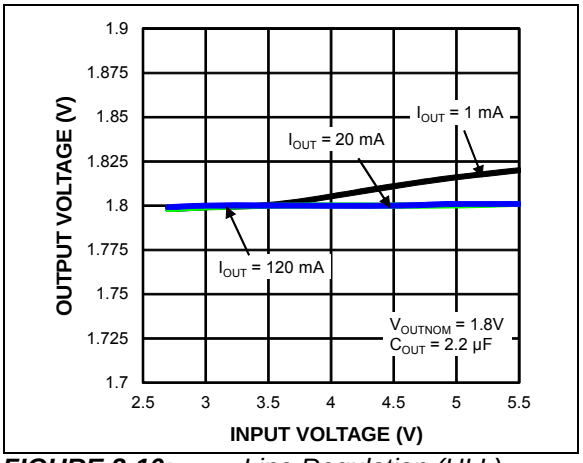


FIGURE 2-10: *Line Regulation (HLL).*

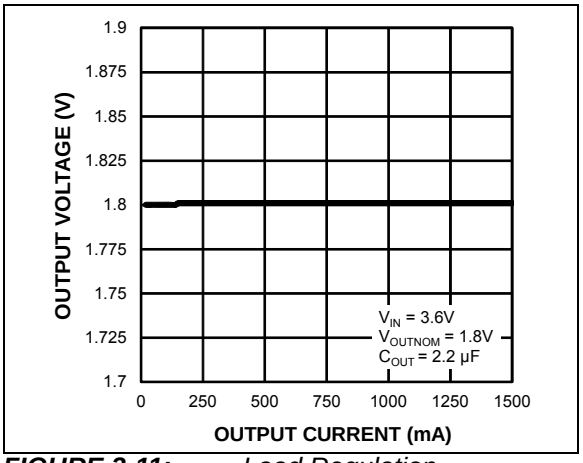


FIGURE 2-11: *Load Regulation.*

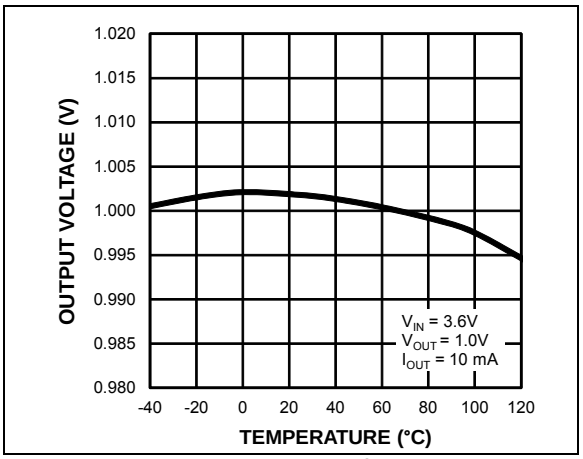


FIGURE 2-12: *Output Voltage vs. Temperature.*

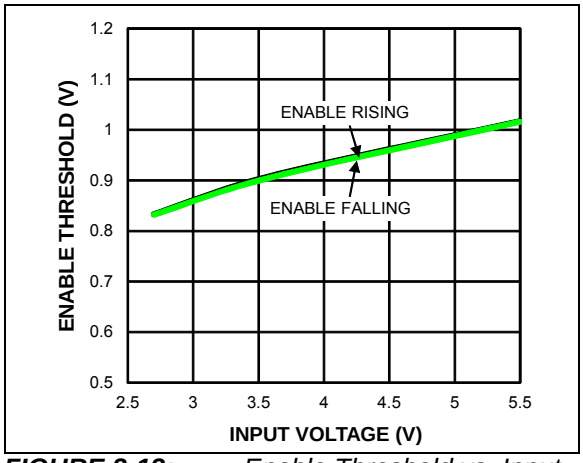


FIGURE 2-13: *Enable Threshold vs. Input Voltage.*

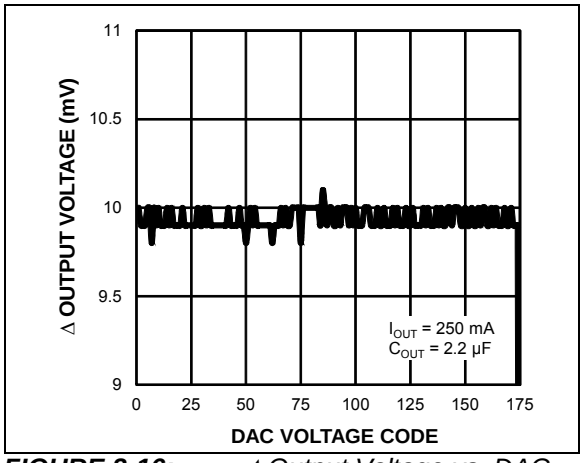


FIGURE 2-16: *Δ Output Voltage vs. DAC DNL.*

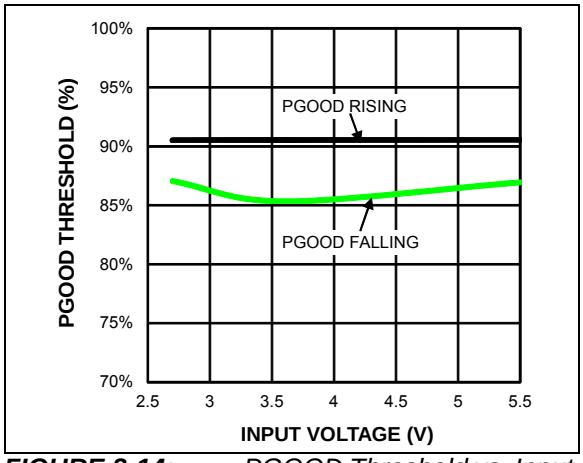


FIGURE 2-14: *PGOOD Threshold vs. Input Voltage.*

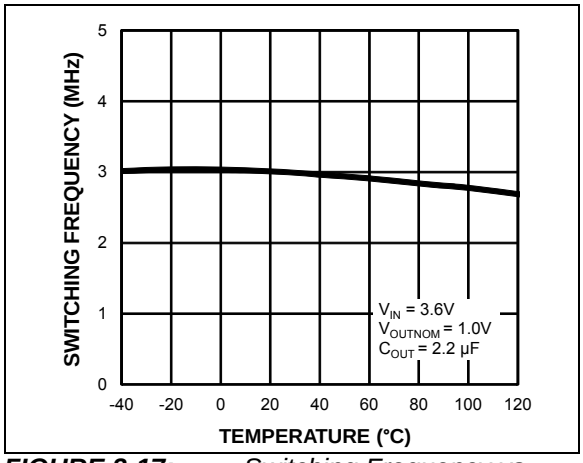


FIGURE 2-17: *Switching Frequency vs. Temperature.*

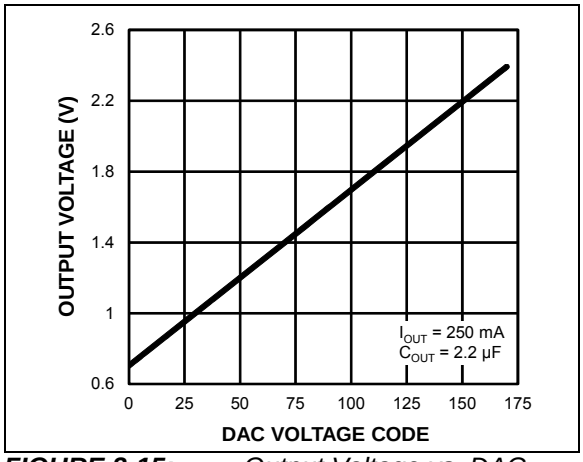


FIGURE 2-15: *Output Voltage vs. DAC Linearity.*

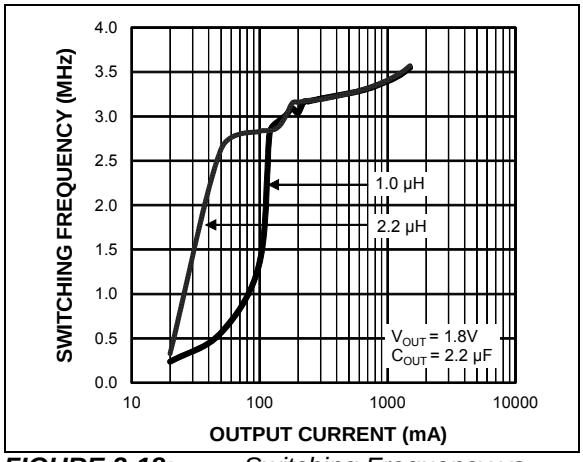


FIGURE 2-18: *Switching Frequency vs. Output Current.*

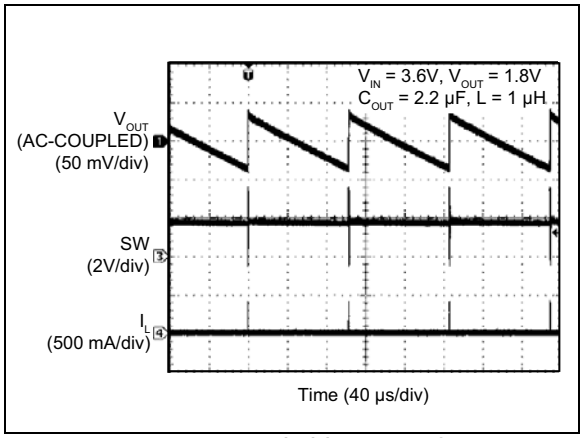


FIGURE 2-19: *Switching Waveform Discontinuous Mode (1 mA).*

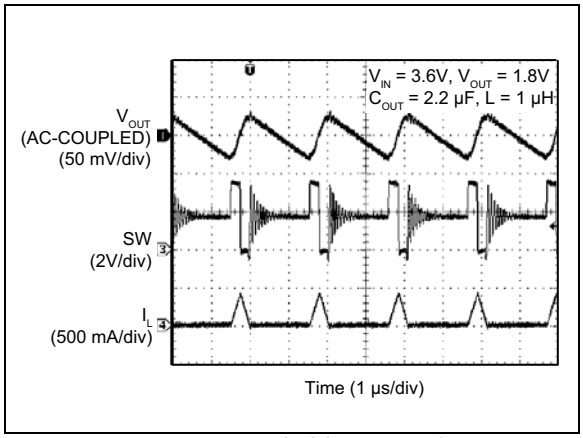


FIGURE 2-20: *Switching Waveform Discontinuous Mode (50 mA).*

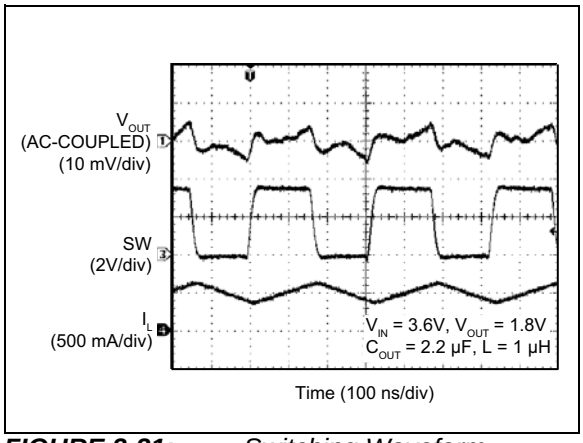


FIGURE 2-21: *Switching Waveform Continuous Mode (500 mA).*

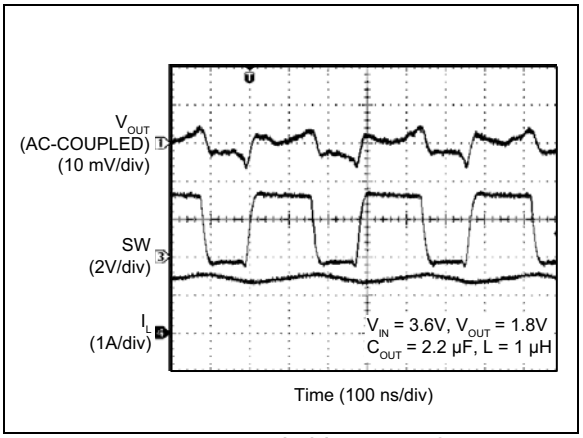


FIGURE 2-22: *Switching Waveform Continuous Mode (1.5A).*

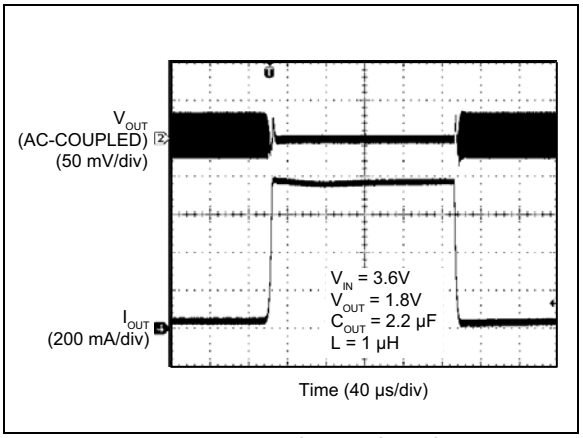


FIGURE 2-23: *Load Transient (50 mA to 750 mA).*

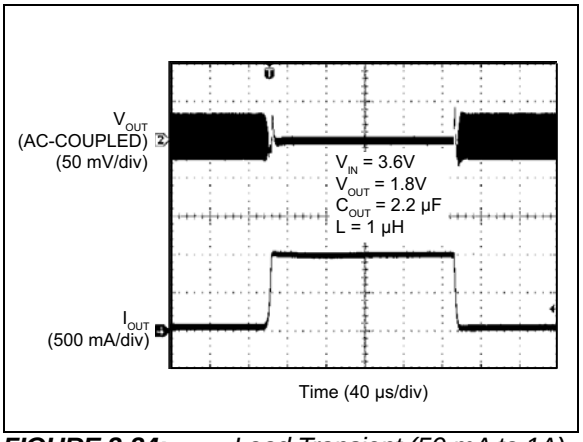


FIGURE 2-24: *Load Transient (50 mA to 1A).*

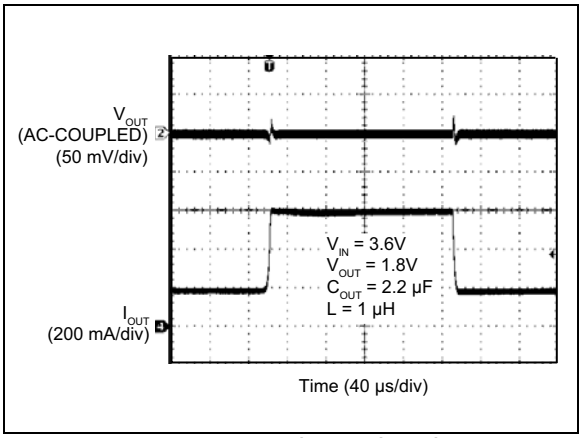


FIGURE 2-25: *Load Transient (200 mA to 600 mA).*

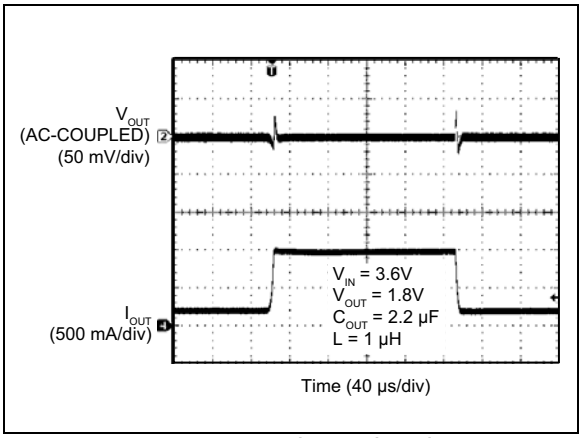


FIGURE 2-26: *Load Transient (200 mA to 1.5A).*

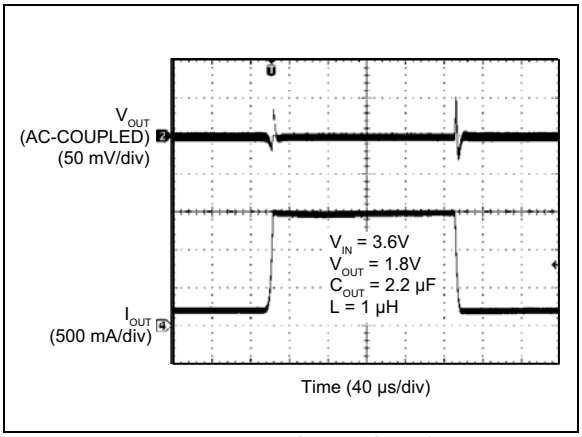


FIGURE 2-27: *Load Transient (200 mA to 1.5A).*

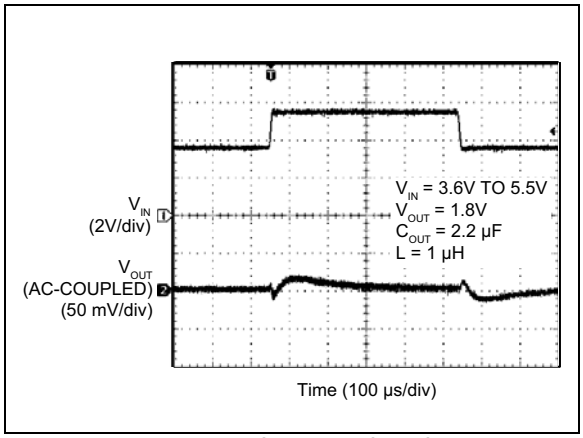


FIGURE 2-28: *Line Transient (3.6V to 5.5V @ 1.5A).*

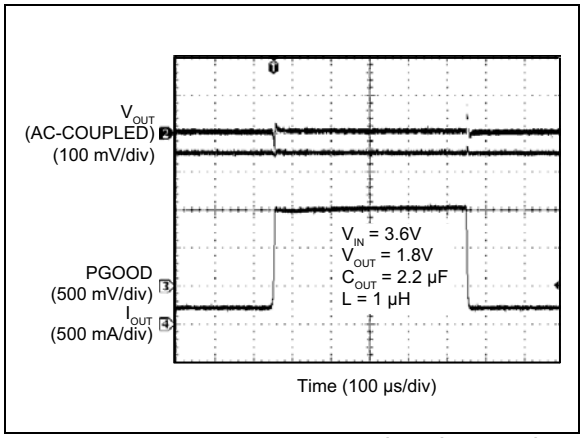


FIGURE 2-29: *Power Good During Load Transient (200 mA to 1.5A).*

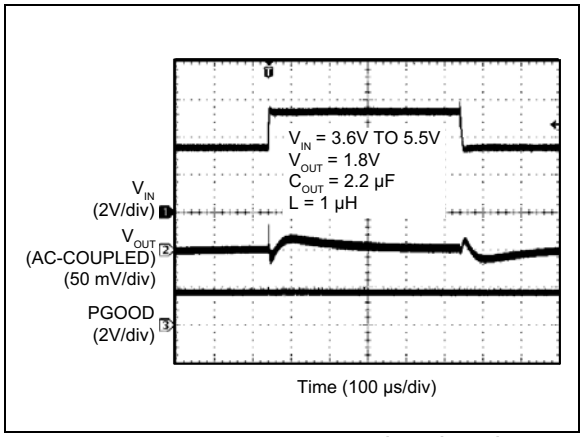


FIGURE 2-30: *Power Good During Line Transient (3.6V to 5.5V @ 1.5A).*

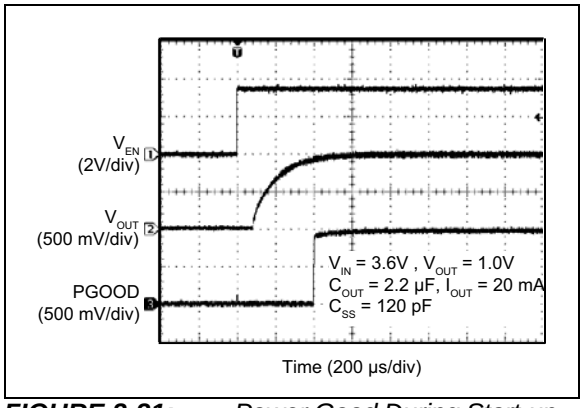


FIGURE 2-31: *Power Good During Start-up.*

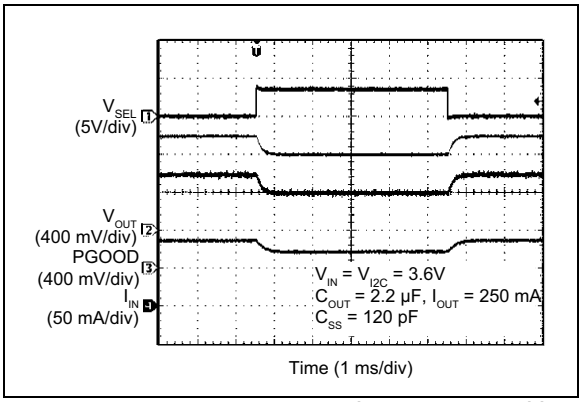


FIGURE 2-33: *V_{OUT} During V_{SEL} Transition.*

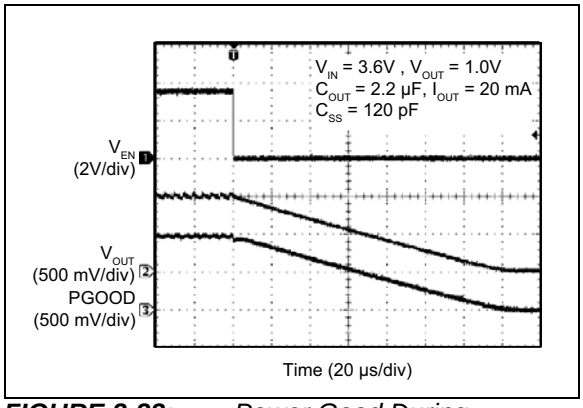


FIGURE 2-32: *Power Good During Shutdown.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Ball Number	Pin Number	Pin Name	Pin Function
WLCSP	QFN		
A1	2	SCL	Fast Mode Plus 1 MHz I^2C Clock Input Pin.
A2	3	SDA	Fast Mode Plus 1 MHz I^2C Data Input/Output Pin.
A3	4	SNS	Sense: Connect to V_{OUT}, close to output capacitor to sense V_{OUT}.
A4	5	SS	Programmable Soft Start: Connect capacitor to AGND.
B1	1	V_{I2C}	Power Connection for I^2C Bus Voltage: Connect this pin to the voltage domain of the I^2C bus supply. Do not leave floating.
B2	11	V_{SEL}	Pin Selectable: Output voltage of either of two I^2C Voltage registers. Do not leave floating.
B3	7	PGOOD	Power Good Indicator: Use an external pull-up resistor to supply.
B4	8	AV_{IN}	Input Voltage to Power Analog Functions: Connect decoupling capacitor to ground.
C1, C2	16, 17	SW	Switch Connection: Internal power MOSFET output switches.
C3, D3	12, 13	PV_{IN}	Input Voltage to Power Switches: Connect decoupling capacitor to ground.
C4	9	AGND	Analog Ground: Connect to central ground point where all high-current paths meet (C_{IN}, C_{OUT}, and PGND) for best operation.
D1, D2	14, 15	PGND	Power Ground Connection.
D4	10	EN	Enable: Logic high enables operation of voltage regulator. Logic low shuts down the device. Do not leave floating.
—	6	NC	No Connect.

4.0 FUNCTIONAL DESCRIPTION

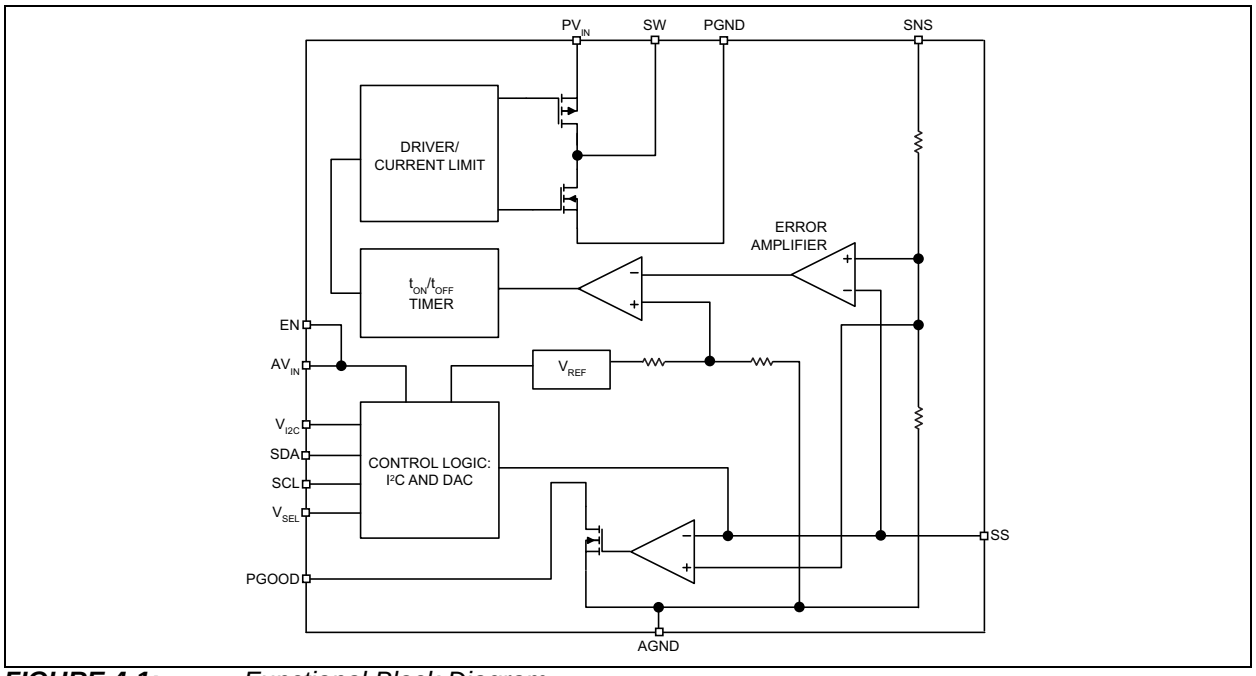


FIGURE 4-1: *Functional Block Diagram.*

4.1 PV_{IN}

The Power Input Supply (PV_{IN}) pin provides power to the internal MOSFETs for the Switch mode regulator section. The PV_{IN} operating range is 2.7V to 5.5V, so an input capacitor with a minimum voltage rating of 6.3V is recommended. Due to the high switching speed, a minimum 2.2 µF bypass capacitor, placed close to PV_{IN} and the Power Ground (PGND) pin, is required.

4.2 AV_{IN}

Analog V_{IN} (AV_{IN}) pin provides power to the internal control and analog supply circuitry. AV_{IN} must be tied to PV_{IN} through a 10Ω RC filter. Careful layout should be considered to ensure that any high-frequency switching noise caused by PV_{IN} is reduced before reaching AV_{IN}. A 2.2 µF capacitor, as close to AV_{IN} as possible, is recommended.

4.3 EN

A logic high signal on the Enable pin activates the output voltage of the device. A logic low signal on the Enable pin deactivates the output and reduces supply current to 0.1 µA. Do not leave the EN pin floating. MIC23156 features external soft start circuitry via the Soft Start (SS) pin that reduces inrush current and prevents the output voltage from overshooting when EN is driven logic high. Do not leave the EN pin floating.

4.4 SW

The Switch (SW) pin connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the SNS pin, output capacitor and the load. Due to the high-speed switching on this pin, the Switch node should be routed away from sensitive nodes whenever possible.

4.5 SNS

The Sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor.

4.6 AGND

The Analog Ground (AGND) pin is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power Ground (PGND) loop.

4.7 PGND

The Power Ground (PGND) pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog Ground (AGND) loop, as applicable.

4.8 PGOOD

The Power Good (PGOOD) pin is an open-drain output, which indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5 kΩ should be connected from PGOOD to V_{OUT}.

4.9 SS

The Soft Start (SS) pin is used to control the output voltage ramp-up time. The approximate equation for the ramp time in seconds is: 820 x 103 x ln(10) x C_{SS}. For example, for C_{SS} = 120 pF, $t_{RISE} \approx$ 230 µs. Refer to the Figure 2-4 graph in **Section 2.0 "Typical Performance Curves"**. The minimum recommended value for C_{SS} is 120 pF.

4.10 V_{I2C}

Power Connection pin for the I^2C bus voltage. Connect this pin to the voltage domain of the I^2C bus supply.

4.11 V_{SEL}

Selectable Output Voltage pin of either of two I^2C Voltage registers. A logic low selects Buck Register 1 and logic high selects Buck Register 2. If no I^2C programming is used, the output voltages will be as per the default Voltage register values. Do not leave floating.

4.12 SCL

The I^2C Clock Input pin provides a reference clock for clocking in the data signal. This is a Fast mode plus 1 MHz input pin and requires a 4.7 kΩ pull-up resistor.

4.13 SDA

The I^2C Data Input/Output pin allows for data to be written to and read from the MIC23156. This is a Fast mode plus 1 MHz I^2C pin and requires a 4.7 kΩ pull-up resistor.

5.0 APPLICATION INFORMATION

The MIC23156 is a high-performance, DC-to-DC step-down regulator offering a small solution size and supporting up to 1.5A. The device is available in a 2.8 mm x 2.5 mm QFN and a 1.81 mm x 1.71 mm WLCSP package. Using the HyperLight Load® switching scheme, the MIC23156 is able to maintain high efficiency and exceptional voltage accuracy throughout the entire load range, while providing ultra-fast load transient response. Another beneficial feature is the ability to dynamically change the output voltage in steps of 10 mV. The following subsections provide additional device application information.

5.1 Input Capacitor

A 2.2 µF (or larger) ceramic capacitor should be placed as close as possible to the PV_{IN} and AV_{IN} pins with a short trace for good noise performance. X5R or X7R type ceramic capacitors are recommended for better tolerance over temperature. The Y5V and Z5U type temperature rating ceramic capacitors are not recommended due to their large reduction in capacitance over temperature, and increased resistance at high frequencies. These issues reduce their ability to filter out high-frequency noise. The rated voltage of the input capacitor should be at least 20% higher than the maximum operating input voltage over the operating temperature range.

5.2 Output Capacitor

Output capacitor selection is also a trade-off between performance, size and cost. Increasing the output capacitor will lead to an improved transient response, however, the size and cost also increase. The MIC23156 is designed for use with a 2.2 µF or greater ceramic output capacitor. A low-Equivalent Series Resistance (low-ESR) ceramic output capacitor is recommended, based upon performance, size and cost. Both the X7R and X5R temperature rating capacitors are recommended. Refer to Table 5-1 for additional information.

5.3 Inductor Selection

Inductor selection is a balance between efficiency, stability, cost, size and rated current. Since the MIC23156 is compensated internally, the recommended inductance of L is limited from 0.47 µH to 2.2 µH to ensure system stability.

For faster transient response, a 0.47 µH inductor will yield the best result. For lower output ripple, a 2.2 µH inductor is recommended.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a +40°C temperature rise or a 10% to 30% loss in inductance.

Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as noted in Equation 5-1:

EQUATION 5-1: CALCULATING PEAK CURRENT

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right]$$

As shown by Equation 5-1, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or the inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends upon the requirements of the application. Refer to the **"Typical Application Schematic"** section for details.

DC Resistance (DCR) is also important. While DCR is inversely proportional to size, it can represent a significant efficiency loss. Refer to **Section 5.6 "Efficiency Considerations"**.

The transition between Continuous Conduction Mode (CCM) to HyperLight Load mode is determined by the inductor ripple current and the load current.

Figure 5-1 shows the signals for the High-Side Drive (HSD) switch for t_{ON} control, the inductor current and the Low-Side Drive (LSD) switch for t_{OFF} control.

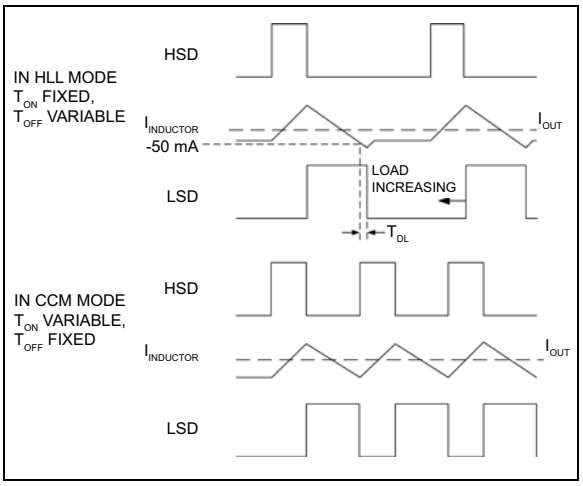


FIGURE 5-1: *HSD Signals for t_{ON} Control, Inductor Current and LSD for t_{OFF} Control.*

In HLL mode, the inductor is charged with a fixed t_{ON} pulse on the High-Side Drive (HSD) switch. After this, the LSD is switched on and current falls at a rate of V_{OUT}/L. The controller remains in HLL mode while the inductor falling current is detected to cross at approximately 200 mA. When the LSD (or t_{OFF}) time reaches its minimum, and the inductor falling current is no longer able to reach this 200 mA threshold, the part is in CCM mode and switching at a virtually constant frequency.

Table 5-1 optimizes the inductor to output capacitor combination for maintaining a minimum phase margin of 45°.

TABLE 5-1: MAXIMUM C_{OUT} vs. INDUCTOR

Inductor	Minimum C_{OUT}	Recommended C_{OUT}	Maximum C_{OUT}
0.47 µH	2.2 µF	4.7 µF	25 µF
1.0 µH	2.2 µF	2.2 µF	15 µF
2.2 µH	2.2 µF	2.2 µF	6.8 µF

5.4 Duty Cycle

The typical maximum duty cycle of the MIC23156 is 80%.

5.5 Thermal Shutdown

When the internal die temperature of MIC23156 reaches 160°C, the internal driver is disabled until the die temperature falls below 140°C.

5.6 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied, as shown in Equation 5-2:

EQUATION 5-2: EFFICIENCY CALCULATION

$$\text{Efficiency \%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

There are two types of losses in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET R_{DSON}, multiplied by the switch current squared. During the off cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required in driving the gates on and off at a constant 3 MHz frequency, and the switching transitions, make up the switching losses.

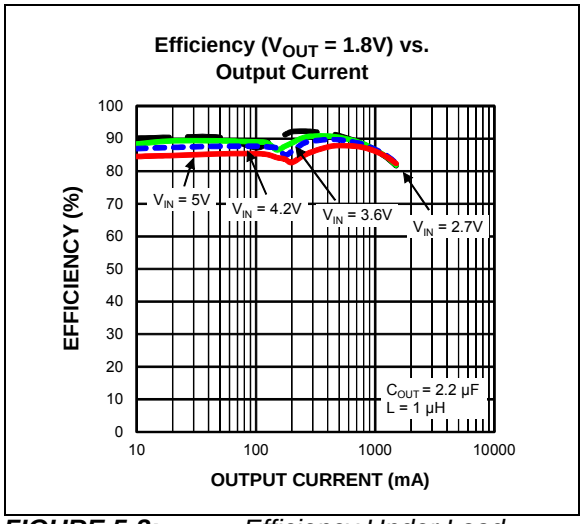


FIGURE 5-2: *Efficiency Under Load.*

Figure 5-2 shows an efficiency curve. From a 10 mA load to 1.5A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load mode, the MIC23156 is able to maintain high efficiency at low-output currents.

Over 200 mA efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC Resistance (DCR) can become quite significant. The DCR losses can be calculated as shown in Equation 5-3:

EQUATION 5-3: CALCULATING DCR LOSSES

$$P_{DCR} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 5-4:

EQUATION 5-4: LOSS IN EFFICIENCY DUE TO INDUCTOR RESISTANCE

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} \times P_{DCR}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

5.7 HyperLight Load Mode

The MIC23156 uses a minimum on and off-time proprietary control loop. When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum on-time; this increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for a lower voltage drop across the switching device when it is on. The synchronous switching combination between the PMOS and the NMOS allows the control loop to work in Discontinuous mode for light load operations. In Discontinuous mode, the MIC23156 works in HyperLight Load to regulate the output. As the output current increases, the off-time decreases, thus providing more energy to the output. This switching scheme improves the efficiency of MIC23156 during light load currents by only switching when it is needed. As the load current increases, the MIC23156 goes into Continuous Conduction Mode (CCM) and switches at a frequency centered at 3 MHz. The equation to calculate the load when the MIC23156 goes into Continuous Conduction Mode may be approximated by Equation 5-5:

EQUATION 5-5: CALCULATING LOAD WHEN IN CONTINUOUS CONDUCTION MODE

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f}\right)$$

As shown in Equation 5-5, the load at which the MIC23156 transitions from HyperLight Load mode to PWM mode is a function of the Input Voltage (V_{IN}), Output Voltage (V_{OUT}), Duty Cycle (D), Inductance (L) and frequency (f). As shown in Figure 5-3, as the output current increases, the switching frequency also increases until the MIC23156 goes from HyperLight Load mode to PWM mode, at approximately 200 mA. The MIC23156 will switch at a relatively constant frequency, around 3 MHz, once the output current is over 200 mA.

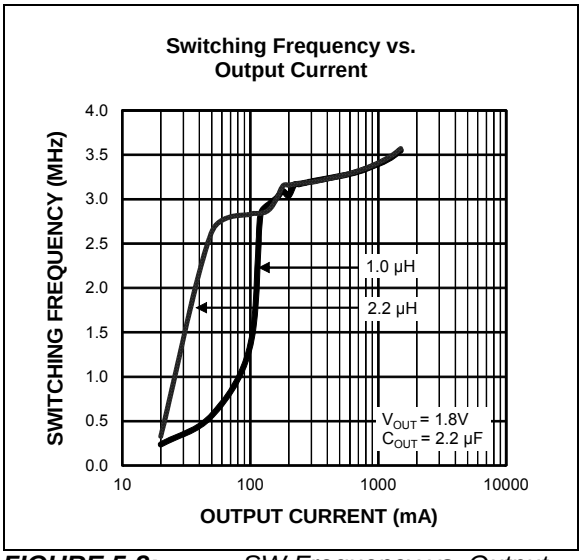


FIGURE 5-3: *SW Frequency vs. Output Current.*

5.8 Output Voltage Setting

The MIC23156 features dynamic voltage scaling and setting hardware that allow the output voltage of the buck regulator to be changed on-the-fly, in increments of 10 mV. The output voltage is set according to one of two registers that behave identically: BUCK_OUT1 when V_{SEL} = 0 and BUCK_OUT2 when V_{SEL} = 1. If the BUCK_OUT value is changed while the V_{SEL} is selected and the regulator is enabled, then the output voltage will immediately change to the new value using Dynamic Voltage Scaling (DVS). Equation 5-6 describes the relationship between the register value and the output voltage:

EQUATION 5-6: REGISTER VALUE AND OUTPUT VOLTAGE RELATIONSHIP

$$V_{OUT} = 0.7 + (0.01 \times REG_{BUCK\_OUT})$$

Note that the maximum output voltage is 2.4V, corresponding to a register setting of 170 (0b10101010, 0xAA). An example of this calculation is demonstrated in **Section 5.13 "Calculating DAC Voltage Code"**.

5.9 I²C Interface

Figure 5-4 shows the communications required for write and read operations via the I²C interface. The black lines show master communications and the red lines show the slave communications. During a write operation, the master must drive SDA and SCL for all stages, except the Acknowledgment (A) stage shown in red, which are provided by the slave (MIC23156).

The read operation begins first with a dataless write to select the register address from which to read. A restart sequence is issued, followed by a read command and a data read.

The MIC23156 responds to a slave address of Hex 0xB6 and 0xB7 for write and read operations, respectively, or binary 1011011x (where 'x' is the read/write bit, 0 = write, 1 = read).

The register address is eight bits wide and carries the address of the MIC23156 register to be operated upon. Only the lower three bits are used.

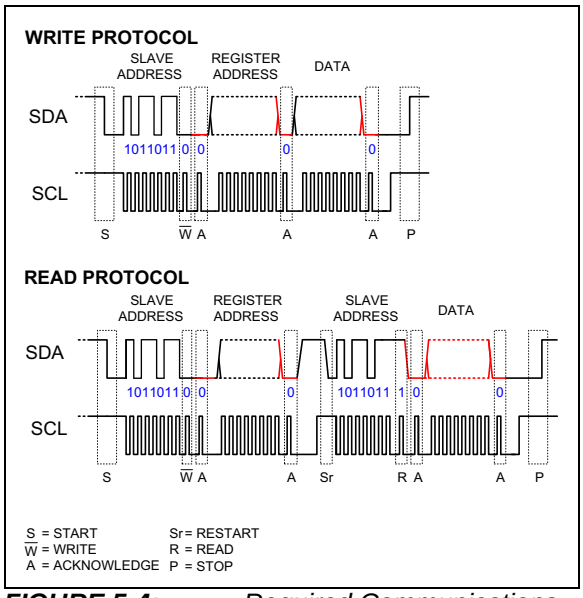


FIGURE 5-4: *Required Communications for Read/Write Operations via I²C Interface.*

5.10 I²C Register Summary

There are three I²C Read/Write registers that are 8 bits in length. All registers are reset to a zero state whenever EN ≤ 0.5V and set (reset) to their default values on the transition of EN ≥ 1.5V. All registers are accessible by I²C.

TABLE 5-2: REGISTER BIT FIELD MAP

Reg.	D7	D6	D5	D4
1	—	TSD	UVLO	PGOOD
2	BUCK_OUT1			
3	BUCK_OUT2			
Reg.	**D3**	**D2**	**D1**	**D0**
1	—	—	SSL	BUCK_EN
2	BUCK_OUT1			
3	BUCK_OUT2			

5.11 Enable/Status Register (001b/01h)

The Enable/Status register is written to enable the output regulator (BUCK_EN) and Soft Start Extension mode (SSL). It is read to interrogate the status of Thermal Shutdown (TSD), Undervoltage Lockout (UVLO) and Power Good (PGOOD) status of the regulator. See Register 5-1 for additional information.

5.12 Buck Register 1 (010b/02h) and Buck Register 2 (011b/03h)

These registers are written to set the output voltage to any one of 170 levels in 10 mV steps. Values above decimal 170 are equivalent to setting the register to 170. The two registers correspond to one of two states, which is selectable by the V_{SEL} input pin. This allows the regulator to be quickly switched between two voltage levels (e.g., enabled and standby). When V_{SEL} = 0, the output voltage is controlled by BUCK_OUT1 (REG2). When V_{SEL} = 1, then the output voltage is controlled by BUCK_OUT2 (REG3). See Register 5-2 and Register 5-3 for additional information.

REGISTER 5-1: REG1: ENABLE AND STATUS REGISTER

r-0	R-0	R-0	R-0	r-0	r-0	R/W-0	R/W-1
—	TSD	UVLO	PGOOD	—	—	SSL	BUCK_EN
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Not used

bit 6 **TSD:** Thermal Shutdown Status bit

This register bit will be set by internal hardware if a thermal shutdown event is triggered by the die temperature which exceeds the shutdown temperature.

bit 5 **UVLO:** Undervoltage Lockout Status bit

This register bit will be set by internal hardware when the undervoltage lockout circuit is active and cleared when V_{IN} exceeds the UVLO threshold.

bit 4 **PGOOD:** Power Good Status bit

This register bit will be set when the buck regulator output voltage is > nominally 10% of the output voltage set points, as specified by V_{SEL}, BUCK_OUT1 and BUCK_OUT2. This regulator has the same function as the PGOOD output pin.

bit 3-2 **Reserved:** Not used

bit 1 **SSL:** Long Soft Start Enable bit

If this bit is set, then the internal soft start resistor is increased and the soft start time will be extended.

bit 0 **BUCK_EN:** Buck Regulator Enable bit

Setting this bit will enable and turn on the buck regulator output. Clearing this bit will disable the buck regulator output.

REGISTER 5-2: REG2: BUCK_OUT1 REGISTER

R/W-0x1E	R/W-0x1E	R/W-0x1E	R/W-0x1E	R/W-0x1E	R/W-0x1E	R/W-0x1E	R/W-0x1E
BUCK_OUT1<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **BUCK_OUT1<7:0>:** Buck Output Voltage 1 bits (setting for V_{SEL} = 0)

Setting this register value will change the output regulation point for the buck regulator when V_{SEL} = 0. If the buck is enabled and V_{SEL} = 0, changing the value will immediately cause the output voltage to transition to the new set point.

REGISTER 5-3: REG3: BUCK_OUT2 REGISTER

R/W-0x0A	R/W-0x0A	R/W-0x0A	R/W-0x0A	R/W-0x0A	R/W-0x0A	R/W-0x0A	R/W-0x0A
BUCK_OUT2<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **BUCK_OUT2<7:0>:** Buck Output Voltage 2 bits (setting for V_{SEL} = 1)

Setting this register value will change the output regulation point for the buck regulator when V_{SEL} = 1. If the buck is enabled and V_{SEL} = 1, changing the value will immediately cause the output voltage to transition to the new set point.

5.13 Calculating DAC Voltage Code

If the desired output voltage is 1.8V, then using Equation 5-7:

EQUATION 5-7: CALCULATING DAC VOLTAGE

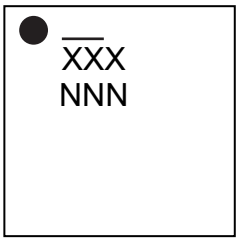
$$V_{OUT} = 0.7 + (0.01 \times REG_{BUCK\_OUT}) \rightarrow REG_{BUCK\_OUT} = \frac{(1.8 - 0.7)}{0.01}$$

Note: REG_{BUCK_OUT} = `110` in decimal, 6E in Hex or '`0110 1110`' in binary.

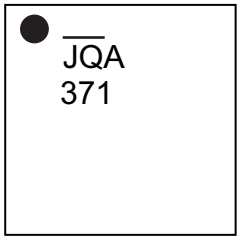
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

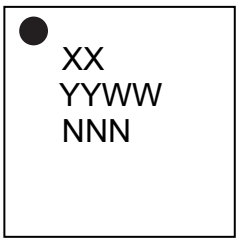
17-Lead QFN*



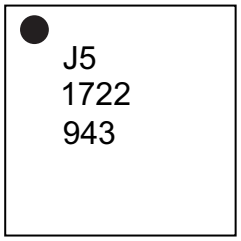
Example



16-Ball WLCSP*



Example



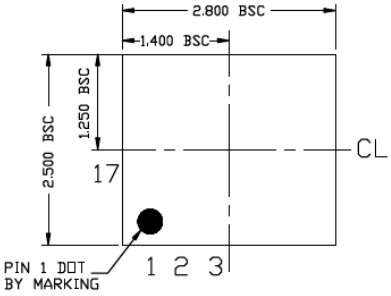
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6.2 Package Details

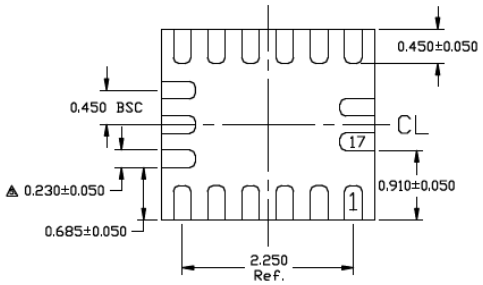
The following sections give the technical details of the packages.

TITLE
17 LEAD COL QFN 2.5x2.8mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

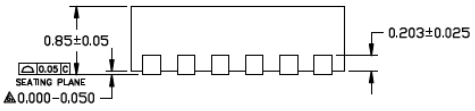
DRAWING #	CQFN2528-17LD-PL-1	UNIT	MM



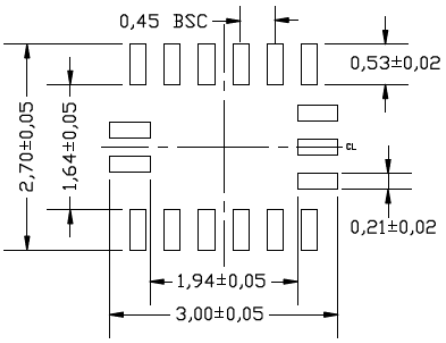
TOP VIEW



BOTTOM VIEW



SIDE VIEW



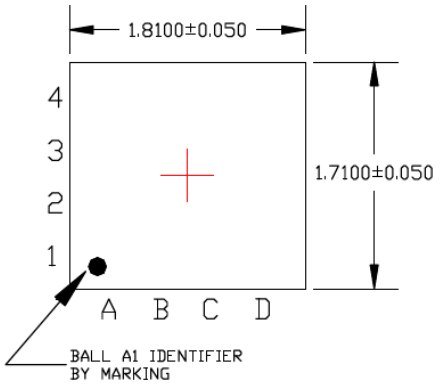
RECOMMENDED LAND PATTERN

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.

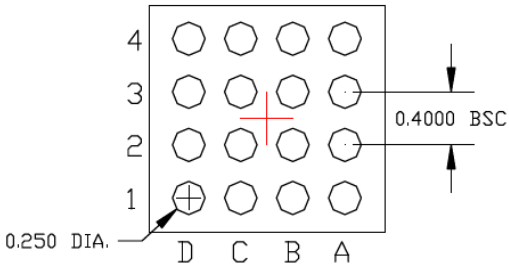
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

TITLE
16 BALL WLCSP 1.81x1.71mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

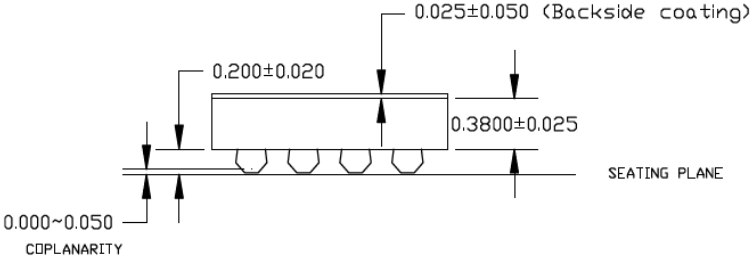
DRAWING #	WLCSP181171Q-16BL-PL-9	UNIT	MM



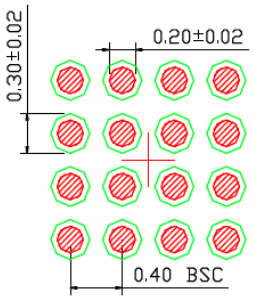
TOP VIEW
NOTE: 1, 2



BOTTOM VIEW
NOTE: 1, 2



SIDE VIEW
NOTE: 1, 2



RECOMMENDED
LAND PATTERN
NOTE: 3, 4

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. NON-SOLDERMASK DEFINED PADS ARE RECOMMENDED FOR BOARD LAYOUT
4. SHADED RED CIRCLES REPRESENT CONTACT PAD AREA. GREEN CIRCLES REPRESENT SOLDER MASK OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December 2017)

- Converted Micrel document MIC23156 to Microchip data sheet DS20005919A.
- Minor text changes throughout document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	X	X	XX	–	XX
Device		Default Output Voltage	Junction Temp. Range	Package		Media Type

Device:	MIC23156:		1.5A, 3 MHz Synchronous Buck Regulator with HyperLight Load® and I²C Control for Dynamic Voltage Scaling
Output Voltage:	0	=	1.0V (V_{SEL} = Low), 0.8V (V_{SEL} = High)
Junction Temperature Range:	Y	=	–40°C to +125°C
Package:	CS	=	16-Ball 1.81 mm x 1.71 mm WLCSP
	ML	=	17-Lead 2.5 mm x 2.8 mm CQFN
Media Type:	T5	=	500/Reel (ML Package only)
	TR	=	5,000/Reel (ML Package only)
	TR	=	3,000/Reel (CS Package only)

Examples:

a) MIC23156-0YCS-TR: MIC23156, 1.0V/0.8V Default Output Voltage, –40°C to +125°C Junction Temp. Range, 16-Ball WLCSP, 3,000/Reel

b) MIC23156-0YML-TR: MIC23156, 1.0V/0.8V Default Output Voltage, –40°C to +125°C Junction Temp. Range, 17-Lead CQFN, 5,000/Reel

c) MIC23156-0YML-T5: MIC23156, 1.0V/0.8V Default Output Voltage, –40°C to +125°C Junction Temp. Range, 17-Lead CQFN, 500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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