

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC540F, TC74VHC540FW, TC74VHC540FT
TC74VHC541F, TC74VHC541FW, TC74VHC541FT**OCTAL BUS BUFFER****TC74VHC540 F / FW / FT INVERTED, 3 - STATE OUTPUTS**
TC74VHC541 F / FW / FT NON - INVERTED, 3 - STATE OUTPUTS

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74VHC540/TC74VHC541 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

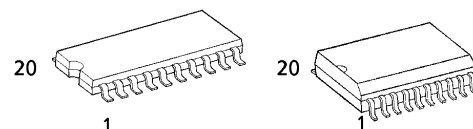
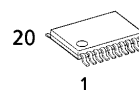
The TC74VHC540 is an inverting type, and the TC74VHC541 is a non-inverting type.

When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

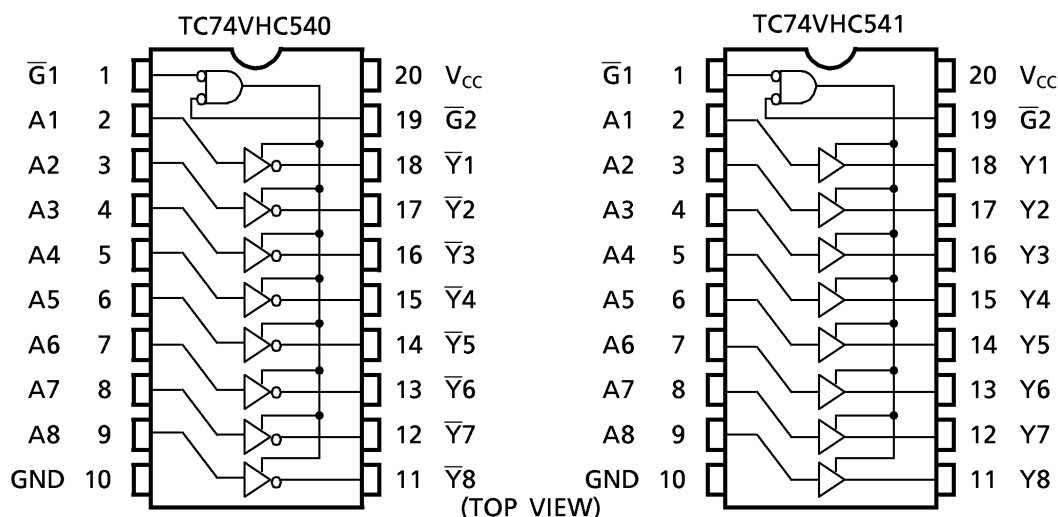
FEATURES:

- High Speed..... $t_{pd} = 3.7\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise..... $V_{OLP} = 1.2\text{V} (\text{Max.})$
- Pin and Function Compatible with 74ALS540/541

F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)FT (TSSOP20-P-0044-0.65)
Weight : 0.08g (Typ.)**TRUTH TABLE**

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	A_n	Y_n	$\overline{Y}_n$
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X : Don't Care
Z : High Impedance
 Y_n : TC74VHC541
 $\overline{Y}_n$: TC74VHC540

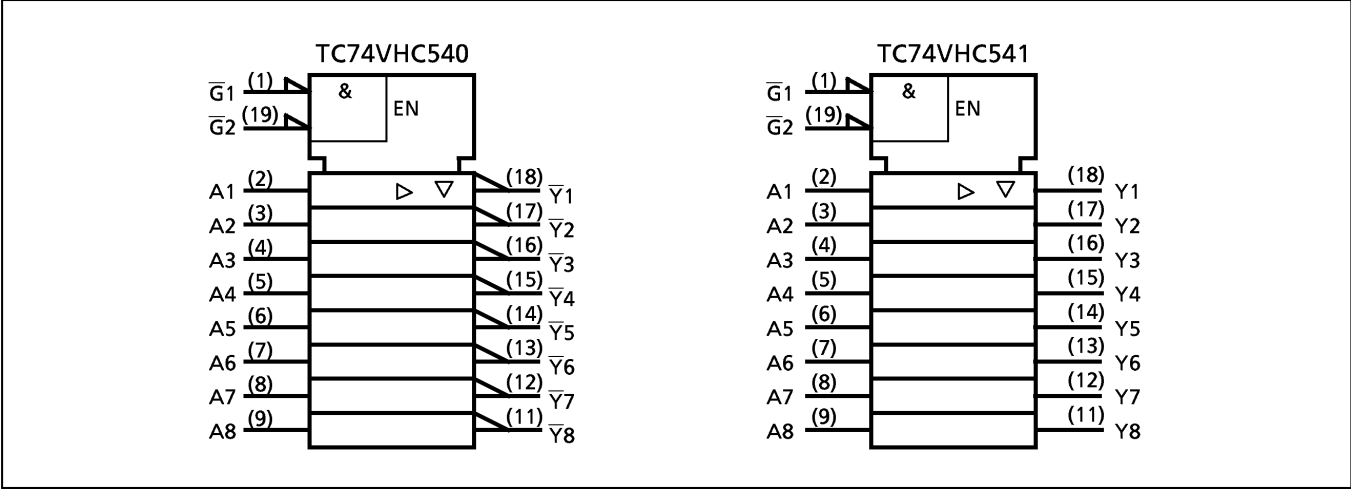
PIN ASSIGNMENT

(TOP VIEW)

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Input Rise and Fall Time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low - Level Input Voltage	V _{IL}			2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I _{OH} = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I _{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
				V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	
Propagation Delay Time (TC74VHC540)	t_{PLH} t_{PHL}		3.3 ± 0.3	15	—	4.8	7.0	1.0	8.5
				50	—	7.3	10.5	1.0	12.0
			5.0 ± 0.5	15	—	3.7	5.0	1.0	6.0
				50	—	5.2	7.0	1.0	8.0
Propagation Delay Time (TC74VHC541)	t_{PLH} t_{PHL}		3.3 ± 0.3	15	—	5.0	7.0	1.0	8.5
				50	—	7.5	10.5	1.0	12.0
			5.0 ± 0.5	15	—	3.5	5.0	1.0	6.0
				50	—	5.0	7.0	1.0	8.0
3— State Output Enable Time	t_{pZL} t_{pZH}	RL = 1k Ω	3.3 ± 0.3	15	—	6.8	10.5	1.0	12.5
				50	—	9.3	14.0	1.0	16.0
			5.0 ± 0.5	15	—	4.7	7.2	1.0	8.5
				50	—	6.2	9.2	1.0	10.5
3— State Output Disable Time	t_{pLZ} t_{pHZ}	RL = 1k Ω	3.3 ± 0.3	50	—	11.2	15.4	1.0	17.5
			5.0 ± 0.5	50	—	6.0	8.8	1.0	10.0
Output to Output Skew	t_{osHL} t_{osLH}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5
			5.0 ± 0.5	50	—	—	1.0	—	1.0
Input Capacitance	C _{IN}				—	4	10	—	10
Output Capacitance	C _{OUT}				—	6	—	—	—
Power Dissipation Capacitance (Note 2)	C _{PD}	TC74VHC540			—	17	—	—	—
		TC74VHC541			—	18	—	—	—

Note (1) Parameter guaranteed by design. $t_{\text{osLH}} = |t_{\text{pLH m}} - t_{\text{pLH n}}|$, $t_{\text{osHL}} = |t_{\text{pHL m}} - t_{\text{pHL n}}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

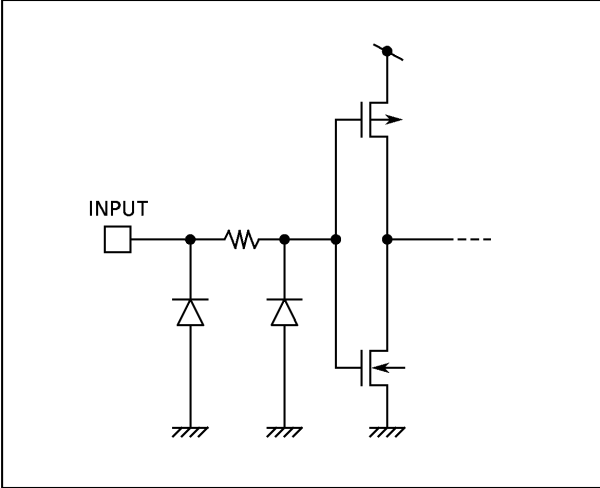
$$I_{\text{CC (opr.)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 8 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

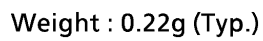
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic VOL	VOLP	CL = 50pF	5.0	0.7 (0.9)	1.0 (1.2)	V
Quiet Output Minimum Dynamic VOL	VOLV	CL = 50pF	5.0	-0.7 (-0.9)	-1.0 (-1.2)	V
Minimum High Level Dynamic Input Voltage	VIHD	CL = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	VILD	CL = 50pF	5.0	—	1.5	V

(Note) The value in () only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT



Unit in mm



Unit in mm

Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm

