

Features

- Very Low-cost Configuration Memory
- Programmable 1,048,576 x 1, 2,097,152 x 1, 4,194,304 x 1 and 7,340,032 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- 1.8V, 2.5V, and 3.3V I/O
- 3.3V Supply Voltage
- Program Support using an Atmel Programmer or Industry-standard Third Party Programmers
- In-System Programmable (ISP) via JTAG Interface (IEEE 1532)
- IEEE 1149.1 Boundary-scan Testability
- Simple Interface to SRAM FPGAs
- Pin Compatible with Xilinx® XCFxxS Series Platform Flash PROM to Configure Xilinx Spartan® and Virtex® FPGAs
- Cascadable Read-back to Support Additional Configurations or Higher-density FPGAs
- Low-power CMOS FLASH Process
- Available in 20-lead TSSOP Package
- Low-power Standby Mode
- Fast Serial Download Speeds up to 33 MHz
- Endurance: 100,000 Write Cycles Typical
- Green (Pb/Halide-free/RoHS Compliant) Package
- Functionally-compatible with Existing AT17 Series Configuration Memories to Configure Atmel AT40KAL Series FPGAs

AT18F Series Configuration Memory Offering

| | AT18F010 | AT18F002 | AT18F040 | AT18F080 |
|---------------------|---------------|----------|----------|----------|
| Density | 1 Mbit | 2 Mbit | 4 Mbit | 7 Mbit |
| JTAG Programming | Yes | | | |
| VCCINT | 3.3V | | | |
| VCCO | 1.8-3.3V | | | |
| VCCJ | 1.8-3.3V | | | |
| Configuration Clock | 33 MHz | | | |
| Package | 20-lead TSSOP | | | |
| Green Package | Yes | | | |

1. Description

The AT18F Series of JTAG In-System Programmable Configuration PROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT18F Series device is packaged in a 20-lead TSSOP. The AT18F Series Configurator uses a simple serial-access procedure to configure one or more FPGA devices.

The AT18F Series Configurators can be programmed with Atmel or industry-standard, third-party, stand-alone programmers such as BP, Data I/O, Hi-Lo, etc.



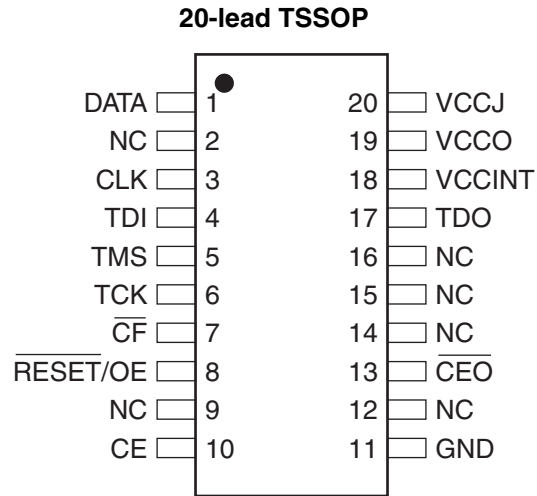
FPGA Configuration Flash Memory

AT18F010
AT18F002
AT18F040
AT18F080

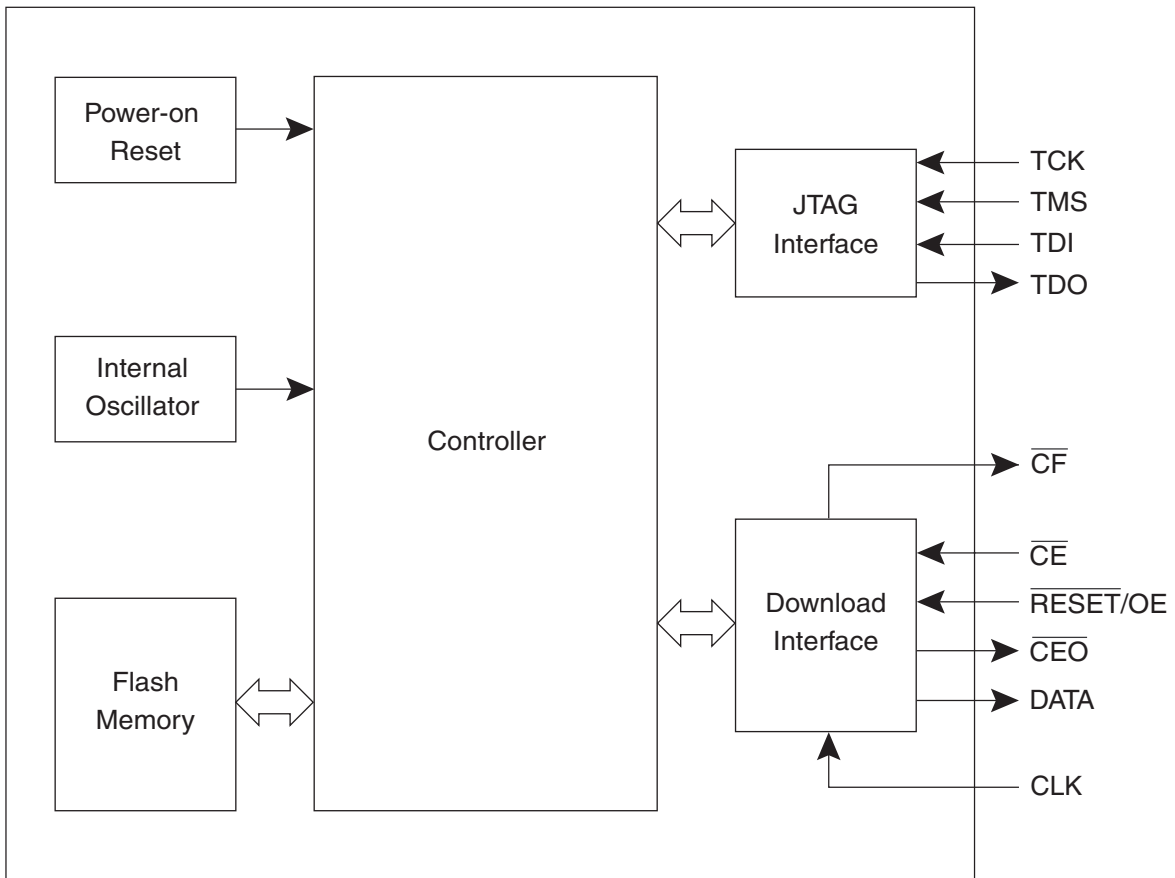
Preliminary



2. Pin Configuration



3. Block Diagram



4. Device Description

The download interface of the configuration memory will directly communicate with the FPGA through the interface-control signals (CLK, $\overline{\text{RESET/OE}}$, $\overline{\text{CE}}$) to initialize and terminate configuration. All FPGA devices in the master serial mode can control the entire configuration process to receive data from the configuration device without requiring an external intelligent controller. When FPGA devices are used in slave serial mode, an external clock signal can be applied to the CLK pin of an AT18F series device as a configuration loading clock. Multiple FPGAs that are setup in Master Serial and Slave Serial modes can also be used to control the configuration process to obtain data from a single configurator or cascaded configurators. Please contact Atmel at configurator@atmel.com for detailed descriptions.

The $\overline{\text{CF}}$ pin is used as an optional input pin for the JTAG CONFIG instruction to initialize the FPGA configuration without requiring powering down the device. The $\overline{\text{RESET/OE}}$ and $\overline{\text{CE}}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{\text{RESET/OE}}$ is driven Low, the configuration device resets its address counter and tri-states its DATA pin. The $\overline{\text{CE}}$ pin also controls the output of the AT18F Series Configurator. If $\overline{\text{CE}}$ is held High after the $\overline{\text{RESET/OE}}$ reset pulse, the counter is reset and the DATA output pin is tri-stated.

When the configurator has driven out all of its data and $\overline{\text{CEO}}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.



AT18F series devices are compatible with a portion of the Xilinx's FPGA device families.

Table 4-1. AT18F Series Configurator Compatibility with Xilinx FPGAs

| Atmel | Xilinx | | Atmel | Xilinx | |
|---------------|--------------|---------------|-----------------|---------------|-----------|
| AT18F010-30XU | Virtex-II | XC2V40 | AT18F040-30XU | Virtex-II Pro | XC2VP4 |
| | | XC2V80 | | Virtex-II | XC2V500 |
| | Virtex-E | XCV50E | | | XC2V1000 |
| | | XCV100E | | Virtex-E | XCV400E |
| | Virtex | XCV50 | | | XCV405E |
| | | XCV100 | | | XCV600E |
| | | XCV150 | | Virtex | XCV400 |
| | Spartan-3E | XC3S100E | | | XCV600 |
| | Spartan-3 | XC3S50 | | Spartan-3E | XC3S500E |
| | | XC3S200 | | | XC3S1200E |
| | Spartan-IIIE | XC2S50E | | Spartan-3L | XC3S1000L |
| | | XC2S100E | | Spartan-3 | XC3S1000 |
| | Spartan-II | XC2S15 | | Spartan-IIIE | XC2S400E |
| | | XC2S30 | | | XC2S600E |
| XC2S50 | | AT18F080-30XU | Virtex-5 LX | XC5VLX30 | |
| XC2S100 | | | Virtex-4 LX | XC4VLX15 | |
| XC2S150 | | | | XC4VLX25 | |
| Virtex-II Pro | XC2VP2 | | Virtex-4 FX | XC4VFX12 | |
| | XC2V250 | | | XC4VFX20 | |
| Virtex-E | XCV200E | | Virtex-II Pro X | XC2VPX20 | |
| | XCV300E | | Virtex-II Pro | XC2VP7 | |
| Virtex | XCV200 | | | XC2VP20 | |
| | XCV300 | | Virtex-II | XC2V1500 | |
| Spartan-3E | XC3S250E | | | XC2V2000 | |
| Spartan-3 | Spartan-IIIE | | XC3S400 | XCV812E | |
| | | | XC2S150E | Virtex-E | XCV1000E |
| XC2S200E | | | XCV1600E | | |
| Spartan-IIIE | XC2S300E | | Virtex | XCV800 | |
| | Spartan-II | XC2S200 | | XCV1000 | |
| | | Spartan-3E | XC3S1600E | | |
| Spartan-3L | XC3S1500L | Spartan-3L | XC3S1500L | | |
| | Spartan-3 | | XC3S1500 | | |
| XC3S2000 | | | | | |

5. Programming

AT18Fxx devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the AT18Fxx via the PC. ISP is performed by using either a download cable or a comparable board tester or a simple microprocessor interface.

To allow ISP programming support by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by the Atmel JCPS Software. Conversion to other ATE tester format beside SVF is also possible

AT18Fxx devices can also be programmed using standard third-party programmers such as BP, Datal/O, Hi-Lo, etc. Factory-preprogrammed devices, as required by customers, are also available for certain ordering quantities.

Contact your local Atmel representatives or Atmel PLD applications for details.

5.1 JTAG-BST Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the AT18F series. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The AT18Fxx series does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The six JTAG BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS and IDCODE. BST on the AT18Fxx series is implemented using the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the AT18Fxx series.

The AT18F series uses the four JTAG-standard I/O pins for In-System programming (ISP). The AT18F series is programmable through the four JTAG pins using programming algorithm compatible with the IEEE JTAG Standard 1532. Programming is performed by using selectable voltage levels of the programming signals from the JTAG ISP interface.

5.2 JTAG Boundary-scan Cell (BSC) Testing

The AT18F series has I/Os that contain boundary-scan cells (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller.

6. Pin Description

Table 6-1. Pin Descriptions

| Name | Type | 20-lead TSSOP |
|------------------------------|--------------|----------------------|
| DATA | I/O | 1 |
| CLK | I | 3 |
| $\overline{\text{RESET/OE}}$ | I | 8 |
| $\overline{\text{CE}}$ | I | 10 |
| $\overline{\text{CF}}$ | I | 7 |
| $\overline{\text{CEO}}$ | O | 13 |
| TMS | I | 5 |
| TCK | I | 6 |
| TDI | I | 4 |
| TDO | O | 17 |
| VCCINT | I | 18 |
| NC | - | 2, 9, 12, 14, 15, 16 |
| VCCO | Power Supply | 19 |
| GND | Ground | 11 |
| VCCJ | Power Supply | 20 |

6.1 DATA (D0)

Open-collector bi-directional data pin. This pin has an internal 20 K Ω pull-up resistor.

6.2 CLK

Clock input. Used to increment the internal address and bit counter for reading and programming. This pin has an internal 20 K Ω pull-up resistor.

6.3 $\overline{\text{RESET/OE}}$

Output Enable (active High) and $\overline{\text{RESET}}$ (active Low). A Low level on $\overline{\text{RESET/OE}}$ resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver. This pin has an internal 20 K Ω pull-up resistor.

6.4 $\overline{\text{CE}}$

Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. This pin has an internal 20 K Ω pull-up resistor.

6.5 $\overline{\text{CF}}$

Configuration Pulse (open-drain output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down the FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.

6.6 $\overline{\text{CEO}}$

Chip Enable Output for configuration download. This output goes Low when the internal address counter of the device has reached its maximum value which signals that all configuration data is being clocked out of the device. In a daisy chain of AT18F Series devices, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. It will stay Low as long as $\overline{\text{CE}}$ is Low and OE is High. It will then follow $\overline{\text{CE}}$ until OE goes Low; thereafter, $\overline{\text{CEO}}$ will stay High until the entire memory device is read again.

6.7 TMS

JTAG Mode Control Input. The state of TMS with the rising edge of TCK determines the state transitions of the Test Access Port (TAP) controller. TMS has an internal 50 K Ω weak pull-up to V_{CCJ} to provide a logic 1 to the device.

6.8 TCK

JTAG Clock Input. This pin is the JTAG clock input to the TAP controller of the device.

6.9 TDI

JTAG Serial Data Input. This pin is the serial input to all JTAG instructions and data registers. An internal 50 K Ω weak pull-up to V_{CCJ} provides a logic 1 to the device.

6.10 TDO

JTAG Serial Data Output. This pin is the serial output to all JTAG instruction and data registers. An internal 50 K Ω weak pull-up to V_{CCJ} provides a logic 1 to the device if the pin is not driven.

6.11 VCCINT

+3.3V supply voltage for internal logic.

6.12 NC

No Connect Pin. This pin is not connected to any internal logic of the device and can be left floating.

6.13 VCCO

Supply voltage for I/O drivers (1.8V, 3.3V, or 3.3V).

6.14 VCCJ

Supply voltage for JTAG I/O drivers (1.8V, 3.3V, or 3.3V).

6.15 GND

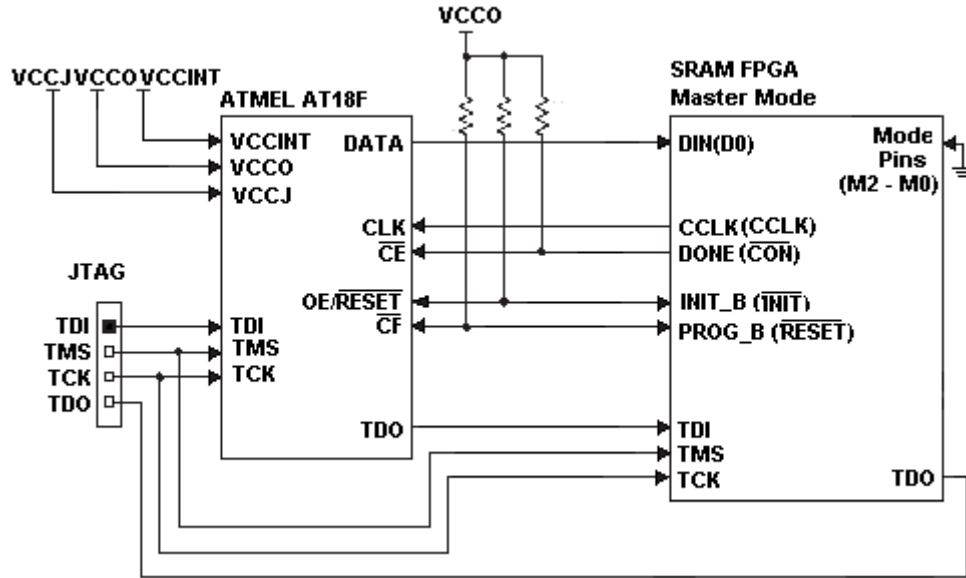
Power supply ground.

7. Standby Mode

The AT18F Series Configurators enter a low-power standby mode whenever the JTAG mode is inactive and $\overline{\text{CE}}$ is asserted High. In this mode, the AT18F Configurator consumes less than 1 mA of current at 3.3V. The output remains in a high-impedance state regardless of the state of the OE input.

8. Configuration Memory to FPGA Device Interface Connection Diagrams

Figure 8-1. General Connection Diagram for Loading FPGA from Configurator and JTAG Signals



- Notes:
1. Signals within parenthesis will be applied to Atmel AT40AK FPGA.
 2. For details of the circuit connection, please contact factory.

9. Absolute Maximum Ratings*

| | |
|---|--------------------------------|
| Operating Temperature..... | -55° C to +125° C |
| Storage Temperature | -65° C to +150° C |
| Voltage on Any Pin with Respect to Ground | -0.1V to V _{CC} +0.5V |
| Supply Voltage (V _{CC}) | -0.5V to +3.6V |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.)..... | 260° C |
| ESD (R _{ZAP} = 1.5K, C _{ZAP} = 100 pF)..... | 2000V |

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

10. Operating Conditions

T_{AI} = -40° C to +85° C for Industrial and 0° C to +70° C for Commercial

| Symbol | Description | Min | Typ | Max | Units | |
|--------------------|-------------------------------------|----------------|-------------------------|-----|-------------------------|---|
| V _{CCINT} | Supply Voltage for Internal Logic | 3.0 | 3.3 | 3.6 | V | |
| V _{CCO} | Supply Voltage for I/O Drivers | 3.3V Operation | 3.0 | 3.3 | 3.6 | V |
| | | 2.5V Operation | 2.3 | 2.5 | 2.7 | |
| | | 1.8V Operation | 1.7 | 1.8 | 1.9 | |
| V _{CCJ} | Supply Voltage for JTAG I/O Drivers | 3.3V Operation | 3.0 | 3.3 | 3.6 | V |
| | | 2.5V Operation | 2.3 | 2.5 | 2.7 | |
| | | 1.8V Operation | 1.7 | 1.8 | 1.9 | |
| V _{IL} | Input Low Voltage | 3.3V Operation | -0.3 | | 0.8 | V |
| | | 2.5V Operation | -0.3 | | 0.7 | |
| | | 1.8V Operation | -0.3 | | 0.35 x V _{CCO} | |
| V _{IH} | Input High Voltage | 3.3V Operation | 2.0 | | 3.9 | V |
| | | 2.5V Operation | 1.7 | | 3.9 | |
| | | 1.8V Operation | 0.65 x V _{CCO} | | 3.9 | |

11. DC Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|--------------|---|--|-----|------------------|------|---------|
| I_{CCINT} | Internal Voltage Supply Current, Active Mode | 33 MHz | | | 10 | mA |
| I_{CCIO} | I/O Drive Supply Current, Active Mode | 33 MHz | | | 10 | mA |
| I_{CCJ} | JTAG Supply Current, Active Mode | | | | 5 | mA |
| I_{CCINTS} | Internal Voltage Supply Current, Standby Mode | $V_{CCINT} = 3.6V$, $V_{CIO} = 3.6V$ | | | 1 | mA |
| I_{CCIOS} | Output Drive Supply Current, Standby Mode | $V_{CCINT} = 3.6V$, $V_{CIO} = 3.6V$ | | | 1 | mA |
| I_{CCJS} | JTAG Supply Current, Standby Mode | $V_{CCINT} = 3.6V$, $V_{CIO} = 3.6V$ | | | 1 | mA |
| I_{IL} | Input or I/O Low Leakage | | | 1 | 10 | μA |
| I_{IH} | Input or I/O High Leakage | | -10 | 10 | 10 | μA |
| V_{OL} | Output Low Voltage | 3.3V Operation | | | 0.4 | V |
| | | 2.5V Operation | | | 0.4 | |
| | | 1.8V Operation | | | 0.45 | |
| V_{OH} | Output High Voltage | 3.3V Operation | | $V_{CCO} - 0.4$ | | V |
| | | 2.5V Operation | | $V_{CCO} - 0.4$ | | |
| | | 1.8V Operation | | $V_{CCO} - 0.45$ | | |

12. AC Characteristics

Figure 12-1. AT18Fxx as Configuration Slave with CLK Input Pin as Clock Source

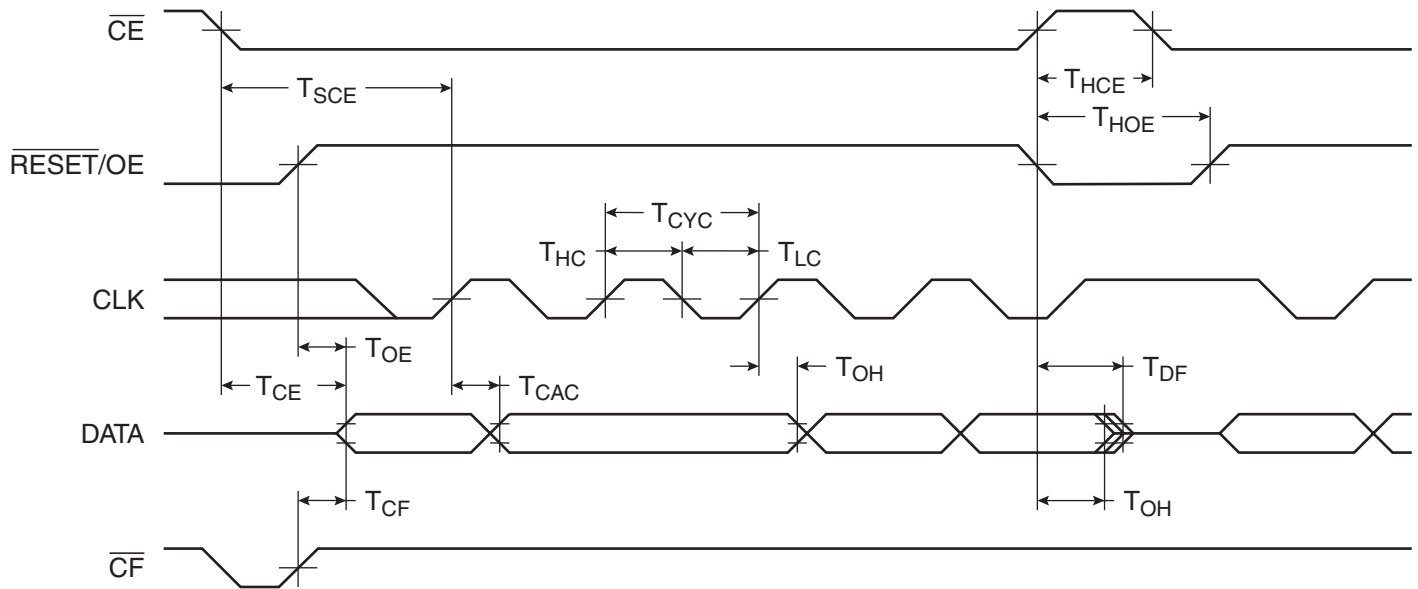


Table 12-1. AC Characteristics over Operating Conditions

| Symbol | Description | Min | Max | Units |
|-------------|--|-----|-----|---------|
| T_{CF} | CF to Data Delay | 20 | 50 | μ s |
| T_{OE} | \overline{RESET}/OE to Data Delay | | 10 | ns |
| T_{CE} | CE to Data Delay | 20 | | μ s |
| T_{CAC} | CLK to Data Delay | | 15 | ns |
| T_{OH} | Data Hold from \overline{CE} , \overline{RESET}/OE , CLK, or \overline{CF} | | 15 | ns |
| T_{DF} | \overline{CE} or \overline{RESET}/OE to Data Float Delay | | 25 | ns |
| T_{CYC} | Clock Period | 30 | | ns |
| T_{LC} | CLK Low Time | 15 | | ns |
| T_{HC} | CLK High Time | 15 | | ns |
| T_{SCE} | \overline{CE} Setup Time to CLK | 20 | | μ s |
| T_{HCE} | \overline{CE} Hold Time | 250 | | ns |
| T_{HOE} | \overline{RESET}/OE Hold Time | 250 | | ns |
| T_{BLKE} | Block Erase Time | 0.7 | 1 | s |
| T_{ERASE} | Bulk Erase Time – 1M | | 3 | s |
| | Bulk Erase Time – 2M | | 5 | s |
| | Bulk Erase Time – 4M | | 9 | s |
| | Bulk Erase Time – 8M | | 15 | s |
| T_{CK_J} | TAP Clock Minimum Period | 100 | | ns |

Figure 12-2. AC Characteristics when Cascading

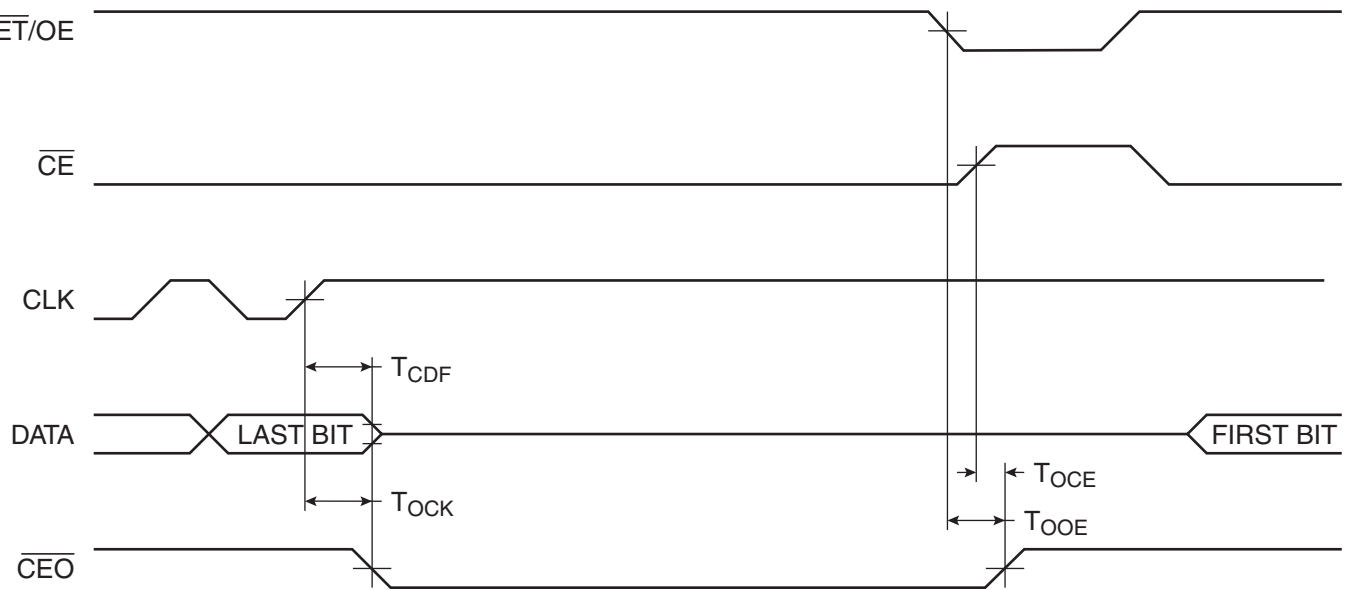


Table 12-2. AC Characteristics When Cascading

| Symbol | Description | Min | Max | Units |
|------------------|---|-----|-----|-------|
| T_{CDF} | CLK to Output Float Delay | | 25 | ns |
| T_{OCK} | CLK to $\overline{\text{CEO}}$ Delay | | 20 | ns |
| T_{OCE} | $\overline{\text{CE}}$ to $\overline{\text{CEO}}$ Delay | | 20 | ns |
| T_{OOE} | $\overline{\text{RESET/OE}}$ to $\overline{\text{CEO}}$ Delay | | 20 | ns |

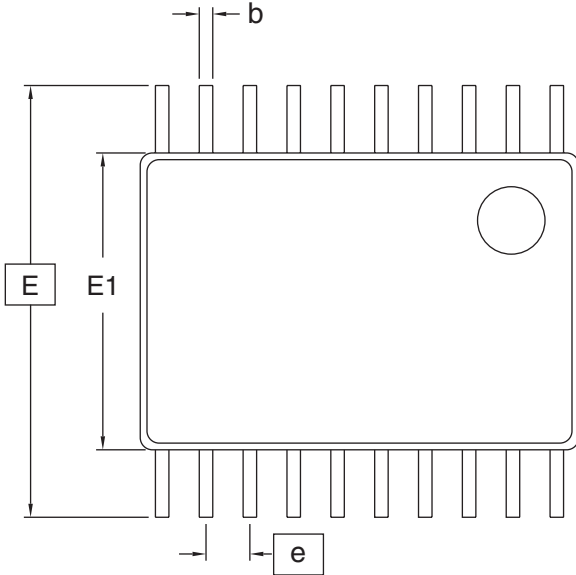
13. Ordering Information

| Memory Size | Ordering Code | Package | Operation Range |
|-------------|---------------|-----------------|---------------------------------|
| 1-Mbit | AT18F010-30XU | 20A2 - 20 TSSOP | Industrial (-40° C to 85° C) |
| 2-Mbit | AT18F002-30XU | 20A2 - 20 TSSOP | Industrial (-40° C to 85° C) |
| 4-Mbit | AT18F040-30XU | 20A2 - 20 TSSOP | Industrial (-40° C to 85° C) |
| 7-Mbit | AT18F080-30XU | 20A2 - 20 TSSOP | Industrial (-40° C to 85° C) |

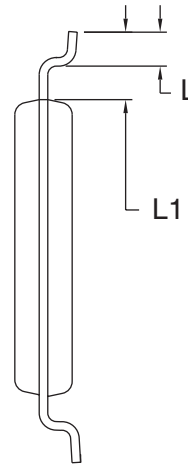
| Package Type | |
|--------------|---|
| 20A2 | 20-lead, 0.65 mm Wide, Plastic Think-Shrink Small Outline (TSSOP) |

14. Packaging Information

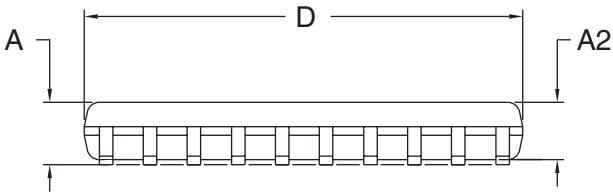
14.1 20A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|------|
| D | 6.40 | 6.50 | 6.60 | 2, 5 |
| E | 6.40 BSC | | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| A | – | – | 1.20 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | – | 0.30 | 4 |
| e | 0.65 BSC | | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | 1.00 REF | | | |

- Notes:
1. This drawing is for general information only. Please refer to JEDEC Drawing MO-153, Variation AC, for additional information.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E1 to be determined at Datum Plane H.

6/3/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20A2, 20-lead (4.4 x 6.5 mm Body), 0.65 pitch,
Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

20A2

REV.

C

15. Revision History

| Revision Level – Release Date | History |
|-------------------------------|------------------|
| A – January 2008 | Initial release. |



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