1 MSPS, 12-/10-/8-Bit ADCs in 6-Lead SOT-23

AD7476/AD7477/AD7478

FEATURES

- **Fast throughput rate: 1 MSPS**
- **Specified for V_{DD} of 2.35 V to 5.25 V**
- **Low power**
  - **3.6 mW at 1 MSPS with 3 V supplies**
  - **15 mW at 1 MSPS with 5 V supplies**
- **Wide input bandwidth**
  - **70 dB SNR at 100 kHz input frequency**
- **Flexible power/serial clock speed management**
- **No pipeline delays**
- **High speed serial interface**
  - **SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible**
- **Standby mode: 1 µA maximum**
- **6-lead SOT-23 package**

APPLICATIONS

- **Battery-powered systems**
  - **Personal digital assistants**
  - **Medical instruments**
  - **Mobile communications**
- **Instrumentation and control systems**
- **Data acquisition systems**
- **High speed modems**
- **Optical sensors**

FUNCTIONAL BLOCK DIAGRAM

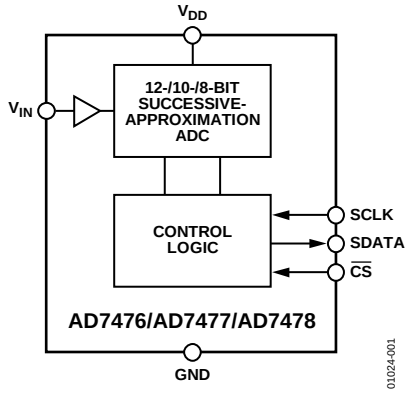


Figure 1.

GENERAL DESCRIPTION

The AD7476/AD7477/AD7478[1] are, respectively, 12-bit, 10-bit, and 8-bit, high speed, low power, successive approximation ADCs. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. Each part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 6 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is initiated at this point. There are no pipeline delays associated with these parts.

The AD7476/AD7477/AD7478 use advanced design techniques to achieve very low power dissipation at high throughput rates. The reference for the parts is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus, the analog input range for the parts are 0 V to V_{DD}. The conversion rate is determined by the SCLK.

[1] Protected by U.S. Patent No. 6,681,332.

PRODUCT HIGHLIGHTS

1. First 12-/10-/8-Bit ADCs in SOT-23 Packages.
2. High Throughput with Low Power Consumption.
3. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced while not converting. The parts also feature a shutdown mode to maximize power efficiency at lower throughput rates. Current consumption is 1 µA maximum when in shutdown mode.
4. Reference Derived from the Power Supply.
5. No Pipeline Delay. The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

Rev. F

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SPECIFICATIONS

AD7476 SPECIFICATIONS

A version: V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted; S and B versions: V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 12 MHz, f_{SAMPLE} = 600 kSPS, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Version[1,2]	B Version[1,2]	S Version[1,2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 100 kHz sine wave
Signal-to-(Noise + Distortion) (SINAD)[3]	69	70	69	dB min	B version, V_{DD} = 2.4 V to 5.25 V
	70		70	dB min	T_A = 25°C
		71.5		dB typ	
Signal-to-Noise Ratio (SNR)[3]	70	71	70	dB min	B version, V_{DD} = 2.4 V to 5.25 V
		72.5		dB typ	
Total Harmonic Distortion (THD)[3]	−80	−78	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−82	−80	−80	dB typ	
Intermodulation Distortion (IMD)[3]					
Second-Order Terms	−78	−78	−78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Third-Order Terms	−78	−78	−78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Aperture Delay	10	10	10	ns typ	
Aperture Jitter	30	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY					S, B versions, V_{DD} = (2.35 V to 3.6 V)[4]; A version, V_{DD} = (2.7 V to 3.6 V)
Resolution	12	12	12	Bits	
Integral Nonlinearity[3]		±1.5	±1.5	LSB max	
	±1	±0.6	±0.6	LSB typ	
Differential Nonlinearity[3]		−0.9/+1.5	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
	±0.75	±0.75	±0.75	LSB typ	
Offset Error[3]		±1.5	±2	LSB max	
	±0.5			LSB typ	
Gain Error[3]		±1.5	±2	LSB max	
	±0.5			LSB typ	
ANALOG INPUT					
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	±1	µA max	
Input Capacitance	30	30	30	pF typ	
LOGIC INPUT					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
	1.8	1.8	1.8	V min	V_{DD} = 2.35 V
Input Low Voltage, V_{INL}	0.4	0.4	0.4	V max	V_{DD} = 3 V
	0.8	0.8	0.8	V max	V_{DD} = 5 V
Input Current, I_{IN}, SCLK Pin	±1	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	±1	±1	µA typ	
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUT					
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	10	10	10	pF max	
Output Coding	Straight (Natural) Binary				

Parameter	A Version[1,2]	B Version[1,2]	S Version[1,2]	Unit	Test Conditions/Comments
CONVERSION RATE					
Conversion Time	0.8	1.33	1.33	µs max	16 SCLK cycles
Track-and-Hold Acquisition Time	500	500	500	ns max	Full-scale step input
	350	400	400	ns max	Sine wave input ≤ 100 kHz
Throughput Rate	1000	600	600	kSPS max	See Serial Interface section
POWER REQUIREMENTS					
V_{DD}	2.35/5.25	2.35/5.25	2.35/5.25	V min/max	
I_{DD}					Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	2	2	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK on or off
	1	1	1	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK on or off
Normal Mode (Operational)	3.5	3	3	mA max	V_{DD} = 4.75 V to 5.25 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[6]
	1.6	1.4	1.4	mA max	V_{DD} = 2.35 V to 3.6 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[6]
Full Power-Down Mode	1	1	1	µA max	SCLK off
	80	80	80	µA max	SCLK on
Power Dissipation[7]					
Normal Mode (Operational)	17.5	15	15	mW max	V_{DD} = 5 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[6]
	4.8	4.2	4.2	mW max	V_{DD} = 3 V, $f_{SAMPLE} = f_{SAMPLE}MAX$[6]
Full Power-Down	5	5	5	µW max	V_{DD} = 5 V, SCLK off
	3	3	3	µW max	V_{DD} = 3 V, SCLK off

[1] Temperature range for A and B versions is −40°C to +85°C; temperature range for S version is −55°C to +125°C.
[2] Operational from V_{DD} = 2.0 V.
[3] See the Terminology section.
[4] Maximum B and S version specifications apply as typical figures when V_{DD} = 5.25 V.
[5] Guaranteed by characterization.
[6] For A version: $f_{SAMPLE}MAX$ = 1 MSPS; B and S versions: $f_{SAMPLE}MAX$ = 600 kSPS.
[7] See the Power vs. Throughput Rate section.

AD7477 SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Version[1,2]	S Version[1,2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 100 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-(Noise + Distortion) (SINAD)	61	61	dB min	
Total Harmonic Distortion (THD)[3]	−73	−73	dB max	
Peak Harmonic or Spurious Noise (SFDR)[3]	−74	−74	dB max	
Intermodulation Distortion (IMD)[3]				
Second-Order Terms	−78	−78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Third-Order Terms	−78	−78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Aperture Delay	10	10	ns typ	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	10	10	Bits	
Integral Nonlinearity[3]	±1	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed no missed codes to 10 bits
Offset Error[3]	±1	±1	LSB max	
Gain Error[3]	±1	±1	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V
	0.4	0.4	V max	V_{DD} = 3 V
Input Current, I_{IN}, SCLK Pin	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	±1	µA typ	
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	400	400	ns max	
Throughput Rate	1	1	MSPS max	See Serial Interface section

Parameter	A Version[1,2]	S Version[1,2]	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	2.7/5.25	2.7/5.25	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	2	mA typ	V_{DD} = 4.75 V to 5.25 V; SCLK on or off
	1	1	mA typ	V_{DD} = 2.7 V to 3.6 V; SCLK on or off
Normal Mode (Operational)	3.5	3.5	mA max	V_{DD} = 4.75 V to 5.25 V; f_{SAMPLE} = 1 MSPS
	1.6	1.6	mA max	V_{DD} = 2.7 V to 3.6 V; f_{SAMPLE} = 1 MSPS
Full Power-Down Mode	1	1	µA max	SCLK off
	80	80	µA max	SCLK on
Power Dissipation[5]				
Normal Mode (Operational)	17.5	17.5	mW max	V_{DD} = 5 V; f_{SAMPLE} = 1 MSPS
	4.8	4.8	mW max	V_{DD} = 3 V; f_{SAMPLE} = 1 MSPS
Full Power-Down	5	5	µW max	V_{DD} = 5 V; SCLK off

[1] Temperature range for A version is −40°C to +85°C; temperature range for S version is −55°C to +125°C.
[2] Operational from V_{DD} = 2.0 V, with input high voltage, V_{INH} = 1.8 V minimum.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

AD7478 SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	A Version[1,2]	S Version[1,2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 100 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-(Noise + Distortion) (SINAD)[3]	49	49	dB min	
Total Harmonic Distortion (THD)[3]	−65	−65	dB max	
Peak Harmonic or Spurious Noise (SFDR)[3]	−65	−65	dB max	
Intermodulation Distortion (IMD)[3]				
Second-Order Terms	−68	−68	dB typ	fa = 498.7 kHz, fb = 508.7 kHz
Third-Order Terms	−68	−68	dB typ	fa = 498.7 kHz, fb = 508.7 kHz
Aperture Delay	10	10	ns typ	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	8	8	Bits	
Integral Nonlinearity[3]	±0.5	±0.5	LSB max	
Differential Nonlinearity[3]	±0.5	±0.5	LSB max	Guaranteed no missed codes to eight bits
Offset Error	±0.5	±0.5	LSB max	
Gain Error	±0.5	±0.5	LSB max	
Total Unadjusted Error (TUE)	±0.5	±0.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V
	0.4	0.4	V max	V_{DD} = 3 V
Input Current, I_{IN}, SCLK Pin	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	±1	µA typ	
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	400	400	ns max	
Throughput Rate	1	1	MSPS max	See Serial Interface section
POWER REQUIREMENTS				
V_{DD}	2.7/5.25	2.7/5.25	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	2	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK on or off
	1	1	mA typ	V_{DD} = 2.7 V to 3.6 V, SCLK on or off
Normal Mode (Operational)	3.5	3.5	mA max	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS
	1.6	1.6	mA max	V_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode	1	1	µA max	SCLK off
	80	80	µA max	SCLK on

Parameter	A Version[1,2]	S Version[1,2]	Unit	Test Conditions/Comments
Power Dissipation[5]				
Normal Mode (Operational)	17.5	17.5	mW max	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS
	4.8	4.8	mW max	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS
Full Power-Down	5	5	µW max	V_{DD} = 5 V, SCLK off

[1] Temperature range for A version is −40°C to +85°C; temperature range for S version is −55°C to +125°C.
[2] Operational from V_{DD} = 2.0 V, with input high voltage, V_{INH} = 1.8 V minimum.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

V_{DD} = 2.35 V to 5.25 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 4.

	Limit at T_{MIN}, T_{MAX}[1]			
Parameter[2,3]	**3 V**	**5 V**	**Unit**	**Description**
f_{SCLK}[4]	10	10	kHz min	
	20	20	MHz max	A version
	12	12	MHz max	B version
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	10	10	ns min	Minimum $\overline{CS}$ pulsewidth
t_2	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[5]	20	20	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[5]	40	20	ns max	Data access time after SCLK falling edge, A version
	70	20	ns max	Data access time after SCLK falling edge, B version
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulsewidth
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulsewidth
t_7	10	10	ns min	SCLK to data valid hold time
t_8[6]	10	10	ns min	SCLK falling edge to SDATA high impedance
	25	25	ns max	SCLK falling edge to SDATA high impedance
$t_{POWER-UP}$[7]	1	1	µs typ	Power-up time from full power-down

[1] 3 V specifications apply from V_{DD} = 2.7 V to 3.6 V for A version; 3 V specifications apply from V_{DD} = 2.35 V to 3.6 V for B version; 5 V specifications apply from V_{DD} = 4.75 V to 5.25 V.
[2] Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[3] Version A timing specifications apply to the AD7477 and AD7478 S version; B version timing specifications apply to the AD7476 S version.
[4] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[5] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[6] t_8 is derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, is the true bus relinquish time of the part and is independent of the bus loading.
[7] See Power-Up Time section.

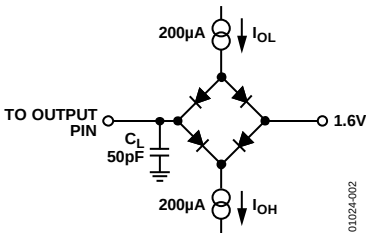


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial Range (A, B Versions)	–40°C to +85°C
Military Range (S Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-23 Package	
θ_{JA} Thermal Impedance	230°C/W
θ_{JC} Thermal Impedance	92°C/W
Lead Temperature, Soldering Reflow	
(10 sec to 30 sec)	235 (0/+5)°C
Pb-free Temperature Soldering Reflow	255 (0/+5)°C
ESD	3.5 kV

[1]Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

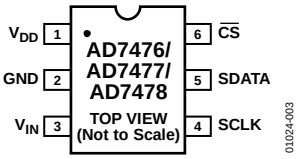


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7476/AD7477/AD7478 is from 2.35 V to 5.25 V.
2	GND	Analog Ground. Ground reference point for all circuitry on the part. All analog input signals should be referred to this GND voltage.
3	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476/AD7477/AD7478 conversion process.
5	SDATA	Data Out. Logic output. The conversion result is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476 consists of four leading zeros followed by the 12 bits of conversion data; this is provided MSB first. The data stream from the AD7477 consists of four leading zeros followed by the 10 bits of conversion data, followed by two trailing zeros, which is also provided MSB first. The data stream from the AD7478 consists of four leading zeros followed by the eight bits of conversion data, followed by four trailing zeros, which is provided MSB first.
6	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476/AD7477/AD7478 and framing the serial data transfer.

TYPICAL PERFORMANCE CHARACTERISTICS

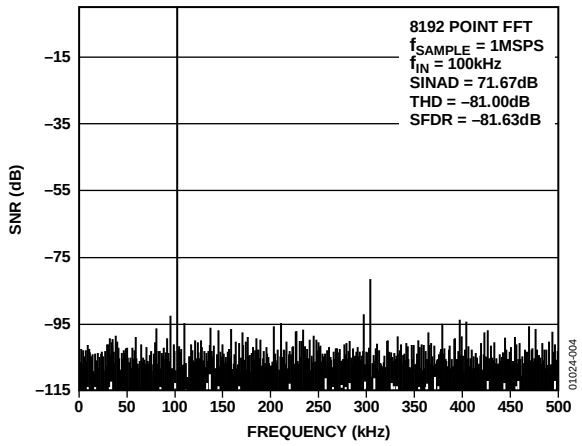


Figure 4. AD7476 Dynamic Performance at 1 MSPS

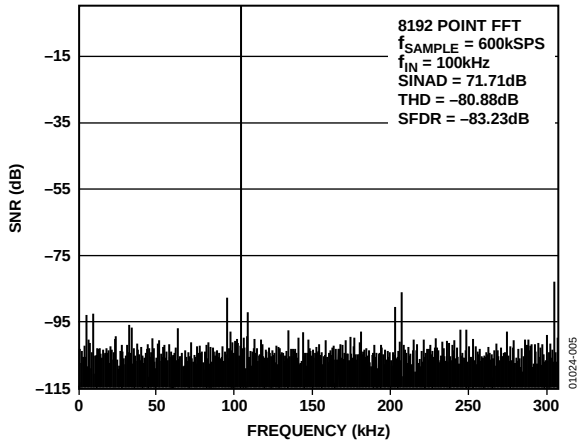


Figure 5. AD7476 Dynamic Performance at 600 kSPS

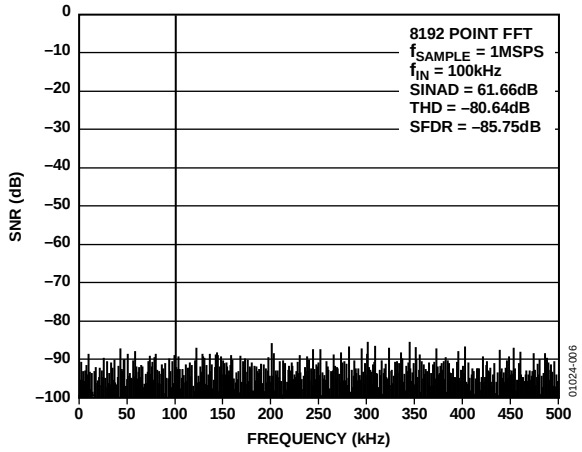


Figure 6. AD7477 Dynamic Performance at 1 MSPS

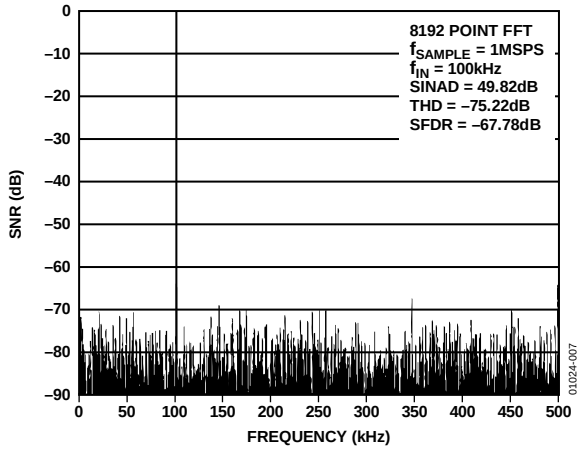


Figure 7. AD7478 Dynamic Performance at 1 MSPS

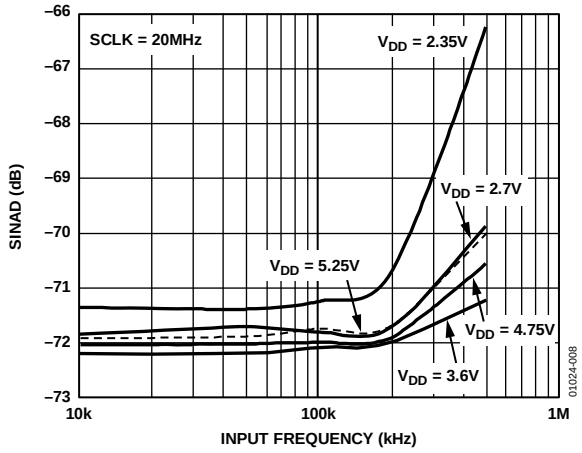


Figure 8. AD7476 SINAD vs. Input Frequency at 993 kSPS

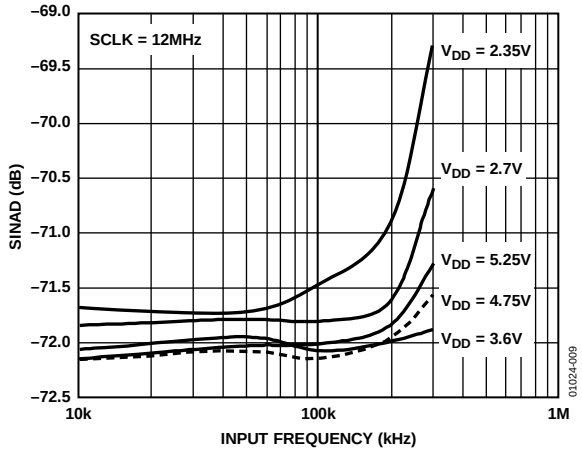


Figure 9. AD7476 SINAD vs. Input Frequency at 605 kSPS

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7476/AD7477, the endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition. For the AD7478, the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (such as AGND + 0.5 LSB). For the AD7478, this is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (such as AGND + 1 LSB).

Gain Error
For the AD7476/AD7477, this is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (such as V_{REF} – 1.5 LSB) after the offset error has been adjusted out. For the AD7478, this is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (such as V_{REF} – 1 LSB) after the offset error has been adjusted.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See the Serial Interface section for more details.

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(Noise + Distortion) = (6.02*N* + 1.76) dB

Thus, for a 12-bit converter, this is 74 dB; for a 10-bit converter it is 62 dB; and for an 8-bit converter it is 50 dB.

Total Unadjusted Error
This is a comprehensive specification that includes gain error, linearity error, and offset error.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7476/AD7477/AD7478, it is defined as:

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7476/AD7477/AD7478 are tested using the CCIF standard where two input frequencies are used (fa = 498.7 kHz and fb = 508.7 kHz). In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dB.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7476/AD7477/AD7478 are, respectively, 12-bit, 10-bit, and 8-bit, fast, micropower, single-supply ADCs. The parts can be operated from a 2.35 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7476/AD7477/AD7478 are capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

Each AD7476/AD7477/AD7478 provides an on-chip, track-and-hold ADC and a serial interface housed in a tiny 6-lead SOT-23 package, which offers considerable space-saving advantages. The serial clock input accesses data from the part and provides the clock source for the successive-approximation ADC. The analog input range is 0 V to V_{DD}. An external reference is not required for the ADC, nor is there a reference on-chip. The reference for the AD7476/AD7477/AD7478 is derived from the power supply and thus provides the widest dynamic input range.

The AD7476/AD7477/AD7478 also feature a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7476/AD7477/AD7478 are successive-approximation analog-to-digital converters based around a charge redistribution DAC. Figure 1 and Figure 11 show simplified schematics of the ADC. Figure 10 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

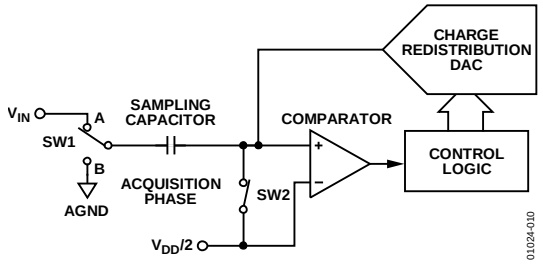


Figure 10. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 11), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 12 and Figure 13 show the ADC transfer function.

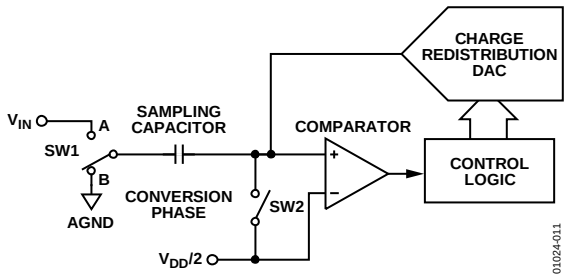


Figure 11. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7476/AD7477/AD7478 is straight binary. For the AD7476/AD7477, designed code transitions occur midway between successive integer LSB values, such as ½ LSB, 1½ LSB, and so on. The LSB size for the AD7476 is $V_{DD}/4096$, and the LSB size for the AD7477 is $V_{DD}/1024$. The ideal transfer characteristic for the AD7476/AD7477 is shown in Figure 12.

For the AD7478, designed code transitions occur midway between successive integer LSB values, such as 1 LSB, 2 LSB, and so on. The LSB size for the AD7478 is $V_{DD}/256$. The ideal transfer characteristic for the AD7478 is shown in Figure 13.

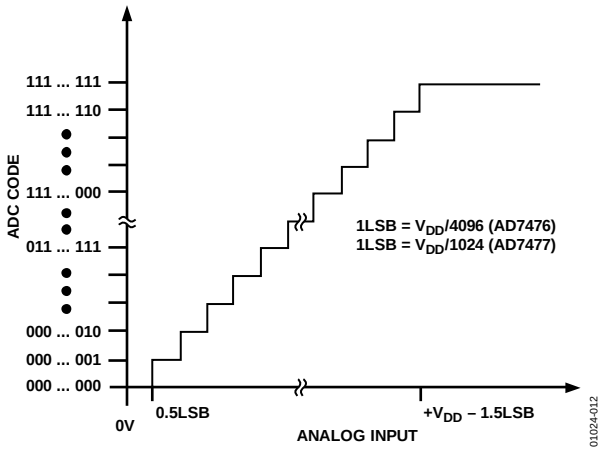


Figure 12. Transfer Characteristic for the AD7476/AD7477

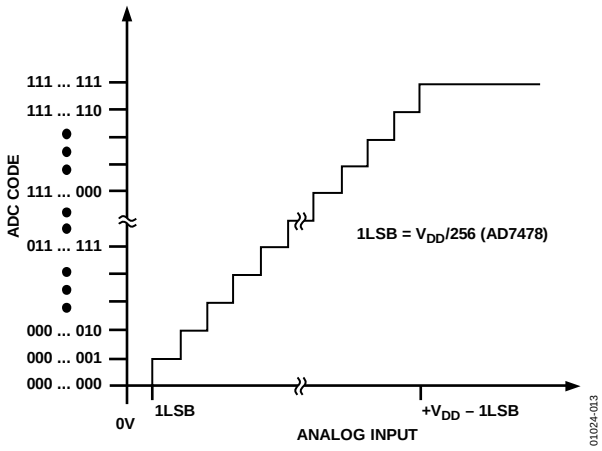


Figure 13. Transfer Characteristic for AD7478

TYPICAL CONNECTION DIAGRAM

Figure 14 shows a typical connection diagram for the AD7476/AD7477/AD7478. V_{REF} is taken internally from V_{DD} and as such, V_{DD} should be well decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit, 10-bit, or 8-bit result. The 10-bit result from the AD7477 is followed by two trailing zeros. The 8-bit result from the AD7478 is followed by four trailing zeros.

Alternatively, because the supply current required by the AD7476/AD7477/AD7478 is so low, a precision reference can be used as the supply source to the part. A REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) can be used to supply the required voltage to the ADC (see Figure 14). This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, such as 15 V.

The REF19x outputs a steady voltage to the AD7476/AD7477/AD7478. If the low dropout REF193 is used, the current it typically needs to supply to the AD7476/AD7477/AD7478 is 1 mA. When the ADC is converting at a rate of 1 MSPS, the REF193 needs to supply a maximum of 1.6 mA to the AD7476/AD7477/AD7478. The load regulation of the REF193 is typically 10 ppm/mA (REF193, V_S = 5 V), which results in an error of 16 ppm (48 μV) for the 1.6 mA drawn from it. This corresponds to a 0.065 LSB error for the AD7476 with V_{DD} = 3 V from the REF193, a 0.016 LSB error for the AD7477, and a 0.004 LSB error for the AD7478.

For applications where power consumption is of concern, the power-down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See the Modes of Operation section.

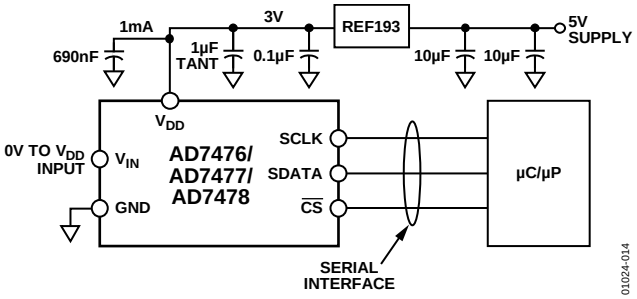


Figure 14. REF193 as Power Supply

Table 7 provides some typical performance data with various references used as a V_{DD} source with a low frequency analog input. Under the same setup conditions, the references are compared and the AD780 proved the optimum reference.

Table 7.

Reference Tied to V_{DD}	AD7476 SNR Performance 1 kHz Input (dB)
AD780 @ 3 V	71.17
REF193	70.4
AD780 @ 2.5 V	71.35
REF192	70.93
AD1582	70.05

Analog Input

Figure 15 shows an equivalent circuit of the analog input structure of the AD7476/AD7477/AD7478. The two diodes, D1 and D2, provide ESD protection for the analog input. Take care to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This causes these diodes to become forward-biased and start conducting current into the substrate. These diodes can conduct a maximum of 10 mA without causing irreversible damage to the part.

The Capacitor C1 in Figure 15 is typically about 4 pF and can primarily be attributed to pin capacitance. The Resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100 Ω. The Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 30 pF. For ac applications, removing high frequency components from the analog input signal is recommended by use of a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate using an input buffer amplifier. The choice of the op amp is a function of the particular application.

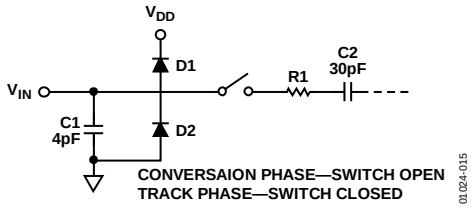


Figure 15. Equivalent Analog Input Circuit

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 16 shows a graph of the total harmonic distortion versus source impedance for different analog input frequencies when using a supply voltage of 2.7 V and sampling at a rate of 605 kSPS. Figure 17 and Figure 18 each show a graph of the total harmonic distortion vs. analog input signal frequency for various supply voltages while sampling at 993 kSPS with an SCLK frequency of 20 MHz and 605 kSPS with an SCLK frequency of 12 MHz, respectively.

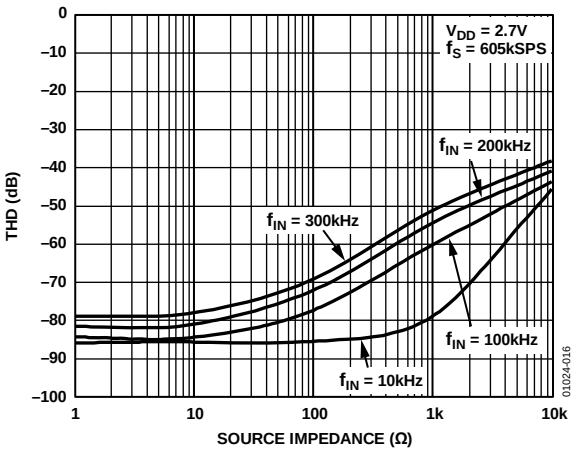


Figure 16. THD vs. Source Impedance for Various Analog Input Frequencies

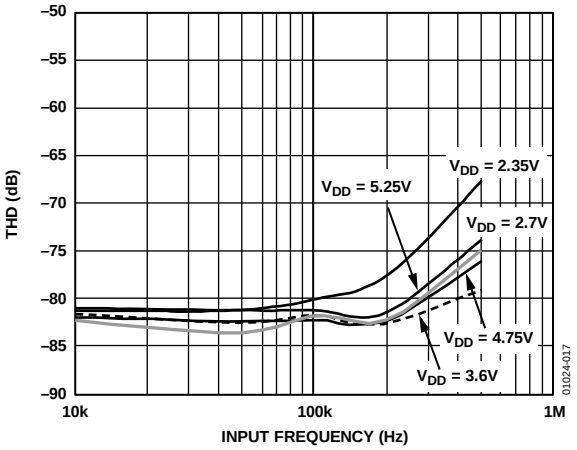


Figure 17. THD vs. Analog Input Frequency, f_s = 993 kSPS

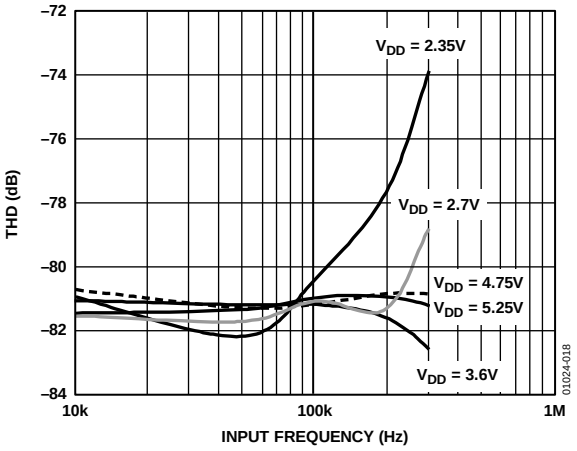


Figure 18. THD vs. Analog Input Frequency, f_s = 605 kSPS

Digital Input

The digital input applied to the AD7476/AD7477/AD7478 is not limited by the maximum ratings that limit the analog input. Instead, the digital input applied can go to 7 V and is not restricted by the V_{DD} + 0.3 V limit as on the analog input. For example, if the AD7476/AD7477/AD7478 are operated with a V_{DD} of 3 V, then 5 V logic levels can be used on the digital input. However, note that the data output on SDATA still has 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK is applied before V_{DD}, there is no risk of latch-up as there is on the analog input when a signal greater than 0.3 V is applied prior to V_{DD}.

MODES OF OPERATION

Select the mode of operation of the AD7476/AD7477/AD7478 by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. The two possible modes of operation are normal mode and power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated determines whether or not the AD7476/AD7477/AD7478 enters power-down mode. Similarly, if already in power-down, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance. Users do not have to worry about power-up times with the AD7476/AD7477/AD7478 remaining fully powered at all times. Figure 19 shows the general diagram of the AD7476/AD7477/AD7478 in normal mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the tenth SCLK falling edge, but before the sixteenth SCLK falling edge, the part remains powered up, but the conversion terminates and SDATA goes back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion (effectively idling $\overline{CS}$ low).

Once a data transfer is complete, (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by again bringing $\overline{CS}$ low.

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered between each conversion, or a series of conversions can be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7476/AD7477/AD7478 is in power-down mode, all analog circuitry is powered down.

To enter power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high any time after the second falling edge of SCLK and before the tenth falling edge of SCLK, as shown in Figure 20. Once $\overline{CS}$ is brought high in this window of SCLKs, the part enters power-down and the conversion initiated by the falling edge of $\overline{CS}$ is terminated and SDATA goes back into three-state.

If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power up the AD7476/AD7477/AD7478 again, perform a dummy conversion. On the falling edge of $\overline{CS}$, the device begins to power up, and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device is fully powered up once 16 SCLKs have elapsed and, as shown in Figure 21, valid data results from the next conversion. If $\overline{CS}$ is brought high before the tenth falling edge of SCLK, the AD7476/AD7477/AD7478 again goes back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. Although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$ as long as it occurs before the tenth SCLK falling edge.

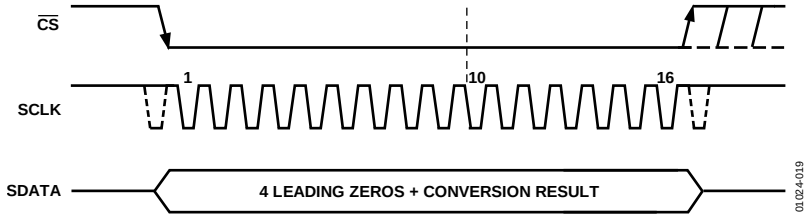


Figure 19. Normal Mode Operation

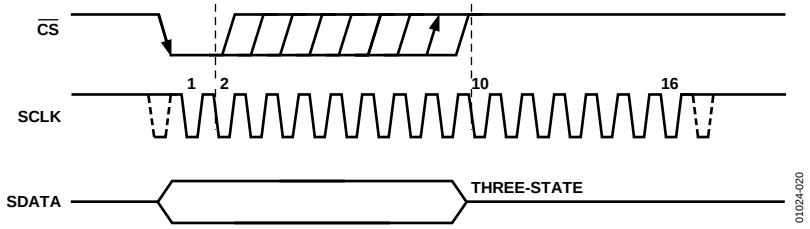


Figure 20. Entering Power-Down Mode

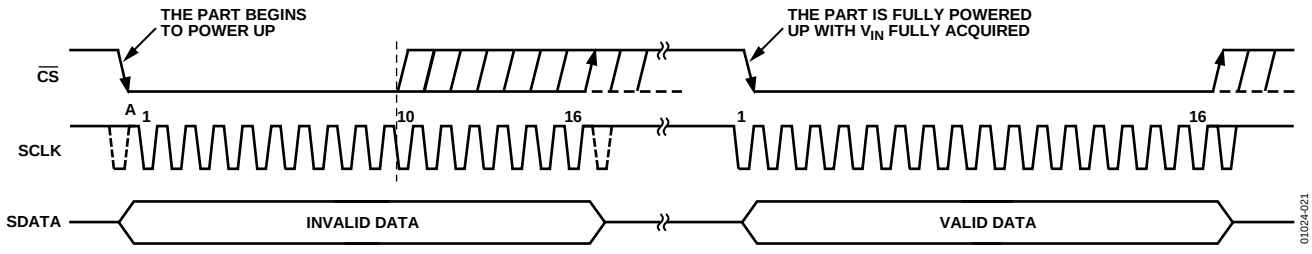


Figure 21. Exiting Power-Down Mode

Power-Up Time

The power-up time of the AD7476/AD7477/AD7478 is typically 1 µs, which means that with any frequency of SCLK up to 20 MHz, one dummy cycle is always sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is acquired properly. The quiet time (t_{QUIET}) must still be allowed from the point at which the bus goes back into three-state (after the dummy conversion), to the next falling edge of $\overline{CS}$. When running at 1 MSPS throughput rate, the AD7476/AD7477/AD7478 powers up and acquires a signal within ±0.5 LSB in one dummy cycle, such as 1 µs.

When powering up from the power-down mode with a dummy cycle, as shown in Figure 21, the track-and-hold, that was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 21. Although at any SCLK frequency, one dummy cycle is sufficient to power up the device and acquire V_{IN}, this does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and fully acquire V_{IN}; 1 µs is sufficient to power up the device and acquire the input signal. If, for example, a 5 MHz SCLK frequency is applied to the ADC, the cycle time is 3.2 µs. In one dummy cycle, 3.2 µs, the part is powered up and V_{IN} is fully acquired. However, after 1 µs with a 5 MHz SCLK, only five SCLK cycles elapse. At this stage, the ADC is fully powered up and the signal acquired. In this case, the $\overline{CS}$ can be brought high after the tenth SCLK falling edge and brought low again after a time, t_{QUIET}, to initiate the conversion.

When power supplies are first applied to the AD7476/AD7477/AD7478, the ADC may power up in either power-down mode or normal mode. Allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, to keep the part in the power-down mode while not in use and then to power up the part in power-down mode, use the dummy cycle to ensure the device is in power-down by executing a cycle such as that shown in Figure 20. Once supplies are applied to the AD7476/AD7477/AD7478, the power-up time is the same when powering up from the power-down mode. It takes approximately 1 µs to fully power up if the part powers up in normal mode. It is not necessary to wait 1 µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, ensure that adequate acquisition time has been allowed.

When powering up from power-down mode, the part returns to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track-and-hold is already in track.

This means that if the ADC powers up in the desired mode of operation, and a dummy cycle is not required to change mode, then a dummy cycle is not required to place the track-and-hold into track.

POWER VS. THROUGHPUT RATE

By using the power-down mode on the AD7476/AD7477/AD7478 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 22 shows that as the throughput rate reduces, the device remains in its power-down state longer, and the average power consumption over time drops accordingly.

For example, if the AD7476/AD7477/AD7478 operates in continuous sampling mode with a throughput rate of 100 kSPS and a SCLK of 20 MHz (V_{DD} = 5 V), and the device is placed in the power-down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 17.5 mW (V_{DD} = 5 V). If the power-up time is one dummy cycle, such as 1 µs, and the remaining conversion time is another cycle, such as 1 µs, then the part is said to dissipate 17.5 mW for 2 µs during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is (2/10) × (17.5 mW) = 3.5 mW. If V_{DD} = 3 V, SCLK = 20 MHz, and the device is again in power-down mode between conversions, the power dissipation during normal operation is 4.8 mW.

The AD7476/AD7477/AD7478 can now be said to dissipate 4.8 mW for 2 µs during each conversion cycle. With a throughput rate of 100 kSPS, the average power dissipated during each cycle is (2/10) × (4.8 mW) = 0.96 mW. Figure 22 shows the power vs. throughput rate when using the power-down mode between conversions with both 5 V and 3 V supplies.

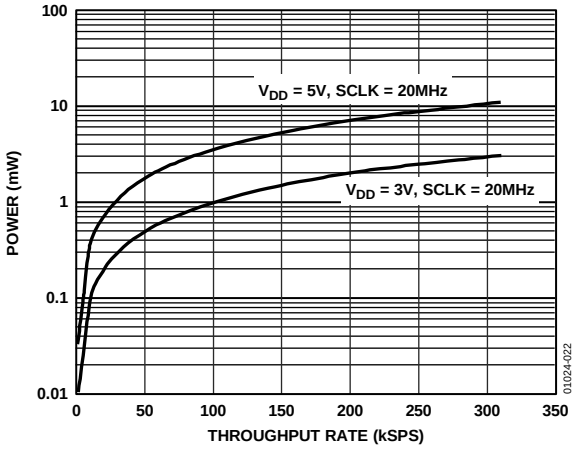


Figure 22. Power vs. Throughput Rate

Power-down mode is intended for use with throughput rates of approximately 333 kSPS and under. At higher sampling rates, power is not saved by using power-down mode.

SERIAL INTERFACE

Figure 23, Figure 24, and Figure 25 show the detailed timing diagrams for serial interfacing to the AD7476, AD7477, and AD7478, respectively. The serial clock provides the conversion clock and controls the transfer of information from the part during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, takes the bus out of three-state, and samples the analog input at this point. The conversion initiates and requires 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge as shown at Point B in Figure 23, Figure 24, and Figure 25. On the sixteenth SCLK falling edge, the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion terminates and the SDATA line goes back into three-state; otherwise, SDATA returns to three-state on the 16th SCLK falling edge as shown in Figure 23, Figure 24, and Figure 25.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476/AD7477/AD7478.

$\overline{CS}$ going low provides the first leading zero to be read by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Thus, the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it is possible to read data on each SCLK rising edge, although the first leading zero has to be read on the first SCLK falling edge after the $\overline{CS}$ falling edge. Therefore, the first rising edge of SCLK after the $\overline{CS}$ falling edge provides the second leading zero. The 15th rising SCLK edge has DB0 provided or the final zero for the AD7477 and AD7478. This may not work with most microcontrollers/DSPs, but could possibly be used with FPGAs and ASICs.

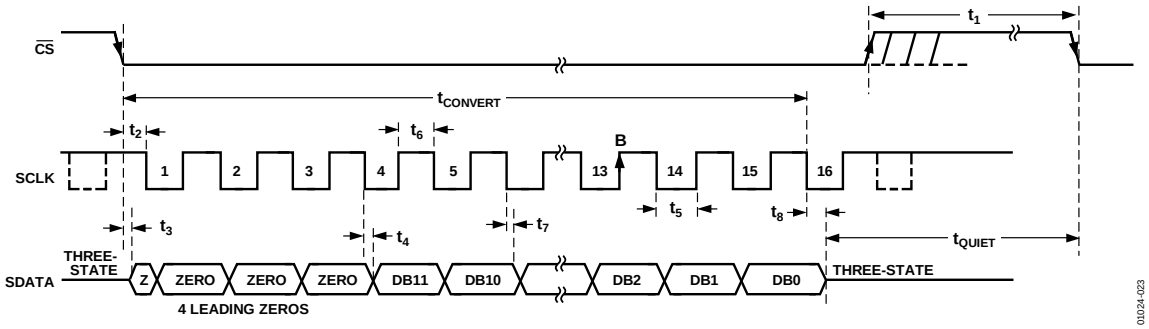


Figure 23. AD7476 Serial Interface Timing Diagram

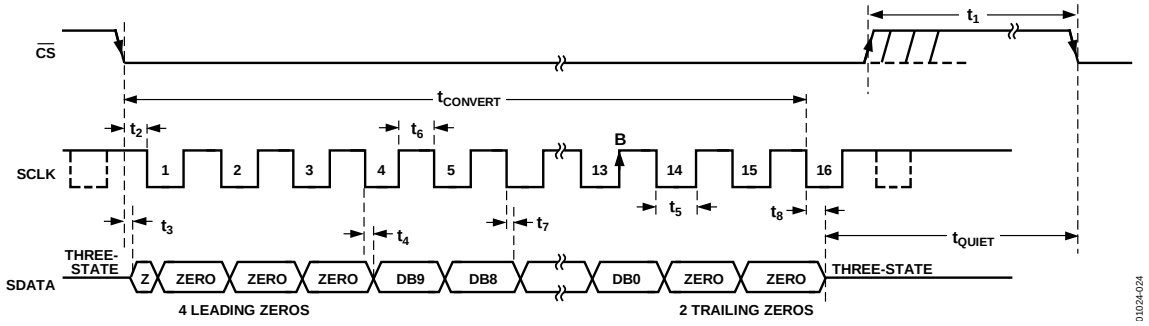


Figure 24. AD7477 Serial Interface Timing Diagram

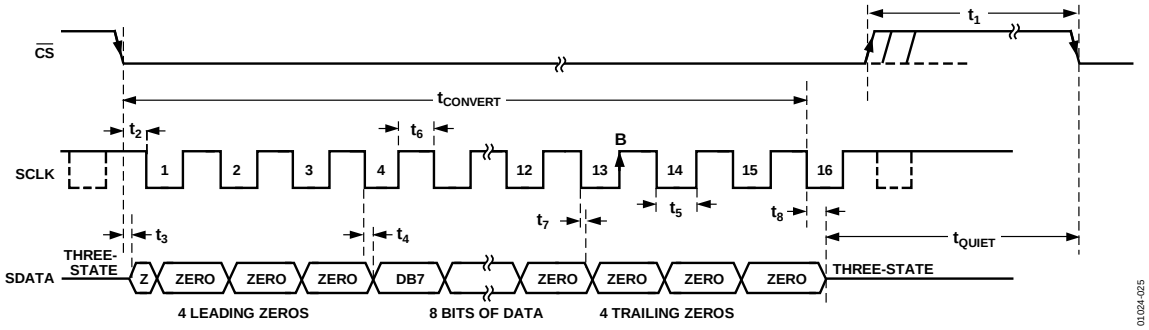


Figure 25. AD7478 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7476/AD7477/AD7478 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7476/AD7477/AD7478 with some of the more common microcontroller and DSP serial interface protocols.

AD7476/AD7477/AD7478 to TMS320C5x/C54x Interface

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices such as the AD7476/AD7477/AD7478. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x/C54x and the AD7476/AD7477/AD7478 without any glue logic required. In addition, the serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (Tx serial clock) and FSX (Tx frame sync).

The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The format bit, FO, can be set to 1 to set the word length to eight bits, in order to implement the power-down mode on the AD7476/AD7477/AD7478. The connection diagram is shown in Figure 26. Note that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C5x/C54x provides equidistant sampling.

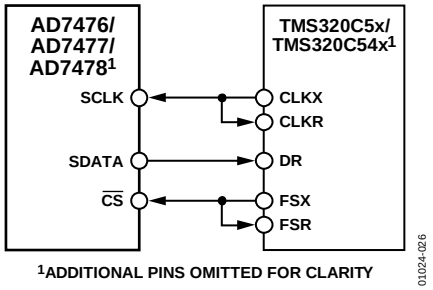


Figure 26. Interfacing to the TMS320C5x/C54x

AD7476/AD7477/AD7478 to ADSP-21xx Interface

The ADSP-21xx family of DSPs are interfaced directly to the AD7476/AD7477/AD7478 without any glue logic required. The SPORT control register is set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data-Words
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0
ITFS = 1

To implement the power-down mode, SLEN is set to 0111 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 27. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT control register is set up as described.

The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt controls the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

The timer registers, for example, are loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS controls the RFS and, therefore, the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, such as, TX0 = AX0, the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data could be transmitted, or it could wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, a SCLK of 2 MHz is obtained, and eight master clock periods elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs occur between interrupts and, subsequently, between transmit instructions. This situation results in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling is implemented by the DSP.

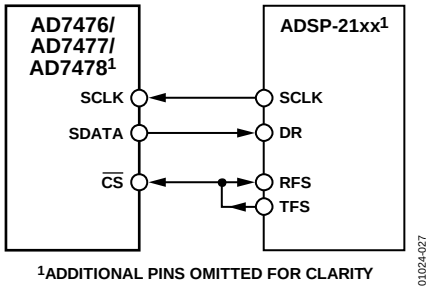


Figure 27. Interfacing to the ADSP-21xx

AD7476/AD7477/AD7478 to DSP56xxx Interface

The connection diagram in Figure 28 shows how the AD7476/AD7477/AD7478 can be connected to the synchronous serial interface (SSI) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in synchronous mode (SYN bit in CRB =1) with internally generated word frame sync for both Tx and Rx (Bits FSL1 = 0 and FSL0 = 0 in CRB). Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA.

To implement the power-down mode on the AD7476/AD7477/AD7478, the word length can be changed to eight bits by setting bits WL1 = 0 and WL0 = 0 in CRA. Note that for signal processing applications, it is imperative that the frame synchronization signal from the DSP56xxx provides equidistant sampling.

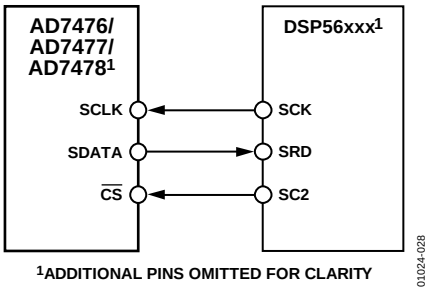


Figure 28. Interfacing to the DSP56xxx

AD7476/AD7477/AD7478 to MC68HC16 Interface

The serial peripheral interface (SPI) on the MC68HC16 is configured for master mode (MSTR = 1), the clock polarity bit (CPOL) = 1, and the clock phase bit (CPHA) = 0. The SPI is configured by writing to the SPI Control Register (SPCR). For more information on the MC68HC16, check with Motorola for the related documentation.

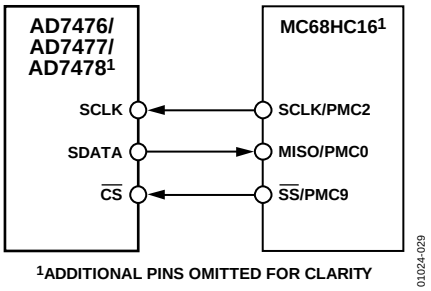
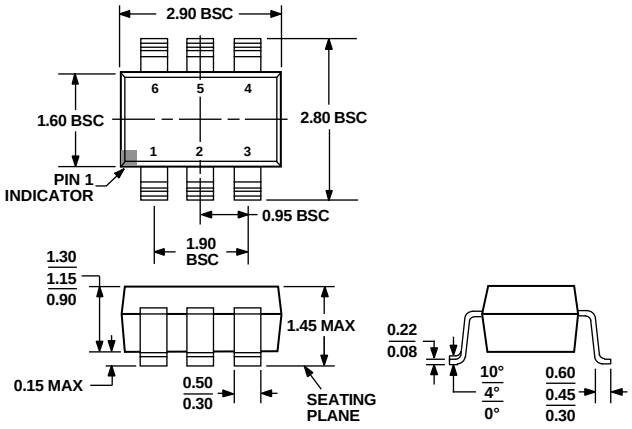


Figure 29. Interfacing to the MC68HC16

The serial transfer takes place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. To implement the power-down mode with an 8-bit transfer, set SIZE = 0. A connection diagram is shown in Figure 29.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 30. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7476ARTZ-500RL7[3]	−40°C to +85°C	±1 typical	RJ-6	CEA#
AD7476ARTZ-REEL[3]	−40°C to +85°C	±1 typical	RJ-6	CEA#
AD7476ARTZ-REEL7[3]	−40°C to +85°C	±1 typical	RJ-6	CEA#
AD7476BRTZ-R2[3]	−40°C to +85°C	±1.5 maximum	RJ-6	CEB#
AD7476BRTZ-REEL[3]	−40°C to +85°C	±1.5 maximum	RJ-6	CEB#
AD7476BRTZ-REEL7[3]	−40°C to +85°C	±1.5 maximum	RJ-6	CEB#
AD7476SRTZ-500RL7[3]	−55°C to +125°C	±1.5 maximum	RJ-6	CES#
AD7476SRTZ-R2[3]	−55°C to +125°C	±1.5 maximum	RJ-6	CES#
AD7476SRTZ-REEL[3]	−55°C to +125°C	±1.5 maximum	RJ-6	CES#
AD7476SRTZ-REEL7[3]	−55°C to +125°C	±1.5 maximum	RJ-6	CES#
AD7476WARJZ-RL7[3, 4]	−40°C to +85°C	±1 typical	RJ-6	CEA#
AD7477ARTZ-500RL7[3]	−40°C to +85°C	±1 maximum	RJ-6	C46[5]
AD7477ARTZ-REEL[3]	−40°C to +85°C	±1 maximum	RJ-6	C46[5]
AD7477ARTZ-REEL7[3]	−40°C to +85°C	±1 maximum	RJ-6	C46[5]
AD7477SRTZ-REEL[3]	−55°C to +125°C	±1 maximum	RJ-6	C3F
AD7478ARTZ-500RL7[3]	−40°C to +85°C	±0.5 maximum	RJ-6	C3Z
AD7478ARTZ-REEL[3]	−40°C to +85°C	±0.5 maximum	RJ-6	C3Z
AD7478ARTZ-REEL7[3]	−40°C to +85°C	±0.5 maximum	RJ-6	C3Z
AD7478SRTZ-REEL7[3]	−55°C to +125°C	±0.5 maximum	RJ-6	C3Y
AD7478WARTZ-RL7[3, 4]	−40°C to +85°C	±0.5 maximum	RJ-6	C3Z
EVAL-AD7476CBZ[3, 6]			Evaluation Board	
EVAL-AD7477CBZ[3, 6]			Evaluation Board	
EVAL-CONTROL BRD2[7]			Control Board	

[1] Linearity error refers to integral linearity error.
[2] RJ = 6-Lead SOT-23.
[3] Z = RoHS Compliant Part, # denotes RoHS compliant part maybe top or bottom marked.
[4] Qualified for automotive.
[5] Prior to 0523 date code, parts are marked with CFA#.
[6] This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[7] This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, users need to order the particular ADC evaluation board, such as the EVAL-AD7476CB, the EVAL-CONTROL BRD2, and a 12 V ac transformer. See relevant evaluation board application note for more information.

NOTES

NOTES

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