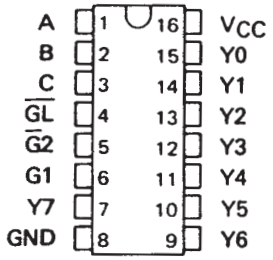
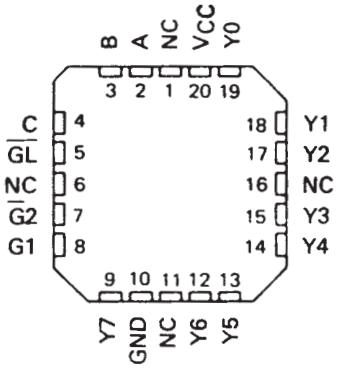
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Enable Inputs to Simplify Cascading**
- **Low Power Dissipation . . . 65 mW Typ**

**SN54LS137 . . . J OR W PACKAGE**
**SN74LS137 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54LS137 . . .FK PACKAGE**
**(TOP VIEW)**

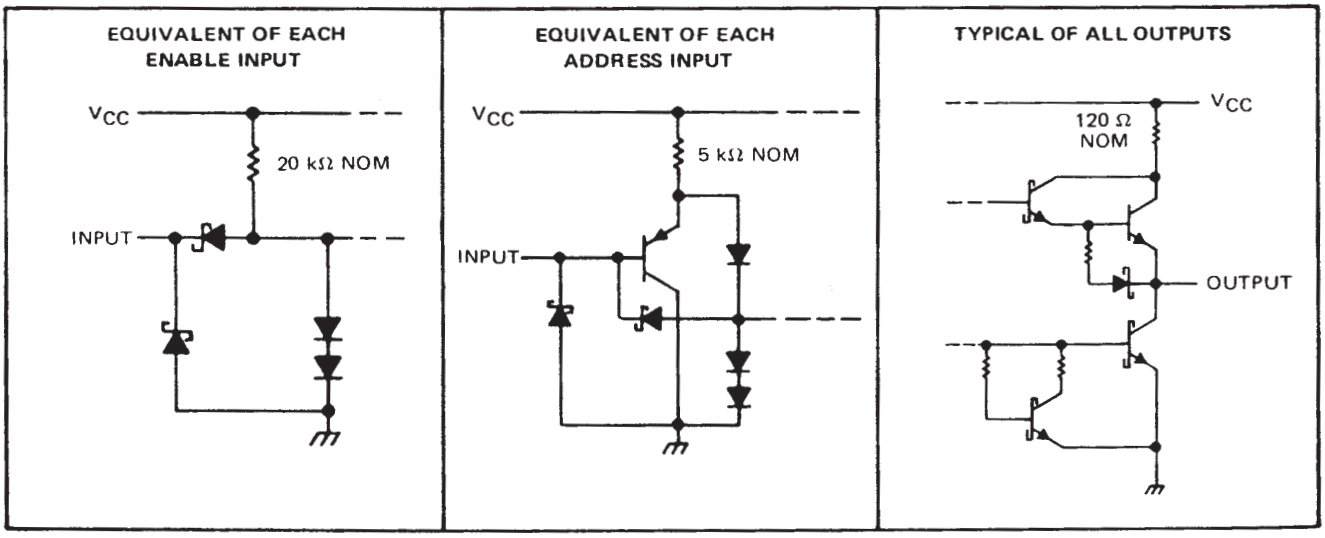



NC - No internal connection

## description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'LS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A,B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

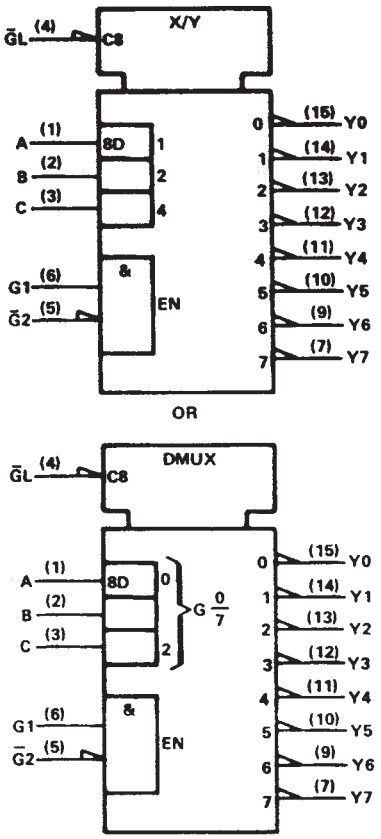
## schematics of inputs and outputs




PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1988, Texas Instruments Incorporated

## logic symbols†



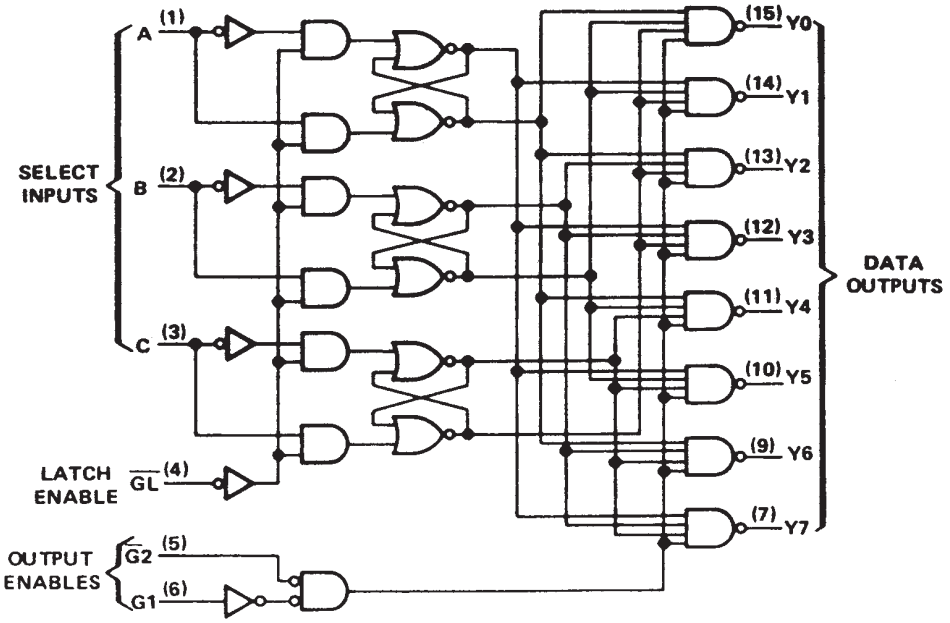

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | | SELECT | | | | | | | | | | |
| $\overline{G1}$ | G1 | $\overline{G2}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Output corresponding to stored address, L; all others, H | | | | | | | |

H = high level, L = low level, X = irrelevant

## logic diagram (positive logic)




Pin numbers shown are for D, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (See Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS137 . . . . . −55°C to 125°C
SN74LS137 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | SN54LS137 | | | SN74LS137 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | –400 | | | –400 | μA |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Width of enabling pulse at $\overline{G}L$, $t_w$ | 15 | | | 15 | | | ns |
| Setup time at A, B, and C inputs, $t_{su}$ | 10 | | | 10 | | | ns |
| Hold time at A, B, and C inputs, $t_h$ | 10 | | | 10 | | | ns |
| Operating free-air temperature, $T_A$ | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS137 | | | SN74LS137 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = –18 mA | | | | –1.5 | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = –400 μA | | 2.5 | 3.5 | | 2.7 | 3.5 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max | $V_{IH}$ = 2 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | Enable | | | –0.4 | | | –0.4 | mA |
| | | | | A, B, C | | | –0.2 | | | –0.2 | |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | | –20 | | –100 | –20 | | –100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | See Note 2 | | | 11 | 18 | | 11 | 18 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: $I_{CC}$ is tested with all inputs grounded and all outputs open.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C, see note 3

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF DELAY | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, C | Y | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 11 | 17 | ns |
| $t_{PHL}$ | | | 4 | | | 25 | 38 | |
| $t_{PLH}$ | A, B, C | Y | 3 | | | 16 | 24 | ns |
| $t_{PHL}$ | | | 3 | | | 19 | 29 | |
| $t_{PLH}$ | Enable $\overline{G}2$ | Y | 2 | | | 13 | 21 | ns |
| $t_{PHL}$ | | | 2 | | | 16 | 27 | |
| $t_{PLH}$ | Enable G1 | Y | 3 | | | 14 | 21 | ns |
| $t_{PHL}$ | | | 3 | | | 18 | 27 | |
| $t_{PLH}$ | Enable $\overline{G}L$ | Y | 3 | | | 18 | 27 | ns |
| $t_{PHL}$ | | | 4 | | | 25 | 38 | |

¶ $t_{PLH}$ = propagation delay time, low-to-high-level output.
$t_{PHL}$ = propagation delay time, high-to-low-level output.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated