High-Voltage Ring Generator

Features

- 105Vrms ring signal
- Output overcurrent protection
- 5.0V CMOS logic control
- Logic enable/disable to save power
- Adjustable deadband in single-control mode
- Power-on reset
- Fault output for problem detection

Applications

- Line access cards
- Set-top/Street box

General Description

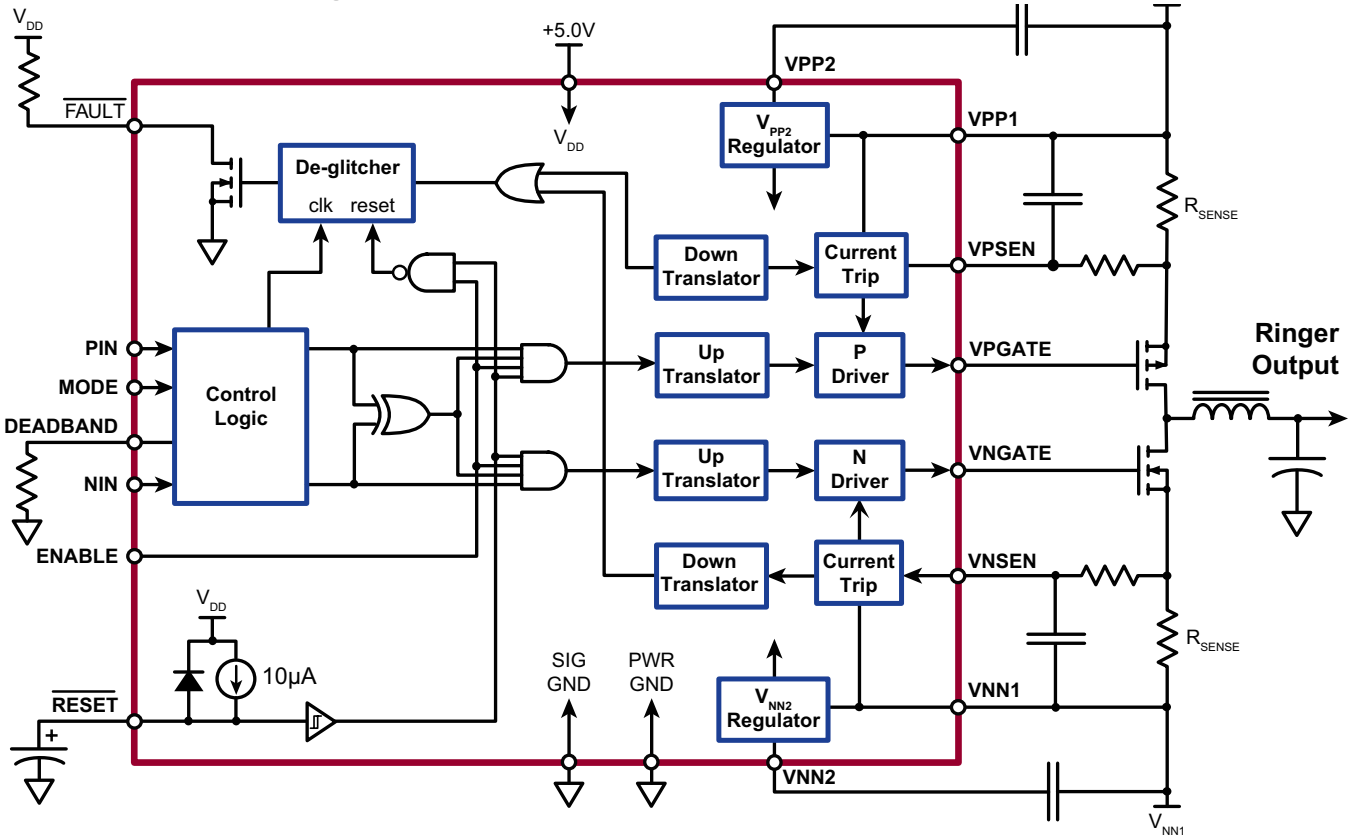
The Supertex HV430 is a high voltage PWM ring generator integrated circuit. The high voltage outputs, V_{PGATE} and V_{NGATE}, are used to drive the gates of external high voltage N-channel and P-channel MOSFETs in a push-pull configuration. Overcurrent protection is implemented for both the P-channel and N-channel MOSFETs. External sense resistors set the over-current trip point.

The RESET input functions as a power-on reset when connected to an external capacitor. The $\overline{\text{FAULT}}$ output indicates an overcurrent condition and is cleared after 4 consecutive cycles with no overcurrent condition. A logic low on RESET or ENABLE clears the $\overline{\text{FAULT}}$ output. It is active-low and open-drain to allow wire OR'ing of multiple drivers.

P_{GATE} and N_{GATE} are controlled independently by logic inputs P_{IN} and N_{IN} when the MODE pin is at logic high. A logic high on P_{IN} will turn on the external P-channel MOSFET. Similarly, a logic high on N_{IN} will turn on the external N-channel MOSFET. Lockout circuitry prevents the N and P switches from turning on simultaneously. A pulse width limiter restricts pulse widths to no less than 100 - 200ns.

For applications where a single control input is desired, the MODE pin should be connected to SGND. The PWM control signal is then input to the N_{IN} pin. A user-adjustable deadband in the control logic ensures break-before-make on the outputs, thus avoiding cross conduction on the high voltage output during switching. A logic high on N_{IN} will turn the external P-Channel MOSFET on and the N-Channel off, and vice versa. The IC can be powered down by applying a logic low on the ENABLE pin, placing both external MOSFETs in the off state.

Functional Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV430WG-G	20-Lead SOW	1000/Reel

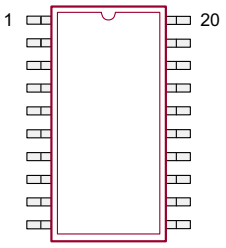
-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{PP1} - V_{NN1}, power supply voltage	+340V
V_{PP1}, positive high voltage supply	+220V
V_{PP2}, positive gate voltage supply	+220V
V_{NN1}, negative high voltage supply	-220V
V_{NN2}, negative gate voltage supply	-220V
V_{DD}, logic supply	+7.5V
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Power dissipation	600mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



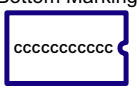
20-Lead SOW
(top view)

Product Marking

Top Marking



Bottom Marking



YY = Year Sealed
WW = Week Sealed
A = Assembler ID
L = Lot Number
C = Country of Origin*
——— = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or ⚡

20-Lead SOW

Typical Thermal Resistance

Package	θ_{ja}
20-Lead SOW	66°C/W

Electrical Characteristics *(Over operating supply voltage unless otherwise specified. T_A = -40°C to +85°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
External Supplies						
V_{PP1}	High voltage positive supply	50	-	200	V	---
I_{PP1Q}	V_{PP1} quiescent current	-	250	500	µA	P_{IN} = N_{IN} = 0V
I_{PP1}	V_{PP1} operating current	-	-	2.0	mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz
V_{NN1}	High voltage negative supply	V_{PP1} -325	-	-50	V	---
I_{NN1Q}	V_{NN1} quiescent current	-	250	500	µA	P_{IN} = N_{IN} = 0V, R_{DB} = 18kΩ
I_{NN1}	V_{NN1} operating current	-	-	1.0	mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz
V_{DD}	Logic supply voltage	4.50	-	5.50	V	---
I_{DDQ}	V_{DD} quiescent current	-	300	400	µA	P_{IN} = N_{IN} = 0V, R_{DB} = 18kΩ
I_{DD}	V_{DD} operating current	-	-	1.0	mA	P_{IN} = N_{IN} = 100KHz, R_{DB} = 18kΩ

Electrical Characteristics *(cont.)* *(Over operating supply voltage unless otherwise specified. T_A = -40°C to +85°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
Internal Supplies						
V_{PP2}	Positive linear regulator output voltage	V_{PP1} -16	-	V_{PP1} -10	V	---
V_{NN2}	Negative linear regulator output voltage	V_{PP1} +10	-	V_{PP1} +14	V	---
Positive High Voltage Output						
V_{PGATE}	Output voltage swing	V_{PP2}	-	V_{PP1}	V	No load on V_{PGATE}
$R_{SOURCEP}$	V_{PGATE} source resistance	-	-	12.5	Ω	I_{OUT} = 80mA
R_{SINKP}	V_{PGATE} sink resistance	-	-	12.5	Ω	I_{OUT} = -80mA
t_{RISEP}	V_{PGATE} rise time	-	-	50	ns	C_{LOAD} = 1.4nF
t_{FALLP}	V_{PGATE} fall time	-	-	50	ns	C_{LOAD} = 1.4nF
$t_{PWP(MIN)}$	V_{PGATE} minimum pulse width (internally limited)	100	150	200	ns	---
t_{DELAYP}	P_{IN} to P_{GATE} delay time	-	-	300	ns	Mode = 1
V_{PSEN}	V_{PGATE} current sense voltage	V_{PP1} -0.85	V_{PP1} -1.0	V_{PP1} -1.15	V	---
t_{SHORTP}	V_{PGATE} current sense off time	-	-	150	ns	---
Negative High Voltage Output						
V_{NGATE}	Output voltage swing	V_{NN2}	-	V_{NN1}	V	No load on V_{NGATE}
$R_{SOURCEN}$	V_{NGATE} source resistance	-	-	15.0	Ω	I_{OUT} = 80mA
R_{SINKN}	V_{NGATE} sink resistance	-	-	15.0	Ω	I_{OUT} = 80mA
t_{RISEN}	V_{NGATE} rise time	-	-	50	ns	C_{LOAD} = 1.4nF
t_{FALLN}	V_{NGATE} fall time	-	-	50	ns	C_{LOAD} = 1.4nF
$t_{PWN(MIN)}$	V_{NGATE} minimum pulse width (internally limited)	100	150	200	ns	---
t_{DELAYN}	N_{IN} to N_{GATE} delay time	-	-	300	ns	Mode = 1
V_{NSEN}	V_{NGATE} current sense voltage	V_{NN1} +0.85	V_{NN1} +1.0	V_{NN1} +1.15	V	---
t_{SHORTN}	V_{NGATE} current sense off time	-	-	150	ns	---
Control Circuitry						
V_{IL}	Logic input low voltage	0	-	0.60	V	V_{DD} = 5.0V
V_{IH}	Logic input high voltage	2.7	-	5.0	V	V_{DD} = 5.0V
I_{INDN}	Input pull-down current	0.5	1.0	5.0	µA	P_{IN}, N_{IN}, ENABLE
R_{UP}	Input pull-up resistance	100	200	300	KΩ	MODE
V_{OL}	Logic output low voltage	-	-	0.50	V	V_{DD} = 5.0V, I_{OUT} = -0.5mA
V_{OH}	Logic output high voltage	4.50	-	-	V	V_{DD} = 5.0V, I_{OUT} = +0.5mA
$V_{RST(OFF)}$	RESET voltage, device off	3.2	-	3.5	V	V_{DD} = 5.0V
$V_{RST(ON)}$	RESET voltage, device on	3.7	-	4.0	V	V_{DD} = 5.0V

Electrical Characteristics *(cont.)*(over operating supply voltage unless otherwise specified. T_A = -40°C to +85°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{RST(HYS)}$	RESET hysteresis voltage	0.3	-	-	V	V_{DD} = 5.0V
I_{RESET}	RESET pull-up current	7.0	10	13	µA	V_{RESET} = 0 - 4.5V
$t_{RST(ON)}$	RESET on delay	-	-	1.0	µs	---
$t_{RST(ON)}$	RESET off delay	-	-	1.0	µs	---
$t_{EN(ON)}$	ENABLE on delay	50	100	150	µs	---
$t_{EN(OFF)}$	ENABLE off delay	-	-	1.0	µs	---
$t_{FLT(HOLD)}$	$\overline{FAULT}$ hold time	-	4	-	N_{IN}/P_{IN} cycles	ENABLE = 1
t_{DB}	Deadband time	35	50	70	ns	Mode = 0, R_{DB} = 5.6kΩ
		105	140	175		Mode = 0, R_{DB} = 18kΩ
$t_{DELAY(N-P)}$	N-off to P-on transistion delay	-	-	300	ns	Mode = 0, R_{DB} < 27kΩ
$t_{DELAY(P-N)}$	P-off to N-on transistion delay	-	-	300	ns	Mode = 0, R_{DB} < 27kΩ
$\Delta t_{DELAY(N-P)}$	Delay difference: $t_{delayN(off)}$ - $t_{delayP(on)}$	-80	0	80	ns	Mode = 1
$\Delta t_{DELAY(P-N)}$	Delay difference: $t_{delayP(off)}$ - $t_{delayN(on)}$	-80	0	80	ns	Mode = 1

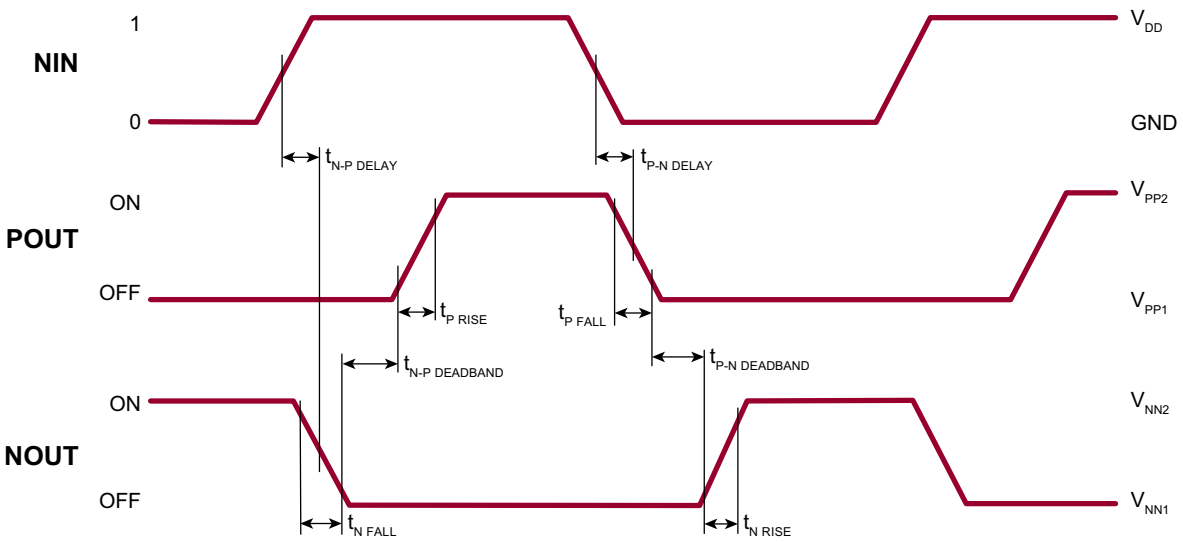
Truth Table

Logic Inputs*				RESET	Output	
N_{IN}	P_{IN}	Mode	EN		Externel N-Channel MOSFET	Externel P-Channel MOSFET
L	L	H	H	$>V_{RESET(ON)}$	OFF	OFF
L	H	H	H	$>V_{RESET(ON)}$	OFF	ON
H	L	H	H	$>V_{RESET(ON)}$	ON	OFF
H	H	H	H	$>V_{RESET(ON)}$	OFF	OFF
H	X	L	H	$>V_{RESET(ON)}$	OFF	ON
L	X	L	H	$>V_{RESET(ON)}$	ON	OFF
X	X	X	L	X	OFF	OFF
X	X	X	X	$<V_{RESET(OFF)}$	OFF	OFF

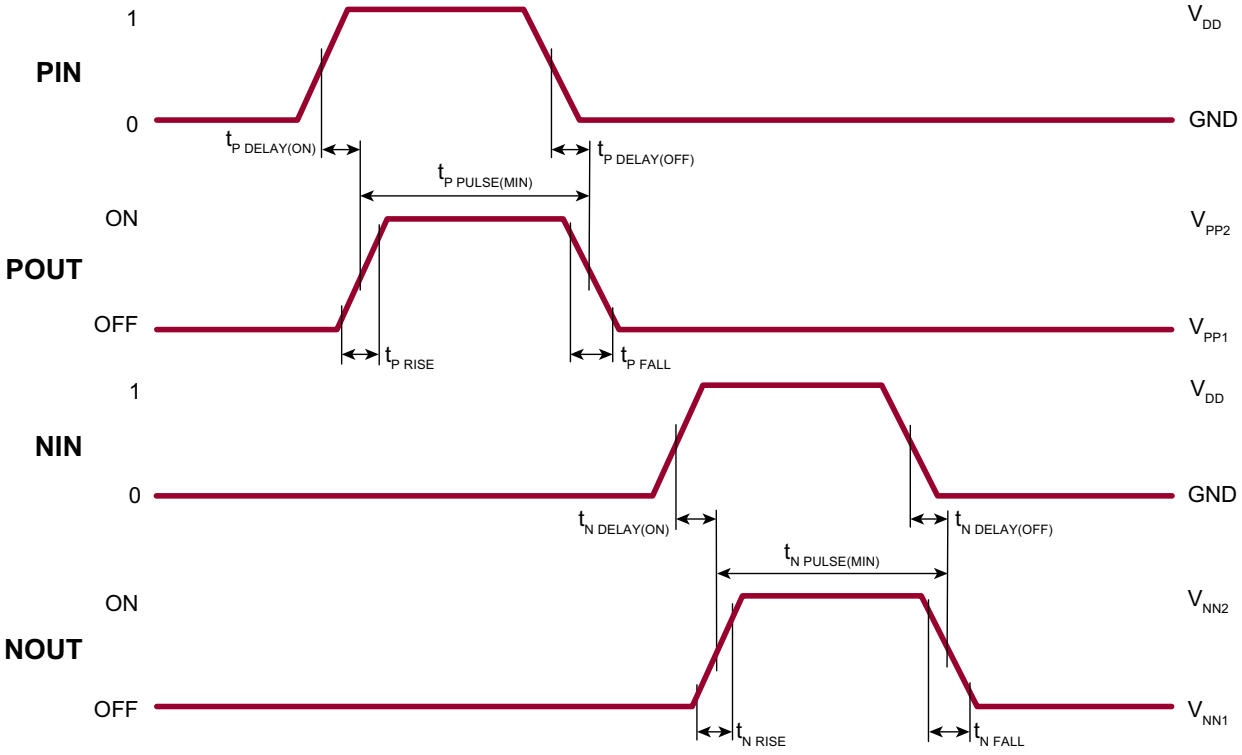
Note:

** Unused logic inputs should be connected to VDD or GND.*

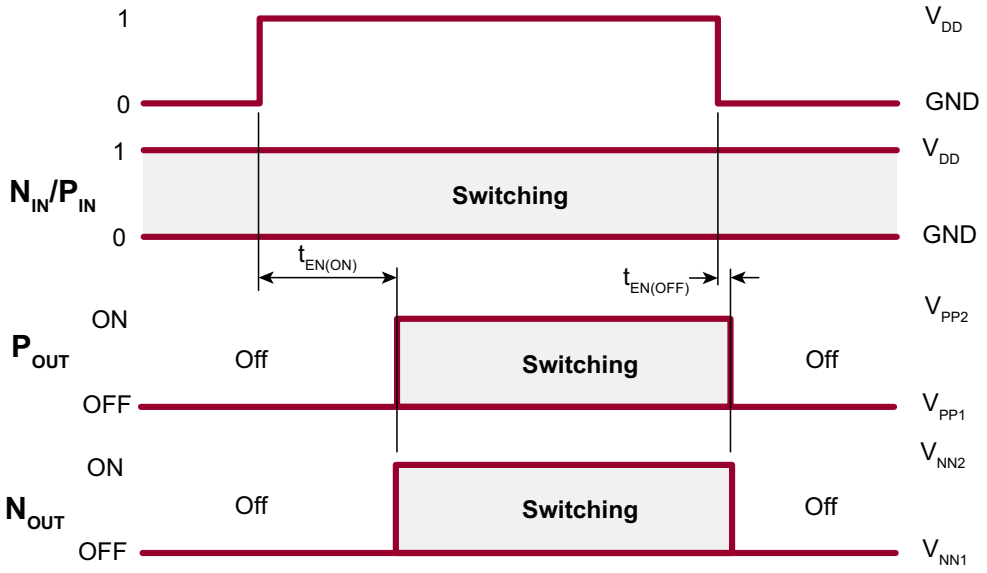
Single-Control Mode Timing



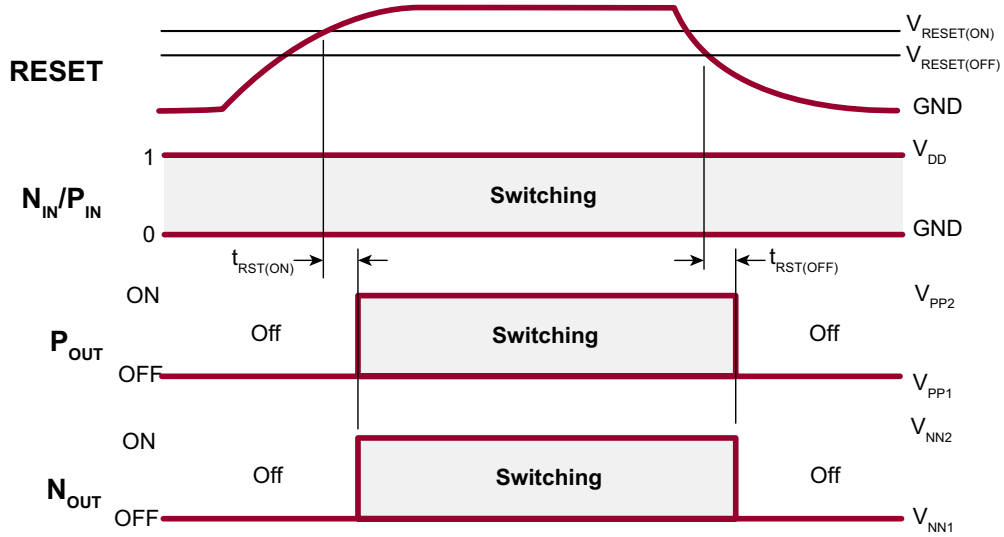
Dual-Control Mode Timing



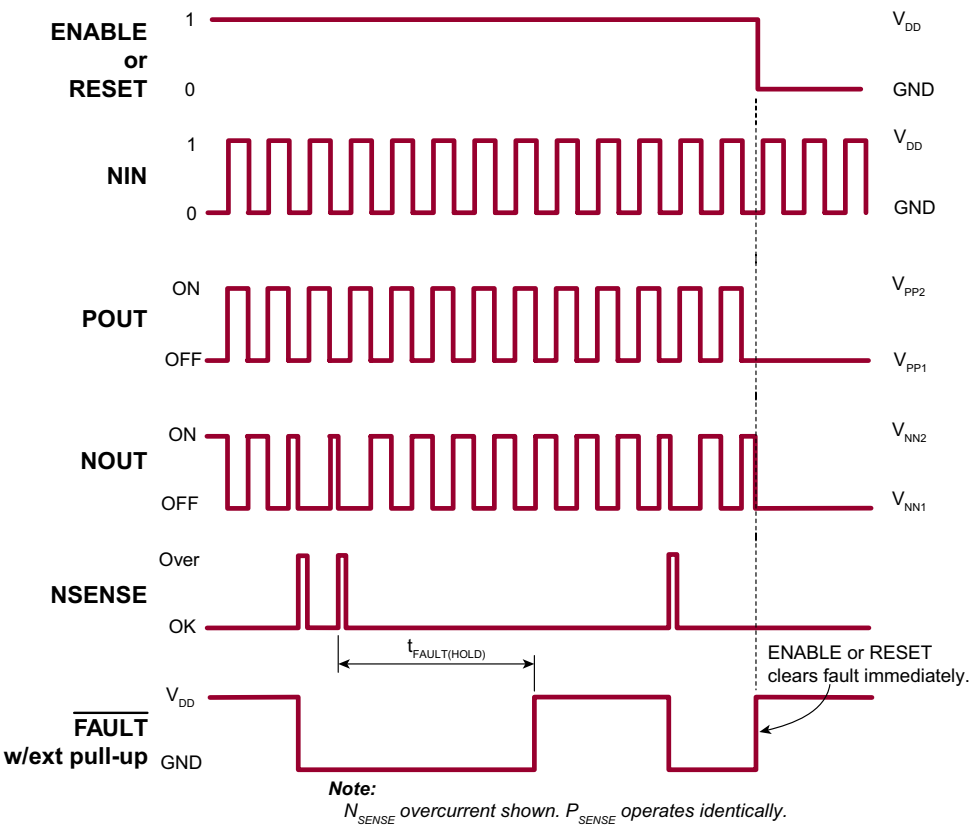
ENABLE Timing



RESET Timing



FAULT Timing



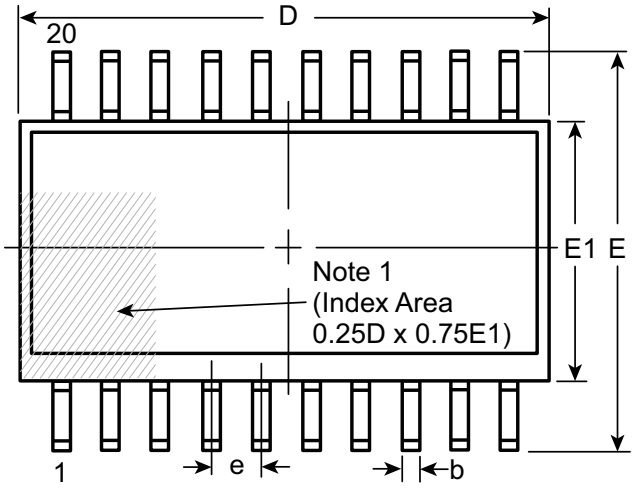
Note:
N_{SENSE} overcurrent shown. P_{SENSE} operates identically.

Pin Description

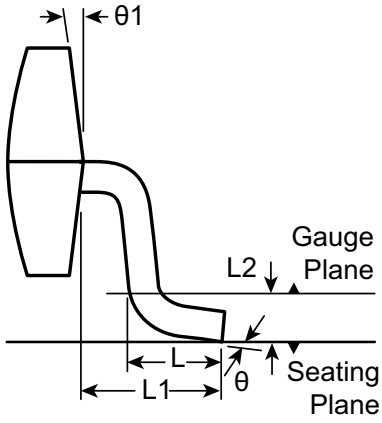
Pin #	Name	Description
1	VDD	Logic supply voltage.
2	$\overline{\text{FAULT}}$	Logic output. Fault is at logic low when either current limit sense pin, VPSEN or VNSEN, is activated. Remains active until overcurrent condition clears or ENABLE = 0 or RESET = 0.
3	MODE	Logic mode input. 0 = single-control; 1 = dual-control. When MODE is high, NIN and PIN independently control N_{OUT} and P_{OUT}, respectively. When MODE is low, NIN controls both outputs in a complementary manner. (See Truth Table)
4	PIN	Logic control input. When mode is high, logic input high turns on the external high voltage P-channel MOSFET. Internally pulled low.
5	NIN	Logic control input. When mode is high, logic input high turns on the external high voltage N-channel MOSFET. Internally pulled low.
6	ENABLE	Logic enable input. Logic high enables IC. Internally pulled low.
7	$\overline{\text{RESET}}$	Power-on reset. A capacitor connected between this pin and ground determines the delay time between application of VDD and when the device outputs are enabled. Low leakage tantalum recommended.
8	DEADBAND	A resistor between this pin and ground sets the ‘break-before-make’ time between output transitions. Applicable only in single-control mode. For minimum deadtime, a 5.6kΩ resistor to ground should be used. For dual-input mode, tie to VDD.
9	SGND	Low voltage logic ground.
10	PGND	High voltage logic ground.
11	VNN2	Negative gate voltage supply. Generated by an internal linear regulator. A 25V, 100nF capacitor should beconnected between VNN2 and VNN1.
12	VNN1	Negative high voltage supply.
13	VNSEN	Pulse by pulse over current sensing for N-Channel MOSFET.
14	VNGATE	Gate drive for external N-channel MOSFET.
15	N/C	No connect.
16		
17	VPGATE	Gate drive for external P-channel MOSFET.
18	VPSEN	Pulse by pulse over current sensing for P-Channel MOSFET.
19	VPP1	Positive high voltage supply.
20	VPP2	Positive gate voltage supply. Generated by an internal linear regulator. A 25V, 100nF capacitor should beconnected between VPP2 and VPP1.

20-Lead SOW (Wide Body) Package Outline (WG)

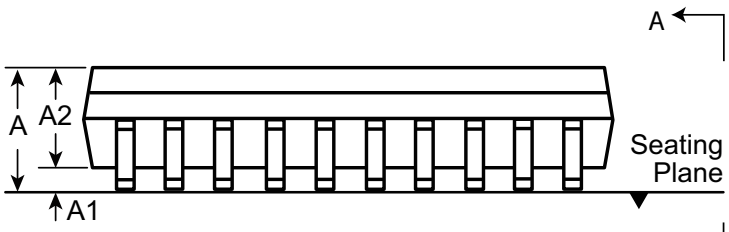
12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



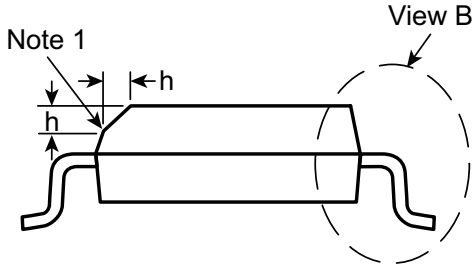
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	12.60*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	12.80	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	13.00*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-20SOWWG, Version D041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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