AsahiKASEI
ASAHI KASEI EMD

AK4646

Stereo CODEC with MIC/SPK-AMP

GENERAL DESCRIPTION

The AK4646 features a stereo CODEC with a built-in Microphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Auto Level Control) circuit, and Output circuits include a Speaker-Amplifier. These circuits are suitable for portable application with recording/playback function. The AK4646 is available in a 32pin QFN, utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Stereo Mic Input (Full-differential or Single-ended)**
- **Stereo Line Input**
- **MIC Amplifier (+32dB/+29dB/+26dB/+23dB/+20dB/+17dB/+10dB/0dB)**
- **Digital ALC (Automatic Level Control)**
  (+36dB ~ –54dB, 0.375dB Step, Mute)
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 86dB (MIC-Amp=+20dB)**
  S/(N+D): 88dB, DR, S/N: 95dB (MIC-Amp=0dB)
- **Wind-noise Reduction Filter**
- **5 Band Notch Filter**
- **Stereo Separation Emphasis**

2. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital ALC (Automatic Level Control)**
  (+36dB ~ –54dB, 0.375dB Step, Mute)
- **Stereo Separation Emphasis**
- **Stereo Line Output**
  - Performance: S/(N+D): 88dB, S/N: 92dB
- **Mono Speaker-Amp**
  - S/(N+D): 60dB@150mW, S/N: 90dB
  - BTL Output
  - Available for both Dynamic and Piezo Speaker
  - Output Power: 400mW@8Ω (SVDD=3.3V)
- **Analog Mixing: Mono Input**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies:**
  12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
  1fs (LRCK pin)
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs

6. Sampling Rate:
- **PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Slave Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

7. μP I/F: 3-wire Serial
8. Master/Slave mode
9. Audio Interface Format: MSB First, 2's compliment
- **ADC: 16bit MSB justified, I²S**
- **DAC: 16bit MSB justified, 16bit LSB justified, 16-24bit I²S**

10. Ta = –30 ~ 85°C
11. Power Supply:
- **AVDD: 2.2 ~ 3.6V (typ. 3.3V)**
- **DVDD: 1.6 ~ 3.6V (typ. 3.3V)**
- **SVDD: 2.2 ~ 4.0 V (typ. 3.3V)**

12. Power supply Current: 19mA
13. Package: 32pin QFN (5mm x 5mm, 0.5mm pitch)
14. Pin/Register Compatible with AK4642EN/AK4643EN

■ Block Diagram

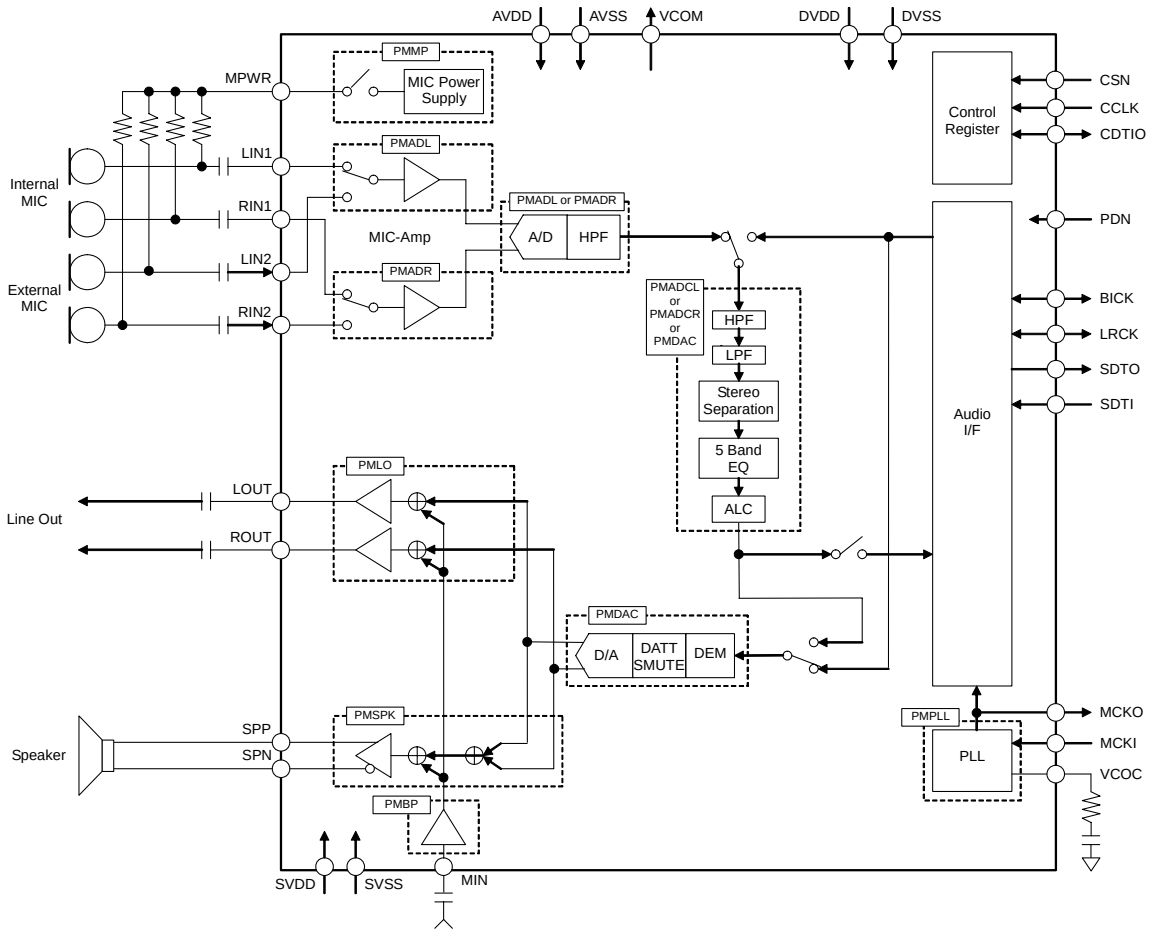
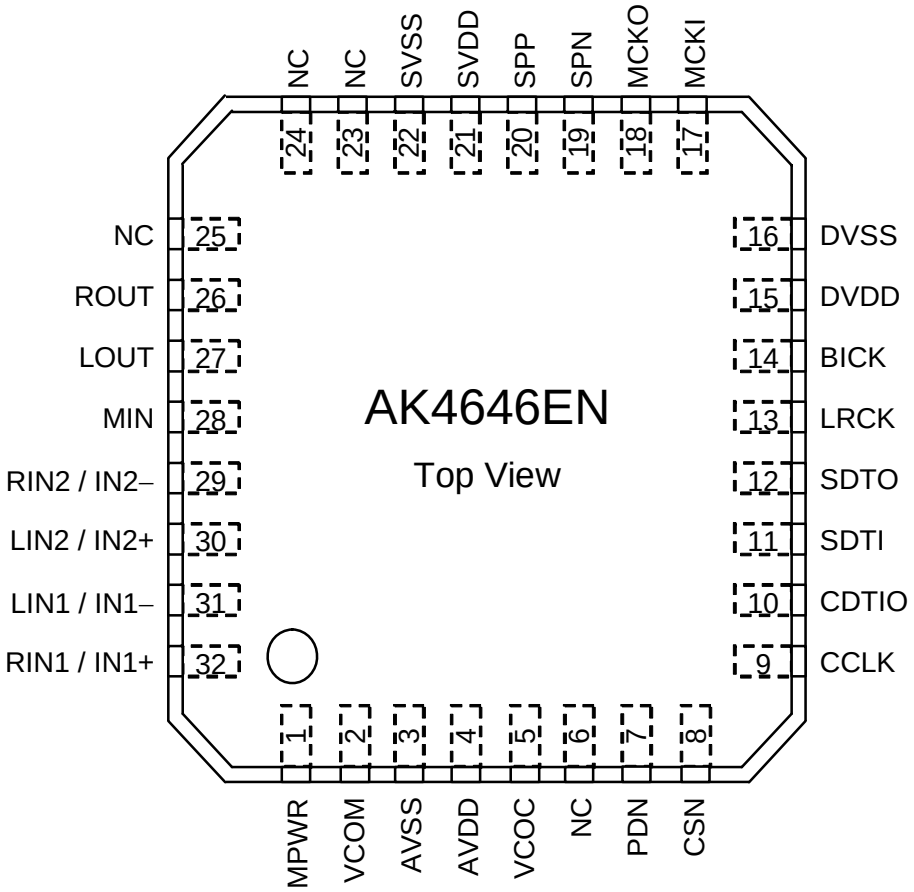


Figure 1. Block Diagram

■ Ordering Guide

AK4646EN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AKD4646	Evaluation board for AK4646	

■ Pin Layout



■ Comparison with AK4642/AK4643

1. Function

Function	AK4642	AK4643	AK4646
AVDD	2.6V ~ 3.6V		2.2V ~ 3.6V
DVDD	2.6V ~ 3.6V		1.6V ~ 3.6V
Power Supply for SPK-Amp	2.6V ~ 5.25V (HVDD)		2.2V ~ 4.0V (SVDD)
Output Voltage of MIC Power	0.75 x AVDD		0.8 x AVDD
MIC-Amp	0dB/+20dB/+26dB/+32dB		0dB/+10dB/+17dB/+20dB/ +23dB/+26dB/+29dB/ +32dB
HPF / LPF	1 Step		HPF : 2 Step, LPF : 1 Step
Notch filter	No		5 Band
ALC Recovery Operation Waiting Period	128/fs ~ 1024/fs	128/fs ~ 16384/fs	128/fs ~ 16384/fs
Read of ALC Volume	No	No	Yes
Output Volume	+12dB ~ -115dB, 0.5dB Step		+36dB ~ -54dB, 0.375dB Step (Note 1) 0dB ~ -18dB, 6dB Step
Headphone-Amp	Yes		No
Bass Boost	Yes		No
Receiver-Amp	No	Yes	No
SPK-Amp Output Power	400mW@3.3V	1.2W@5V	400mW@3.3V
Analog Mixing	1 Mono	2 Stereo	1 Mono
ADC Input Selector	2 Stereo	3 Stereo	2 Stereo
SPK-Amp Maximum Output Voltage for Piezo Speaker	8.5Vpp@SVDD=5V		6.33Vpp@SVDD=3.8V
μP I/F	3-Wire(Write only), I2C-Bus		3-Wire(Read/Write)
Audio I/F Format DSP Mode	No	Yes	No
EXT Master Mode	No	Yes	No
Master Clock frequency for PLL Mode	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz 24MHz, 27MHz		12MHz, 13.5MHz, 24MHz, 27MHz

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume function at same time for both recording and playback mode.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MPWR	O	MIC Power Supply Pin
2	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs and DAC outputs.
3	AVSS	-	Analog Ground Pin
4	AVDD	-	Analog Power Supply Pin
5	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resistor and capacitor in series.
6	NC	-	No Connect Pin No internal bonding. This pin should be connected to Ground.
7	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register.
8	CSN	I	Chip Select Pin
9	CCLK	I	Control Data Clock Pin
10	CDTIO	I/O	Control Data Input and Output Pin
11	SDTI	I	Audio Serial Data Input Pin
12	SDTO	O	Audio Serial Data Output Pin
13	LRCK	I/O	Input / Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	DVDD	-	Digital Power Supply Pin
16	DVSS	-	Digital Ground Pin
17	MCKI	I	External Master Clock Input Pin
18	MCKO	O	Master Clock Output Pin
19	SPN	O	Speaker Amp Negative Output Pin
20	SPP	O	Speaker Amp Positive Output Pin
21	SVDD	-	Speaker Amp Power Supply Pin
22	SVSS	-	Speaker Amp Ground Pin
23 24 25	NC	-	No Connect Pin No internal bonding. This pin should be connected to Ground or Open.
26	ROUT	O	Rch Stereo Line Output Pin
27	LOUT	O	Lch Stereo Line Output Pin
28	MIN	I	Mono Signal Input Pin
29	RIN2	I	Rch Analog Input 2 Pin (MDIF2 bit = "0", Single-ended Input)
	IN2−	I	Microphone Negative Input 2 Pin (MDIF2 bit = "1", Full-differential Input)
30	LIN2	I	Lch Analog Input 2 Pin (MDIF2 bit = "0", Single-ended Input)
	IN2+	I	Microphone Positive Input 2 Pin (MDIF2 bit = "1", Full-differential Input)
31	LIN1	I	Lch Analog Input 1 Pin (MDIF1 bit = "0", Single-ended Input)
	IN1−	I	Microphone Negative Input 1 Pin (MDIF1 bit = "1", Full-differential Input)
32	RIN1	I	Rch Analog Input 1 Pin (MDIF1 bit = "0", Single-ended Input)
	IN1+	I	Microphone Positive Input 1 Pin (MDIF1 bit = "1", Full-differential Input)

Note 2. All input pins except analog input pins (MIN, LIN1, RIN1, LIN2, RIN2) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, VCOC, SPN, SPP, ROUT, LOUT, MIN, RIN2/IN2−, LIN2/IN2+, LIN1/IN1−, RIN1/IN1+	These pins should be open.
Digital	MCKO	This pin should be open.
	MCKI	This pin should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, SVSS=0V; Note 3)

Parameter			Symbol	min	max	Units
Power Supplies:	Analog		AVDD	–0.3	4.6	V
	Digital		DVDD	–0.3	4.6	V
	Speaker-Amp		SVDD	–0.3	4.6	V
	|AVSS – DVSS|	(Note 4)	ΔGND1	-	0.3	V
	|AVSS – SVSS|	(Note 4)	ΔGND2	-	0.3	V
Input Current, Any Pin Except Supplies			IIN	-	±10	mA
Analog Input Voltage (Note 5)			VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)			VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)			Ta	–30	85	°C
Storage Temperature			Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)			Pd1	-	450	mW

Note 3. All voltages are with respect to ground.
Note 4. AVSS, DVSS and SVSS must be connected to the same analog ground plane.
Note 5.MIN, RIN2/IN2−, LIN2/IN2+, LIN1/IN1−, RIN1/IN1+ pins
Note 6. PDN, CSN, CCLK, CDTIO, SDTI, LRCK, BICK, MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to DVDD or less voltage.
Note 7. In case that PCB wiring density is 100%. This power is the AK4646 internal dissipation that does not include power of externally connected speaker.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, SVSS=0V; Note 3)

Parameter		Symbol	min	typ	Max	Units
Power Supplies (Note 8)	Analog	AVDD	2.2	3.3	3.6	V
	Digital	DVDD	1.6	3.3	3.6	V
	SPK-Amp (Note 9)	SVDD	2.2	3.3	4.0	V
	Difference	DVDD−AVDD	-	-	+0.3	V
		DVDD−SVDD	-	-	+0.3	V

Note 3. All voltages are with respect to ground.
Note 8. The power-up sequence between AVDD, DVDD and SVDD is not critical. When AVDD or SVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. When the power supplies are partially powered OFF, the AK4646 must be reset by bringing PDN pin "L" after these power supplies are powered ON again.
Note 9. SVDD = 2.2 ~ 3.6V when 8Ω dynamic speaker is connected to the AK4646.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, SVDD=3.3V; AVSS=DVSS=SVSS=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
MIC Amplifier: LIN1, RIN1, LIN2, RIN2 pins; MDIF1 = MDIF2 bits = "0" (Single-ended inputs)						
Input Resistance			20	30	40	kΩ
Gain	MGAIN2-0 bits = "000"		-	0	-	dB
	MGAIN2-0 bits = "001"		-	+20	-	dB
	MGAIN2-0 bits = "010"		-	+26	-	dB
	MGAIN2-0 bits = "011"		-	+32	-	dB
	MGAIN2-0 bits = "100"		-	+10	-	dB
	MGAIN2-0 bits = "101"		-	+17	-	dB
	MGAIN2-0 bits = "110"		-	+23	-	dB
	MGAIN2-0 bits = "111"		-	+29	-	dB
MIC Amplifier: IN1+, IN1−, IN2+, IN2− pins; MDIF1 = MDIF2 bits = "1" (Full-differential input)						
Input Voltage (Note 10)						
	MGAIN2-0 bits = "001"		-	-	0.242	Vpp
	MGAIN2-0 bits = "010"		-	-	0.121	Vpp
	MGAIN2-0 bits = "011"		-	-	0.061	Vpp
	MGAIN2-0 bits = "100"		-	-	0.765	Vpp
	MGAIN2-0 bits = "101"		-	-	0.342	Vpp
	MGAIN2-0 bits = "110"		-	-	0.171	Vpp
	MGAIN2-0 bits = "111"		-	-	0.086	Vpp
MIC Power Supply: MPWR pin						
Output Voltage (Note 11)			2.38	2.64	2.90	V
Load Resistance			0.5	-	-	kΩ
Load Capacitance			-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2 pins → ADC → IVOL, IVOL=0dB, ALC=OFF						
Resolution			-	-	16	Bits
Input Voltage (Note 12)		(Note 13)	0.178	0.210	0.242	Vpp
		(Note 14)	1.78	2.10	2.42	Vpp
S/(N+D)	(−1dBFS)	(Note 13)	73	83	-	dBFS
		(Note 14)	-	88	-	dBFS
D-Range	(−60dBFS, A-weighted)	(Note 13)	76	86	-	dB
		(Note 14)	-	95	-	dB
S/N	(A-weighted)	(Note 13)	76	86	-	dB
		(Note 14)	-	95	-	dB
Interchannel Isolation		(Note 13)	75	90	-	dB
		(Note 14)	-	100	-	dB
Interchannel Gain Mismatch		(Note 13)	-	0.1	0.8	dB
		(Note 14)	-	0.1	0.8	dB

Note 10. The voltage difference between IN1/2+ and IN1/2− pins. AC coupling capacitor should be inserted in series at each input pin. Full-differential mic input is not available at MGAIN2-0 bits = "000". Maximum input voltage of IN1+, IN1−, IN2+ and IN2− pins is proportional to AVDD voltage, respectively.
Vin = |(IN1/2+) – (IN1/2−)| = 0.073 x AVDD (max)@MGAIN2-0 bits = "001", 0.037 x AVDD (max)@MGAIN2-0 bits = "010", 0.018 x AVDD (max)@MGAIN2-0 bits = "011", 0.232 x AVDD (max)@MGAIN2-0 bits = "100", 0.104 x AVDD (max)@MGAIN2-0 bits = "101", 0.052 x AVDD (max)@MGAIN2-0 bits = "110", 0.026 x AVDD (max)@MGAIN2-0 bits = "111"

Note 11. Output voltage is proportional to AVDD voltage. Vout = 0.8 x AVDD (typ)

Note 12. Input voltage is proportional to AVDD voltage Vin = 0.0636 x AVDD (typ)@MGAIN2-0 bits = "001" (+20dB), Vin = 0.636 x AVDD (typ)@MGAIN2-0 bits = "000" (0dB)

Note 13. MGAIN2-0 bits = "001" (+20dB)

Note 14. MGAIN2-0 bits = "000" (0dB)

Parameter		min	typ	max	Units
DAC Characteristics:					
Resolution		-	-	16	Bits
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, OVOL=0dB, LOVL1-0 bit = "00", R_L=10kΩ					
Output Voltage (Note 15)	LOVL1-0 bit = "00"	1.78	1.98	2.18	Vpp
	LOVL1-0 bit = "01"	2.25	2.50	2.75	Vpp
S/(N+D) (–3dBFS)		78	88	-	dBFS
S/N (A-weighted)		82	92	-	dB
Interchannel Isolation		85	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.8	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, OVOL=0dB, R_L=8Ω, BTL, SVDD=3.3V					
Output Voltage (Note 16)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	1.79	-	Vrms
S/(N+D)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	60	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		20	50	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	20	-	dB
S/N (A-weighted)		80	90	-	dB
Load Resistance		8	-	-	Ω
Load Capacitance		-	-	30	pF

Note 15. Output voltage is proportional to AVDD voltage.Vout = 0.6 x AVDD (typ)@LOVL bit = "0".

Note 16. Output voltage is proportional to AVDD voltage.
In case of Full-differential, Vout = 0.94 x AVDD (typ)@SPKG1-0 bits = "00", 1.21 x AVDD (typ)@SPKG1-0 bits = "01", 2.05 x AVDD (typ)@SPKG1-0 bits = "10", 2.58 x AVDD (typ)@SPKG1-0 bits = "11"

Parameter			min	typ	max	Units
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF,OVOL=0dB, C_L=3μF, R_{serial}=10Ω x 2, BTL, SVDD=3.8V						
Output Voltage (Note 16)	SPKG1-0 bits = "11", -0.5dBFS		-	6.33	-	Vpp
S/(N+D) (Note 17)	SPKG1-0 bits = "11", -0.5dBFS		-	60	-	dB
S/N	(A-weighted)		-	90	-	dB
Load Impedance (Note 18)			50	-	-	Ω
Load Capacitance (Note 18)			-	-	3	μF
Mono Input: MIN pin (External Input Resistance=20kΩ)						
Maximum Input Voltage (Note 19)			-	1.98	-	Vpp
Gain (Note 20)						
MIN → LOUT/ROUT		LOVL1-0 bit = "00"	-4.5	0	+4.5	dB
		LOVL1-0 bit = "01"	-	+2	-	dB
		LOVL1-0 bit = "10"	-	+4	-	dB
		LOVL1-0 bit = "11"	-	+6	-	dB
MIN → SPP/SPN						
	ALC bit = "0", SPKG1-0 bits = "00"		+0.1	+4.6	+9.1	dB
	ALC bit = "0", SPKG1-0 bits = "01"		-	+6.6	-	dB
	ALC bit = "0", SPKG1-0 bits = "10"		-	+8.6	-	dB
	ALC bit = "0", SPKG1-0 bits = "11"		-	+10.6	-	dB
	ALC bit = "1", SPKG1-0 bits = "00"		-	+6.6	-	dB
	ALC bit = "1", SPKG1-0 bits = "01"		-	+8.6	-	dB
	ALC bit = "1", SPKG1-0 bits = "10"		-	+10.6	-	dB
	ALC bit = "1", SPKG1-0 bits = "11"		-	+12.6	-	dB
Power Supplies:						
Power Up (PDN pin = "H")						
All Circuit Power-up (Note 21)						
	AVDD+DVDD		-	15	23	mA
	SVDD (No Output)		-	4	12	mA
Power Down (PDN pin = "L") (Note 22)						
AVDD+DVDD+SVDD			-	1	100	μA

Note 17. In case of measuring at SPP and SPN pins.

Note 18. Load impedance is total impedance of series resistance and piezo speaker impedance at 1kHz in Figure 34. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Note 19. Maximum voltage is in proportion to both AVDD and external input resistance (Rin).
Vin = 0.636 x AVDD x Rin / 20kΩ (typ).

Note 20. The gain is in inverse proportion to external input resistance

Note 21. PLL Master Mode (MCKI=12MHz); PMADL = PMADR = PMDAC = PMLO = PMSPK = PMVCM = PMPLL = MCKO = PMBP = PMMP = M/S bits = "1". MPWR pin outputs 0mA.
AVDD= 10mA(typ), DVDD=5mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=10mA(typ), DVDD=4mA(typ).

Note 22. All digital input pins are fixed to DVDD or DVSS.

FILTER CHARACTERISTICS

(Ta = 25°C; AVDD =2.2 ~ 3.6V, DVDD =1.6 ~ 3.6V, SVDD =2.2 ~ 4.0V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 23)	±0.16dB	PB	0	-	17.3	kHz
	−0.66dB		-	19.4	-	kHz
	−1.1dB		-	19.9	-	kHz
	−6.9dB		-	22.1	-	kHz
Stopband		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 24)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
DAC Digital Filter (LPF):						
Passband (Note 23)	±0.05dB	PB	0	-	20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 24)		GD	-	20	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 23. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB = 20.0kHz = 0.454*fs (@-1.0dB). Each response refers to that of 1kHz.

Note 24. The calculation delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal.

DC CHARACTERISTICS

(Ta = 25°C; AVDD =2.2 ~ 3.6V, DVDD =1.6 ~ 3.6V, SVDD =2.2 ~ 4.0V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(DVDD ≥ 2.2V)	VIH	70%DVDD	-	-	V
	(DVDD < 2.2V)		80%DVDD	-	-	V
Low-Level Input Voltage	(DVDD ≥ 2.2V)	VIL	-	-	30%DVDD	V
	(DVDD < 2.2V)		-	-	20%DVDD	V
High-Level Output Voltage	(Iout=−80μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage	(Iout= 80μA)	VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD =2.2 ~ 3.6V, DVDD =1.6 ~ 3.6V, SVDD =2.2 ~ 4.0V; C_L=20pF)

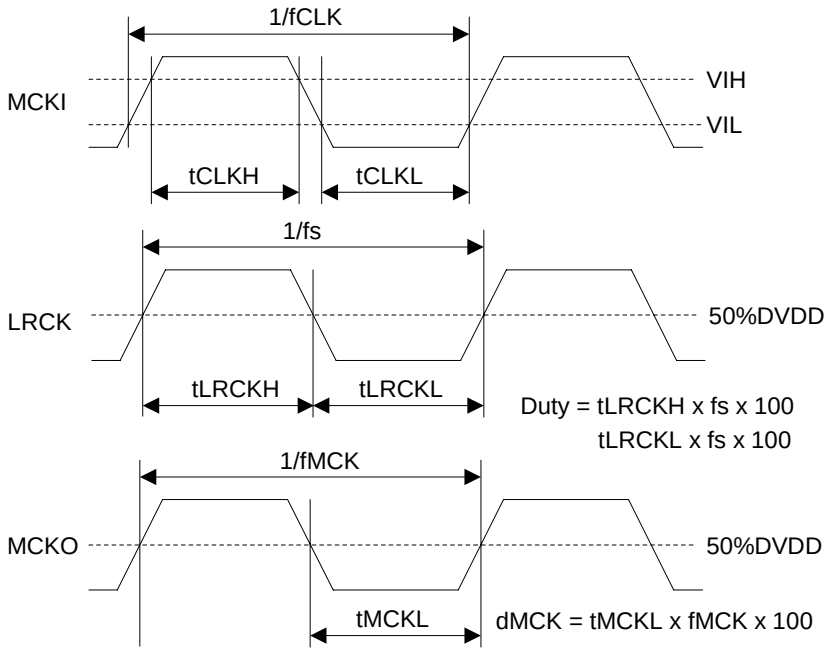
Parameter		Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	12	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	12	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	240	-	-	ns
Pulse Width High		tBCKH	240	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	26	kHz
	1024fs	fs	7.35	-	13	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Input Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 25)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 25)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 25)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 26)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 26)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)	tCCZ	-	-	70	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 27)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 28)	tPDV	-	1059	-	1/fs

Note 25. BICK rising edge must not occur at the same time as LRCK edge.
Note 26. CCLK rising edge must not occur at the same time as CSN edge.
Note 27. The AK4646 can be reset by the PDN pin = "L".
Note 28. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram



Note 29. MCKO is not available at EXT Master mode.
Figure 2. Clock Timing (PLL / EXT Master mode)

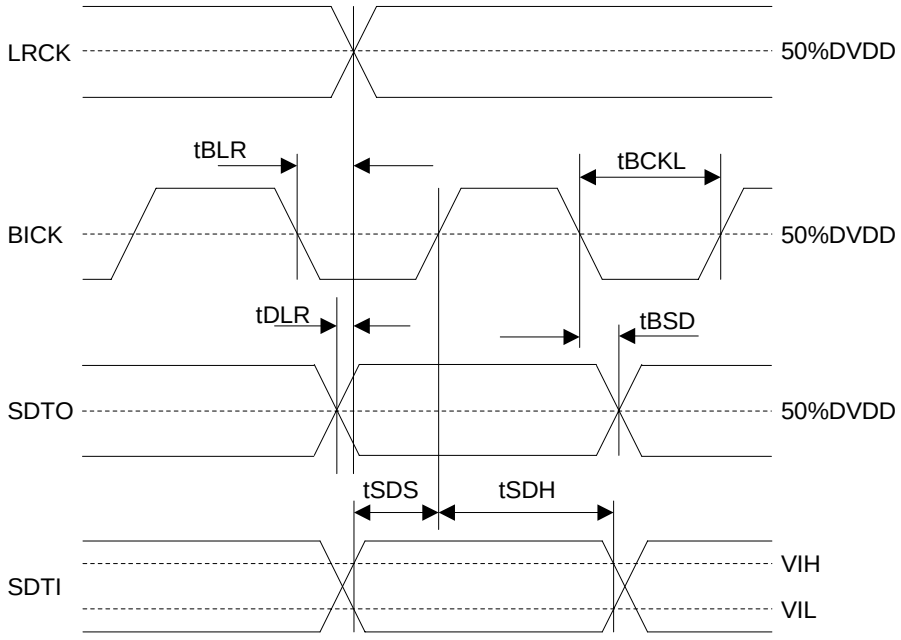


Figure 3. Audio Interface Timing (PLL/EXT Master mode)

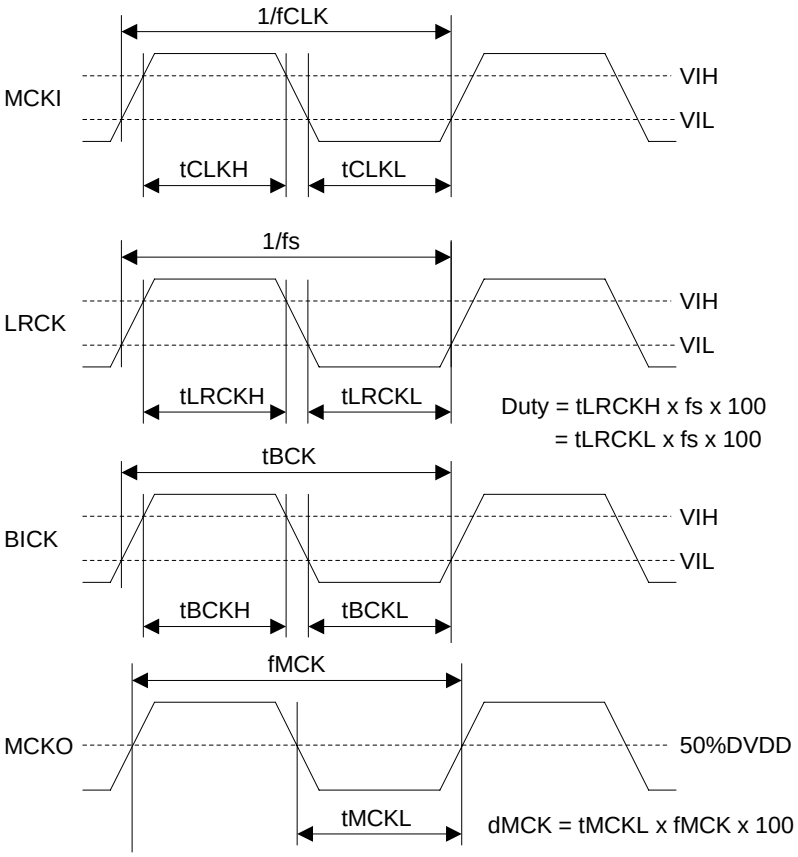


Figure 4. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

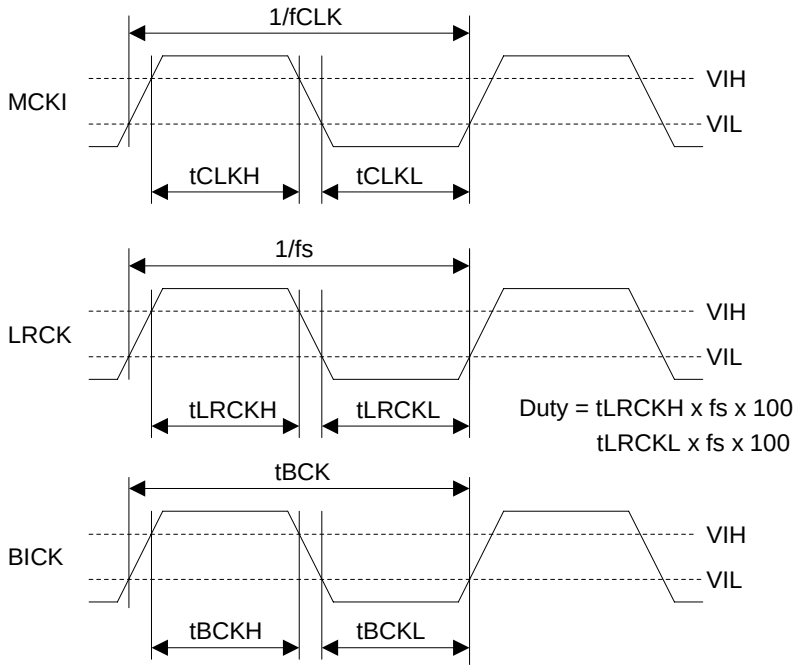


Figure 5. Clock Timing (EXT Slave mode)

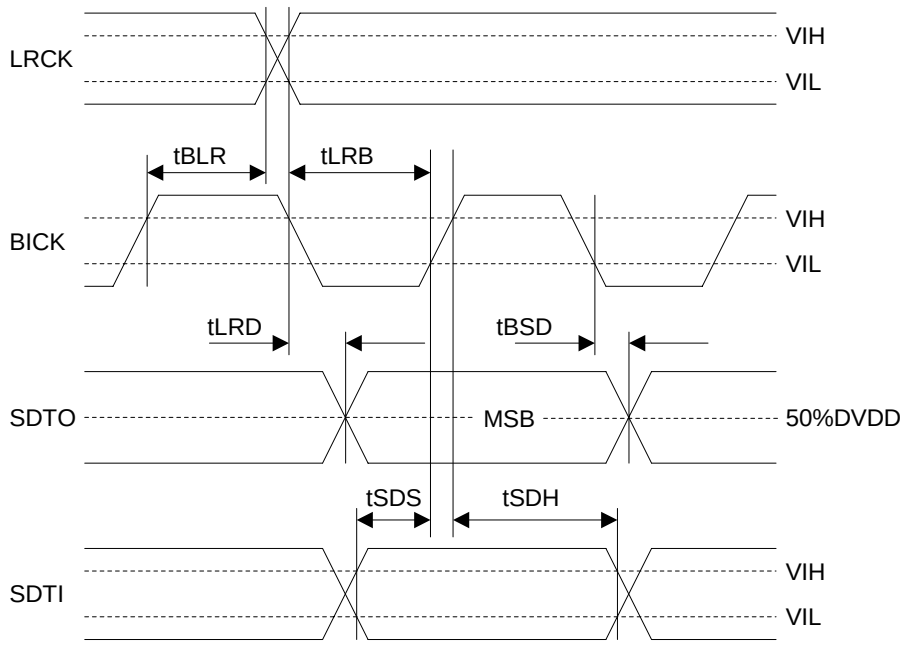


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

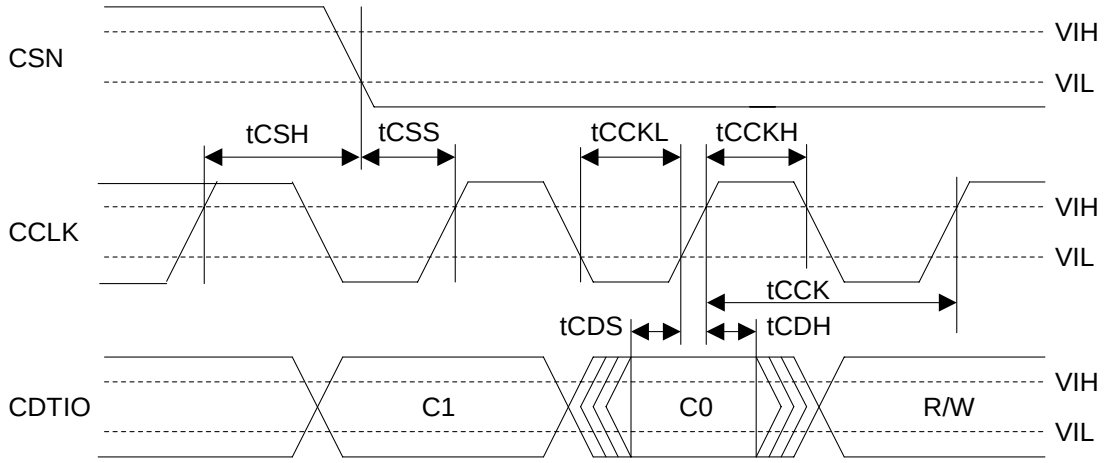


Figure 7. WRITE Command Input Timing

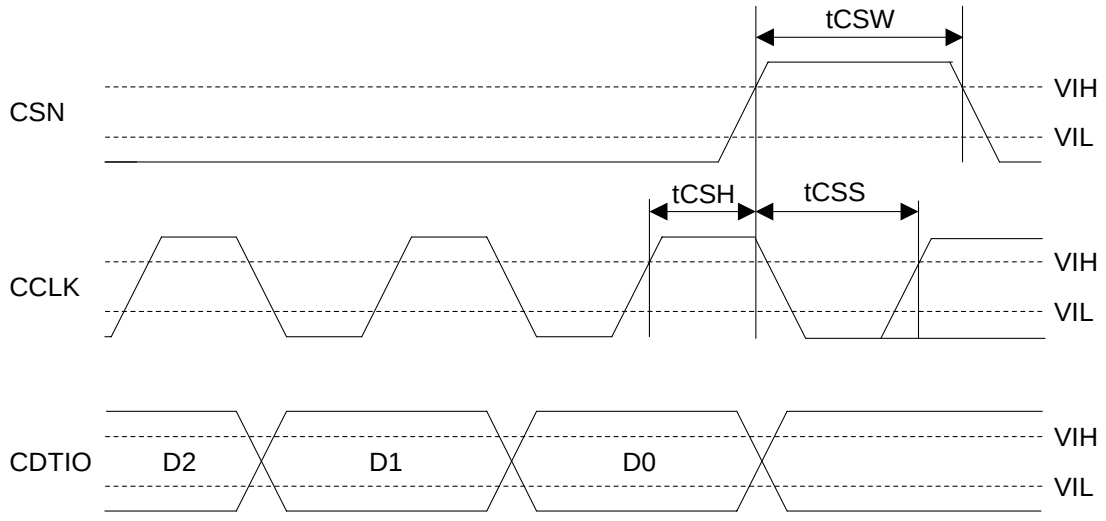


Figure 8. WRITE Data Input Timing

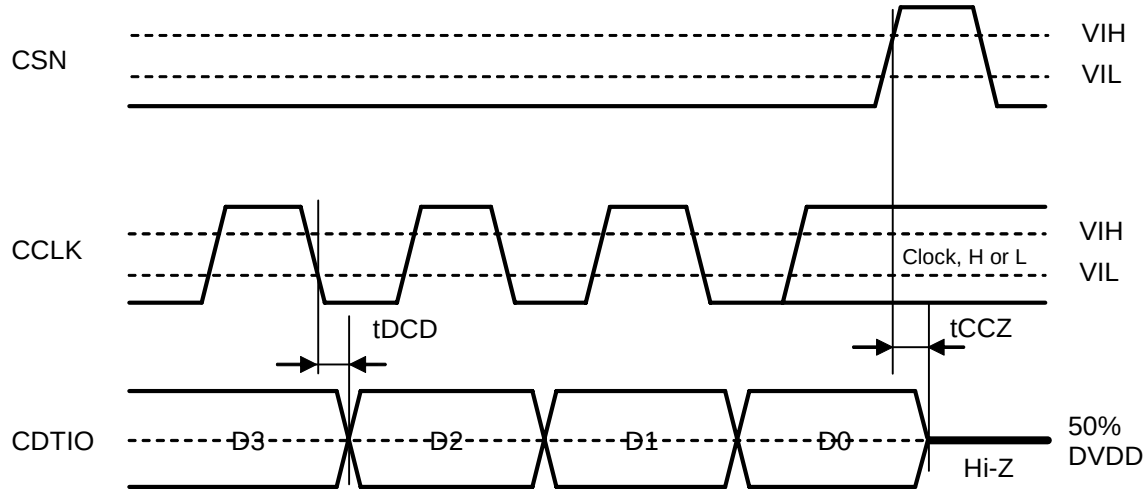


Figure 9. Read Data Output Timing

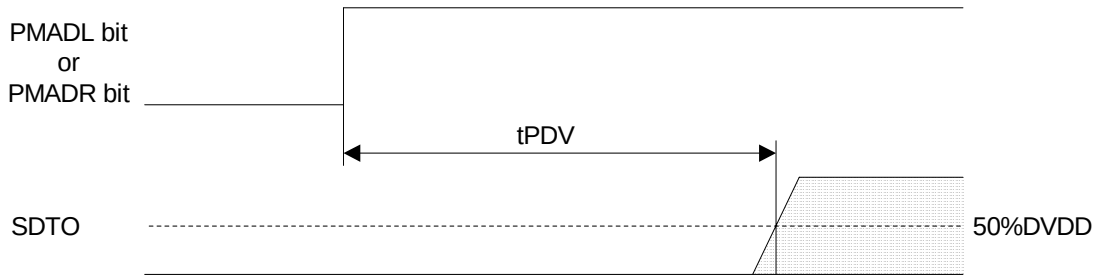


Figure 10. Power Down & Reset Timing 1

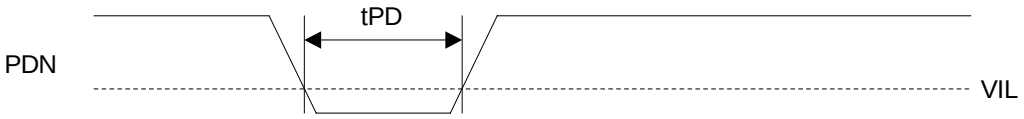


Figure 11. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1 and Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 30)	1	1	Table 4	Figure 12
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 13
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 14 Figure 15
EXT Slave Mode	0	0	x	Figure 16
EXT Master Mode	0	1	x	Figure 17

Note 30. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	"L"	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	"L"	Selected by PLL3-0 bits	Input (Selected by BCKO bit)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	"L"	GND	Input (Selected by BCKO bit)	Input (1fs)
EXT Slave Mode	0	"L"	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	"L"	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 31. When PMVCM bit = M/S bit = "1" and MCKI is input, LRCK and BICK are output, even if PMDAC bit = PMADL bit = PMADR bit = "0".

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4646 is power-down mode (PDN pin = "L") and exits reset state, the AK4646 is slave mode. After exiting reset state, the AK4646 goes to master mode by changing M/S bit = "1".

When the AK4646 is on the master mode, LRCK and BICK pins are a floating state until M/S bit becomes "1". LRCK and BICK pins of the AK4646 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, when the AK4646 is supplied stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or when the sampling frequency is changed.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms	(default)
1	0	0	0	1	N/A	-	-	-	-	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
6	0	1	1	0	MCKI pin	12MHz	10k	10n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	10n	40ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
Others	Others				N/A					

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	(default)
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (Reference Clock = MCKI pin)

When PLL2 bit is "0" (PLL reference clock input is LRCK or BICK pin), the sampling frequency is selected by FS3 and FS2 bits. (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	Don't care	Don't care	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	Don't care	Don't care	12kHz < fs ≤ 24kHz	
2	1	0	Don't care	Don't care	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2
(PLL Reference: Clock: LRCK or BICK pin)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BICK pins go to "L" and irregular frequency clock is output from MCKO pins at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", MCKO pin goes to "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACL and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (12MHz, 13.5MHz, 24MHz or 27MHz) is input to MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

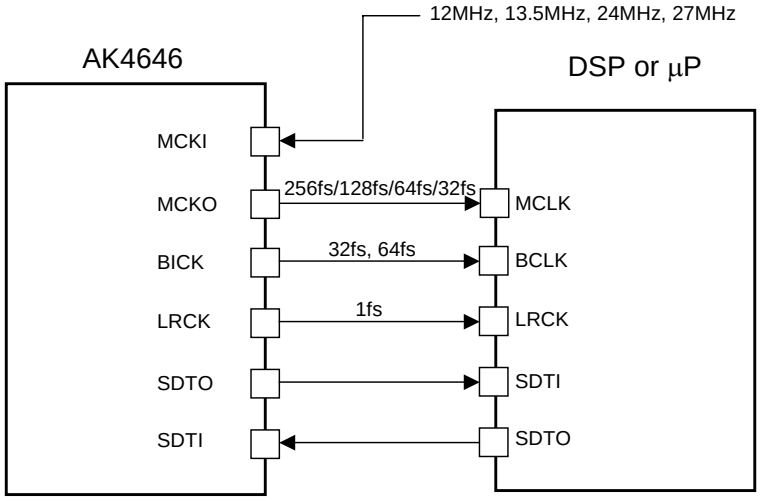


Figure 12. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to MCKI, BICK or LRCK pin. The required clock for the AK4646 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

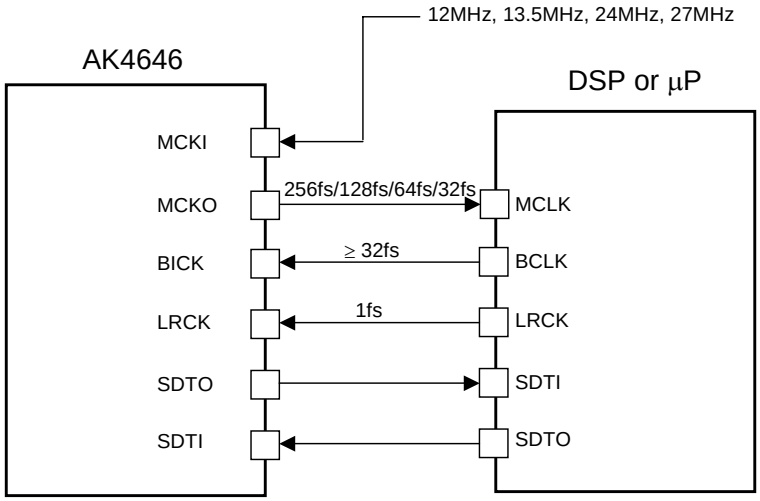


Figure 13. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

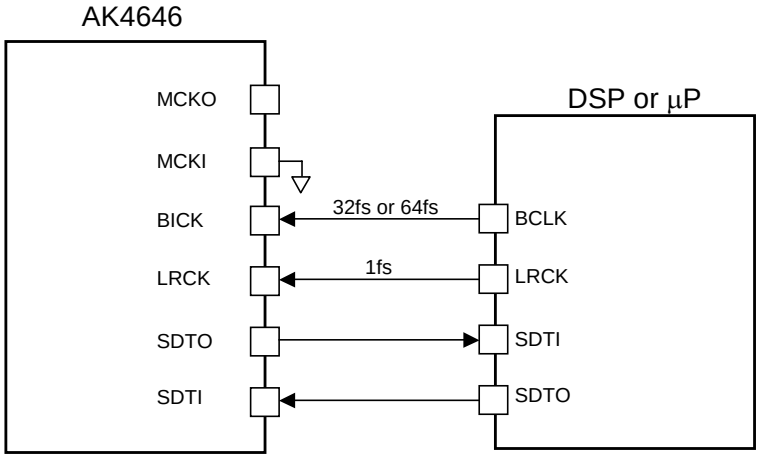


Figure 14. PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)

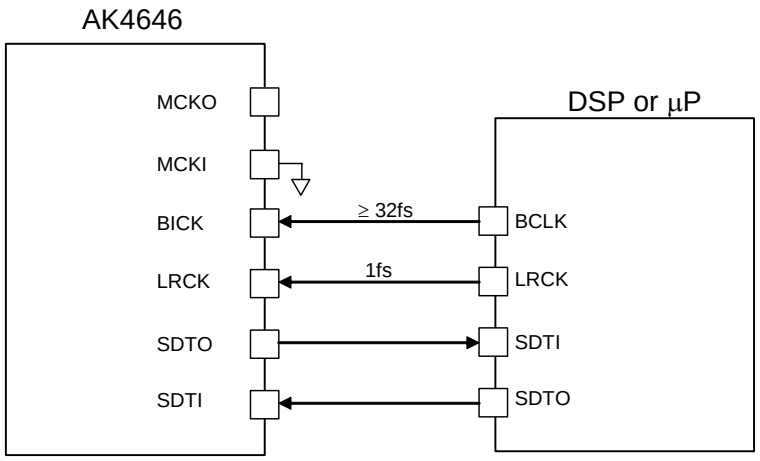


Figure 15 PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4646 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = "0").

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4646 becomes EXT mode. Master clock can directly be inputted from MCKI pin, without the internal PLL circuit operation. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate this mode are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	Don't care	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	Don't care	0	1	1024fs	7.35kHz ~ 13kHz	
2	Don't care	1	0	512fs	7.35kHz ~ 26kHz	
3	Don't care	1	1	256fs	7.35kHz ~ 48kHz	
Others	Others			N/A	N/A	

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83dB
512fs	93dB
1024fs	93dB

Table 12. Relationship between MCKI and S/N of LOUT/ROUT pins

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4646 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. When the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = "0").

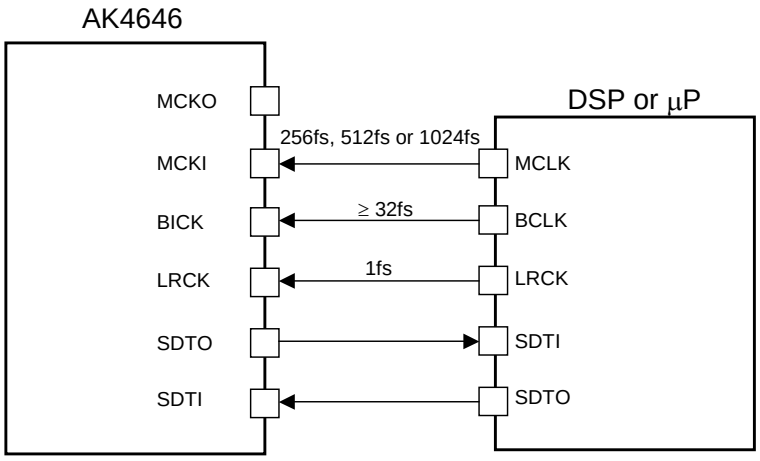


Figure 16. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4646 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock is input from MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 13).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	Don't care	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	Don't care	0	1	1024fs	7.35kHz ~ 13kHz	
2	Don't care	1	0	256fs	7.35kHz ~ 48kHz	
3	Don't care	1	1	512fs	7.35kHz ~ 26kHz	

Table 13. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 14.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83dB
512fs	93dB
1024fs	93dB

Table 14. Relationship between MCKI and S/N of LOUT/ROUT pins

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = "1", PMADR bit = "1" or PMDAC bit = "1"). If MCKI is not provided, the AK4646 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = "0").

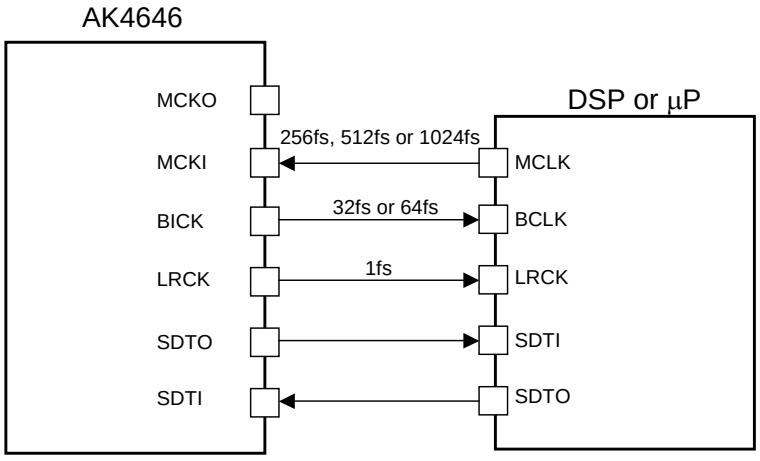


Figure 17. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 15. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the PDN pin should be "L" and be changed from "L" to "H" after all power supply are supplied. "L" time of 150ns or more is needed to reset in the AK4646. This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADL or PMADR bit is changed from "0" to "1". The initialization cycle time is 1059/fs=24ms@fs=44.1kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". The ADC output reflects the analog input signal after the initialization cycle is complete.

The DAC outputs unexpected data after PMDAC bit "0" → "1" until 67/fs = 1.52ms@fs = 44.1kHz, then the DAC starts outputting the normal voltage.

(Note) The initial data of ADC has the offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset isn't small, don't use the initial data of ADC.

■ Audio Interface Format

Three types of data formats are available and selected by setting the DIF1-0 bits (Table 16). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4646 in master mode, but must be input to the AK4646 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑").

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	N/A	N/A	N/A	-	
1	0	1	MSB justified	LSB justified	≥ 32fs	Figure 18	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 19	(default)
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 20	

Table 16. Audio Interface Format

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "−1" at 16bit data is converted to "−1" at 8-bit data. And when the DAC playbacks this 8-bit data, "−1" at 8-bit data will be converted to "−256" at 16-bit data which is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

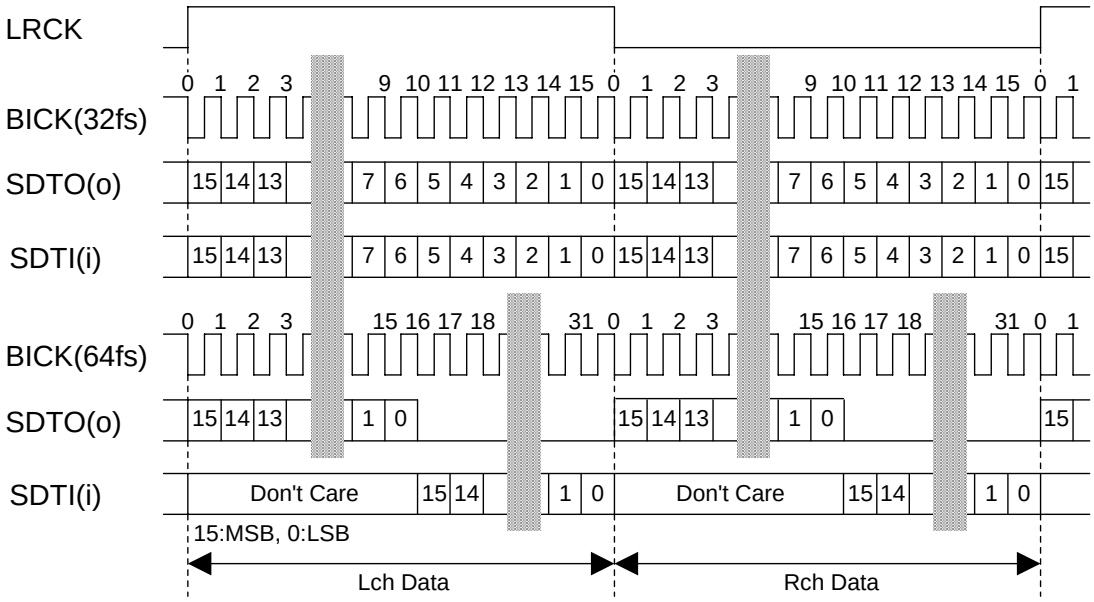


Figure 18. Mode 1 Timing

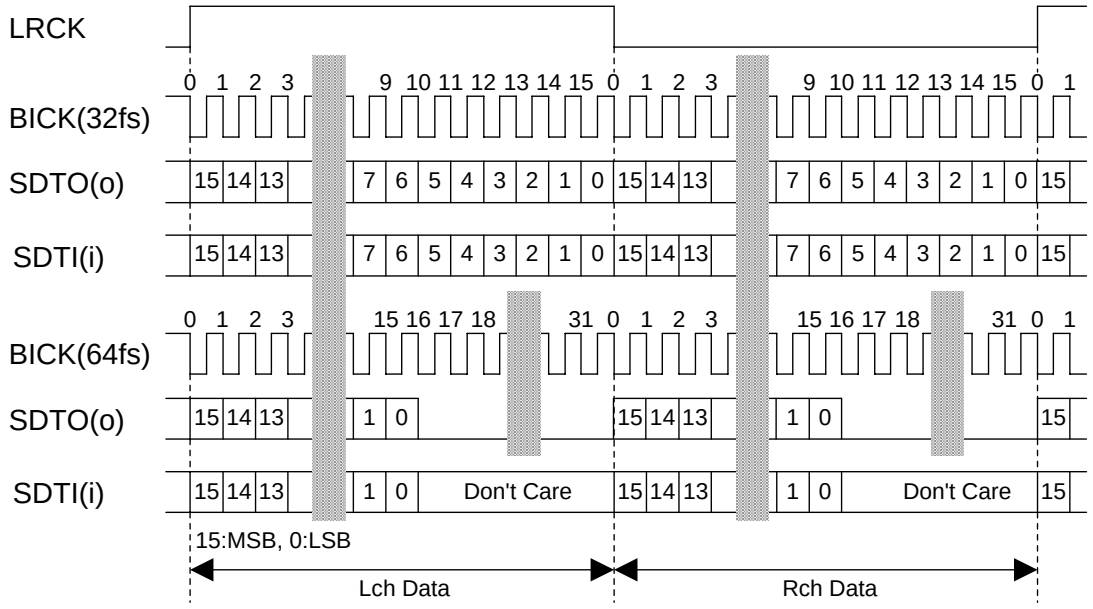


Figure 19. Mode 2 Timing

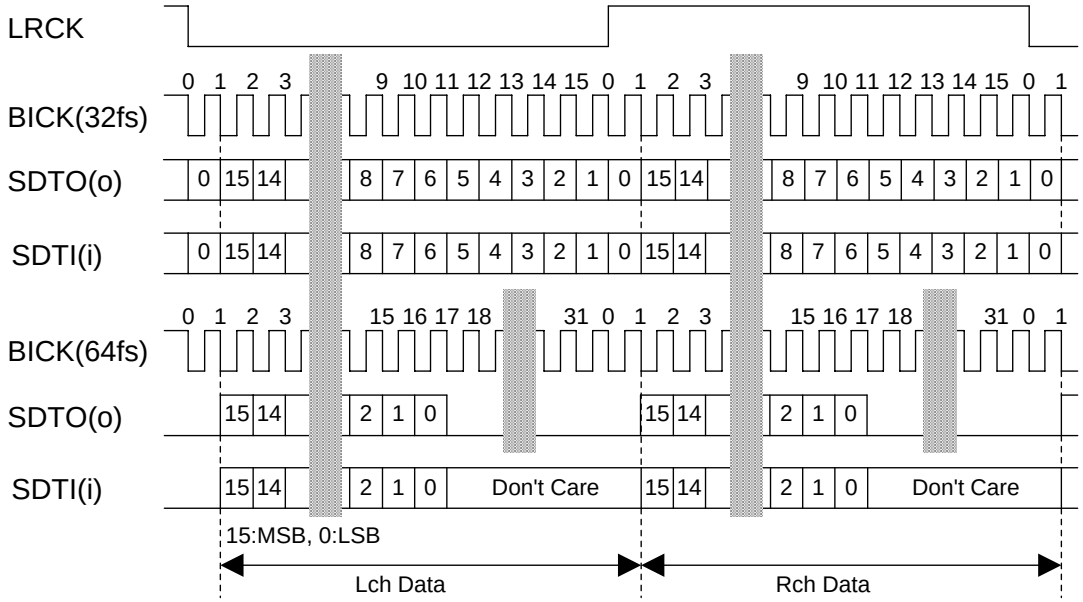


Figure 20. Mode 3 Timing

■ Mono/Stereo Mode

PMADL and PMADR bits set mono/stereo ADC operation.
When changing ADC operation, PMADL and PMADR bits should be set "0" at first.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 17. Mono/Stereo ADC operation

■ MIC/LINE Input Selector

The AK4646 has an input selector. When MDIF1 and MDIF2 bits are "0", INL and INR bits select LIN1/LIN2 and RIN1/RIN2, respectively. When MDIF1 and MDIF2 bits are "1", LIN1, RIN1, LIN2 and RIN2 pins become IN1−, IN1+, IN2+ and IN2− pins respectively. In this case, full-differential input is available (Figure 22).

MDIF1 bit	MDIF2 bit	INL bit	INR bit	Lch	Rch	
0	0	0	0	LIN1	RIN1	(default)
			1	LIN1	RIN2	
		1	0	LIN2	RIN1	
			1	LIN2	RIN2	
	1	0	x	LIN1(Note 32)	IN2+/−	
		1	x	N/A	N/A	
1	0	x	0	N/A	N/A	
			1	IN1+/−	RIN2(Note 33)	
	1	x	x	IN1+/−	IN2+/−	

Note 32. Any signal should be input to RIN1 pin, when MDIF1 bit = "0", MDIF2 bit = "1" and INL bit = "0".
Note 33. Any signal should be input to LIN2 pin, when MDIF1 bit = "1", MDIF2 bit = "0" and INL bit = "1".
Table 18. MIC/Line in Path Select

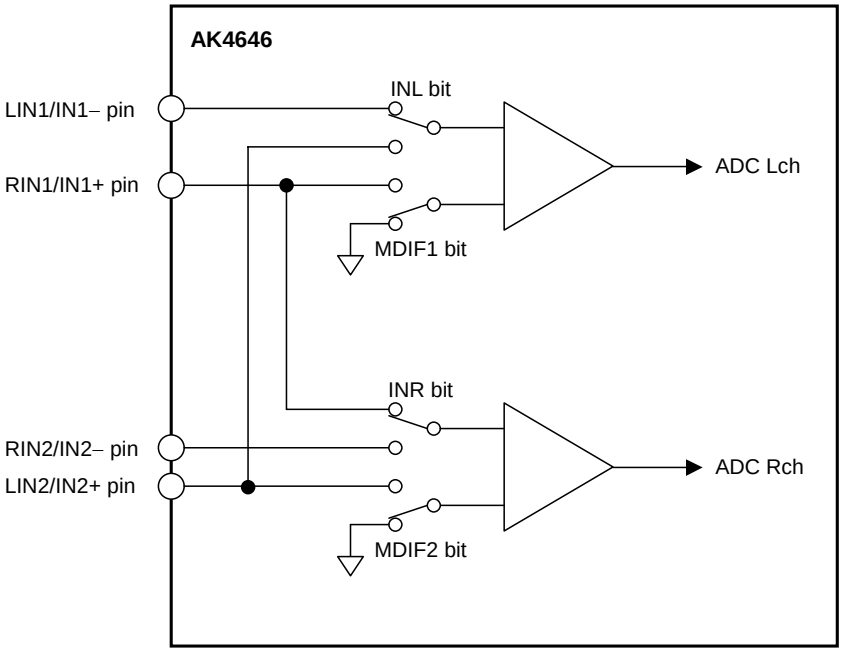


Figure 21. Mic/Line Input Selector

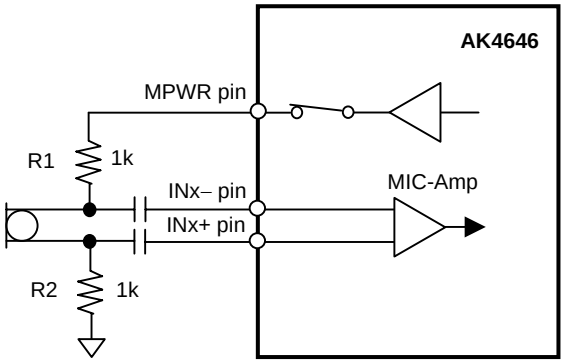


Figure 22. Connection Example for Full-differential Mic Input (MDIF1/2 bits = "1")

■ MIC Gain Amplifier

The AK4646 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN2-0 bits (Table 19). The typical input impedance is 30kΩ (typ).

MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0dB	
0	0	1	+20dB	(default)
0	1	0	+26dB	
0	1	1	+32dB	
1	0	0	+10dB	
1	0	1	+17dB	
1	1	0	+23dB	
1	1	1	+29dB	

Table 19. Mic Input Gain

■ MIC Power

When PMMP bit = "1", the MPWR pin supplies power for the microphone. This output voltage is typically 0.8 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo microphone, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to MPWR pin (Figure 23).

PMMP bit	MPWR pin	
0	Hi-Z	(default)
1	Output	

Table 20. MIC Power

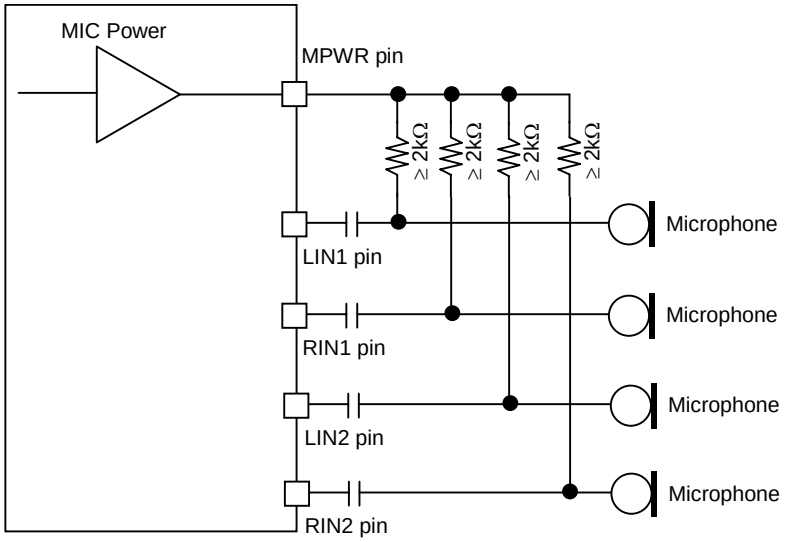
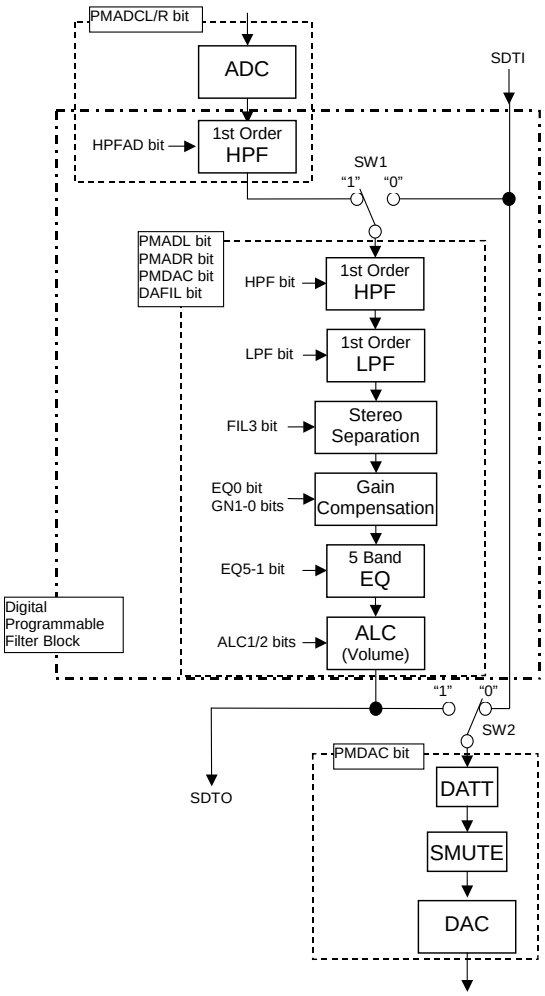


Figure 23. MIC Block Circuit

■ Digital Block

The digital block consists of block diagram as shown in Figure 24. HPF ~ ALC blocks are used for recording path when DAFIL bit = "0" and either ADC (Lch or Rch) is powered-up. Also HPF ~ ALC blocks are used for playback path when DAFIL bit = "1" or both ADC (Lch and Rch) are powered-down (Figure 24 ~ Figure 27, Table 21). The SDTO pin outputs "L" when DAFIL bit = "1", even if ADC is powered-up.



SW1, SW2: see Table 21

(1) ADC: Include the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) DAC: Include the Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(3) HPF: High Pass Filter. Applicable to use as Wind-Noise Reduction Filter. (See "Programmable Filter")
(4) LPF: Low Pass Filter (See "Digital Programmable Filter".)
(5) Stereo Separation: Digital Separation Emphasis Filter (See "Digital Programmable Filter")
(6) Gain Compensation: Composed of the Equalizer (EQ0) and the Gain (0bB/+12dB/+24dB). Compensate the frequency response and the gain after the Stereo Separation Emphasis Filter.
(7) 5-Band Notch: Applicable to use as Equalizer or Notch Filter. (See "Digital Programmable Filter")
(8) ALC: Input Digital Volume with ALC function. (See "Input Digital Volume" and "ALC")
(9) DATT: 4-band Digital Volume for recording path. (See "Digital Volume 2")
(10) SMUTE: Soft mute. (See "Soft Mute".)

Figure 24 Digital Block Path Select

Mode	PMADL bit	PMADR bit	PMDAC bit	DAFIL bit	LOOP bit	Figure 24 SW		Figure
						SW1	SW2	
Recording Mode	1	1	x	0	0	1	0	Figure 25
	1	0	x	0	0	1	0	
	0	1	x	0	0	1	0	
Playback Mode	0	0	1	0	0	0	1	Figure 26
	x	x	1	1	0	0	1	
Loop Through Mode	1	1	1	0	1	1	1	Figure 27
	1	0	1	0	1	1	1	
	0	1	1	0	1	1	1	

"x": Don't Care

Table 21. Recording Playback Mode

LPF bit, HPF bit, FIL3 bit, EQ0 bit, EQ1 bit, EQ2 bit, EQ3 bit, EQ4 bit, EQ5 bit, ACL1 bit and ALC2 bit should be "0" when selecting those modes.

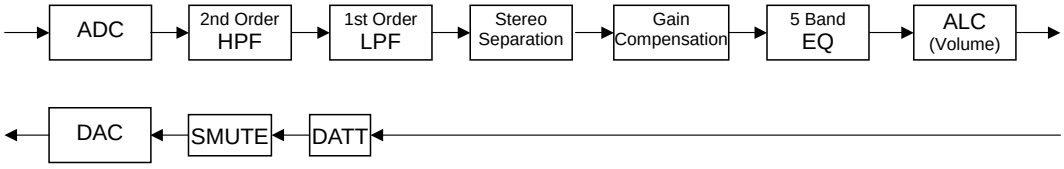


Figure 25. Path at Recording Mode (default)

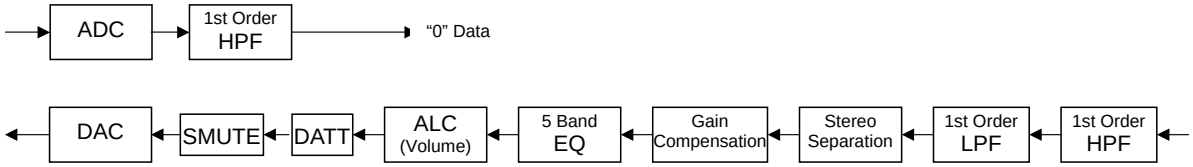


Figure 26. Path at Playback Mode

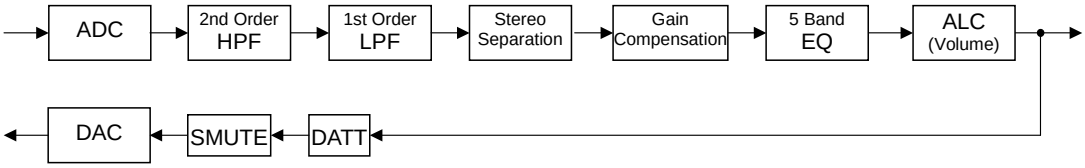


Figure 27. Path at Loop Through Mode

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF)

Normally, this HPF is used for a Wind-Noise Reduction Filter. This is composed with 2 steps of 1st order HPF. The coefficient of both HPF is the same and set by F1A13-0 bits and F1B13-0 bits. HPFAD bit controls ON/OFF of the 1st step HPF and HPF bit controls ON/OFF of the 2nd step HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when HPFAD=HPF bits = "0" or PMADL=PMADR= PMDAC bits = "0".

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 34)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when LPF bit = "0" or PMADL=PMADR=PMDAL=PMDAR bits = "0".

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 34)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F1B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

FIL3 is used to emphasize the stereo separation of stereo mic recording data or playback data. F3A13-0 and F3B13-0 bits set the filter coefficient of FIL3. FIL3 becomes High Pass Filter (HPF) at F3AS bit = "0", and Low Pass Filter (LPF) at F3AS bit = "1". FIL3 bit controls ON/OFF of FIL3. When Stereo Separation Emphasis Filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit = "0" or PMADL = PMADR = PMDAC bits = "0".

1) When FIL3 is set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Note 34)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) When FIL3 is set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
K: Filter gain [dB] (0dB ≥ K ≥ −10dB)

Register setting (Note 34)
FIL3: F3AS bit = "1", F3A [13:0] bits =A, F3B [13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation (EQ0)

Gain Compensation is used to compensate the frequency response and the gain that is changed by Stereo Separation Emphasis Filter. Gain Compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0, E0B13-0 and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 22). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMADL=PMADR= PMDAC bits = "0".

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting (Note 34)
E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

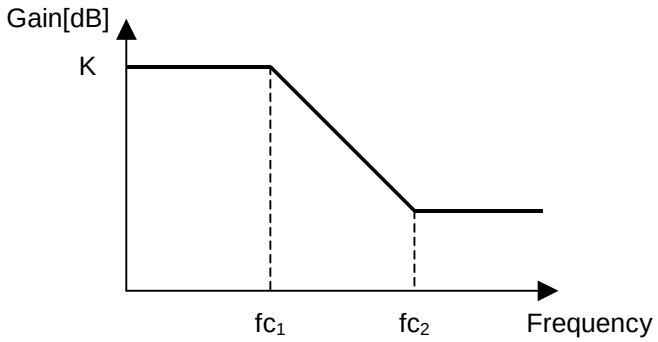


Figure 28. EQ0 Frequency Response

GN1	GN0	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 22. Gain select of gain block (x: Don't care)

(5) 5-band Notch

This block can be used as Equalizer or Notch Filter. 5-band Equalizer (EQ1, EQ2, EQ3, EQ4 and EQ5) is selected ON/OFF independently by EQ1, EQ2, EQ3, EQ4 and EQ5 bits. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient should be set when EQx bit = "0" or PMADL=PMADR= PMDAC bits = "0".

fs: Sampling frequency
$fo_1 \sim fo_5$: Center frequency
$fb_1 \sim fb_5$: Band width where the gain is 3dB different from center frequency
$K_1 \sim K_5$: Gain ($-1 \le K_n \le 3$)

Register setting (Note 34)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function

$$H(z) = 1 + h_1(z) + h_2(z) + h_3(z) + h_4(z) + h_5(z)$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency should be set as below.
$fo_n / fs < 0.497$

When gain of K is set to "-1", the equalizer becomes notch filter. When it is used as notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revise a gap of frequency and calculate the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 34. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block when ALC bit is "1". When both Lch and Rch of ADC are powered-down or DAFIL bit is "1", ALC circuit operates at playback path. When either Lch and Rch of ADC is powered-up and DAFIL bit is "0", ALC circuit operates at recording path.

Note 35. In this section, VOL means IVL and IVR for recording path, OVL and OVR for playback path.
Note 36. In this section, ALC bit means ALC1 bit for recording path, ALC2 bit for playback path.
Note 37. In this section, REF means IREF for recording path, OREF for playback path.

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 23), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 24). The VOL is then set to the same value for both channels.

When ZELMN bit = "0" (zero cross detection is enabled), the VOL value is changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 25). In addition, when LFST bit = "1", in the case of a output level exceeding FS, it is changed in 1Step (L/R common) instantly (cycle: 1/fs). In the case of an output level does not exceeding FS, it is zero crossing or VOL value is changed at the time of being zero crossing timeout.

When ZELMN bit = "1" (zero cross detection is disabled), VOL value is immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless as the setting of LMAT1-0 bits.

The attenuation operation is done continuously until the input signal level becomes ALC limiter detection level (Table 23) or less. After completing the attenuation operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1	LMTH0	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ −2.5dBFS	−2.5dBFS > ALC Output ≥ −4.1dBFS	(default)
0	1	ALC Output ≥ −4.1dBFS	−4.1dBFS > ALC Output ≥ −6.0dBFS	
1	0	ALC Output ≥ −6.0dBFS	−6.0dBFS > ALC Output ≥ −8.5dBFS	
1	1	ALC Output ≥ −8.5dBFS	−8.5dBFS > ALC Output ≥ −12dBFS	

Table 23. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1	LMAT0	ALC1 Limiter ATT Step				
		ALC1 Output ≥ LMTH	ALC1 Output ≥ FS	ALC1 Output ≥ FS + 6dB	ALC1 Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 24. ALC Limiter ATT Step (x: Don't care)

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 25. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 26) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 23) during the wait time, the ALC recovery operation is done. The VOL value is automatically incremented by RGAIN1-0 bits (Table 27) up to the set reference level (Table 28) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 25). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is done at a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is done.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to "01", VOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits(Table 30).

WTM2	WTM1	WTM0		ALC Recovery Operation Waiting Period			
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 26. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 27. ALC Recovery GAIN Step

IREF7-0bits	GAIN(0dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 28. Reference Level at ALC Recovery operation for recoding

OREF5-0bits	GAIN(0dB)	Step	
3CH	+36.0	1.5dB	(default)
3BH	+34.5		
3AH	+33.0		
:	:		
28H	+6.0		
:	:		
25H	+1.5		
24H	0.0		
23H	-1.5		
:	:		
2H	-51.0		
1H	-52.5		
0H	-54.0		

Table 29. Reference Level at ALC Recovery operation for playback

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	Quad Speed	(default)
0	1	8times	
1	0	16times	
1	1	N/A	

Table 30. First Recovery Speed Setting

3. The Volume at the ALC Operation

The current volume value at the ALC operation is reflected by VOL7-0 bits. It is enable to check the current volume value with reading the register value of VOL7-0 bits.

VOL7-0bits	GAIN(0dB)
F1H	+36.0
F0H	+35.625
EFH	+35.25
:	:
C5H	+19.5
:	:
92H	+0.375
91H	0.0
90H	-0.375
:	:
2H	-53.625
1H	-54.0
0H	MUTE

Table 31. Value of VOL7-0 bits

4. Example of ALC Operation

Table 32 and Table 33 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same data as ZTM1-0 bits	001	32ms	100	46.4ms
IREF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC1	ALC enable	1	Enable	1	Enable

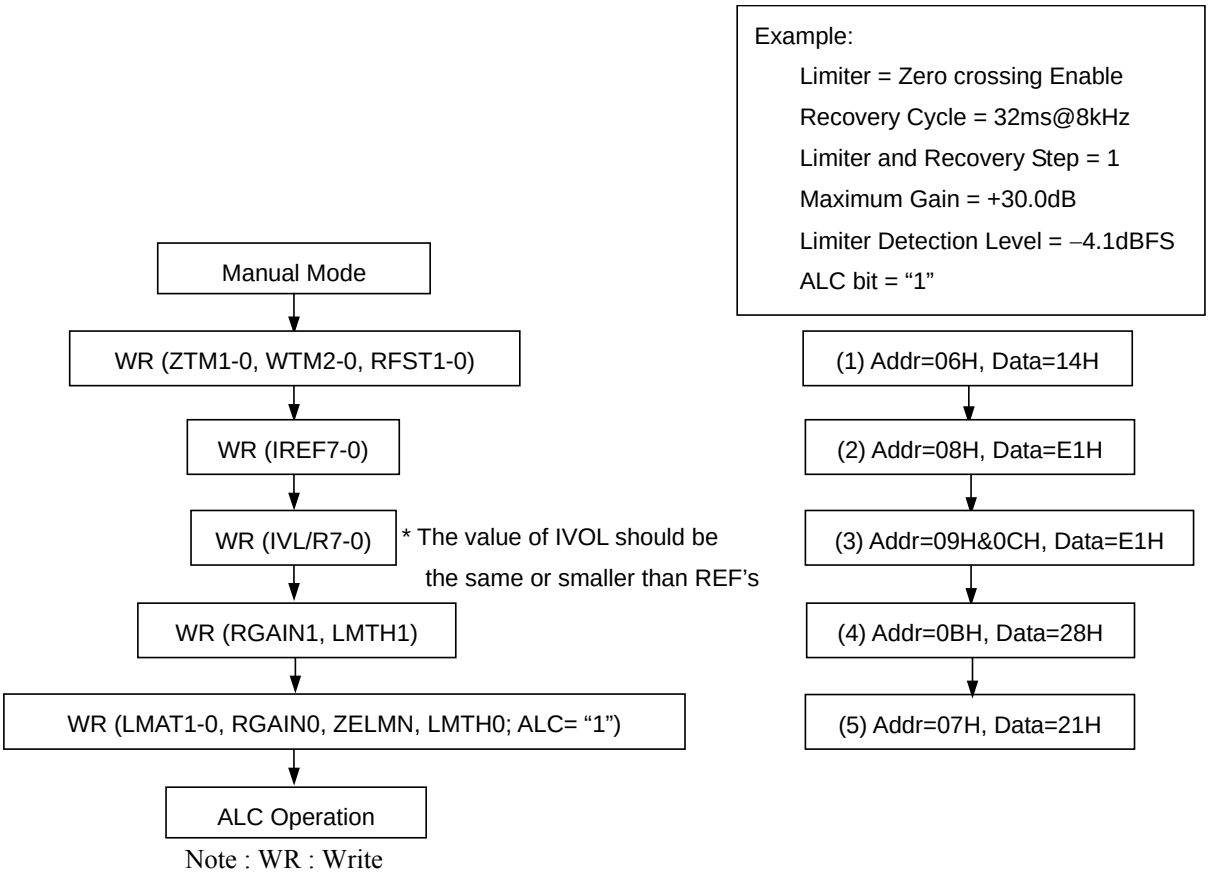
Table 32. Example of the ALC setting (Recording)

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same data as ZTM1-0 bits	001	32ms	100	46.4ms
OREF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
OVL7-0, OVR7-0	Gain of VOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC2	ALC enable	1	Enable	1	Enable

Table 33. Example of the ALC Setting (Playback)

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0" or PMADL=PMADR bits = "0".

- **LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0, LFST**



Note : WR : Write

Figure 29. Registers set-up sequence at ALC operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode at ALC1 bit = "0" when either Lch and Rch of ADC is powered-up (PMADL bit = "1" or PMADR bit = "1") and DAFIL bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 34). The IVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = "0", IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to "1".

If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = "0", IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to "1".

IVL7-0 IVR7-0	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		(default)
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 34. Input Digital Volume Setting

■ Output Digital Volume (Manual Mode)

The ALC block becomes output digital volume (manual mode) by setting ALC2 bit to "0" when both Lch and Rch of ADC are powered-down (PMADL = PMADR bits = "1") or DAFIL bit is "1". The output digital volume gain is set by the OVL7-0 bit and the OVR7-0 bit (Table 35). When the OVOLC bit = "1", the OVL7-0 bits control both Lch and Rch volume levels. When the OVOLC bit = "0", the OVL7-0 bits control Lch level and the OVR7-0 bits control Rch level. The OVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits.

OVL7-0 bits OVR7-0 bits	GAIN(0dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 35. Output Digital Volume Setting

When writing to the OVL7-0 bits and OVR7-0 bit continuously, the control register should be written by an interval more than zero crossing timeout. If not, the zero crossing counter is reset at each time and the volume will not be changed. However, it could be ignored when writing the same register value as the last time. In this case, zero crossing counter will not be reset, so that it could be written by an interval less than zero crossing timeout.

■ Output Digital Volume 2

AK4646 has 4 steps output volume in addition to the volume setting by DATT1-0 bits. Lch and Rch have the same volume values, which are set by DATT1-0 bits as shown in Table 36.

DATT1-0bits	GAIN(0dB)	Step	
0H	0.0	6.0dB	(default)
1H	-6.0		
2H	-12.0		
3H	-18.1		

Table 36. Output Digital Volume2 Setting

■ De-emphasis Filter

The AK4646 includes the digital de-emphasis filter (tc = 50/15μs) which corresponds 3 kinds frequency (32kHz, 44kHz, 48kHz) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 37).

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 37. De-emphasis Control

■ Soft Mute

Soft mute operation is performed in the digital input domain. When the SMUTE bit goes to "1", the input signal is attenuated by –∞ ("0") during the cycle of 256/fs (5.8msec@fs=44.1kHz). When the SMUTE bit is returned to "0", the mute is cancelled and the input attenuation gradually changes to 0dB during the cycle of 256/fs (5.8msec@fs=44.1kHz). If the soft mute is cancelled within the cycle of 256/fs (5.8msec@fs=44.1kHz), the attenuation is discontinued and returned to 0dB. The soft mute for Playback operation is effective for changing the signal source without stopping the signal transmission.

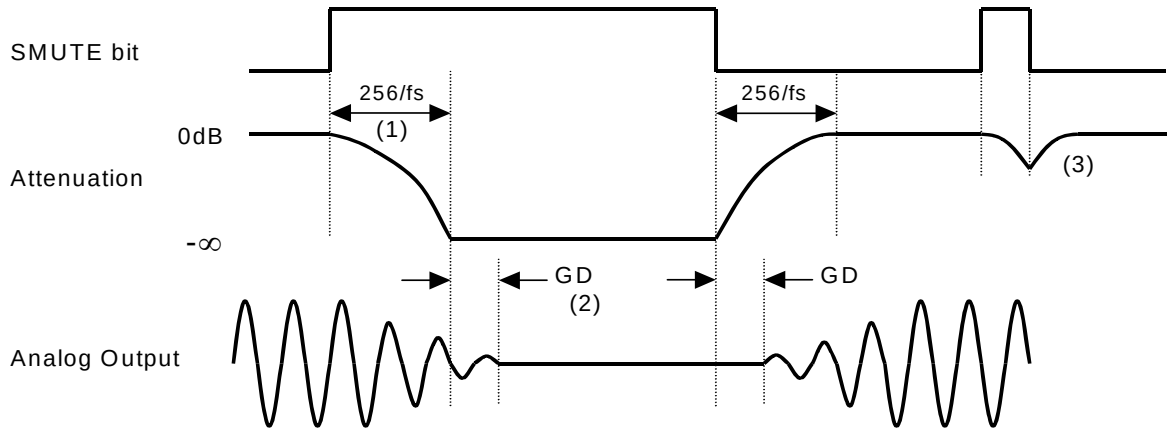


Figure 30. Soft Mute Function

(1) The input signal is attenuated by –∞ ("0") during the cycle of 256/fs (5.8msec@fs=44.1kHz).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle of 256/fs (5.8msec@fs=44.1kHz), the attenuation is discounted and returned to 0dB within the same cycle.

■ Analog Mixing: Mono Input

When the PMBP bit is set to "1", the mono input is powered-up. When the BEEPS bit is set to "1", the input signal from the MIN pin is output to Speaker-Amp. When the BEEPH bit is set to "1", the input signal from the MIN pin is output to Headphone-Amp. When the BEEPL bit is set to "1", the input signal from the MIN pin is output to the stereo line output amplifier. The external resister Ri adjusts the signal level of MIN input. Table 38, and Table 39 show the typical gain example at R_i = 20k Ω. This gain is in inverse proportion to R_i.

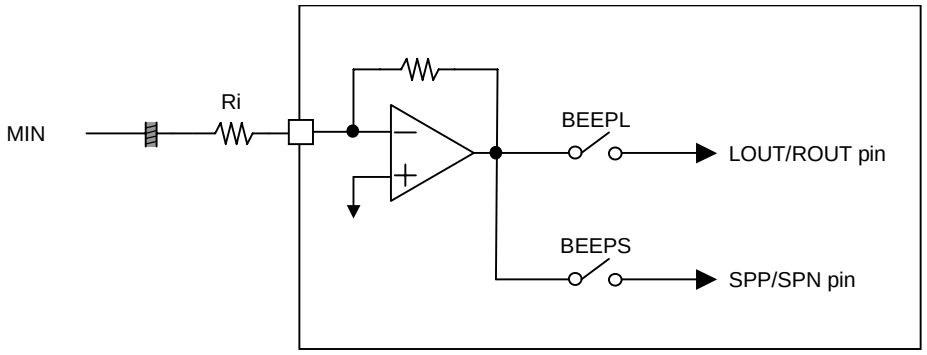


Figure 7. Block Diagram of MIN pin

LOVL1-0 bits	MIN → LOUT/ROUT	
00	0dB	(default)
01	+2dB	
10	+4dB	
11	+6dB	

Table 38. MIN Input → LOUT/ROUT Output Gain (typ) at R_i = 20kΩ

SPKG1-0 bits	MIN → SPP/SPN		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	+4.6dB	+6.6dB	(default)
01	+6.6dB	+8.6dB	
10	+8.6dB	+10.6dB	
11	+10.6dB	+12.6dB	

Table 39. MIN Input → Speaker-Amp Output Gain (typ) at R_i = 20kΩ

■ Stereo Line Output (LOUT/ROUT pins)

When DACL bit is "1", Lch/Rch signal of DAC is output from the LOUT/ROUT pins which is single-ended. When DACL bit is "0", output signal is muted and LOUT/ROUT pins output VCOM voltage. The load impedance is 10kΩ (min.). When the PMLO bit = LOPS bit = "0", the stereo line output enters power-down mode and the output is pulled-down to AVSS by 100kΩ(typ). When the LOPS bit is "1", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit at LOPS bit = "1". In this case, output signal line should be pulled-down to AVSS by 20kΩ after AC coupled as Figure 32. Rise/Fall time is 300ms (max) at C=1μF. When PMLO bit = "1" and LOPS bit = "0", stereo line output is in normal operation.

LOVL bit set the gain of stereo line output.

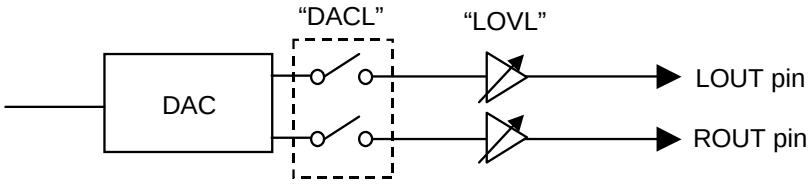


Figure 31. Stereo Line Output

LOPS	PMLO	Mode	LOUT/ROUT pin	
0	0	Power-down	Pull-down to AVSS	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to AVSS	
	1	Power-save	Rise up to VCOM	

Table 40. Stereo Line Output Mode Select (x: Don't care)

LOVL1-0 bits	Gain	
00	0dB	(default)
01	+2dB	
10	+4dB	
11	+6dB	

Table 41. Stereo Line Output Volume Setting

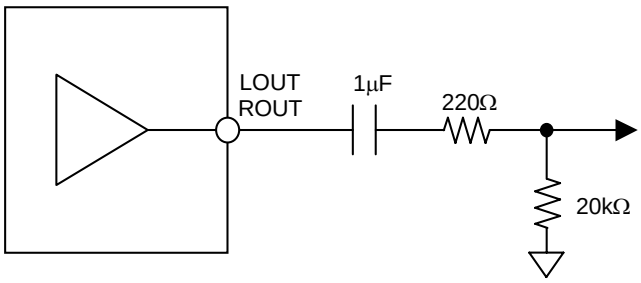


Figure 32. External Circuit for Stereo Line Output (in case of using Pop Reduction Circuit)

[Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)]

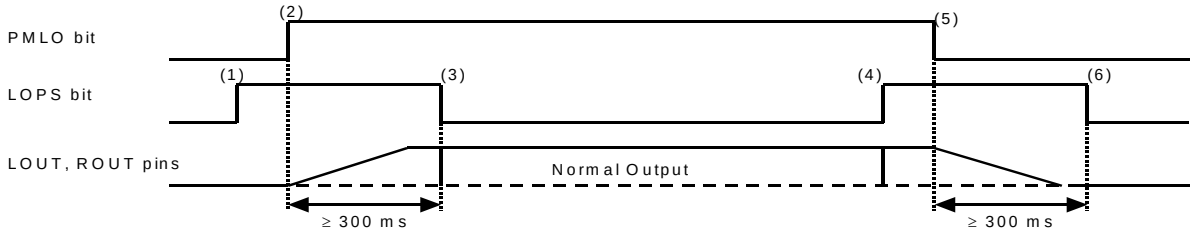


Figure 33. Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)

(1) Set LOPS bit = "1". Stereo line output enters the power-save mode.
(2) Set PMLO bit = "1". Stereo line output exits the power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF.
(3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to AVSS. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits the power-save mode.

■ Speaker Output

Power supply for Speaker-Amp (SVDD) is 2.2V to 4.0V. In case of dynamic (electromagnetic) speaker (load resistance < 50Ω), SVDD is 2.2V to 3.6V.

Speaker Type	Dynamic Speaker	Piezo (Ceramic) Speaker
Load Resistance (min)	8Ω	50Ω (Note 18)
Load Capacitance (max)	30pF	3μF (Note 18)

Note 18. Load impedance is total impedance of series resistance and piezo speaker impedance at 1kHz in 36HFigure 34. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Table 42. Speaker Type and Power Supply Range

The DAC output signal is input to the Speaker-amp as [(L+R)/2]. The Speaker-amp is mono and BTL output. The gain is set by SPKG1-0 bits. Output level depends on AVDD voltage and SPKG1-0 bits.

SPKG1-0 bits	Gain		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	+4.6dB	+6.6dB	(default)
01	+6.6dB	+8.6dB	
10	+8.6dB	+10.6dB	
11	+10.6dB	+12.6dB	

Table 43. SPK-Amp Gain

SPKG1-0 bits	SPK-Amp Output (DAC Input = 0dBFS)	
	ALC2 bit = "0"	ALC2 bit = "1" (LMTH1-0 bits = "00")
00	3.37Vpp	3.17Vpp
01	4.23Vpp (Note 38)	4.00Vpp
10	5.33Vpp (Note 38)	5.04Vpp (Note 38)
11	6.71Vpp (Note 38)	6.33Vpp (Note 38)

Note 38. The output level is calculated by assuming that output signal is not clipped. In actual case, output signal may be clipped when DAC outputs 0dBFS signal. DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is 4.0Vpp or less and output signal is not clipped.

Table 44. SPK-Amp Output Level

<Caution for using Piezo Speaker>

When a piezo speaker is used, resistances more than 10Ω should be inserted between SPP/SPN pins and speaker in series, respectively, as shown in Figure 34. Zener diodes should be inserted between speaker and GND as shown in Figure 34, in order to protect SPK-Amp of AK4646 from the power that the piezo speaker outputs when the speaker is pressured. Zener diodes of the following zener voltage should be used.

0.92 x SVDD ≤ Zener voltage of zener diodo (ZD in Figure 34) ≤ SVDD+0.3V
Ex) In case of SVDD = 3.8V: 3.5V ≤ ZD ≤ 4.1V
For example, zener diode which zener voltage is 3.9V (Min: 3.7V, Max: 4.1V) can be used.

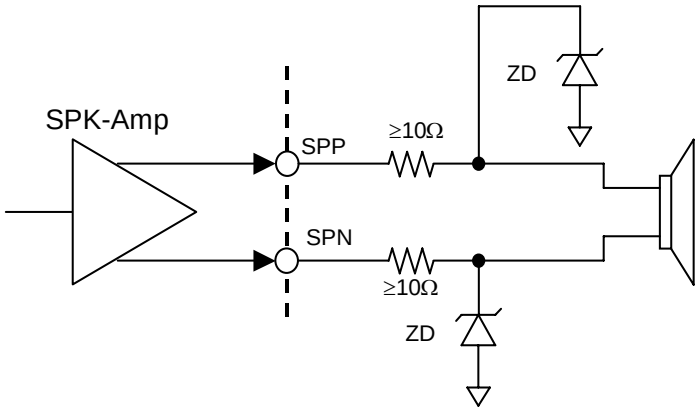


Figure 34. Speaker Output Circuit (In case of using piezo spearker)

<Speaker-Amp Control Sequence>

Speaker-Amp is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pins are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the Speaker-Amp enters power-save mode. In this mode, SPP pin is placed in Hi-Z state and SPN pin goes to SVDD/2 voltage.

When the PMSPK bit is "1" after PDN pin is controlled from "L" to "H", the SPP and SPN pins rise up from power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. Because the SPP and SPN pins rise up at power-save-mode, this mode can reduce pop noise. When the AK4646 is powered-down, pop noise can be also reduced by first entering power-save-mode.

PMSPK	SPPSN	Mode	SPP	SPN	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	0	Power-save	Hi-Z	SVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 45. Speaker-Amp Mode Setting (x: Don't care)

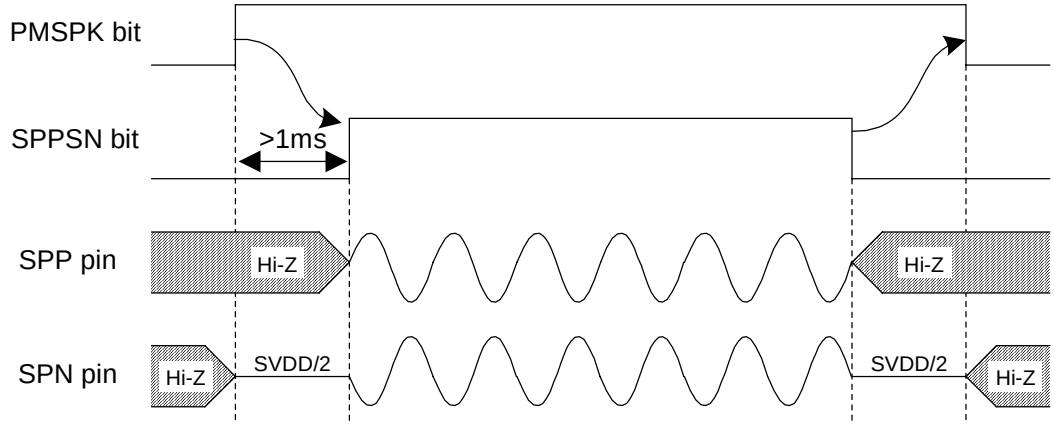
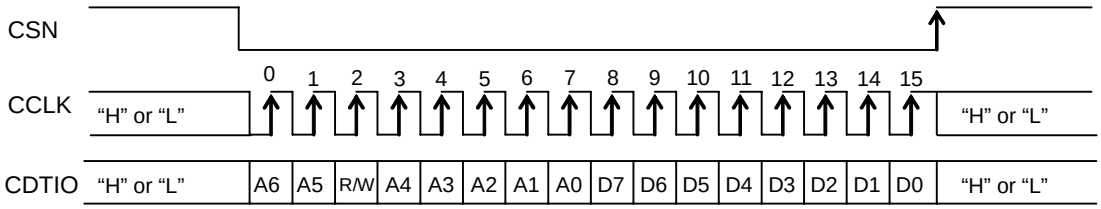


Figure 35. Power-up/Power-down Timing for Speaker-Amp

■ Serial Control Interface

Internal registers may be written by using the 3-wire μP interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. It is available for writing data on the rising edge of CSN. When reading operation, CDTIO pin has become an output mode at the falling edge of 8th CCLIC and outputs D7-D0. The output finishes on the rising edge of CSN. The CDTIO is placed in a Hi-Z state except outputting data at read operation mode. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by PDN pin = "L".

Note 38. It is available for reading the address 00H~11H. When reading the address 12H ~ 7FH, the register values are invalid.



R/W: READ/WRITE ("1": WRITE, "0": READ)
A6-A0: Register Address
D7-D0: Control data (Input) at Write Command
Output data (Output) at Read Command

Figure 36. Serial Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMBP	PMSPK	PMLO	PMDAC	0	PMADL
01H	Power Management 2	0	0	0	0	M/S	0	MCKO	PMPLL
02H	Signal Select 1	SPPSN	BEEPS	DACS	DACL	0	PMMP	MGAIN2	MGAIN0
03H	Signal Select 2	DAFIL	LOPS	MGAIN1	SPKG1	SPKG0	BEEPL	LOVL1	LOVL0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
05H	Mode Control 2	PS1	PS0	FS3	0	0	FS2	FS1	FS0
06H	Timer Select	0	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
07H	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
08H	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
09H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0AH	Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
0CH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
0DH	ALC LEVEL	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0EH	Mode Control 3	READ	LOOP	SMUTE	OVOLC	DATT1	DATT0	DEM1	DEM0
0FH	Mode Control 4	0	0	0	0	IVOLC	0	0	0
10H	Power Management 3	0	0	0	MDIF2	MDIF1	INR	INL	PMADR
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ0	FIL3	0	HPFAD
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ0-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
17H	EQ0-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
18H	EQ0-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
19H	EQ0-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
1AH	EQ0-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
1BH	EQ0-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
20H	Reserved	0	0	0	0	0	0	0	0
21H	Reserved	0	0	0	0	0	0	0	0
22H	Reserved	0	0	0	0	0	0	0	0
23H	Reserved	0	0	0	0	0	0	0	0
24H	Reserved	0	0	0	0	0	0	0	0
25H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
26H	Reserved	0	0	0	0	0	0	0	0
27H	Reserved	0	0	0	0	0	0	0	0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Reserved	0	0	0	0	0	0	0	0
2BH	Reserved	0	0	0	0	0	0	0	0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 39. PDN pin = “L” resets the registers to their default values.
Note 40. Unused bits must contain a “0” value.
Note 41. Reading of address 26H ~ 2FH, 12H ~ 24H and 32H ~ 7FH are not possible.
Note 42. Address 0DH is a read only register. Writing access to 0DH does not effect the operation.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	PMVCM	PMBP	PMSPK	PMLO	PMDAC	0	PMADL
R/W		R	R/W	R/W	R/W	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	0

PMADL: MIC-Amp Lch and ADC Lch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

PMLO: Stereo Line Out Power Management
0: Power-down (default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMBP: MIN Input Power Management
0: Power-down (default)
1: Power-up
Both PMDAC and PMBP bits should be set to "1" when DAC is powered-up for playback. After that, BEEPL or BEEPS bit is used to control each path when MIN input is used.

PMVCM: VCOM Power Management
0: Power-down (default)
1: Power-up
When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when all power management bits of 00H, 01H,02H, 10H and MCKO bits are "0".

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When all power management bits are "0" in the 00H, 01H, 02H and 10H addresses and MCKO bit is "0", all blocks are powered-down. The register values remain unchanged.

When neither ADC nor DAC are used, external clocks may not be present. When ADC or DAC is used, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	M/S	0	MCKO	PMPLL
R/W		R	R	R	R	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power-Down (default)
1: PLL Mode and Power-up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPPSN	BEEPS	DACS	DACL	0	PMMP	MGAIN2	MGAIN0
R/W		R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

MGAIN2-0: MIC-Amp Gain Control (Table 19)
MGAIN1 bit is D5 bit of 03H.

PMMP: MPWR pin Power Management
0: Power-down: Hi-Z (default)
1: Power-up

DACL: Switch Control from DAC to Stereo Line Output
0: OFF (default)
1: ON
When PMLO bit is "1", DACL bit is enabled. When PMLO bit is "0", the LOUT/ROUT pins go to AVSS.

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPS: Switch Control from MIN pin to Speaker-Amp
0: OFF (default)
1: ON
When BEEPS bit is "1", mono signal is input to Speaker-Amp.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is on power-save mode. In this mode, SPP pin goes to Hi-Z and SPN pin is outputs SVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "L", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	DAFIL	LOPS	MGAIN1	SPKG1	SPKG0	BEEPL	LOVL1	LOVL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LOVL1-0: Output Stereo Line Gain Select (Table 41)
Default: 00(0dB)

BEEPL: Switch Control from MIN pin to Stereo Line Output
0: OFF (default)
1: ON
When PMLO bit is "1", BEEPL bit is enabled. When PMLO bit is "0", the LOUT/ROUT pins go to AVSS.

SPKG1-0: Speaker-Amp Output Gain Select (Table 43)

MGAIN1: MIC-Amp Gain Control (Table 19)

LOPS: Stereo Line Output Power-Save Mode
0: Normal Operation (default)
1: Power-Save Mode

DAFIL: Filter/ALC Path Select When PMADL bit = "1" or PMADR bit = "1"
0: ADC/Recording Path (default)
1: DAC/Playback Path
The SDTO pin outputs "L" with regardless of PMADL and PMADR bits when DAFIL bit = "1" and PMDAC bit = "1".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 16)
Default: "10" (Left justified)

BCKO: BICK Output Frequency Select at Master Mode (Table 10)

PLL3-0: PLL Reference Clock Select (Table 4)
Default: "0000" (LRCK pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 2	PS1	PS0	FS3	0	0	FS2	FS1	FS0
R/W		R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Select (Table 5 and Table 6.) and MCKI Frequency Select (Table 11.)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

PS1-0: MCKO Output Frequency Select (Table 9)
Default: "00" (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Timer Select	0	WTM2	ZTM1	ZTM0	WTM1	WTM0	RFST1	RFST0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

WTM2-0: ALC Recovery Waiting Period (Table 26.)

A period of recovery operation when any limiter operation does not occur during the ALC1 operation Default is "000" (128/fs).

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 25.)

When the IPGA perform zero crossing or timeout, the IPGA value is changed by the μP WRITE operation, ALC1 recovery operation. Default is "00" (128/fs).

RFST1-0: ALC First recovery Speed(Table 30)

Default: "00" (4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	RGAIN0	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 23.)

Default: "00"

LMTH1 bit is D6 bit of 0BH.

RGAIN1-0: ALC Recovery GAIN Step (Table 27.)

Default: "00"

RGAIN1 bit is D7 bit of 0BH.

LMAT1-0: ALC Limiter ATT Step (Table 24.)

Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation

0: Enable (default)

1: Disable

ALC1: ALC Enable for Recording

0: Recording ALC Disable (default)

1: Recording ALC Enable

ALC2: ALC Enable for Playback

0: Playback ALC Disable (default)

1: Playback ALC Enable

LFST: Limiter function of ALC when the output was bigger than Fs.

0: Output is zero crossing or being changed value of volume at the time of the output is zero crossing time out.

1: When output of ALC is bigger than FS, VOL value is changed instantly.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 28.)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0CH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 34.)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Lch Digital Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
25H	Rch Digital Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

OVL7-0, OVR7-0: Output Digital Volume (Table 35)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 3	RGAIN1	LMTH1	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	0

OREF5-0: Reference value at Playback ALC Recovery Operation. 0.375dB step, 50 Level (Table 29)
Default: "28H" (+6.0dB)

LMTH1: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 23.)

RGAIN1: ALC Recovery GAIN Step (Table 27.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		-	-	-	-	-	-	-	-

VOL7-0: Current ALC volume value; 0.375dB step, 242 Level. Read operation only (Table 31)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Mode Control 3	READ	LOOP	SMUTE	OVOLC	DATT1	DATT0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

DEM1-0: De-emphasis Frequency Select (Table 37)
Default: "01" (OFF)

DATT1-0: Output Digital Volume2; 6dB step, 4 Level (Table 36)
Default: "00H" (0.0dB)

OVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume level, while register values of OVL7-0 bits are not written to OVR7-0 bits. When OVOLC bit = "0", OVL7-0 bits control Lch level and OVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

LOOP: Digital Loopback Mode
0: SDTI → DAC (default)
1: SDTO → DAC

READ: Read function Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Mode Control 4	0	0	0	0	IVOLC	0	0	0
R/W		R	R	R	R	R/W	R	R	R
Default		0	0	0	0	1	0	0	0

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management 3	0	0	0	MDIF2	MDIF1	INR	INL	PMADR
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADR: MIC-Amp Lch and ADC Rch Power Management
0: Power-down (default)
1: Power-up

INL: ADC Lch Input Source Select
0: LIN1 pin (default)
1: LIN2 pin

INR: ADC Rch Input Source Select
0: RIN1 pin (default)
1: RIN2 pin

MDIF1: ADC Lch Input Type Select
0: Single-ended input (LIN1/LIN2 pin: Default)
1: Full-differential input (IN1+/IN1– pin)

MDIF2: ADC Rch Input Type Select
0: Single-ended input (RIN1/RIN2 pin: Default)
1: Full-differential input (IN2+/IN2– pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Digital Filter Select 1	GN1	GN0	LPF	HPF	EQ0	FIL3	0	HPFAD
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF Control of ADC
0: Disable
1: Enable (default)
When HPFAD bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPFAD bit is “0”, HPFAD block is through (0dB).

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3 bit is “1”, the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit is “0”, FIL3 block is OFF (MUTE).

EQ: EQ (Gain Compensation Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ bit is “1”, the settings of EQA15-0, EQB13-0 and EQC15-0 bits are enabled. When EQ bit is “0”, EQ block is through (0dB).

HPF: HPF Coefficient Setting Enable
0: Disable (default)
1: Enable
When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, HPF block is through (0dB).

LPF: LPF Coefficient Setting Enable
0: Disable (default)
1: Enable
When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, LPF block is through (0dB).

GN1-0: Gain Select at GAIN block (Table 22)
Default: “00”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
13H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
14H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
15H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
16H	EQ0-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
17H	EQ0-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
18H	EQ0-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
19H	EQ0-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
1AH	EQ0-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
1BH	EQ0-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: "0000H"

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select
0: HPF (default)
1: LPF

EQA15-0, EQB13-0, EQC15-C0: EQ (Gain Compensation Filter) Coefficient (16bit x 2 + 14bit x 1)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	HPF Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1DH	HPF Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1EH	HPF Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1FH	HPF Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		W	W	W	W	W	W	W	W
Default		F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD							

F1A13-0, F1B13-0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD
fc = 150Hz@fs=44.1kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2CH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
2DH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
2EH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
2FH	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: FIL2 (LPF) Coefficient (14bit x 2)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is "0", EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is "0", EQ4 block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is "1", the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is "0", EQ5 block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		W	W	W	W	W	W	W	W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

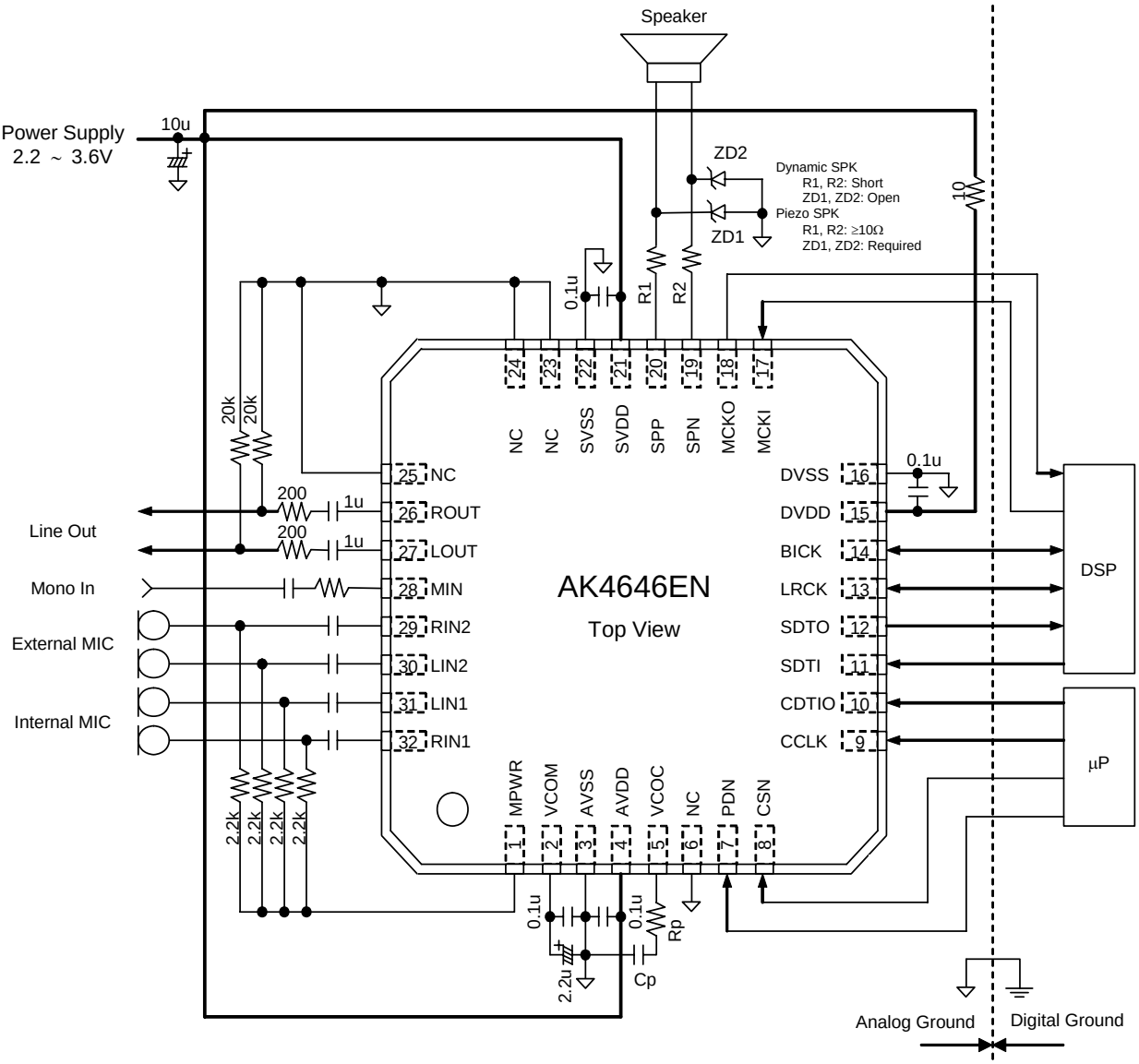
E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

SYSTEM DESIGN

Figure 37 shows the system connection diagram for the AK4646. An evaluation board [AKD4646] is available which demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- AVSS, DVSS and SVSS of the AK4646 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4646 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK4646 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 4.
- When piezo speaker is used, 2.2 ~ 4.0V power should be supplied to SVDD and 10Ω or more series resistors should be connected to both SPP and SPN pins, respectively.
- When the AK4646 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, around 100kΩ pull-up resistor should be connected to LRCK and BICK pins of the AK4646.

Figure 37. System Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4646 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and SVDD are usually supplied from the system's analog supply. If AVDD, DVDD and SVDD are supplied separately, the power-up sequence is not critical. AVSS, DVSS and SVSS of the AK4646 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4646 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor should be attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4646.

3. Analog Inputs

The Mic, Line and MIN inputs are single-ended. The inputs signal range scales with nominally at 0.0636 x AVDD Vpp (typ) for the Mic input and 0.636 x AVDD Vpp (typ) for the MIN input, centered around the internal common voltage (0.5 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$. The AK4646 can accept input voltages from AVSS to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH (@16bit) and a negative full scale for 8000H (@16bit). The ideal output is VCOM voltage for 0000H (@16bit). Stereo Line Output is centered at 0.5 x AVDD (typ). The Headphone-Amp and Speaker-Amp outputs are centered at SVDD/2.

CONTROL SEQUENCE

■ Clock Set up

When ADC or DAC is powered-up, the clocks must be supplied.

1. PLL Master Mode.

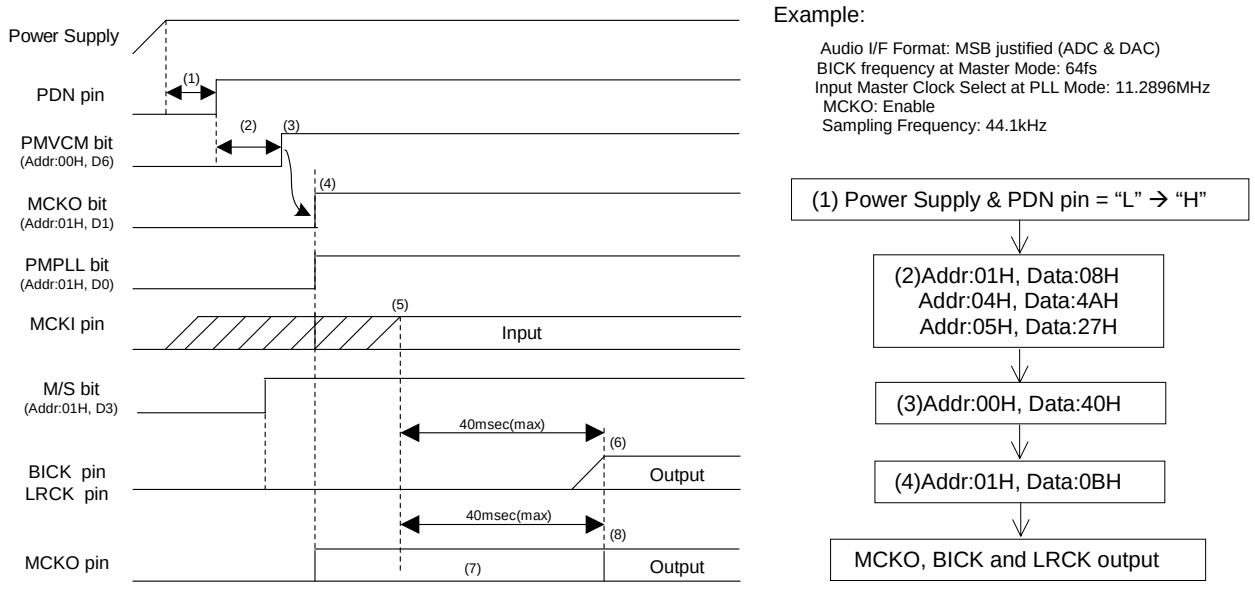


Figure 38. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin = "L" → "H"
"L" time of 150ns or more is needed to reset the AK4646.

(2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL lock time is 40ms (max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.

(6) The AK4646 starts to output the LRCK and BICK clocks after the PLL becomes stable. Then normal operation starts.

(7) The invalid frequency is output from MCKO pin during this period if MCKO bit = "1".

(8) The normal clock is output from MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (LRCK or BICK pin)

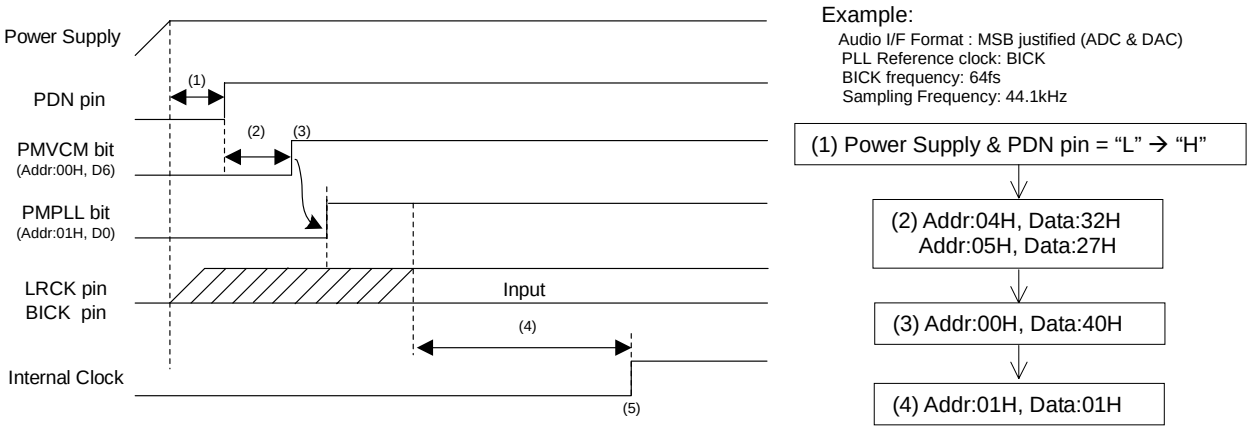


Figure 39. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4646.

(2) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BICK pin) is supplied. PLL lock time is 160ms (max) when LRCK is a PLL reference clock. And PLL lock time is 2ms (max) when BICK is a PLL reference clock.

(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

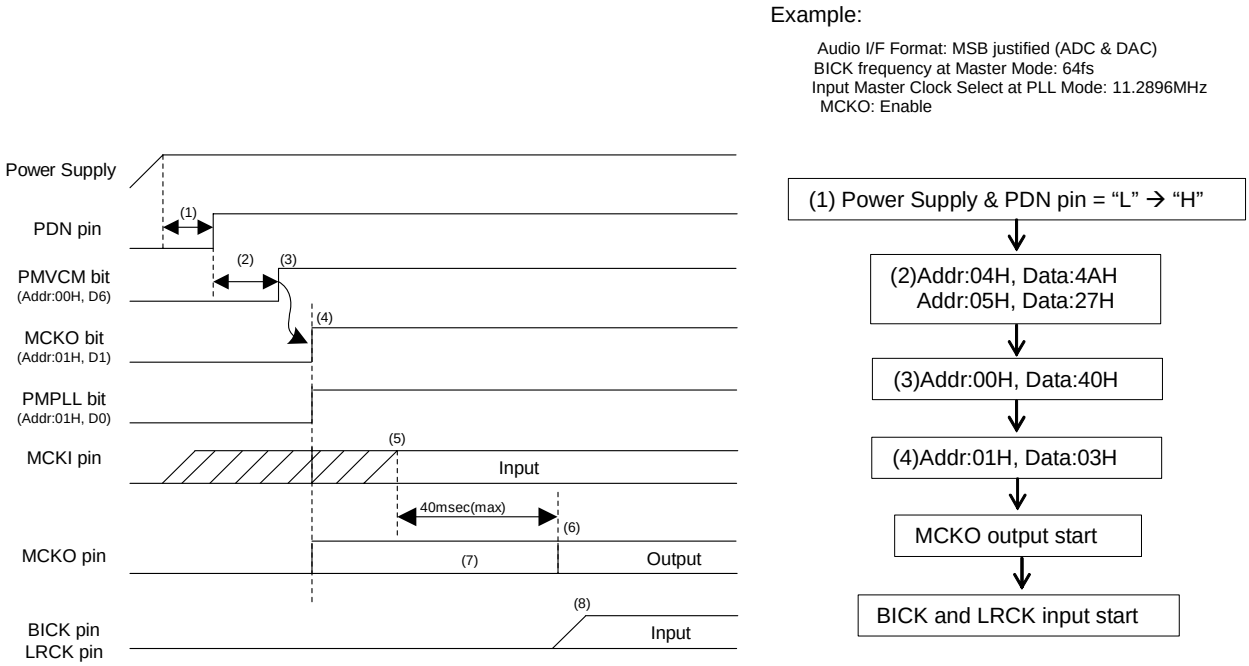


Figure 40. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4646.
(2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 40ms (max).
(6) The normal clock is output from MCKO after PLL is locked.
(7) The invalid frequency is output from MCKO during this period.
(8) BICK and LRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

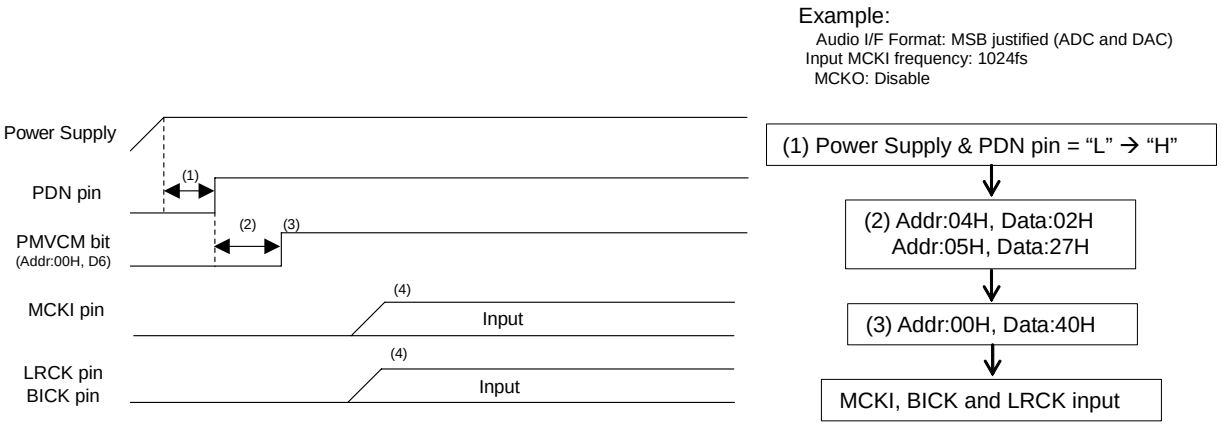


Figure 41. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4646.

(2) DIF1-0 and FS1-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

■ MIC Input Recording (Stereo)

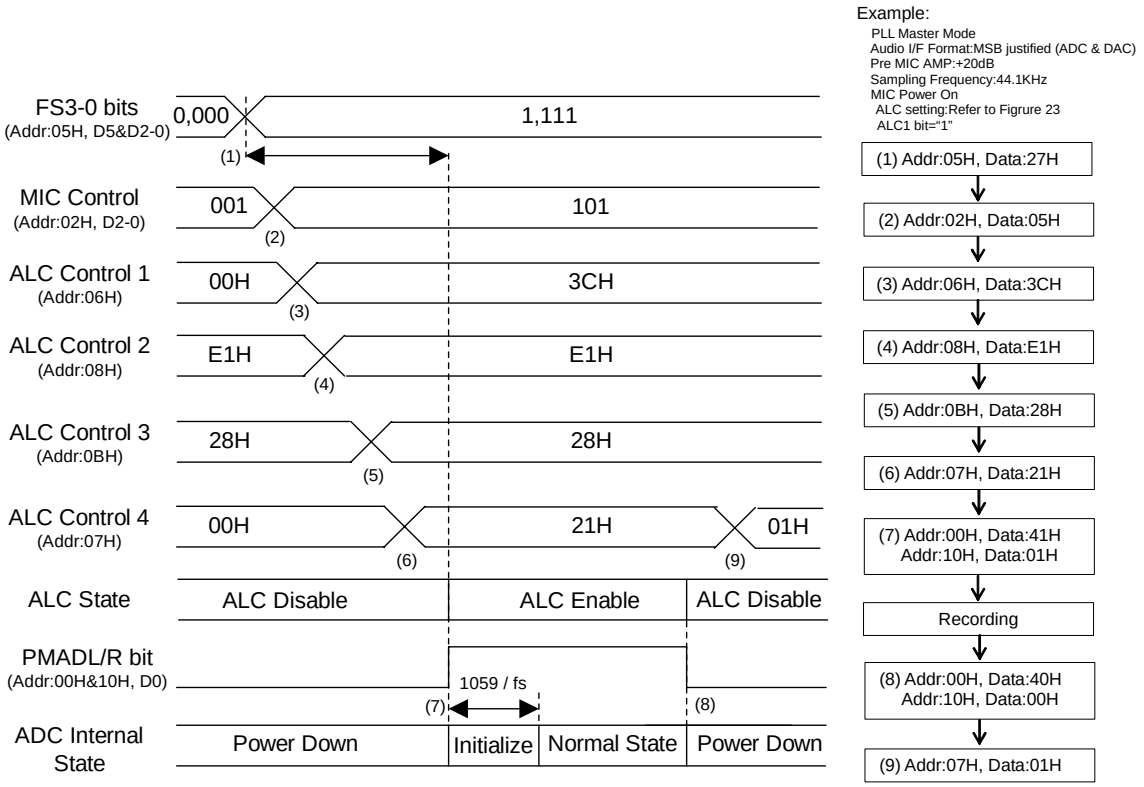


Figure 42. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Figure 29. Registers set-up sequence at ALC operation"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK4646 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up MIC input (Addr: 02H)

(3) Set up Timer Select for ALC (Addr: 06H)

(4) Set up IREF value for ALC (Addr: 08H)

(5) Set up LMTH1 and RGAIN1 bits (Addr: 0BH)

(6) Set up LMTH0, RGAIN0, LMAT1-0 and ALC bits (Addr: 07H)

(7) Power Up MIC and ADC: PMADL = PMADR bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=24ms@fs=44.1kHz.
After the ALC bit is set to "1" and MIC&ADC block is powered-up, the ALC operation starts from IVOL default value (+30dB).
The time of offset voltage going to "0" after the ADC initialization cycle depends on both the time of analog input pin going to the common voltage and the constant time of the offset cancel digital HPF. This time can be shorter by using the following sequence:
At first, PMVCM and PMMP bits should set to "1". Then, the ADC should be powered-up. The waiting time to power-up the ADC should be longer than 4 times of the time constant that is determined by the AC coupling capacitor at analog input pin and the internal input resistance 30k(typ).

(8) Power Down MIC and ADC: PMADL = PMADR bits = "1" → "0"
When the registers for the ALC operation are not changed, ALC bit may be keeping "1". The ALC operation is disabled because the MIC&ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be done after the AK4646 goes to the manual mode (ALC bit = "0") or MIC&ADC block is powered-down (PMADL=PMADR bits = "0"). IVOL gain is not reset when PMADL=PMADR bits = "0", and then IVOL operation starts from the setting value when PMADC or PMADR bit is changed to "1".

(9) ALC Disable: ALC bit = "1" → "0"

■ Speaker-amp Output

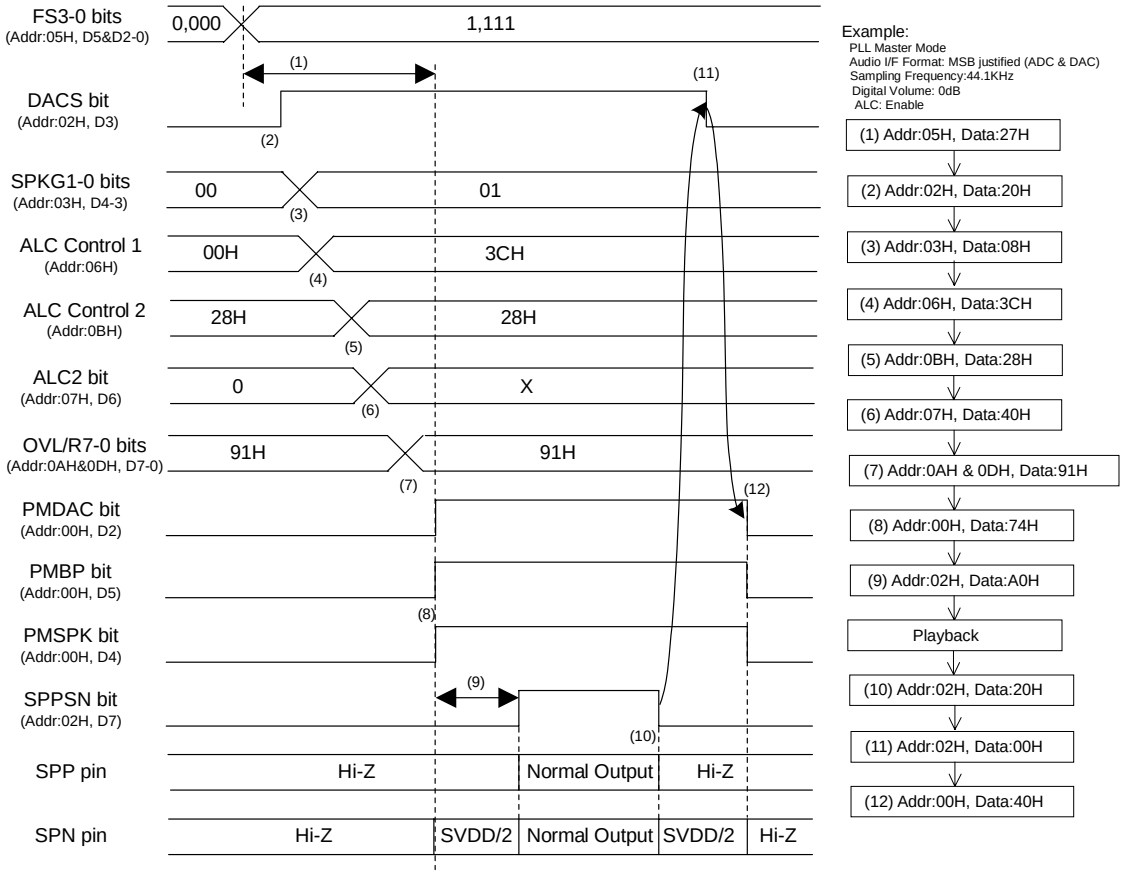


Figure 43. Speaker-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4646 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up the path of "DAC → SPK-Amp": DACS bit = "0" → "1"

(3) SPK-Amp gain setting: SPKG1-0 bits = "00" → "01"

(4) Set up Timer Select for ALC (Addr: 06H)

(5) Set up REF value for ALC (Addr: 0BH)

(6) Set up LMTH0, RGAIN0, LMAT1-0 and ALC2 bits (Addr: 07H)

(7) Set up the output digital volume (Addr: 0AH and 0DH).

When OVOLC bit is "1" (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition. ALC/OVOL are invalid to DAC when (PMADL bit = "1" or PMADR bit = "1") and DAFIL bit = "0".

(8) Power Up of DAC, MIN-Amp and Speaker-Amp: PMDAC = PMBP = PMSPK bits = "0" → "1"

The DAC outputs invalid voltage for 67/fs = 1.52ms@fs = 44.1kHz after powered-up, then it starts outputting normal voltage.

(9) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"

"(9)" time depends on the time constant of external resistor and capacitor connected to MIN pin. If Speaker-Amp output is enabled before input of MIN-Amp becomes stable, pop noise may occur.

e.g. R=20k, C=0.1μF: Recommended wait time is more than 5τ = 10ms.

(10) Enter the power-save-mode of Speaker-Amp: SPPSN bit = "1" → "0"

(11) Disable the path of "DAC → SPK-Amp": DACS bit = "1" → "0"

(12) Power Down DAC, MIN-Amp and Speaker-Amp: PMDAC = PMBP = PMSPK bits = "1" → "0"

■ Mono signal output from Speaker-Amp

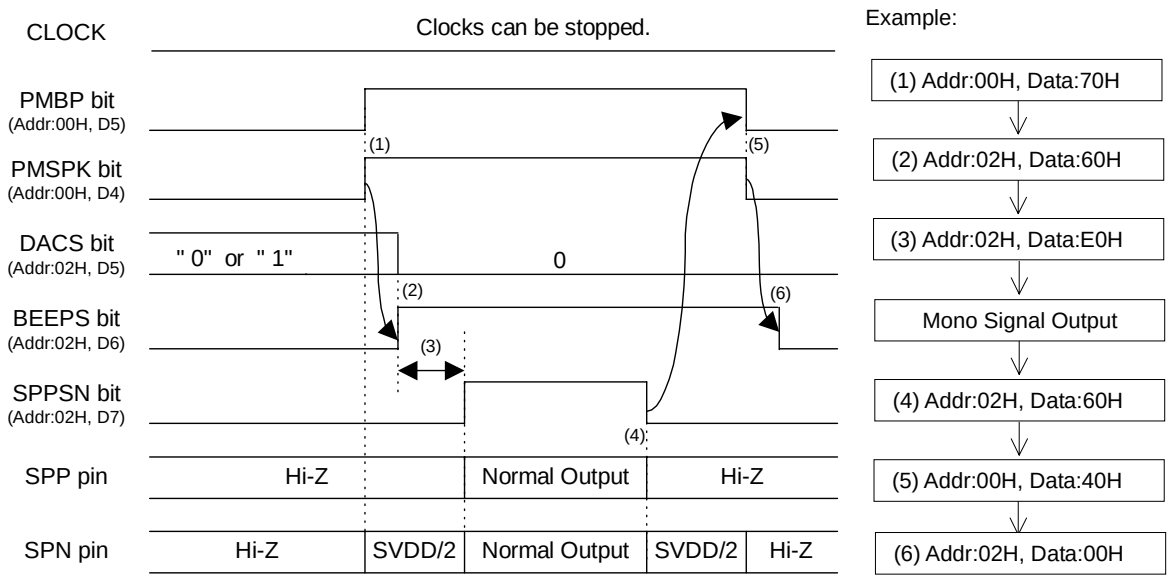


Figure 44. "MIN-Amp → Speaker-Amp" Output Sequence

<Example>

The clocks can be stopped when only MIN-Amp and Speaker-Amp are operating.

(1) Power Up MIN-Amp and Speaker-Amp: PMBP = PMSPK bits = "0" → "1"
(2) Disable the path of "DAC → SPK-Amp": DACS bit = "0"
Enable the path of "MIN → SPK-Amp": BEEPS bit = "0" → "1"
(3) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
"(3)" time depends on the time constant of external resistor and capacitor connected to MIN pin. If Speaker-Amp output is enabled before input of MIN-Amp becomes stable, pop noise may occur.
e.g. R=20k, C=0.1μF: Recommended wait time is more than 5τ = 10ms.
(4) Enter the power-save-mode of Speaker-Amp: SPPSN bit = "1" → "0"
(5) Power Down MIN-Amp and Speaker-Amp: PMBP = PMSPK bits = "1" → "0"
(6) Disable the path of "MIN → SPK-Amp": BEEPS bit = "1" → "0"

■ Stereo Line Output

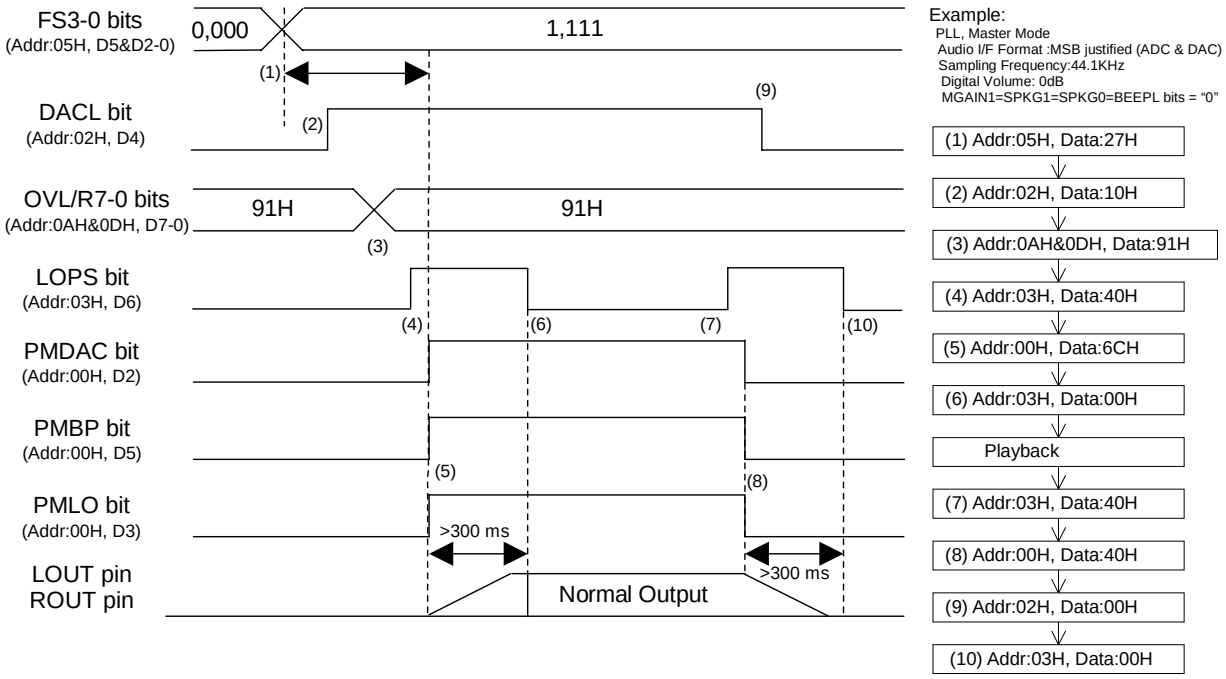


Figure 45. Stereo Lineout Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4646 is PLL mode, DAC and Stereo Line-Amp should be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up the path of "DAC → Stereo Line Amp": DACL bit = "0" → "1"
(3) Set up the output digital volume (Addr: 0AH and 0DH)
When OVOLC bit is "1" (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
(4) Enter power-save mode of Stereo Line Amp: LOPS bit = "0" → "1"
(5) Power-up DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMBP = PMLO bits = "0" → "1"
The DAC outputs invalid voltage for 67/fs = 1.52ms@fs = 44.1kHz after powered-up, then it starts outputting normal voltage. LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to "1". Rise time is 300ms (max) at C=1μF.
(6) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit should be set to "0" after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to "0".
(7) Enter power-save mode of Stereo Line-Amp: LOPS bit: "0" → "1"
(8) Power-down DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMBP = PMLO bits = "1" → "0"
LOUT and ROUT pins fall down to AVSS. Fall time is 300ms (max) at C=1μF.
(9) Disable the path of "DAC → Stereo Line-Amp": DACL bit = "1" → "0"
(10) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit should be set to "0" after LOUT and ROUT pins fall down.

■ Stop of Clock

Master clock can be stopped when ADC and DAC are not used.

1. PLL Master Mode

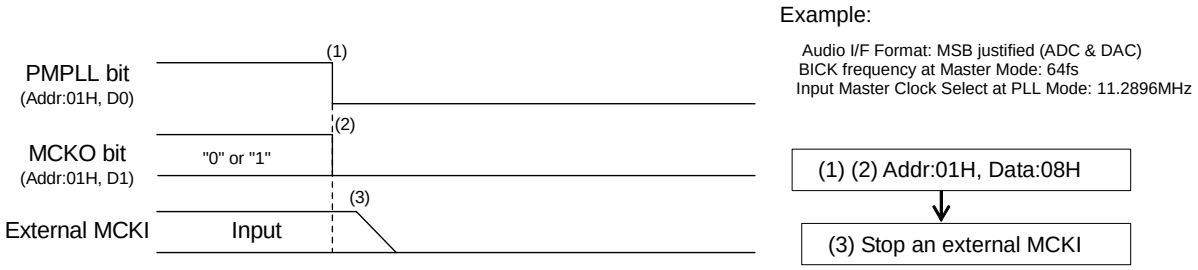


Figure 46. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (LRCK or BICK pin)

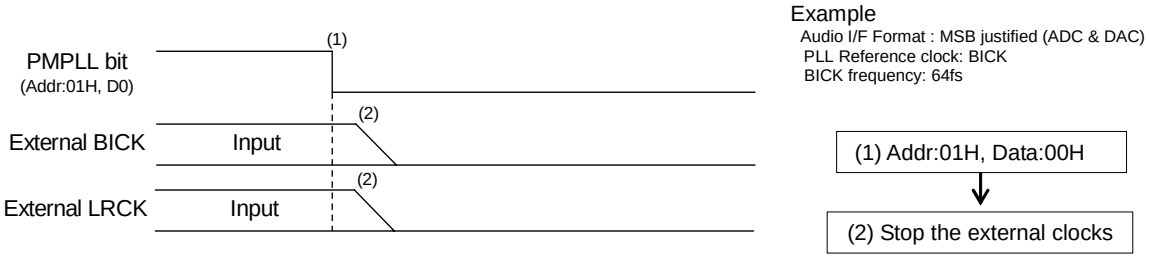


Figure 47. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and LRCK clocks

3. PLL Slave (MCKI pin)

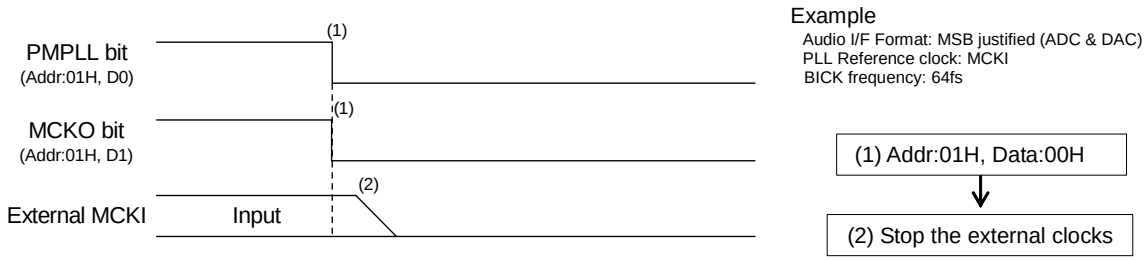


Figure 48. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. EXT Slave Mode

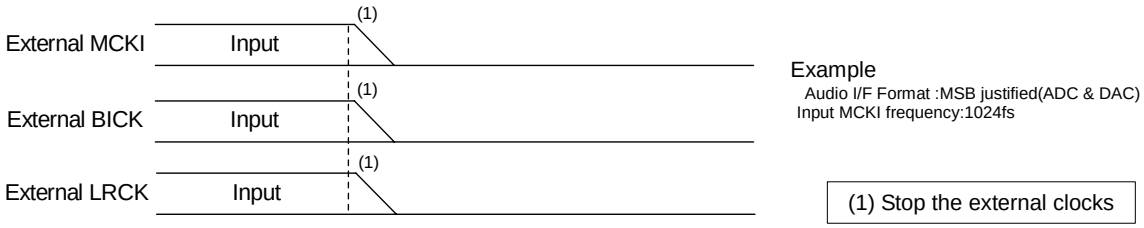


Figure 49. Clock Stopping Sequence (4)

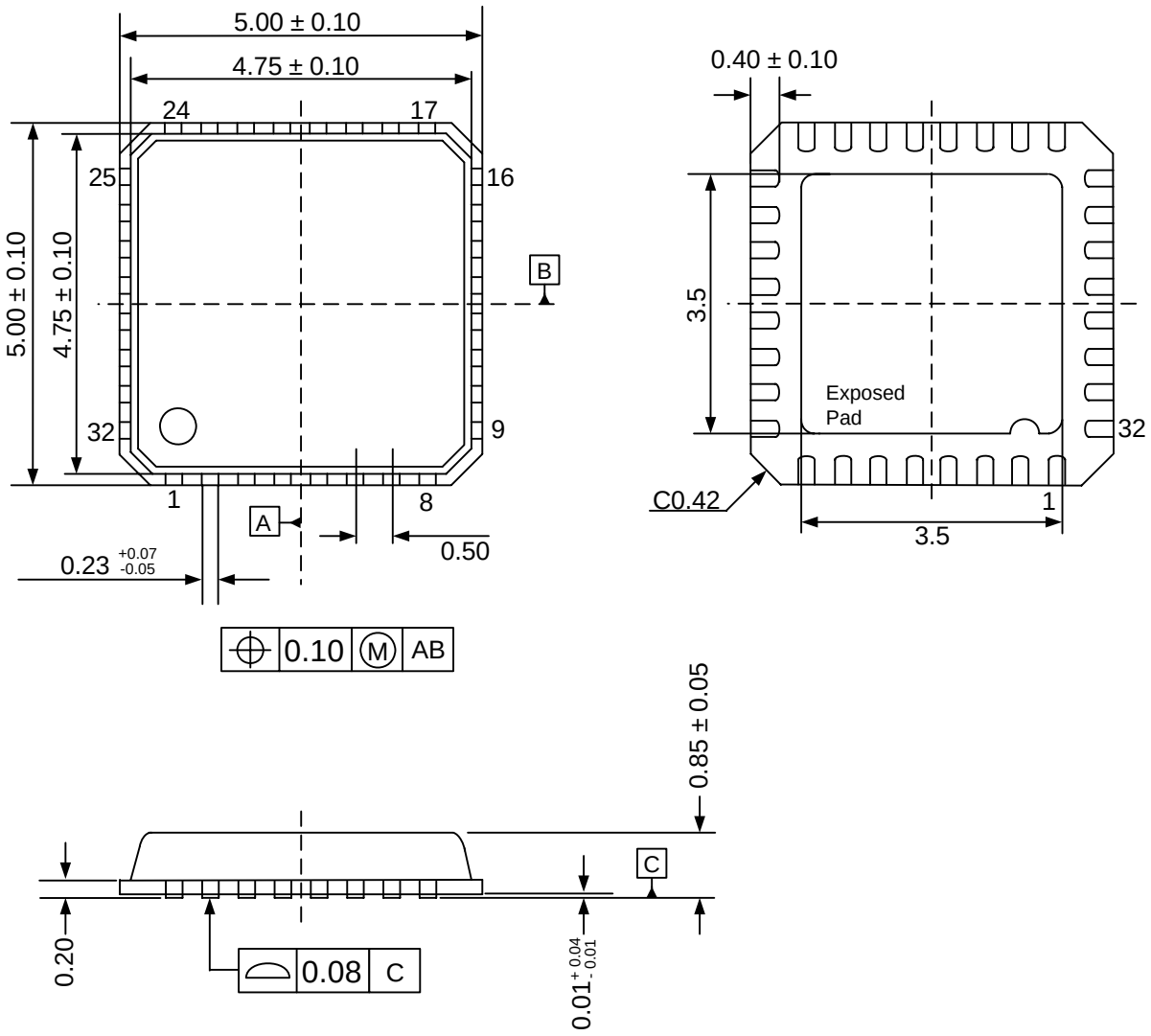
<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

■ Power down

Power supply current can be shut down (typ. 1μA) by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 1μA) by stopping clocks and setting PDN pin = "L". When PDN pin = "L", the registers are initialized.

PACKAGE

● 32pin QFN (Unit: mm)

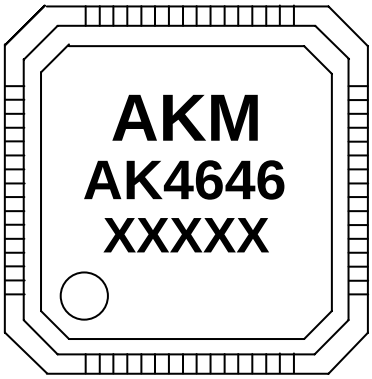


Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXX: Date code identifier (5 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/05/14	02	First Edition		

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei EMD Corporation (AKEMD) or authorized distributors as to current status of the products.
- AKEMD assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKEMD products are neither intended nor authorized for use as critical components$_{Note1)}$ in any safety, life support, or other hazard related device or system$_{Note2)}$, and AKEMD assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKEMD. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKEMD products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKEMD harmless from any and all claims arising from the use of said product in the absence of such notification.