SN74HC595-Q1 8-Bit Shift Registers With 3-State Output Registers

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classifcation Level C5
- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Low Power Consumption: 80-μA (Maximum) I_{CC}
- t_{pd} = 13 ns (Typical)
- ±6-mA Output Drive at 5 V
- Low Input Current: 1 μA (Maximum)
- Shift Register Has Direct Clear

2 Applications

- Output expansion
- LED matrix control
- 7-segment display control
- 8-bit data storage

3 Description

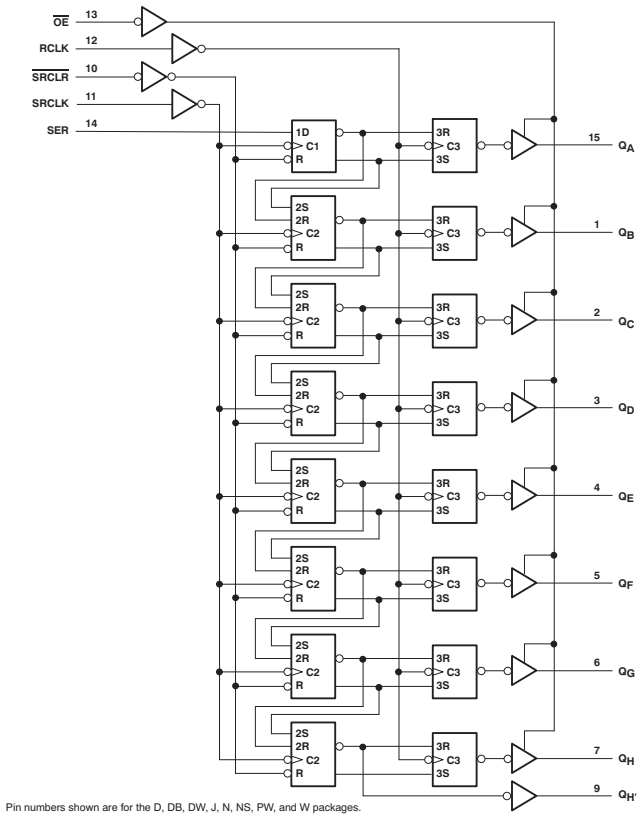
The SN74HC595-Q1 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC595QPWRQ1	TSSOP (16)	5.00 mm x 4.40 mm
SN74HC595QDRQ1	SOIC (16)	9.90 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Figure 1. Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

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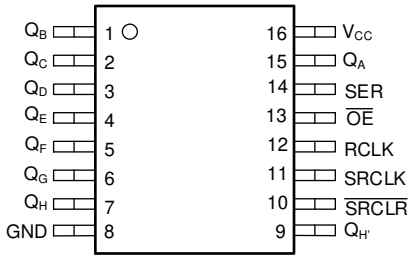
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2020	*	Initial release.

5 Pin Configuration and Functions

D and PW
16-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Q_B	1	Output	Q_B output
Q_C	2	Output	Q_C output
Q_D	3	Output	Q_D output
Q_E	4	Output	Q_E output
Q_F	5	Output	Q_F output
Q_G	6	Output	Q_G output
Q_H	7	Output	Q_H output
GND	8	—	Ground
$Q_{H'}$	9	Output	Serial output, can be used for cascading
$\overline{SRCLR}$	10	Input	Shift register clear, active low
SRCLK	11	Input	Shift register clock, rising edge triggered
RCLK	12	Input	Output register clock, rising edge triggered
$\overline{OE}$	13	Input	Output Enable, active low
SER	14	Input	Serial input
Q_A	15	Output	Q_A output
V_{CC}	16	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HC595-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			-40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9			V
				4.5 V	4.4	4.499		4.4			
				6 V	5.9	5.999		5.9			
			$Q_{H'}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7			
			Q_A – Q_H, I_{OH} = –6 mA		3.98	4.3		3.7			
			$Q_{H'}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2			
			Q_A – Q_H, I_{OH} = –7.8 mA		5.48	5.8		5.2			
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1			0.1	V
				4.5 V		0.001	0.1			0.1	
				6 V		0.001	0.1			0.1	
			$Q_{H'}$, I_{OH} = 4 mA	4.5 V		0.17	0.26			0.4	
			Q_A – Q_H, I_{OH} = 6 mA			0.17	0.26			0.4	
			$Q_{H'}$, I_{OH} = 5.2 mA	6 V		0.15	0.26			0.4	
			Q_A – Q_H, I_{OH} = 7.8 mA			0.15	0.26			0.4	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V			±0.1			±1	µA
I_{OZ}		V_O = V_{CC} or 0	Q_A – Q_H	6 V		±0.01	±0.5			±5	µA
I_{CC}	Supply current	V_I = V_{CC} or 0	I_O = 0	6 V			8			80	µA
C_i	Input capacitance			2 V to 6 V		3	10			10	pF

6.6 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	Operating free-air temperature (T_A)				UNIT
				25°C		–40°C to 125°C		
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2	MHz
			4.5 V		31		21	
			6 V		36		25	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		$\overline{SRCLR}$ low	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
t_{su}	Setup time	SER before SRCLK↑	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		25		
		SRCLK↑ before RCLK↑	2 V	75		113		
			4.5 V	15		23		
			6 V	13		19		
		$\overline{SRCLR}$ low before RCLK↑	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
t_h	Hold time	SER after SRCLK↑	2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

6.7 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

PARAMETER		FROM	TO	LOAD CAPACITANCE	V_{CC}	Operating free-air temperature (T_A)						UNIT
						25°C			–40°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Max switching frequency			50 pF	2 V	6	26		4.2			MHz
					4.5 V	31	38		21			
					6 V	36	42		25			
t_{pd}	Propagation delay	SRCLK	$Q_{H'}$	50 pF	2 V		50	160			240	ns
					4.5 V		17	32			48	
					6 V		14	27			41	
		RCLK	Q_A - Q_H	50 pF	2 V		50	150			225	
					4.5 V		17	30			45	
					6 V		14	26			38	
		RCLK	Q_A - Q_H	150 pF	2 V		51	175			261	
					4.5 V		18	35			52	
					6 V		15	30			44	

Switching Characteristics (continued)

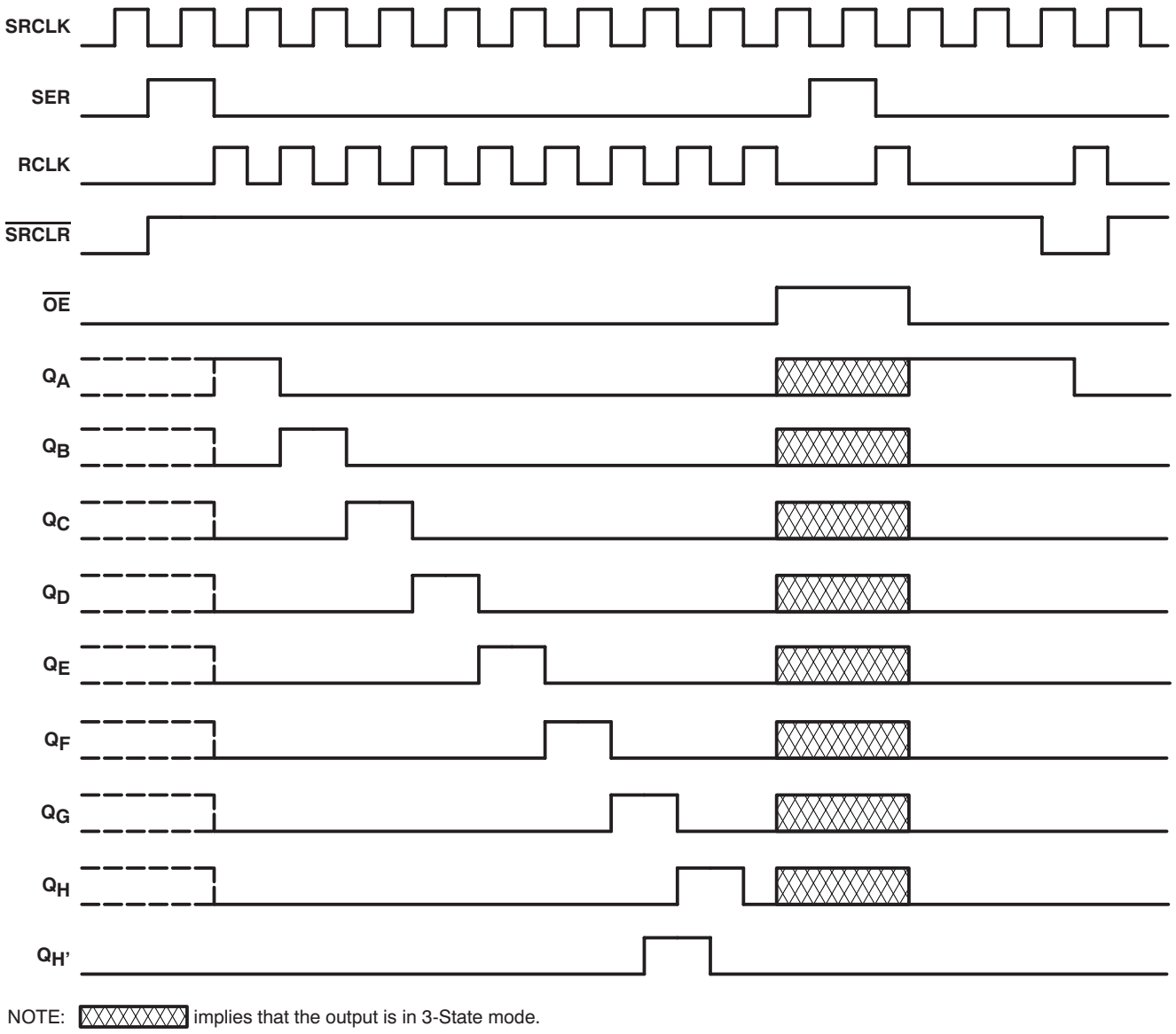
C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See Parameter Measurement Information.

PARAMETER		FROM	TO	LOAD CAPACITANCE	V_{CC}	Operating free-air temperature (T_A)						UNIT
						25°C			–40°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay	$\overline{SRCLR}$	$Q_{H'}$	50 pF	2 V		40	150			255	ns
					4.5 V		15	30			45	
					6 V		13	26			38	
t_{en}	Enable time	$\overline{OE}$	Q_A - Q_H	50 pF	2 V		42	200			300	ns
					4.5 V		23	40			60	
					6 V		20	34			51	
		$\overline{OE}$	Q_A - Q_H	150 pF	2 V		28	60			90	
					4.5 V		8	12			18	
					6 V		6	10			15	
t_{dis}	Disable time	$\overline{OE}$	Q_A - Q_H	50 pF	2 V		28	75			110	ns
					4.5 V		8	15			22	
					6 V		6	13			19	
t_t	Transition-time		Q_A - Q_H	50 pF	2 V		60	200			300	ns
					4.5 V		22	40			60	
					6 V		19	34			51	
			$Q_{H'}$	50 pF			70	200			298	
							23	40			60	
							19	34			51	
			Q_A - Q_H	150 pF	2 V		45	210			315	
					4.5 V		17	42			63	
					6 V		13	36			53	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		400		pF



NOTE: ▨ implies that the output is in 3-State mode.

Figure 2. Timing Diagram

6.9 Typical Characteristics

T_A = 25°C

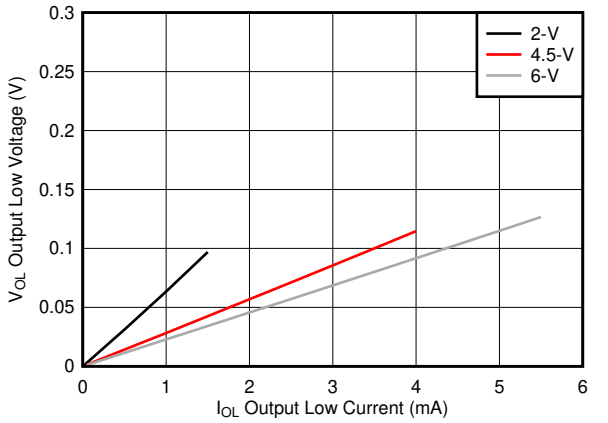


Figure 3. Output voltage versus output current in low state

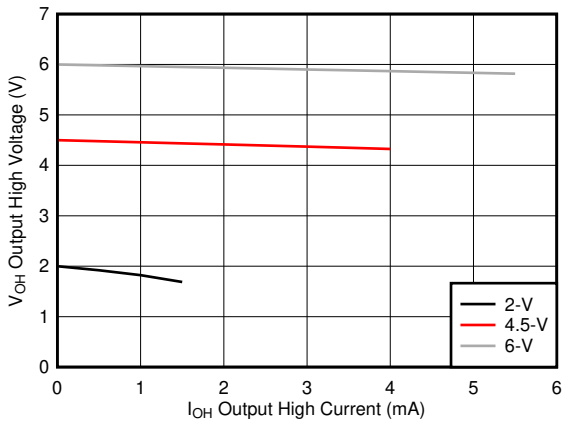


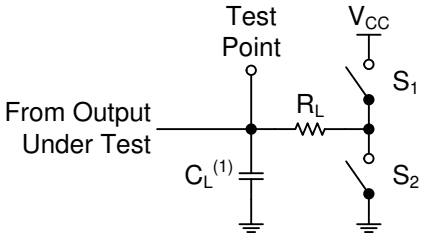
Figure 4. Output voltage versus output current in high state

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



C_L= 50 pF and includes probe and jig capacitance.

Figure 5. Load Circuit

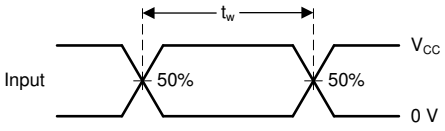


Figure 6. Voltage Waveforms, Pulse Duration

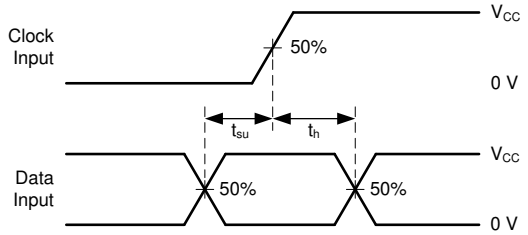
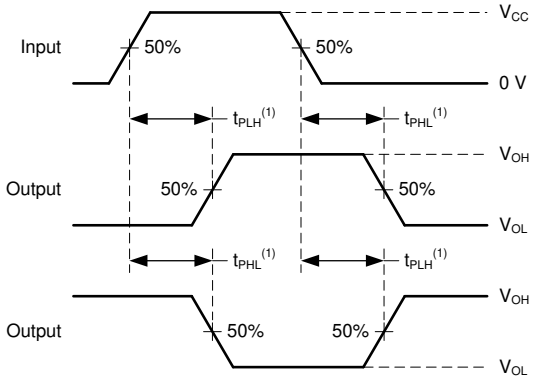


Figure 7. Voltage Waveforms, Setup and Hold Times



Voltage Waveforms, Propagation Delay specifications t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 8. Voltage Waveforms, Propagation Delays

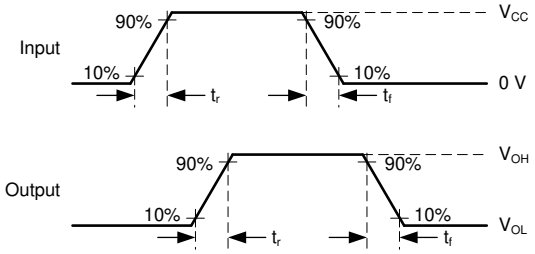


Figure 9. Voltage Waveforms, Input and Output Transition Times

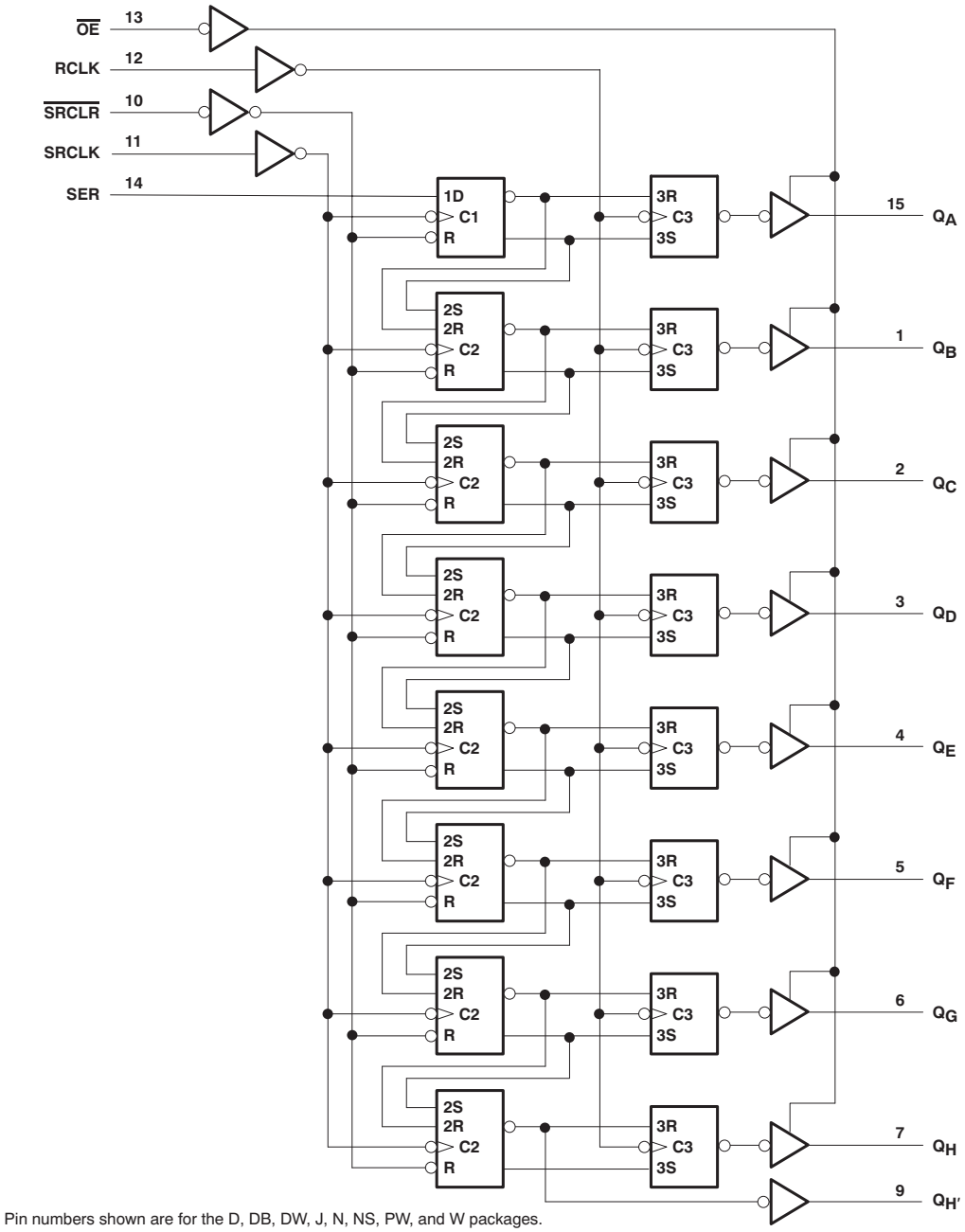
8 Detailed Description

8.1 Overview

The SN74HC595-Q1 is part of the HC family of logic devices intended for CMOS applications. The SN74HC595-Q1 is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

Figure 10. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74HC595-Q1 devices are 8-bit Serial-In, Parallel-Out Shift Registers. They have a wide operating current of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The devices have a low power consumption of 80-μA (Maximum) I_{CC}. Additionally, the devices have a low input current of 1 μA (Maximum) and a ±6-mA Output Drive at 5 V.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74HC595-Q1 devices.

Table 1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

9 Application and Implementation

9.1 Application Information

The SN74HC595-Q1 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

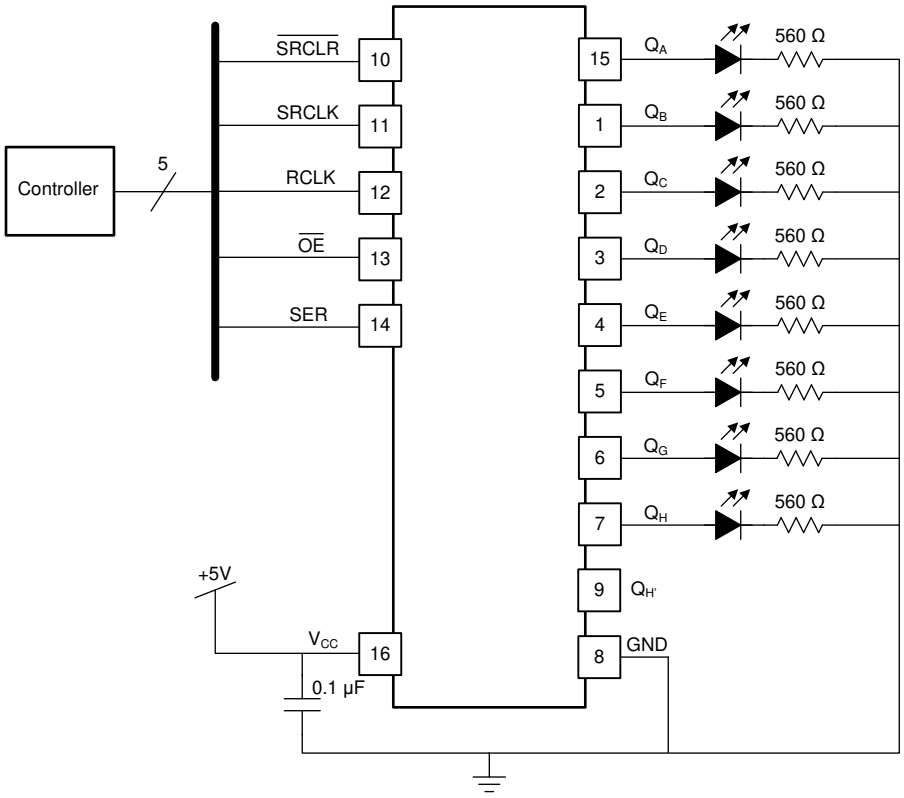


Figure 11. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions
  - Specified high and low levels. See (V_{IH} and V_{IL}) in the table.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in the table.
- Recommend output conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above V_{CC}

Typical Application (continued)

9.2.3 Application Curves

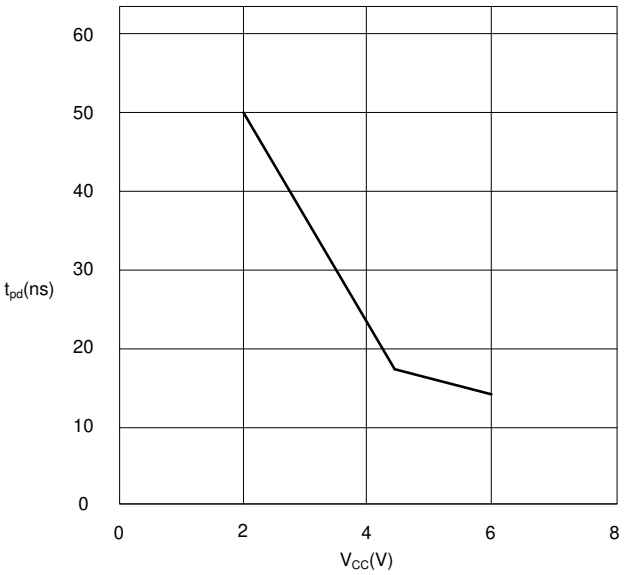


Figure 12. SN75HC595-Q1 t_{pd} vs. V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

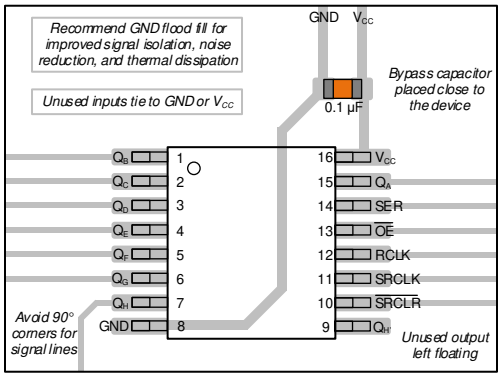


Figure 13. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC595QDRQ1	PREVIEW	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125		
SN74HC595QPWRQ1	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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