EM78P153B

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Official Release Version	2012/09/25
1.1	Revised the Min./Max. values of theDC Characteristics (Section 7)	2012/10/16
1.2	Added DC Charasteristics of LVR	2013/01/07
1.3	Modified the descriptions related to Sub IRC	2015/10/14
1.4	1. Modified the package type in the Features section 2. Modified package type in the Pin Assignment section 3. Modified Appendix A “Ordering and Manufacturing Information”	2016/04/25

1 General Description

The EM78P153B is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 1024×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides three protection bits to prevent intrusion of user's OTP memory code. Fifteen code option bits are also available to meet user's special requirements.

With enhanced OTP-ROM features, the EM78P153B provides a convenient method of developing and verifying user's programs. Moreover, this OTP device offers easy and effective program updates with the use of development and programming tools. You can avail of ELAN's Writer to easily program your development codes.

2 Features

- CPU Configuration
  - 1k × 13 bits on-chip ROM
  - 32 × 8 bits on-chip registers (SRAM, general purpose)
  - 5-level stacks for subroutine nesting
  - Less than 1.5 mA at 5V / 4 MHz
  - Typically 15 µA at 3V / 32kHz
  - Typically 1 µA during Sleep mode
- I/O Port Configuration
  - 2 bidirectional I/O ports : P5, P6
  - 12 I/O pins
  - Wake-up port : P6
  - 6 Programmable pull-down I/O pins
  - 7 programmable pull-high I/O pins
  - 7 programmable open-drain I/O pins
  - External interrupt : P60
- Operating Voltage Range:
  - 2.3V ~ 5.5V at 0 ~ 70°C (Commercial Grade)
- Operating Frequency Range (Base on 2 clocks):
  - Crystal Mode**:**
    DC ~ 20 MHz / 2clks @ 5V
    DC ~ 8 MHz / 2clks @ 3V
    DC ~ 4 MHz / 2clks @ 2.3V
    The transient point of system frequency between HXT and LXT is 400kHz.
  - ERC Mode**:**
    DC ~ 2MHz / 2clks @ 2.1V
  - IRC Mode**:**
    Oscillation Mode**:** 4 / 8 / 1MHz and 455kHz
    Process Deviation**:** Type: Max. ± 3%
    Temperature Deviation**:** ± 2% (0 ~ 70°C)

Internal RC Freq.	Drift Rate			
	Temp. (0~70°C)	Voltage	Process	Total
4 MHz	±1.5%	±8%@2.3~5.5V	±2%	±11.5%
8 MHz	±1.5%	±8%@3.0~5.5V	±2%	±11.5%
1 MHz	±1.5%	±8%@2.3~5.5V	±2%	±11.5%
455kHz	±1.5%	±8%@2.3~5.5V	±2%	±11.5%

- Peripheral Configuration
  - 8-bit real time clock / counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power on reset and 3 programmable level voltage reset
    POR**:** 1.8V (Default), LVR: 4.0, 3.5, 2.7V
  - 2- / 4- clocks per instruction cycle selected by code option
- Three Available Interrupts**:**
  - TCC overflow interrupt
  - Input-port status changed interrupt (Wake-up from Sleep mode)
  - External interrupt
- Special Features
  - Programmable free running watchdog timer
  - Power saving Sleep mode
  - Selectable oscillation mode
  - Programmable prescaler of oscillator set-up time
- Package Type**:**
  - 14-pin DIP 300mil : EM78P153BD14
  - 14-pin SOP 150mil : EM78P153BSO14
  - 10-pin SSOP 150mil : EM78P153BSS10

NOTE
These are all Green Products which do not contain hazardous substances.

3 Pin Assignment

14-Pin DIP/SOP

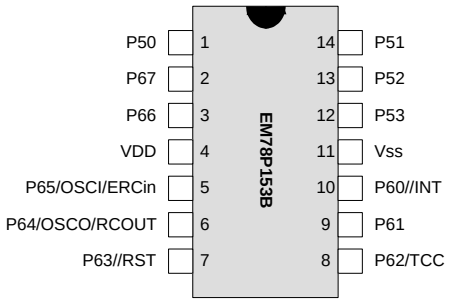


Figure 3-1a EM78P153BD14, EM78P153BSO14

10-Pin SSOP

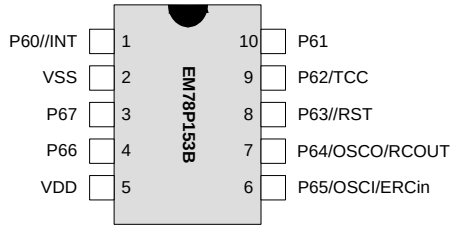


Figure 3-1b EM78P153BSS10

4 Pin Description

Name	Function	Input Type	Output Type	Description
P50 P51 P52	P50 P51 P52	ST	CMOS	Bidirectional I/O pin with programmable pull-low
P53	P53	ST	CMOS	Bidirectional I/O pin
P60/INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-low, open-drain and wake-up pin from Sleep mode when the pin status changes.
	/INT	ST	–	External interrupt pin triggered by a falling edge
P61	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-low, open-drain and wake-up pin from Sleep mode when the pin status changes.
P62/TCC	P62	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake-up pin from Sleep mode when the pin status changes.
	TCC	ST	–	External Input of real Time Clock / Counter Clock
P63//RESET	P63	ST	–	Input pin and wake-up pin from Sleep mode when the pin status changes.
	/RESET	ST	–	External pull-high reset pin, active low.
P64/OSCO/ RCOUT	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain and wake-up pin from Sleep mode when the pin status changes.
	OSCO	–	XTAL	Clock output of Crystal/Resonator Oscillator
	RCOUT	–	CMOS	Clock output of internal RC Oscillator and External RC Oscillator

(Continuation)

Name	Function	Input Type	Output Type	Description
P65/OSCI/ ERCin	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain and wake-up pin from Sleep mode when the pin status changes.
	OSCI	XTAL	–	Clock input of Crystal/Resonator Oscillator
	ERCin	AN	–	External RC input pin
P66 P67	P66 P67	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain and wake-up pin from Sleep mode when the pin status changes.
VDD	VDD	Power	–	Power supply for chip
VSS	VSS	Power	–	Ground for chip

5 Functional Description

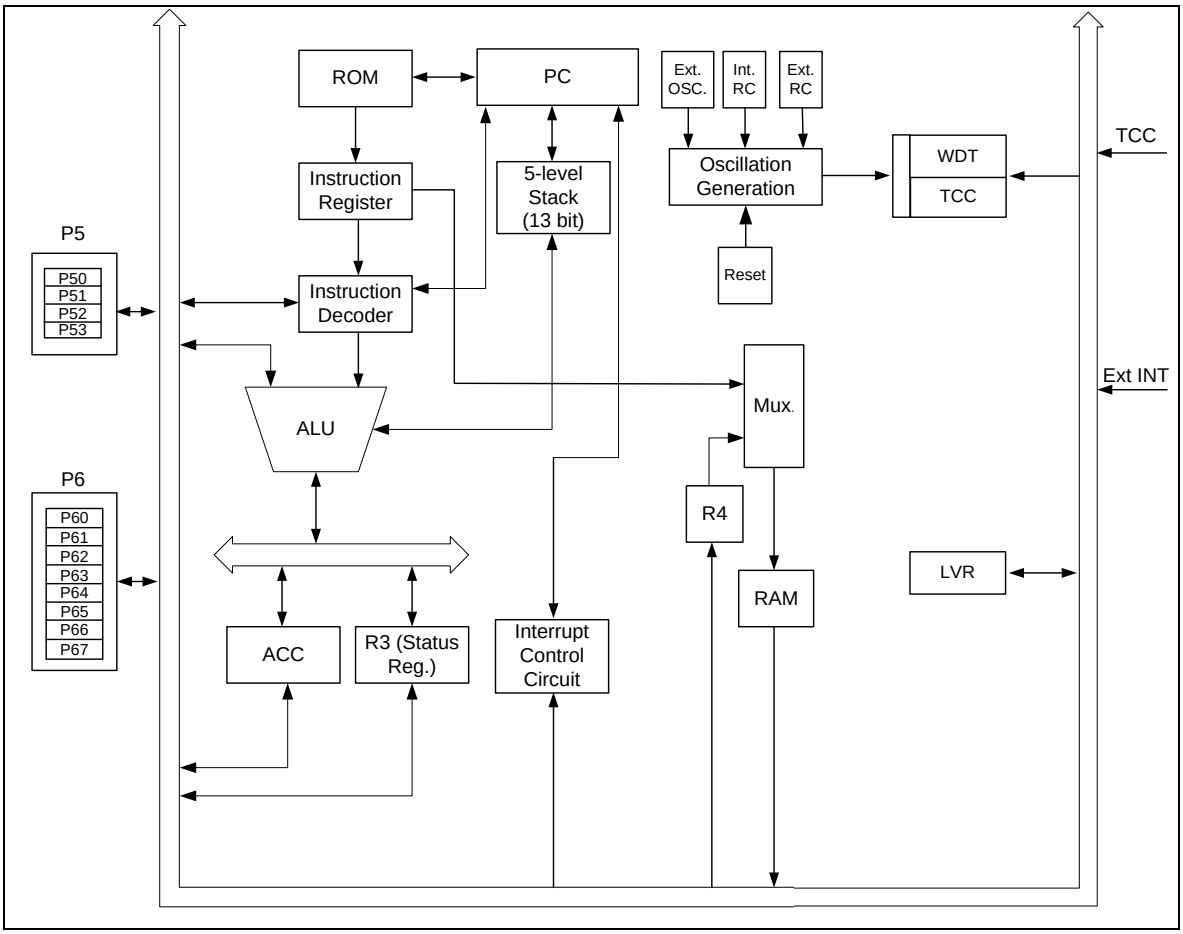


Figure 5-1 EM78P153B Functional Block Diagram

5.1 Operation Registers

5.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

5.1.2 R1 (Timer Clock/Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

5.1.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

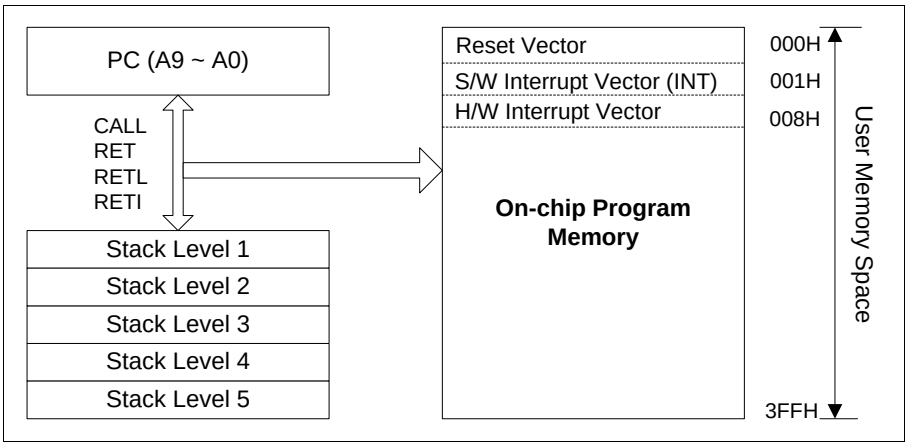


Figure 5-2 Program Counter Organization

- The configuration structure generates 1024 × 13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "**0**" when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

- "CALL" instruction loads the lower 10 bits of the PC, and then PC + 1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- Any instruction written to R2 (e.g., “ADD R2, A”, "MOV R2, A", "BC R2, 6",···) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to be cleared. Hence, the computed jump is limited to the first 256 locations of a page.
- All instructions are single instruction cycle (FCLK / 2 or FCLK / 4) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.
- The Data Memory Configuration is as follows**:**

Address	R Registers	IOC Registers
		CONT (Control Register)
00	R0 (Indirect Addressing Register)	Reserve
01	R1 (TCC Buffer)	Reserve
02	R2 (Program Counter)	Reserve
03	R3 (Status Register)	Reserve
04	R4 (Ram Select Register)	Reserve
05	R5 (Port 5 I/O Data)	IOC5 (I/O Port Control Register)
06	R6 (Port 6 I/O Data)	IOC6 (I/O Port Control Register)
07	Reserve	Reserve
08	Reserve	Reserve
09	Reserve	Reserve
0A	Reserve	Reserve
0B	Reserve	IOCB (Pull-Down Control Register)
0C	Reserve	IOCC (Open-Drain Control Register)
0D	Reserve	IOCD (Pull-high Control Register)
0E	Reserve	IOCE (WDT Control Register)
0F	RF (Interrupt Status Register)	IOCF (Interrupt Mask Register)
10 : 2F	General Registers	

5.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GP1	GP0	T	P	Z	DC	C

Bit 7 (RST): Bit for reset type

0: Set to "**0**" if the device wakes up from other reset type

1: Set to "**1**" if the device wakes up from Sleep mode on a pin change

Bits 6 ~ 5 (GP1 ~ GP0): General-purpose read/write bits

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up; and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power on or by a "WDTC" command; and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

5.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Not used (Read only). Set to "**1**" all the time.

Bits 5 ~ 0: Are used to select registers (Address**:** 0x00 ~ 0x06, 0x0F ~ 0x2F) in indirect addressing mode. See the table on Data Memory Configuration in Section 5.1.3, *R2 (Program Counter and Stack)*.

5.1.6 R5 ~ R6 (Port 5 ~ Port 6)

R5 and *R6* are I/O registers.

Only the lower 4 bits of R5 are available.

The upper 4 bits of R5 are fixed to "**0**".

P63 is input only.

5.1.7 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

Bits 7 ~ 3: Not used. Set to "**0**" all the time.

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on /INT pin, reset by software.

0: No interrupt occurs

1: Interrupt is requested

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

0: No interrupt occurs

1: Interrupt is requested

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

0: No interrupt occurs

1: Interrupt is requested

NOTE

- *RF can be cleared by instruction but cannot be set.*
- *IOCF is the interrupt mask register.*
- *The result of reading RF is the "logic AND" of RF and IOCF.*

5.1.8 R10 ~ R2F

These are all 8-bit general-purpose registers.

5.2 Special Function Registers

5.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator; which is not an addressable register.

5.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (GP): General purpose register

Bit 6 (/INT): Interrupt Enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock. P62 is a bidirectional I/O pin.

1: Transition on TCC pin

Bit 4 (TE): TCC signal edge

0: Increment if the transition from low to high takes place on the TCC pin

1: Increment if the transition from high to low takes place on the TCC pin

Bit 3 (PAB): Prescaler assigned bit

0: TCC

1: WDT

Bits 2 ~ 0 (PSR2 ~ PSR0): TCC / WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable by instruction “CONTW” and “CONTR”.

5.2.3 IOC5 ~ IOC6 (I/O Port Control Register)

0: Defines the relative I/O pin as output

1: Puts the relative I/O pin into high impedance

Only the lower 4 bits of IOC5 are available to be defined.

IOC5 and IOC6 registers are both readable and writable.

5.2.4 IOCB (Pull-Down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/PD62	/PD61	/PD60	-	/PD52	/PD51	/PD50

Bit 7: Not used. Set to “**1**” all the time.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bit 3: Not used. Set to "**1**" all the time.

Bit 2 (/PD52): Control bit used to enable pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

The IOCB Register is both readable and writable.

5.2.5 IOCC (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	-	OD62	OD61	OD60

Bit 7 (OD67): Control bit used to enable open-drain of the P67 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3: Not used. Set to "**0**" all the time.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin.

The IOCC Register is both readable and writable.

5.2.6 IOCD (Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	-	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit is used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3: Not used. Set to "**1**" all the time.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

5.2.7 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	-	-	-	-

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of the P60 (/INT) pin.

0: P60, bidirectional I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "**1**."

When EIS is "**0**," the path of the /INT is masked. When EIS is "**1**," the status of the /INT pin can also be read through Port 6 (R6).
See Figure 5-4b under Section 5.4, *I/O Ports;* for reference.

EIS is both readable and writable.

Bits 5 ~ 0: Not used. Set to "**0**" all the time.

5.2.8 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Bits 7 ~ 3: Not used. Set to "**1**" all the time.

Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 5-6 in Section 5.6, *Interrupt*.

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

The IOCF register is both readable and writable.

5.3 TCC/WDT and Prescaler

An 8-bit counter is provided as prescaler for the TCC or WDT. The prescaler is only available for either TCC or WDT at a time. The PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0 ~ PSR2 bits determine the ratio. The prescaler is cleared each time an instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. Figure 5-3 below depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be an internal or external clock input (edge selectable from TCC pin). If the TCC signal source is from an internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). Refer to the following figure (Figure 5-3) to determine whether CLK = FOSC/2 or CLK = FOSC/4 is used. It will depend on the status of the Code Option bit CLK. CLK = FOSC/2 is used if CLK bit is "**0**", and CLK = FOSC/4 is used if CLK bit is "**1**". If the TCC signal source is from an external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.

- The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of the IOCE register (Section 5.2.7). Without prescaler, the WDT time-out period is approximately 23.5ms[1] (default).

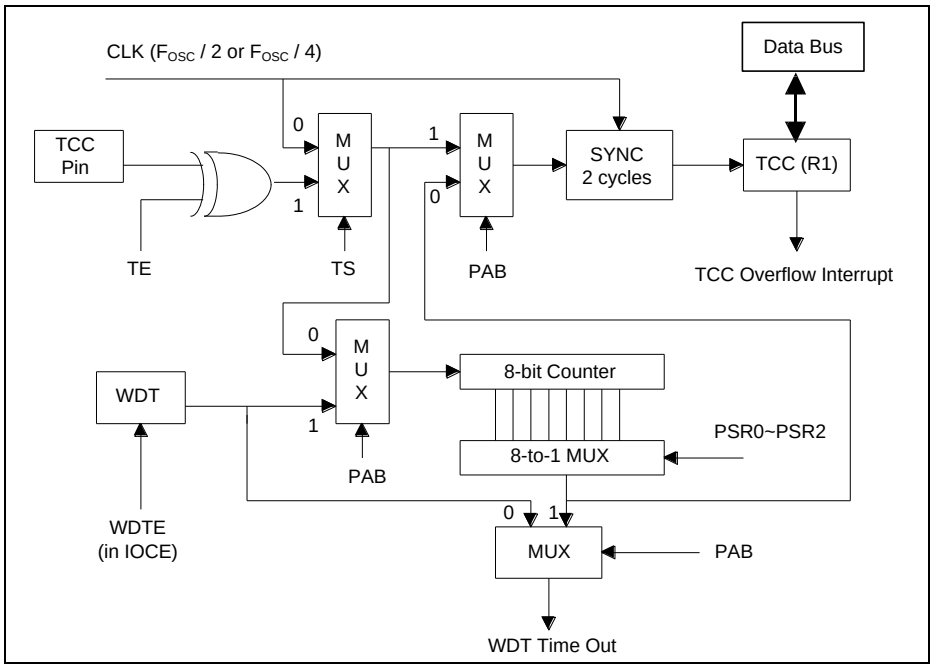
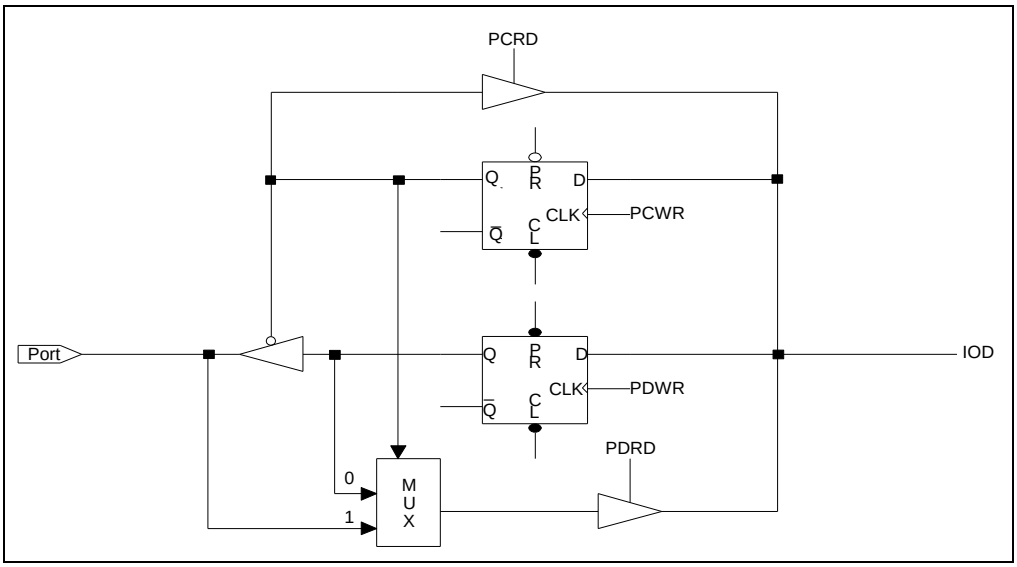


Figure 5-3 TCC and WDT Block Diagram

[1] *V_{DD} = 5V, set up time period = 23.5ms ± 30% at* 25°C
V_{DD} = 3V, set up time period = 26ms ± 30% at 25°C

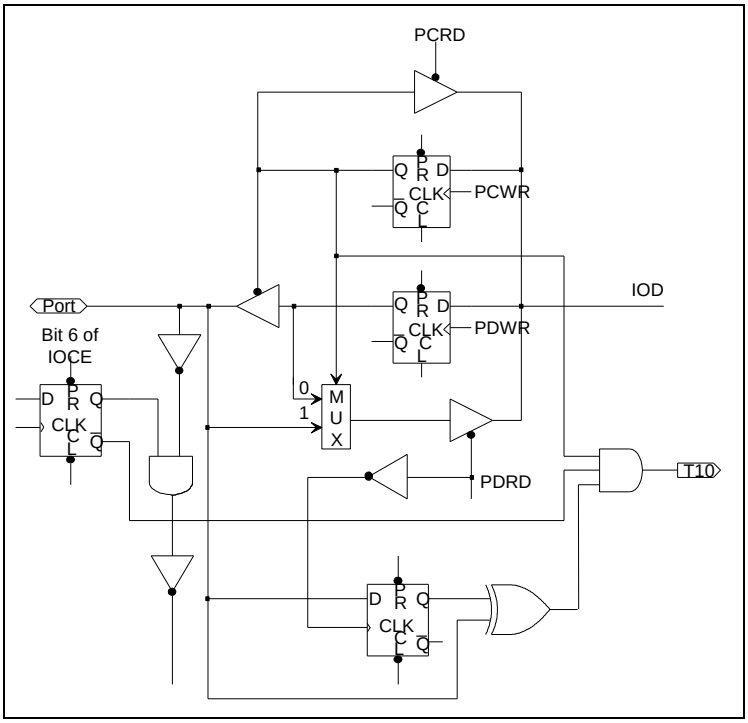
5.4 I/O Ports

The I/O registers, Port 5 and Port 6 are both bidirectional tri-state I/O ports. Port 6 can be pulled-high internally by software except for P63 pin. In addition, Port 6 can also have open-drain output by software except for P63 pin. Input status change interrupt (or Wake-up) function is also available from Port 6. Pins P50 ~ P52 and P60 ~ P62 can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6) except for P63 pin. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in Figures 5-4a to 5-4d below.



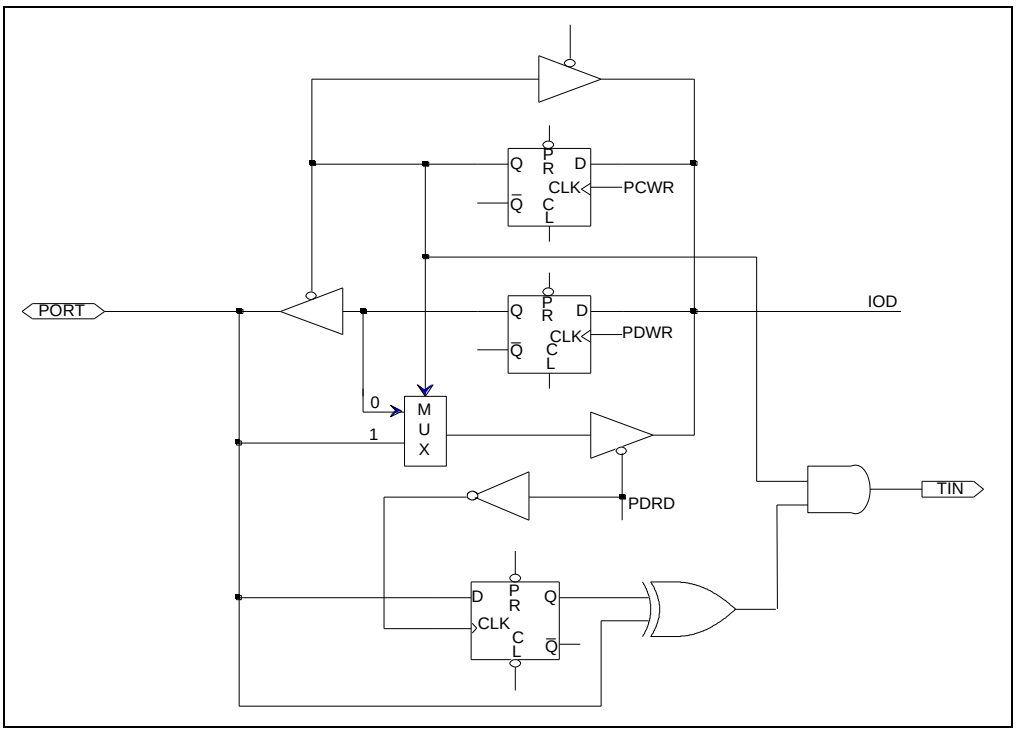
NOTE: *Pull-down is not shown in the figure.*

Figure 5-4a I/O Port and I/O Control Register Circuit for Port 5



NOTE: *Pull-high (down) and open-drain are not shown in the figure.*

Figure 5-4b I/O Port and I/O Control Register Circuit for P60 (/INT)



NOTE: *Pull-high (down) and open-drain are not shown in the figure.*

Figure 5-4c I/O Port and I/O Control Register Circuit for P61, P62, and P64~P67

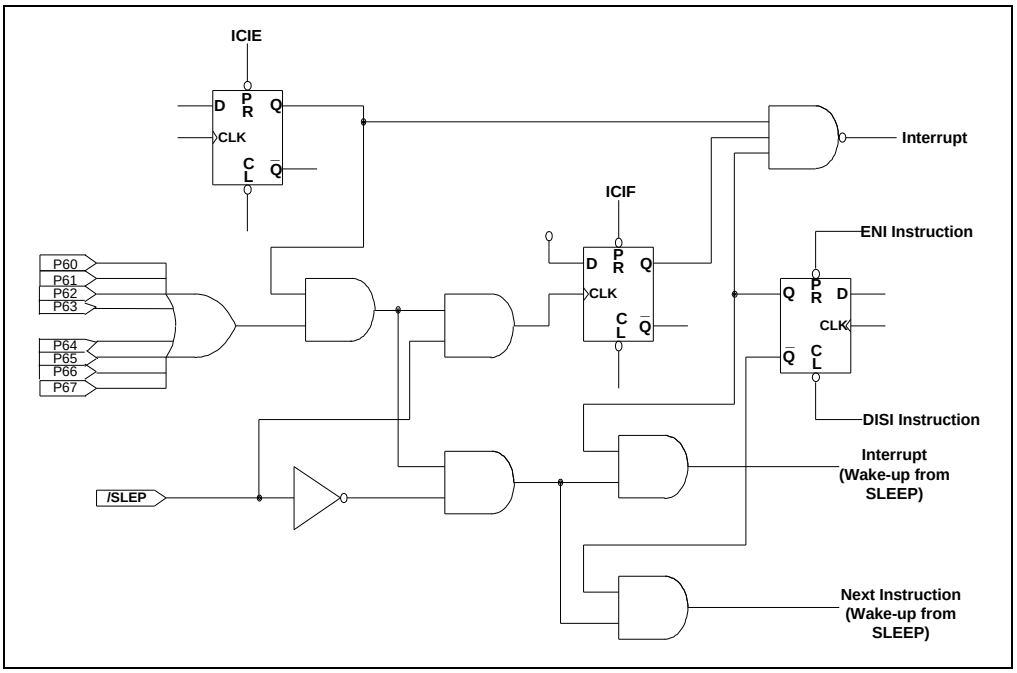


Figure 5-4d Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-Up

5.4.1 Usage of Port 6 Input Change Wake-Up / Interrupt Function

1. Wake-up from Input Status Change
a) Before SLEEP:
1) Disable WDT
2) Read I/O Port 6 (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Interrupt (Set IOCF.1)
5) Execute "SLEP" instruction
b) After Wake-up:
1) IF "ENI" → Interrupt vector (008H)
2) IF "DISI" → Next instruction

2. Input Status Change Interrupt
1) Read I/O Port 6 (MOV R6, R6)
2) Execute "ENI"
3) Enable Interrupt (Set IOCF.1)
4) IF Port 6 Change (Interrupt)
→ Interrupt Vector (008H)

5.5 Reset and Wake-up

5.5.1 Reset

A Reset is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)
4) Low Voltage Reset

The device is kept under reset condition for a period of approximately 23.5ms[2] (one oscillator start-up timer period) after a reset is detected. Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**."
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "**1**" except for Bit 6 (INT flag).
- The bits of the IOCB register are set to all "**1**".
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "**1**."
- Bit 7 of the IOCE register is set to "**1**" and Bit 6 is cleared.
- Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by**:**

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) Port 6 Input Status changes (if enabled)

[2] *V_{DD} = 5V, set up time period = 23.5ms ± 30% at 25°C*
V_{DD} = 3V, set up time period = 26ms ± 30% at 25°C

The first two cases will cause the EM78P153B to reset. The T and P flags of R3 are used to determine the source of the reset (Wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 008H after Wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after a Wake-up.

Only one of Cases 2 and 3 can be enabled before going into the Sleep mode. That is;

a] If Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P153B can be awakened only by Case 1 or Case 3.

b) If WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P153B can be awakened only by Case 1 or Case 2. Refer to Section 5.6, *Interrupt* for further details.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P153B (Case [a] above), the following instructions must be executed before SLEP**:**

```
MOV A, @xxxx1110b     ; Select the WDT prescaler, it must be
                      ; set over 1:1
CONTW
WDTC                  ; Clear WDT and prescaler
MOV A, @0xxxxxxxb     ; Disable WDT
IOW RE
MOV R6, R6            ; Read Port 6
MOV A, @00000x1xb     ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)         ; Enable (or disable) global interrupt
SLEP                  ; Sleep
```

NOTE

1. *After waking up from Sleep mode, the WDT is automatically enabled. WDT enable / disable operation after waking up from Sleep mode must be appropriately defined in the software.*
2. *To avoid a reset from occurring when Port 6 Input Status Change Interrupt enters into an interrupt vector or is used to Wake-up the MCU, the WDT prescaler must be set above the 1:1 ratio.*

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5.5.2 Wake-up and Interrupt Modes Operation Summary

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Condition Signal	Sleep Mode		Normal Mode	
		DISI	ENI	DISI	ENI
External INT	EXIE = 0	Wake-up is invalid		INT is invalid	
	EXIE = 1			Next Inst.	INT + INT Vector
Port 6 Pin change	ENWDT = 1 ICIE = 0	Wake-up is invalid		INT is invalid	
	ENWDT = 1 ICIE = 1	Wake-up is invalid	Wake-up + INT Vector	Next Inst.	INT + INT Vector
	ENWDT = 0 ICIE = 0	Wake-up is invalid		INT is invalid	
	WDTEN = 0 ICIE = 1	Wake-up is invalid	Wake up + INT Vector	Next Inst.	INT + INT Vector
TCC Overflow	TCIE = 0	Wake-up is invalid		INT is invalid	
	TCIE = 1			Next Inst.	INT + INT Vector
WDT Timeout	WDTE = 1	Wake up + Reset		Reset	
Low Voltage Reset	–	Wake up + Reset		Reset	

5.5.3 Summary of Registers Initialized Values

Legend: *x: Not used* ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	*	*	P	P	P
		Wake-up from Pin Change	1	P	P	*	*	P	P	P
0×04	R4 (RSR)	Bit Name			-	-	-	-	-	-
		Power-on	1	1	U	U	U	U	U	U
		/RESET and WDT	1	1	P	P	P	P	P	P
		Wake-up from Pin Change	1	1	P	P	P	P	P	P
0×05	P5	Bit Name	×	×	×	×	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR)	Bit Name	×	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	N	P

* *Refer to tables provided in Sections 5.5.4 "Status of RST, T and P of the Status Register"*

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	CONT	Bit Name	×	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
0×05	IOC5	Bit Name	×	×	×	×	C53	C52	C51	C50
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0×06	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	IOCB	Bit Name	×	/PD66	/PD65	/PD64	x	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	IOCC	Bit Name	OD67	OD66	OD65	OD64	×	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	/PH67	/PH66	/PH65	/PH64	×	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE	Bit Name	WDTE	EIS	×	×	×	×	×	×
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	1	P	1	1	1	1	1	1
0×0F	IOCF	Bit Name	×	×	×	×	×	EXIE	ICIE	TCIE
		Power-on	1	1	1	1	1	0	0	0
		/RESET and WDT	1	1	1	1	1	0	0	0
		Wake-up from Pin Change	1	1	1	1	1	P	P	P
0×10 ∫ 0×2F	R10 ∫ R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

5.5.4 Status of RST, T, and P of the Status Register

A Reset condition is initiated by the following events:

1) A power-on condition
2) A high-low-high pulse on /RESET pin
3) Watchdog timer time-out

■ **Values of RST, T, and P after a Reset:**

The values of T and P as listed in the following table are used to check how the processor wakes up.

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	*P
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

■ **Status of T and P being Affected by Events:**

The following table shows the events that may affect the status of T and P.

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

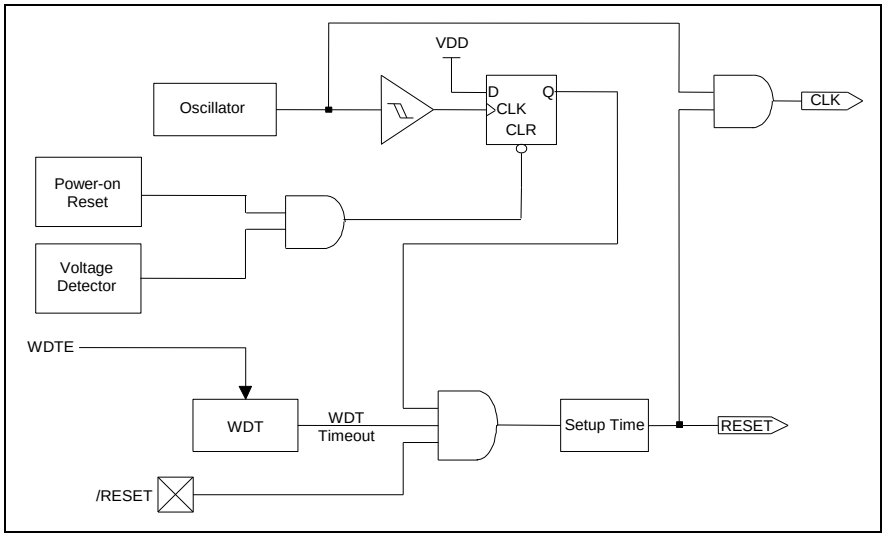


Figure 5-5 Controller Reset Block Diagram

5.6 Interrupt

The EM78P153B has three falling-edge interrupts as listed below**:**

1) TCC overflow interrupt
2) Port 6 Input Status Change Interrupt
3) External interrupt [(P60, /INT) pin]

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin that is configured as /INT is excluded from this function. The Port 6 Input Status Change Interrupt can wake up the EM78P153B from Sleep mode if Port 6 is enabled prior to going into Sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt Vector 008H.

RF is the Interrupt Status Register that records the interrupt requests in the relative flags/bits. IOCF is an Interrupt Mask Register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one enabled interrupt occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Figure 5-6 below). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (if enabled), the next instruction will be fetched from Address 001H.

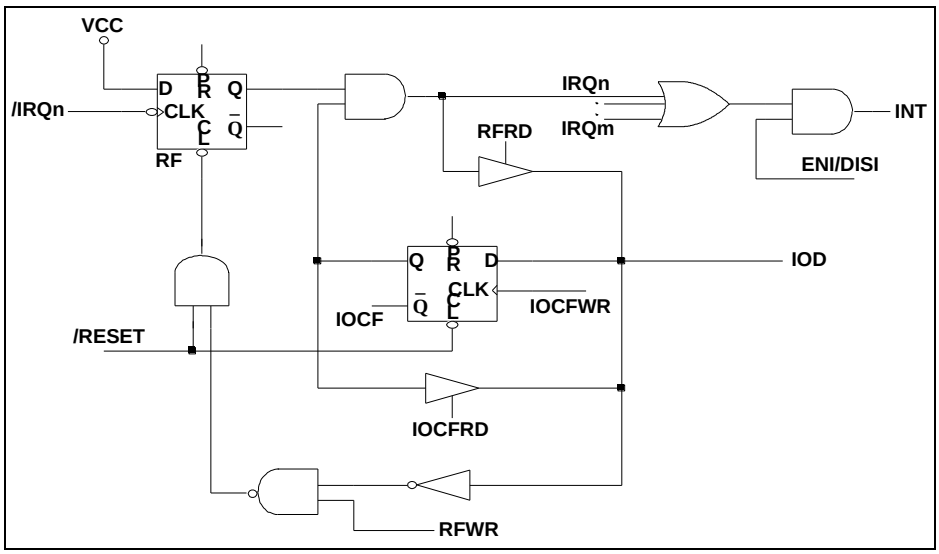


Figure 5-6 Interrupt Input Circuit

5.7 Oscillator

5.7.1 Oscillator Modes

The EM78P153B can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode (IRC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). The desired mode can be selected by programming OSC1 ~ OSC0 in the Code Option register. Table below describes how these four oscillator modes are defined.

■ **Oscillator Modes Defined by OSC**

Oscillator Modes	RCOUT	OSC1	OSC0
LXT (Low crystal oscillator mode, Freq. range is over 400kHz)	x	0	0
HXT (High crystal oscillator mode, Freq. range is above 400kHz)	x	0	1
ERC[1] (External RC oscillator mode); P64/RCOUT act as P64	0	1	0
ERC[1] (External RC oscillator mode); P64/RCOUT act as RCOUT	1	1	0
IRC[2] (Internal RC oscillator mode); P64/RCOUT act as P64	0	1	1
IRC[2] (Internal RC oscillator mode); P64/RCOUT act as RCOUT	1	1	1

[1] *Under ERC mode, ERCin is used as oscillator pin. RCOUT/P64 is defined by Code Option Word 1 Bit 3.*

[2] *In IRC mode, P64 is normal I/O pin. RCOUT/P64 is defined by Code Option Word 1 Bit 3.*

The maximum operating frequency of the crystal/resonator under different VDD is listed below.

■ **Summary of Maximum Operating Speeds**

Conditions	VDD	Max Freq. (MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

5.7.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P153B can be driven by an external clock signal through the OSCI pin as shown in the figure at right.

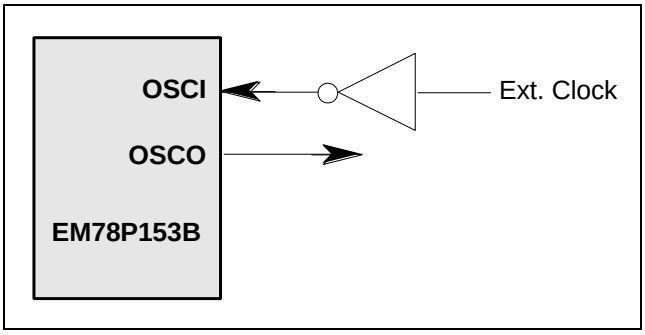


Figure 5-7 Circuit for External Clock Input

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 5-8a depicts such a circuit. The same thing applies whether it is in the HXT mode or in the LXT mode.

In Figure 5-8b, when the connected resonator in OSCI and OSCO is used in applications, the 1 MΩ R1 needs to be shunted with a resonator.

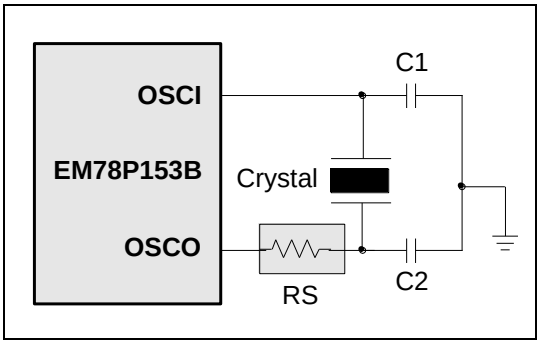


Figure 5-8a Circuit for Crystal/Resonator

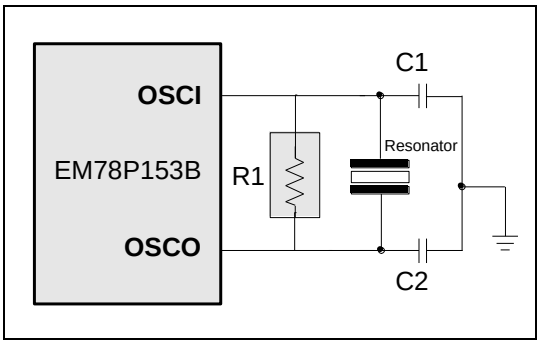


Figure 5-8b Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attributes, refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100 ~ 150	100 ~ 150
		2.0 MHz	20 ~ 40	20 ~ 40
		4.0 MHz	10 ~ 30	10 ~ 30
Crystal Oscillator	LXT	32768Hz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20 ~ 40	20 ~ 150
		1.0 MHz	15 ~ 30	15 ~ 30
		2.0 MHz	15	15
		4.0 MHz	15	15

5.7.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (right figure) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (REXT), the capacitor (CEXT), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations. In order to maintain a stable system frequency, the value of the CEXT should not be lesser than 20pF, and that of REXT should not be greater than 1 MΩ. If they cannot be kept under this range, the frequency can be easily affected by noise, humidity, and leakage.

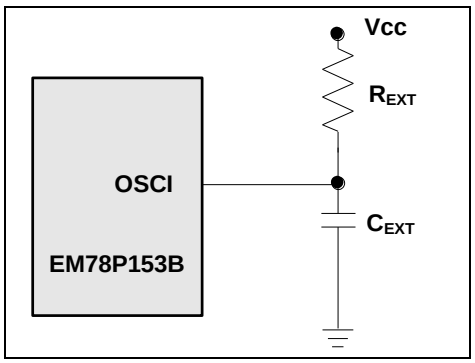


Figure 5-9 External RC Oscillator Mode Circuit

The smaller the REXT value in the RC oscillator, the faster its frequency will be. However, a very low REXT value of less than 3.3k, for instance 1 kΩ; the oscillator will become unstable as the NMOS will not be able to correctly discharge the capacitance current.

Based on the above reason, it must be kept in mind that the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, may affect the system frequency.

■ **RC Oscillator Frequencies**

C_{EXT}	R_{EXT}	Average F_{OSC} 5V, 25°C	Average F_{OSC} 3V, 25°C
20pF	3.3k	2.064MHz	1.901MHz
	5.1k	1.403MHz	1.316MHz
	10k	750kHz	719.7kHz
	100k	81.45kHz	81.33kHz
100pF	3.3k	647.3kHz	615.1MHz
	5.1k	430.8kHz	414.3kHz
	10k	225.8kHz	219.8kHz
	100k	23.88kHz	23.96kHz
300pF	3.3k	256.6kHz	245.3kHz
	5.1k	169.5kHz	163.0kHz
	10k	88.53kHz	86.14kHz
	100k	9.283kHz	9.255kHz

NOTE

1) *These are measured in DIP packages*
2) *The values are for design reference only*
3) *The frequency drift is ±30%*

5.7.4 Internal RC Oscillator Mode

EM78P153B offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the Option Bits C0 ~ C4. The table below describes the EM78P153B internal RC drift with variation of voltage, temperature, and process.

■ **Internal RC Drift Rate (T_A = 25˚C, V_{DD} = 5V, V_{SS} = 0V)**

Internal RC Freq.	Drift Rate			
	Temp. (0˚C ~ 70˚C)	Voltage	Process	Total
4 MHz	± 1.5%	± 8% @ 2.3V ~ 5.5V	± 2%	± 11.5%
8 MHz	± 1.5%	± 8% @ 3.0V ~ 5.5V	± 2%	± 11.5%
1 MHz	± 1.5%	± 8% @ 2.3V ~ 5.5V	± 2%	± 11.5%
455kHz	± 1.5%	± 8% @ 4.0V ~ 5.5V	± 2%	± 11.5%

NOTE: *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

5.8 Code Option Register

The EM78P153B has a Code Option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

■ **Code Option Register and Customer ID Register Arrangement Distribution:**

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

5.8.1 Code Option Register (Word 0)

Word 0											
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2~0
Mnemonic	RESETEN	ENWDT	CLKS	LVR1	LVR0	–	WDTPS1	WDTPS0	–	–	Protect
1	Disable	Disable	4 clocks	High	High	–	High	High	–	–	Disable
0	Enable	Enable	2 clocks	Low	Low	–	Low	Low	–	–	Enable

Bit 12 (RESETEN): Define Pin 63 as a Reset pin

0: /RESET enable

1: /RESET disable

Bit 11 (ENWDT): Watchdog timer enable bit

0: Enable

1: Disable

Bit 10 (CLKS): Instruction period option bit.

0: Two oscillator periods

1: Four oscillator periods

Refer to the Instruction Set (Section 5.13).

Bits 9 ~ 8 (LVR1 ~ LVR0): Low Voltage Reset control bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.0V

Bit 7: Not used. Set to "**1**" all the time.

Bits 6 ~ 5 (WDTPS1 ~ WDTPS0): WDT Time-out Period of device bits.

■ WDT Time-out Period for Device Programming

WDTPS1	WDTPS0	*WDT Time-out Period
1	1	23.5 ms
1	0	5.9 ms
0	1	376 ms
0	0	94 ms

*****_These are values tested in Laboratory._
Actual values may vary depending on the actual process

Bits 4 ~ 3: Not used. Set to "**1**" all the time

Bits 2 ~ 0 (Protect): Protect Bits. Each protect status is as follows:

Protect Bits	Protect
0	Enable
1	Disable (Default)

5.8.2 Code Option Register (Word 1)

Word 1													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**–**	**C4**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**	**–**	**RCOUT**	**OSC1**	**OSC0**	**–**
1	–	High	High	High	High	High	High	High	–	High	High	High	–
0	–	Low	Low	Low	Low	Low	Low	Low	–	Low	Low	Low	–

Bit 12: Not used. Set to "**1**" all the time.

Bits 11 ~ 7 (C4 ~ C0): Internal RC mode Calibration bits. These bits must always be set to "**1**" only (Auto calibration).

Bits 6 ~ 5 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	* Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

**These are theoretical values provided for reference only.*
Actual values may vary depending on the actual process

Bit 4: Not used. Set to "**1**"all the time.

Bit 3 (RCOUT Selection bit of oscillator output or I/O port (see table below)

0: P64

1: OSCO

Bits 2 ~ 1 (OSC1 and OSC0): Oscillation mode select bits

■ **Oscillation modes selection:**

Oscillation Modes	RCOUT	OSC1	OSC0
LXT (Low crystal oscillator mode, Freq. range is over 400kHz)	–	0	0
HXT (High crystal oscillator mode, Freq. range is above 400kHz)	–	0	1
ERC[1] (External RC oscillator mode); P64/RCOUT acts as P64	0	1	0
ERC[1] (External RC oscillator mode); P64/RCOUT acts as RCOUT	1	1	0
IRC[2] (Internal RC oscillator mode); P64/RCOUT acts as P64	0	1	1
IRC[2] (Internal RC oscillator mode); P64/RCOUT acts as RCOUT	1	1	1

[1] *In ERC mode, ERCin is used as oscillator pin. RCOUT/P64 is defined by Code Option Word 1 Bit 3 ~ Bit 1.*

[2] *In IRC mode, P64 is normal I/O pin. RCOUT/P64 is defined by Code Option Word 1 Bit 3 ~ Bit 1.*

Bit 0: Not used. Set to "**1**" all the time.

5.8.3 Code Option Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bits 12 ~ 0: Bits 12 ~ 0 of Customer's ID code

5.9 Power-On Considerations

Any microcontroller is not guaranteed to start operating properly before the power supply stabilizes at steady state. Under customer application, when power is OFF, VDD must drop to below 1.8V and remains OFF for 10µs before power can be switched ON again. In this way, the EM78P153B will reset and operate normally. The extra external reset circuit will work well if VDD can rise at a very fast speed (50ms or less). However, under critical applications, extra devices are still required to assist in solving the power-up problems.

5.10 Programmable Oscillator Set-up Time

The Code Option Register Words (Word 0/1/2) contains SUT0 and SUT1 which are used to define the oscillator set-up time. Theoretically, its range is from 6.5ms to 104ms. For most of the crystal or ceramic resonators, the lower the operation frequency is, the longer the set-up time may be required.

5.11 External Power-on Reset Circuit

The circuitry in the figure at right implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for VDD to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time.

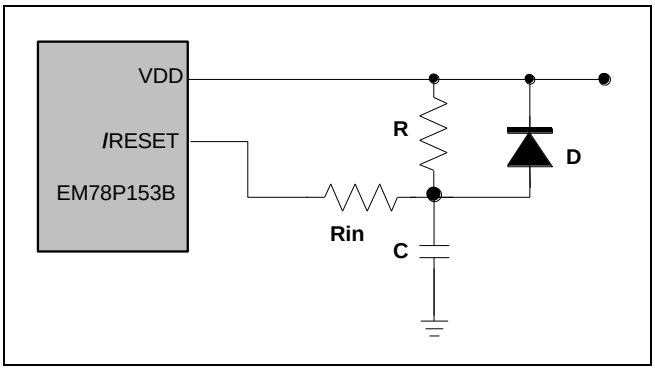


Figure 5-10 External Power-up Reset Circuit

Since the current leakage from the /RESET pin is ± 5µA, it is recommended that R should not be greater than 40k in order for the /RESET pin voltage to remain and kept at below 0.2V. The diode (D) functions as a short circuit at the instant of power down. The capacitor C will discharge rapidly and fully. The current-limited resistor (Rin), will prevent high current or ESD (electrostatic discharge) from flowing into /RESET pin.

5.12 Residue-Voltage Protection

When the battery is replaced, the device power (VDD) is cut off but residue-voltage remains. The residue-voltage may trips below the minimum VDD, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to accomplish a proper residue-voltage protection circuit for the EM78P153B.

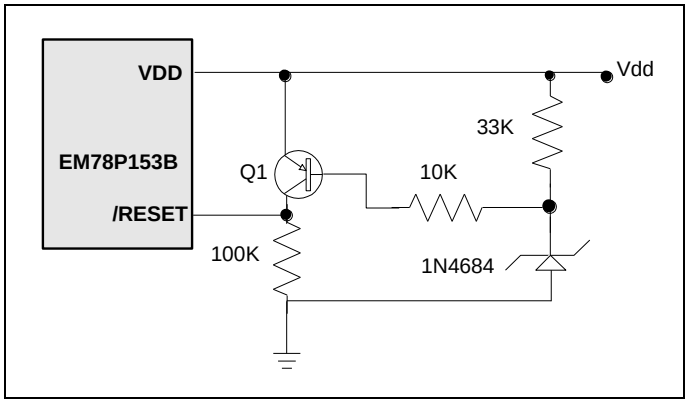


Figure 5-11a Residue Voltage Protection Circuit 1

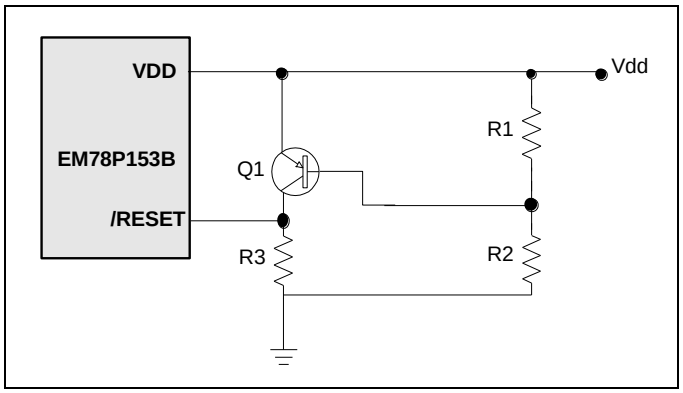


Figure 5-11b Residue Voltage Protection Circuit 2

NOTE

Circuits should be designed to ensure that the voltage of the /RESET pin is larger than V_{IH} (min).

5.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instructions "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2, 6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

A) Modify one instruction cycle to consist of four oscillator periods.

B) "JMP," "CALL," "RET," "RETL," "RETI," or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case A is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low; and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case A, the internal clock source to TCC should be CLK = FOSC/4, instead of FOSC/2.

Moreover, the Instruction Set also offers the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

■ Instruction Set Table:

The following symbols are used in the Instruction Set table:

"**R**" *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

"**b**" *Bit field designator that selects the value for the bit located in the register **R** and which affects the operation.*

"**k**" *8 or 10-bit constant or literal value*

Mnemonic		Operation	Status Affected
NOP		No Operation	None
DAA		Decimal Adjust A	C
CONTW		A → CONT	None
SLEP		0 → WDT, Stop oscillator	T, P
WDTC		0 → WDT	T, P
IOW	R	A → IOCR	None*
ENI		Enable Interrupt	None
DISI		Disable Interrupt	None
RET		[Top of Stack] → PC	None
RETI		[Top of Stack] → PC, Enable Interrupt	None
CONTR		CONT → A	None
IOR	R	IOCR → A	None*
MOV	R, A	A → R	None
CLRA		0 → A	Z
CLR	R	0 → R	Z
SUB	A, R	R - A → A	Z, C, DC
SUB	R, A	R - A → R	Z, C, DC
DECA	R	R - 1 → A	Z
DEC	R	R - 1 → R	Z
OR	A, R	A ∨ R → A	Z
OR	R, A	A ∨ R → R	Z
AND	A, R	A & R → A	Z
AND	R, A	A & R → R	Z
XOR	A, R	A ⊕ R → A	Z
XOR	R, A	A ⊕ R → R	Z
ADD	A, R	A + R → A	Z, C, DC
ADD	R, A	A + R → R	Z, C, DC
MOV	A, R	R → A	Z
MOV	R, R	R → R	Z

** This instruction is applicable to IOC5~IOC6, IOCB ~ IOCF only.*

(Continuation)

Mnemonic		Operation	Status Affected
COMA	R	/R → A	Z
COM	R	/R → R	Z
INCA	R	R + 1 → A	Z
INC	R	R + 1 → R	Z
DJZA	R	R - 1 → A, skip if zero	None
DJZ	R	R - 1 → R, skip if zero	None
RRCA	R	R(n) → A(n - 1), R(0) → C, C → A(7)	C
RRC	R	R(n) → R(n – 1), R(0) → C, C → R(7)	C
RLCA	R	R(n) → A(n + 1), R(7) → C, C → A(0)	C
RLC	R	R(n) → R(n + 1), R(7) → C, C → R(0)	C
SWAPA	R	R(0 - 3) → A(4 - 7), R(4 - 7) → A(0 - 3)	None
SWAP	R	R(0 - 3) ↔ R(4 - 7)	None
JZA	R	R + 1 → A, skip if zero	None
JZ	R	R + 1 → R, skip if zero	None
BC	R, b	0 → R(b)	None*
BS	R, b	1 → R(b)	None**
JBC	R, b	if R(b) = 0, skip	None
JBS	R, b	if R(b) = 1, skip	None
CALL	k	PC + 1 → [SP], (Page, k) → PC	None
JMP	k	(Page, k) → PC	None
MOV	A, k	k → A	None
OR	A, k	A ∨ k → A	Z
AND	A, k	A & k → A	Z
XOR	A, k	A ⊕ k → A	Z
RETL	k	k → A, [Top of Stack] → PC	None
SUB	A, k	k - A → A	Z, C,DC
INT		PC + 1 → [SP], 001H → PC	None
ADD	A, k	k + A → A	Z, C, DC

* *This instruction is not recommended for RF operation.*

** *This instruction cannot operate under RF.*

6 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	V_{SS} - 0.3V	to	V_{DD} + 0.5V
Output voltage	V_{SS} - 0.3V	to	V_{DD} + 0.5V
Working Voltage	2.3V	to	5.5V
Working Frequency	DC	to	20 MHz

NOTE

These parameters are theoretical values only and have not been tested or verified.

7 Electrical Characteristics

7.1 DC Characteristics

■ **TA = 25°C, VDD = 5V, VSS = 0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 2.3V	Two cycles with two clocks	DC	–	4.0	MHz
	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8.0	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20.0	MHz
ERC	ERC: VDD to 5V	R: 5kΩ, C: 39 pF	F±30%	750	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	µA
VIH1	Input High Voltage (VDD = 5V)	Ports 5, 6	2	–	–	V
VIL1	Input Low Voltage (VDD = 5V)	Ports 5, 6	–	–	0.8	V
VIHT1	Input High Threshold Voltage (VDD = 5V)	/RESET, TCC (Schmitt trigger)	2	–	VDD+0.3	V
VILT1	Input Low Threshold Voltage (VDD = 5V)	/RESET, TCC (Schmitt trigger)	VSS-0.3	–	0.8	V
VIHX1	Clock Input High Voltage (VDD = 5V)	OSCI	2.5	–	VDD+0.3	V
VILX1	Clock Input Low Voltage (VDD = 5V)	OSCI	VSS-0.3	–	1.0	V
VIH2	Input High Voltage (VDD = 3V)	Ports 5, 6	1.5	–	VDD+0.3	V
VIL2	Input Low Voltage (VDD = 3V)	Ports 5, 6	VSS-0.3	–	0.4	V
VIHT2	Input High Threshold Voltage (VDD = 3V)	/RESET, TCC (Schmitt trigger)	1.5	–	VDD+0.3	V
VILT2	Input Low Threshold Voltage (VDD = 3V)	/RESET, TCC (Schmitt trigger)	VSS-0.3	–	0.4	V

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIHX2	Clock Input High Voltage (VDD = 3V)	OSCI	1.5	–	VDD+0.3	V
VILX2	Clock Input Low Voltage (VDD = 3V)	OSCI	VSS-0.3	–	0.6	V
IOH	High Drive Current (Ports 5 and 6)	VOH = 2.4V	-12	-17		mA
IOL	Low Sink Current (Ports 5 and 6)	VOL = 0.4V	10.5	15		mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	-37.5	-57.5	-77.5	µA
IPD	Pull-down current	Pull-down active, Input pin at VDD	17.5	37.5	57.5	µA
LVR1	Low voltage reset Level 1 (2.7V)	Ta = 25°C	2.41	2.7	2.99	V
		Ta = -40°C ~ 85°C	2.15	2.7	3.29	V
LVR2	Low voltage reset Level 2 (3.5V)	Ta = 25°C	3.1	3.5	3.9	V
		Ta = -40°C ~ 85°C	2.73	3.5	4.27	V
LVR3	Low voltage reset Level 3 (4.0V)	Ta = 25°C	3.55	4.0	4.44	V
		Ta = -40°C ~ 85°C	3.16	4.0	4.82	V
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	0.5	1	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	5	10	µA
ICC1	Operating supply current at two clocks (VDD = 3V)	/RESET = 'High', F_{OSC} = 32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	15	30	µA
ICC2	Operating supply current at two clocks (VDD = 3V)	/RESET = 'High', F_{OSC} = 32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	19	35	µA
ICC3	Operating supply current at two clocks (VDD = 5.0V)	/RESET = 'High', F_{OSC} = 4MHz (Crystal type, CLKS="0"), Output pin floating	–	–	2.0	mA
ICC4	Operating supply current at two clocks (VDD = 5.0V)	/RESET = 'High', F_{OSC} = 10MHz (Crystal type, CLKS="0"), Output pin floating	–	–	4.0	mA

NOTE

These parameters are theoretical values only and have not been tested or verified.

7.2 AC Characteristics

■ **TA = 25°C, VDD = 5V, VSS = 0V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	-	DC	ns
		RC type	500	-	DC	ns
Ttcc	TCC input period	-	(Tins + 20) / N [5]	-	-	ns
Tdrh	Device reset hold time	TXAL, SUT1, SUT0=1, 1	23.5 - 30%	23.5	23.5 + 30%	ms
Trst	/RESET pulse width	-	2000	-	-	ns
Twdt1 [1]	Watchdog timer period	SUT1, SUT0=1,1	23.5 - 30%	23.5	23.5 + 30%	ms
Twdt2 [2]	Watchdog timer period	SUT1, SUT0=1,0	5.9 - 30%	5.9	5.9 + 30%	ms
Twdt3 [3]	Watchdog timer period	SUT1, SUT0=0,1	376 - 30%	376	376 + 30%	ms
Twdt4 [4]	Watchdog timer period	SUT1, SUT0=0,0	94 - 30%	94	94 + 30%	ms
Tset	Input pin setup time	-	-	0	-	ns
Thold	Input pin hold time	-	-	20	-	ns
Tdelay	Output pin delay time	C_{LOAD} = 20pF	-	50	-	ns

[1] *Twdt1: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (23.5 ms).*

[2] *Twdt2: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (5.9 ms).*

[3] *Twdt3: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (376 ms).*

[4] *Twdt4: The Option word (SUT1, SUT0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (94 ms).*

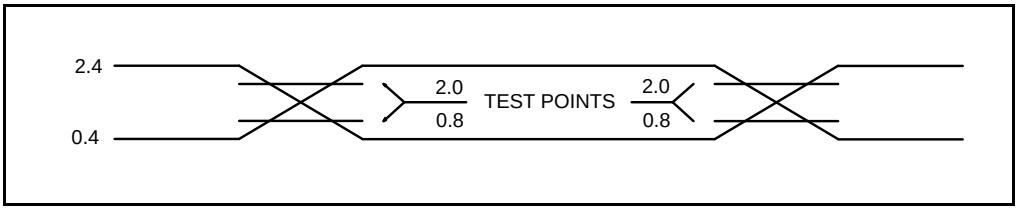
[5] *N = Selected prescaler ratio*

NOTE

- *These parameters are theoretical values only and have not been tested or verified.*
- *The Watchdog Timer duration is determined by Option Code (Bit 6, Bit 5)*

8 Timing Diagrams

■ AC Test Input/Output Waveform



Note: *AC Testing: Input are driven at 2.4V for logic "**1**," and 0.4V for logic "**0**"*
*Timing measurements are made at 2.0V for logic "**1**," and 0.8V for logic "**0**"*

Figure 8-1a AC Test Input/Output Waveform Timing Diagram

■ Reset Timing (CLK = "0")

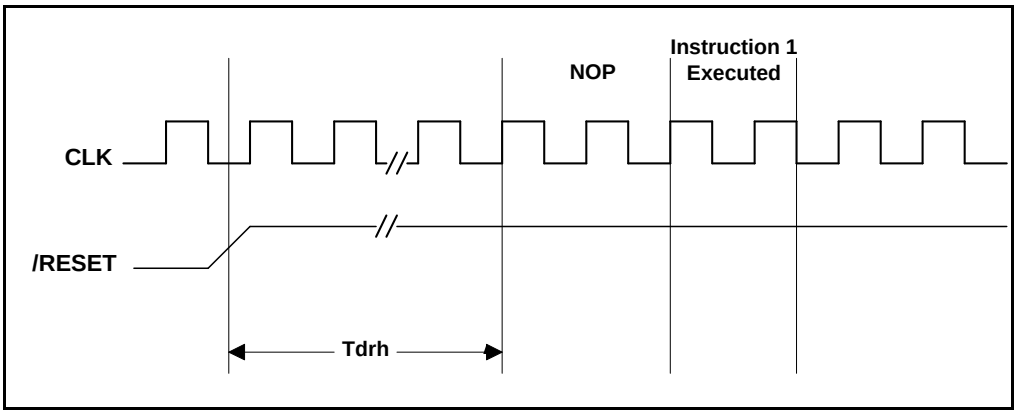


Figure 8-1b Reset Timing Diagram

■ TCC Input Timing (CLKS = "0")

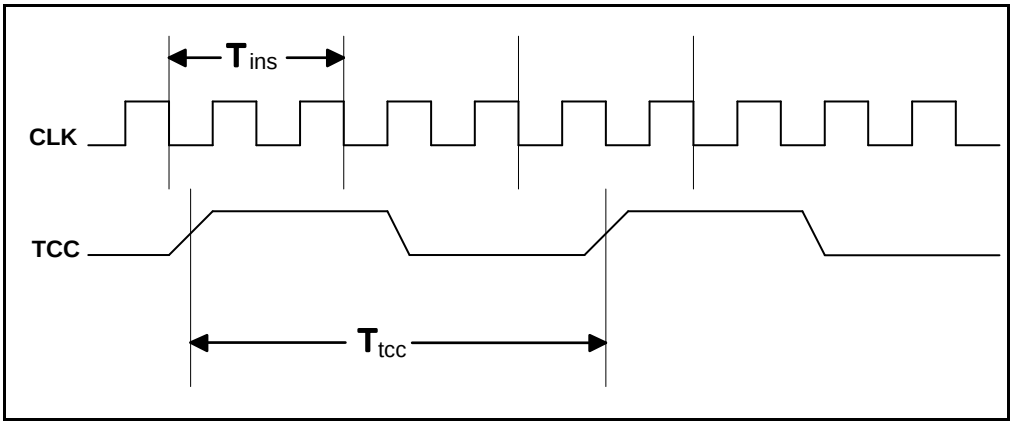
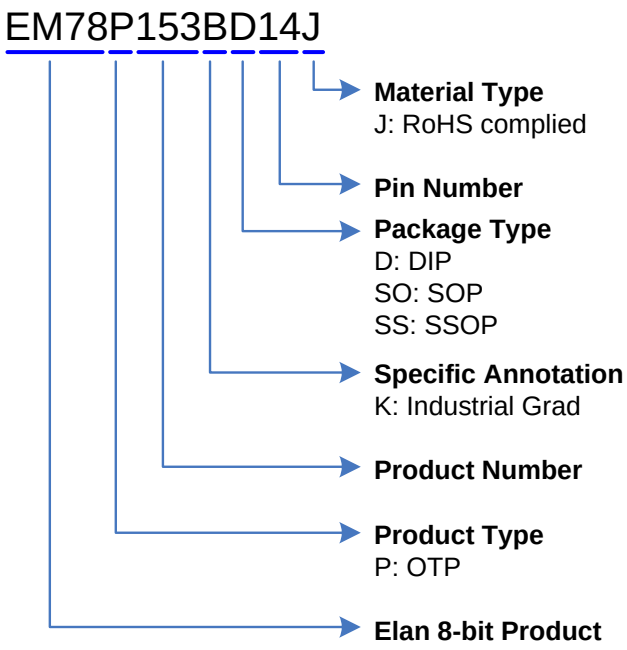


Figure 8-1c TCC Input Timing Diagram

APPENDIX

A Ordering and Manufacturing Information

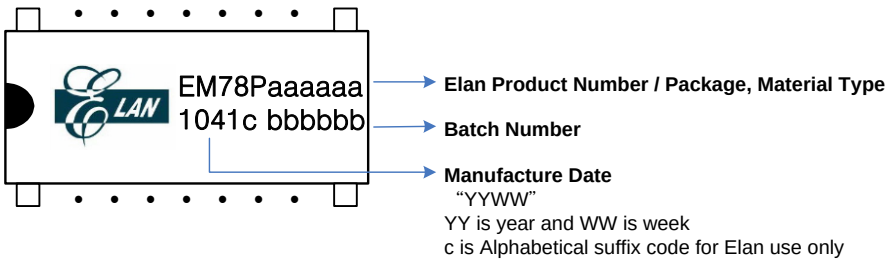


For example:

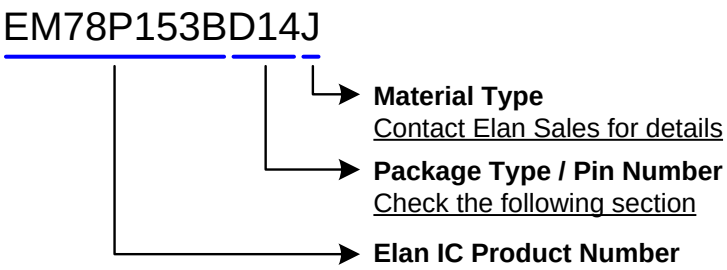
EM78P153BSO14J

is EM78P153B with OTP program memory, product, in 14-pin SOP 300mil package with RoHS complied

IC Mark



Ordering Code



B Package Type

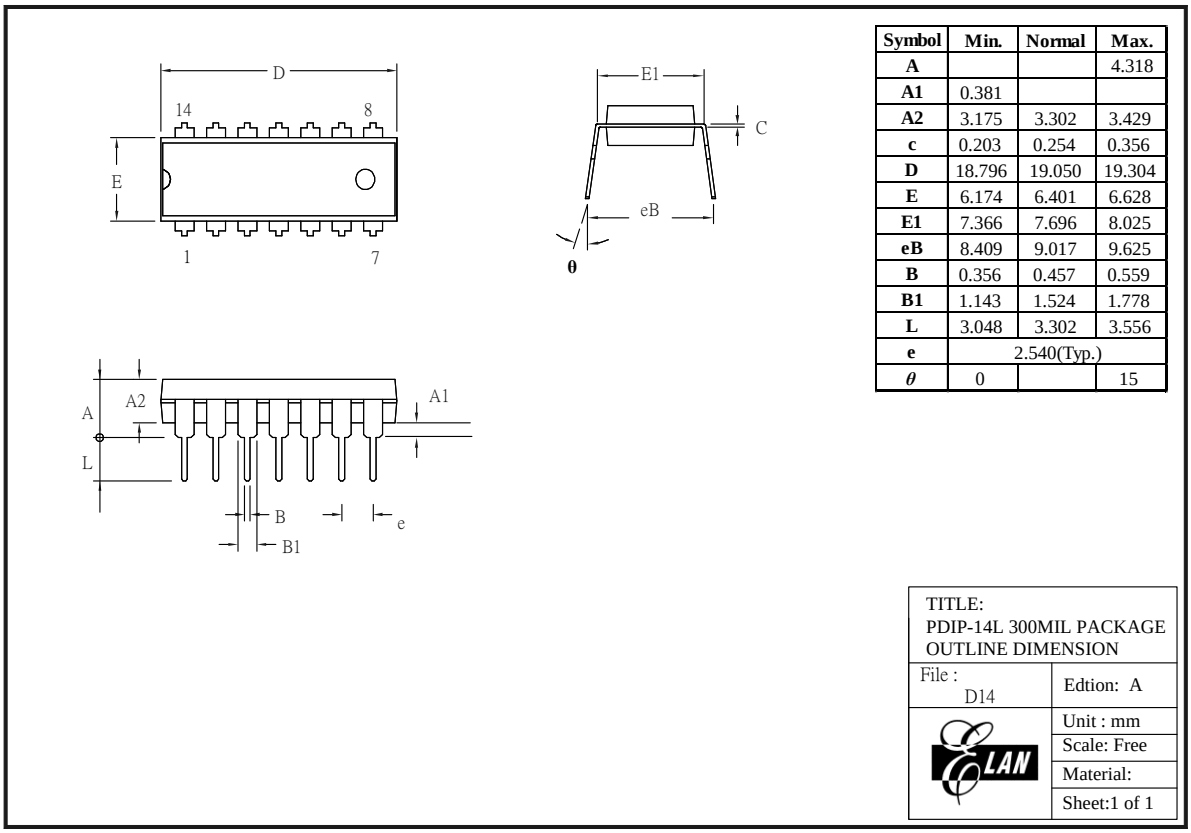
OTP MCU	Package Type	Pin Count	Package Size
EM78P153BD14	DIP	14	300 mil
EM78P153BSO14	SOP	14	150 mil
EM78P153BSS10	SSOP	10	150 mil

These are Green products that comply with RoHS specifications.

Part No.	EM78P153BD14J, EM78P153BSO14J, EM78P153BSS10J
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	> 50%

C Package Information

■ 14-Lead Plastic Dual in-line (DIP) — 300 mil

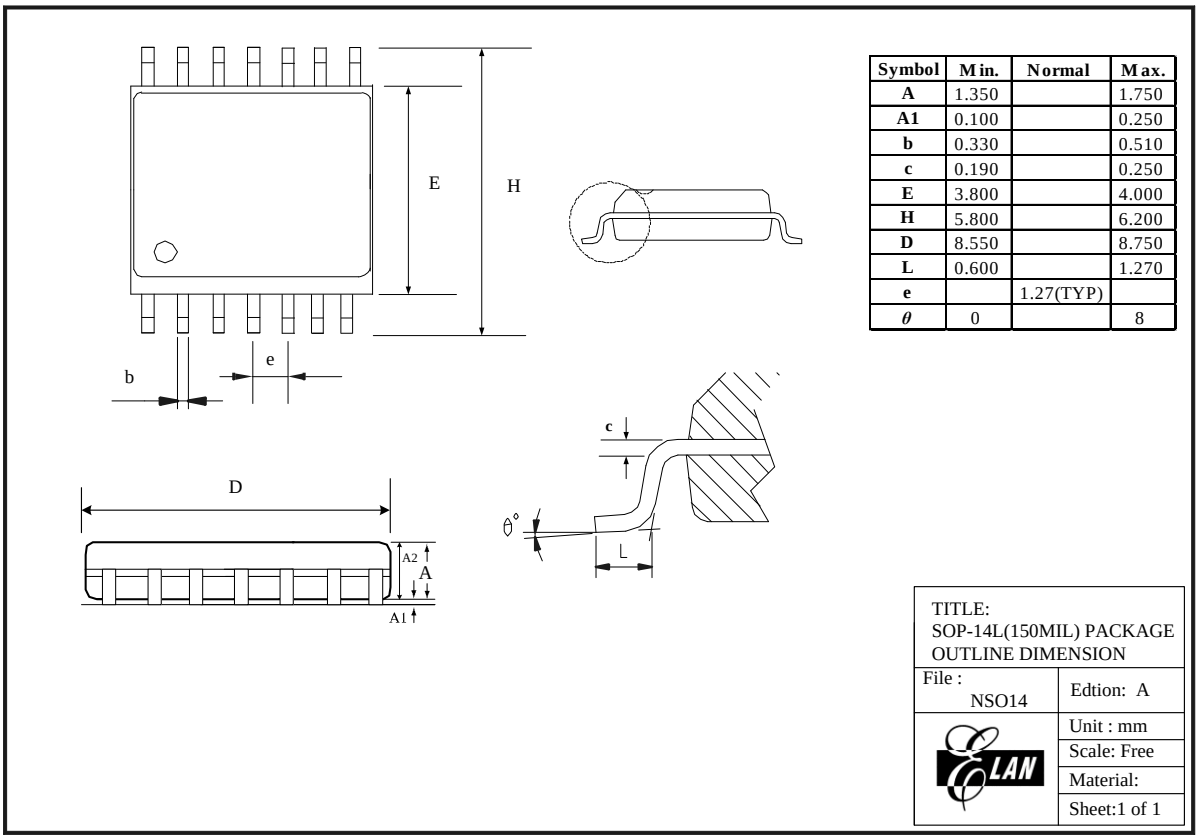


Symbol	Min.	Normal	Max.
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(Typ.)		
θ	0		15

TITLE: PDIP-14L 300MIL PACKAGE OUTLINE DIMENSION	
File : D14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1a EM78P153B 14-Lead DIP Package Type

■ **14-Lead Small-Outline Package (SOP) — 150 mil**

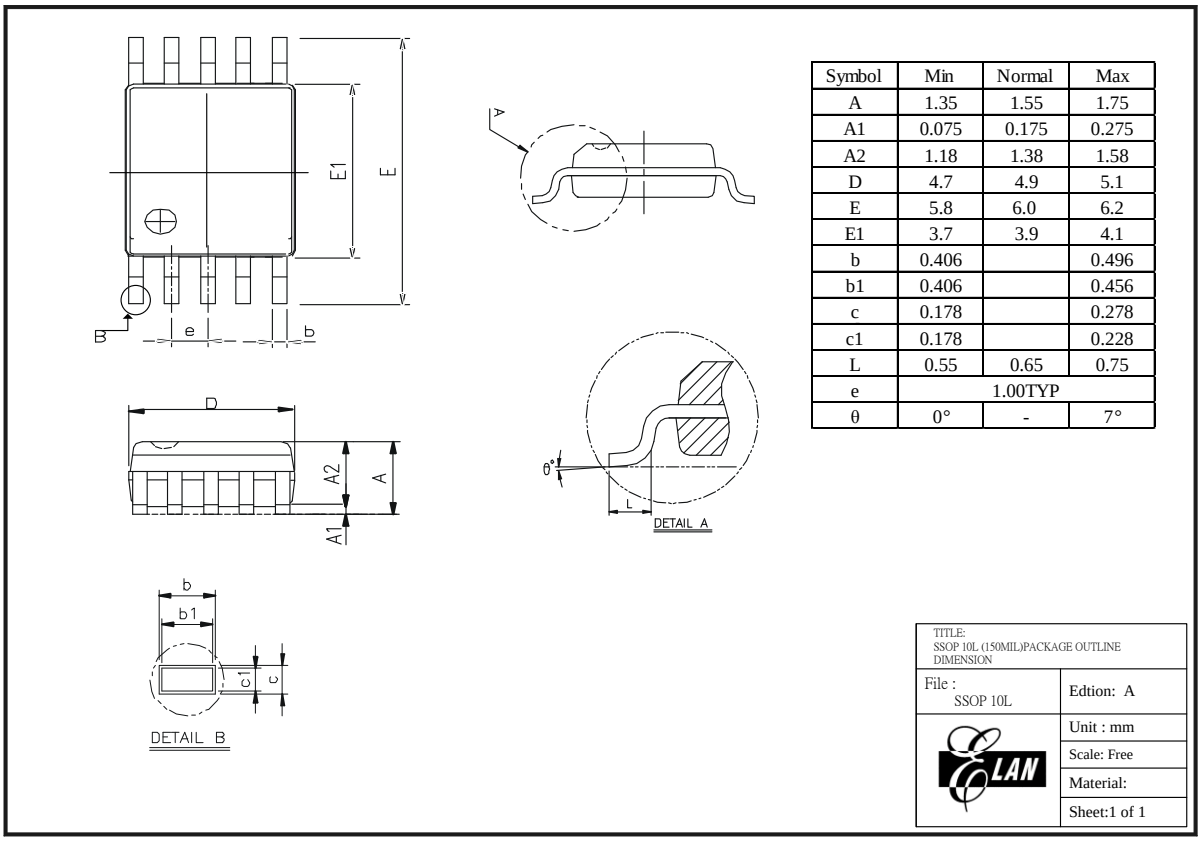


Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e		1.27(TYP)	
θ	0		8

TITLE: SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION	
File : NSO14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1b EM78P153B 14-Lead DIP/SOP Package Type

■ 10-Lead Shrink Small-Outline Package (SSOP) — 150 mil



Symbol	Min	Normal	Max
A	1.35	1.55	1.75
A1	0.075	0.175	0.275
A2	1.18	1.38	1.58
D	4.7	4.9	5.1
E	5.8	6.0	6.2
E1	3.7	3.9	4.1
b	0.406		0.496
b1	0.406		0.456
c	0.178		0.278
c1	0.178		0.228
L	0.55	0.65	0.75
e		1.00TYP	
θ	0°	-	7°

Figure C-1c EM78P153B 10-Lead SSOP Package Type