NEC

MOS FIELD EFFECT TRANSISTOR

μPA1850

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μPA1850 is a switching device which can be driven directly by a 2.5-V power source.

The μPA1850 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

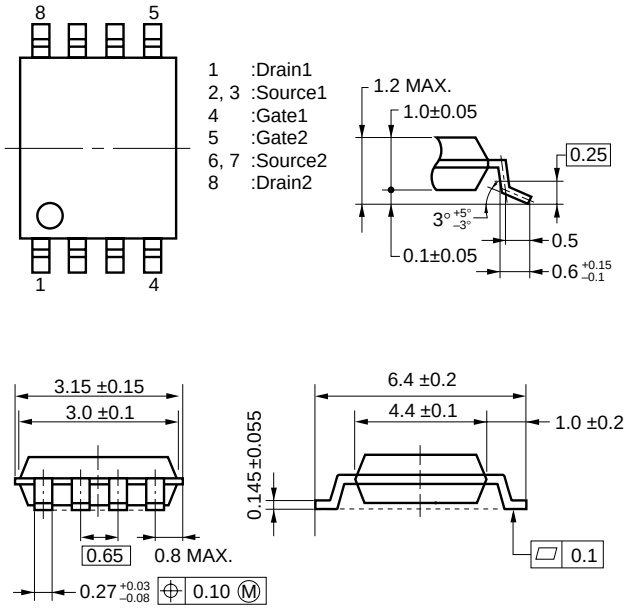
FEATURES

- Can be driven by a 2.5-V power source
- Low on-state resistance
  $R_{DS(on)1}$ = 115 mΩ MAX. (V_{GS} = –4.5 V, I_D = –1.5 A)
  $R_{DS(on)2}$ = 130 mΩ MAX. (V_{GS} = –4.0 V, I_D = –1.5 A)
  $R_{DS(on)3}$ = 200 mΩ MAX. (V_{GS} = –2.5 V, I_D = –1.5 A)
- Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1850GR-9JG	Power TSSOP8

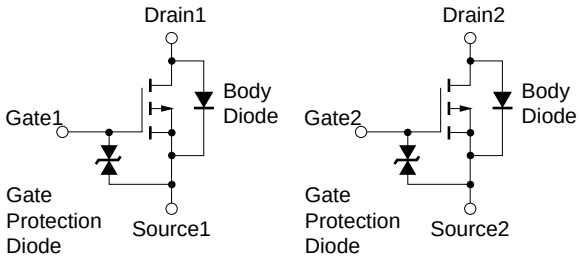
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	–12	V
Gate to Source Voltage	V_{GSS}	–10/+5	V
Drain Current (DC)	$I_{D(DC)}$	∓2.5	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓10	A
Total Power Dissipation Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 5000 mm^2 x 1.1 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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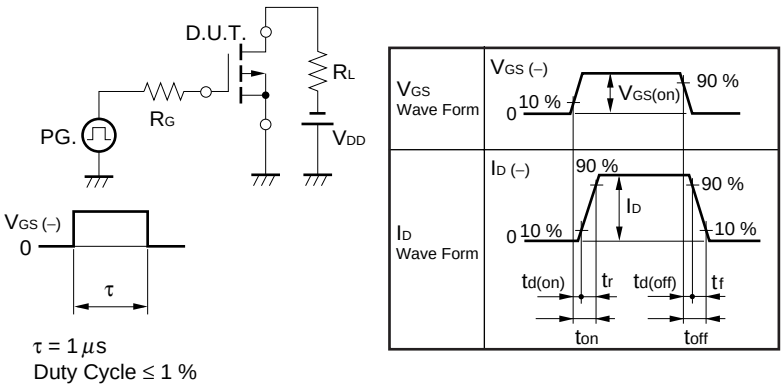
The mark ★ shows major revised points.

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ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

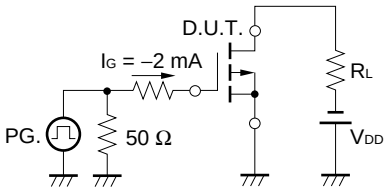
	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Drain Cut-off Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			–10	μA
	Gate Leakage Current	I_{GSS}	V_{GS} = ∓ 10 V, V_{DS} = 0 V			∓ 10	μA
★	Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–0.5	–1.0	–1.5	V
★	Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –1.5 A	2.0	5.0		S
	Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –4.5 V, I_D = –1.5 A		80	115	mΩ
		$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –1.5 A		85	130	mΩ
		$R_{DS(on)3}$	V_{GS} = –2.5 V, I_D = –1.5 A		127	200	mΩ
	Input Capacitance	C_{iss}	V_{DS} = –10 V		260		pF
	Output Capacitance	C_{oss}	V_{GS} = 0 V		300		pF
	Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		45		pF
	Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –10 V		120		ns
	Rise Time	t_r	I_D = –1.5 A		420		ns
	Turn-off Delay Time	$t_{d(off)}$	$V_{GS(on)}$ = –4.0 V		520		ns
	Fall Time	t_f	R_G = 10 Ω		430		ns
	Total Gate Charge	Q_G	V_{DD} = –10 V		12		nC
	Gate to Source Charge	Q_{GS}	I_D = –2.5 A		2		nC
	Gate to Drain Charge	Q_{GD}	V_{GS} = –4.0 V		5		nC
	Diode Forward Voltage	$V_{F(S-D)}$	I_F = 2.5 A, V_{GS} = 0 V		0.80		V
★	Reverse Recovery Time	t_{rr}	I_F = 2.5 A, V_{GS} = 0 V		750		ns
★	Reverse Recovery Charge	Q_{rr}	di/dt = 10 A/μs		950		nC

TEST CIRCUIT 1 SWITCHING TIME



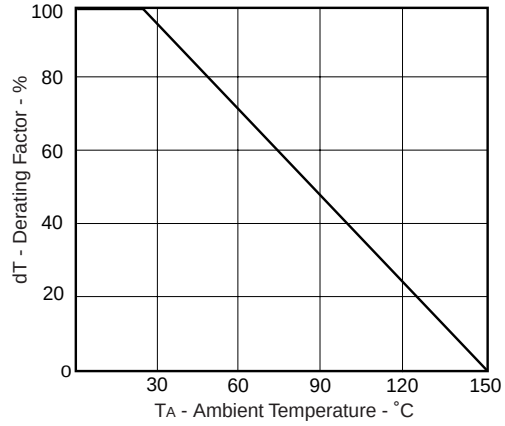
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

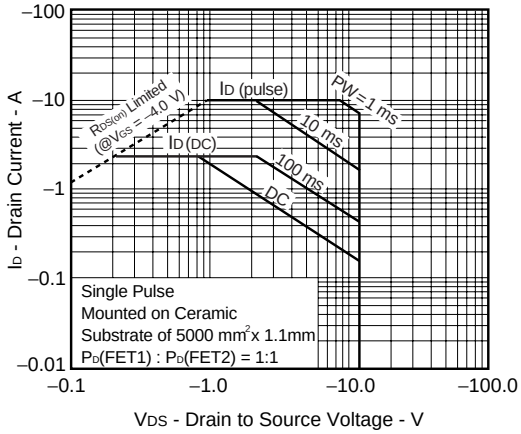


★ TYPICAL CHARACTERISTICS (T_A = 25°C)

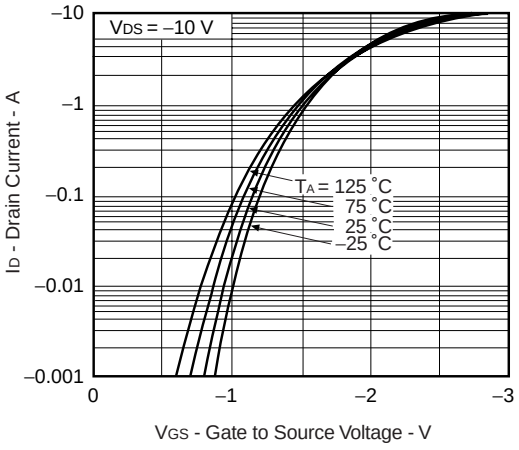
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



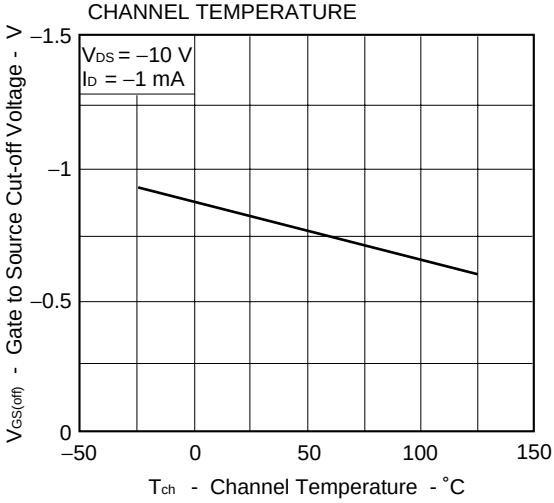
FORWARD BIAS SAFE OPERATING AREA



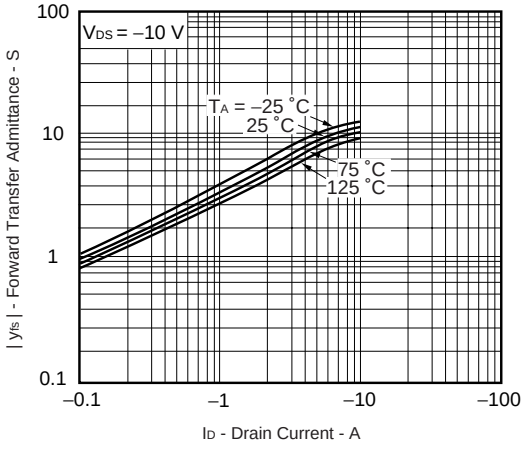
TRANSFER CHARACTERISTICS



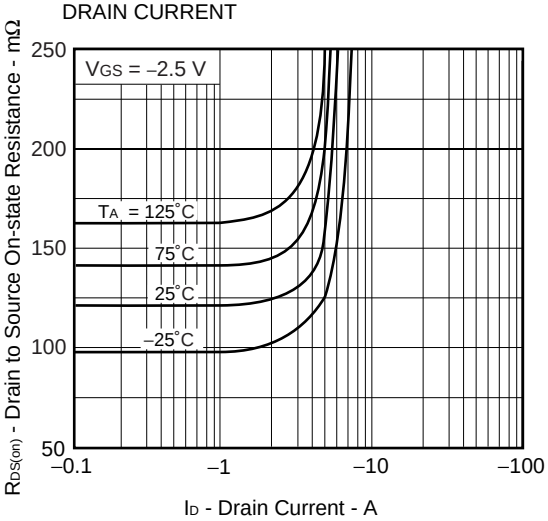
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



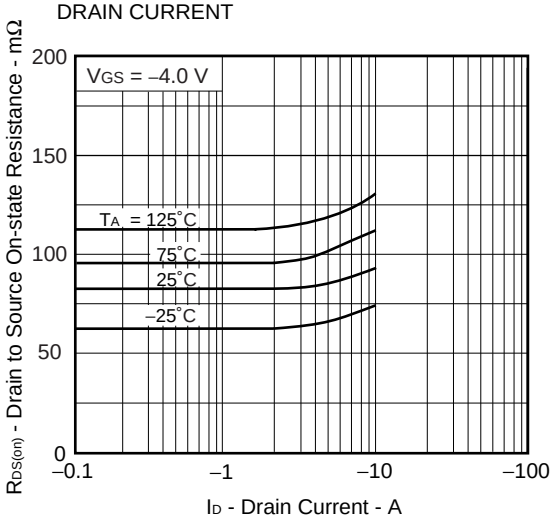
FORWARD TRANSFER ADMMITTANCE vs. DRAIN CURRENT



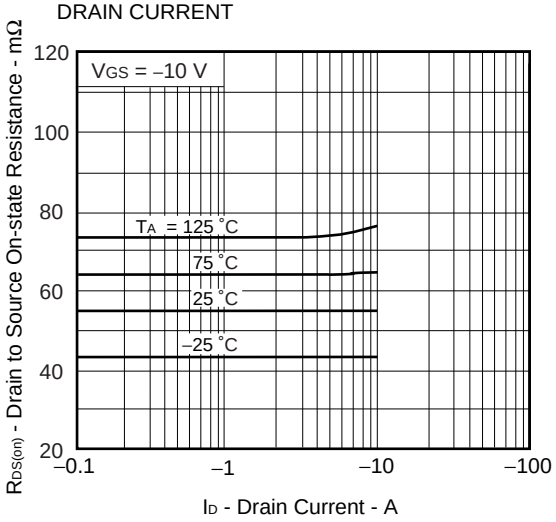
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



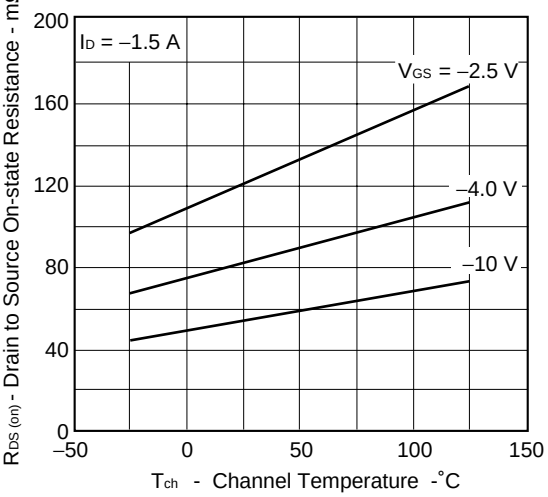
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



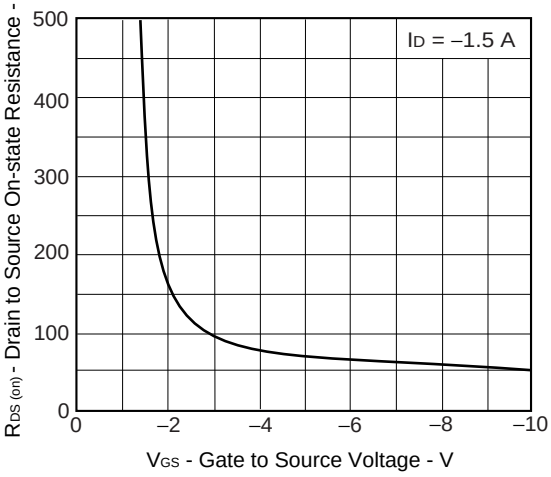
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



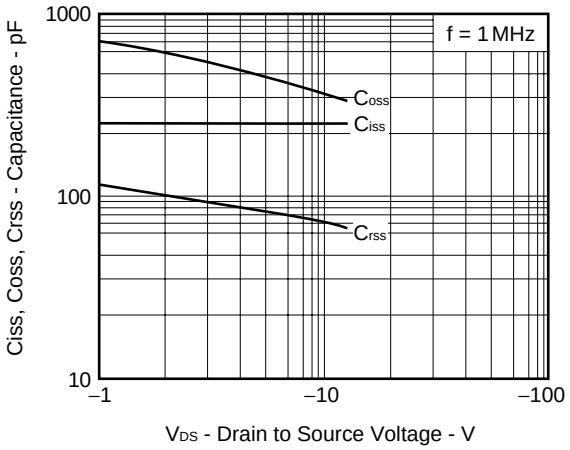
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



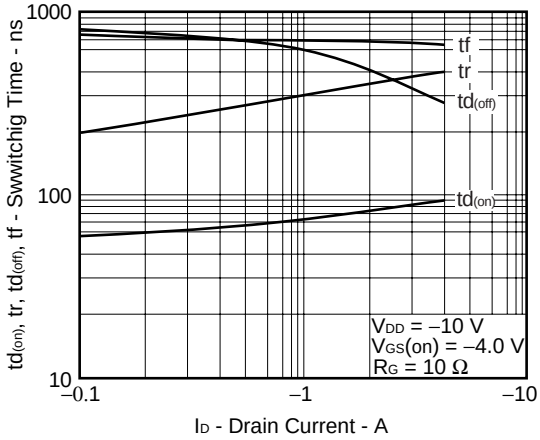
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



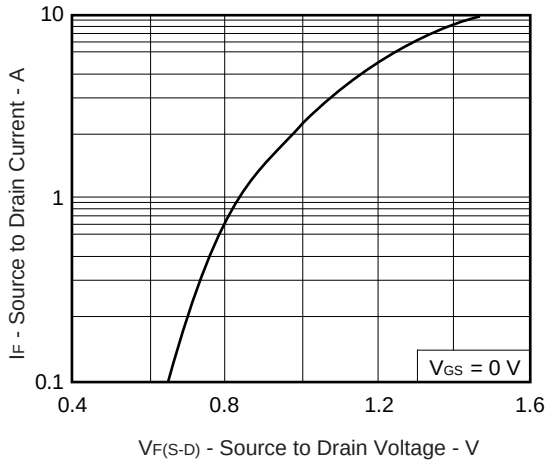
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



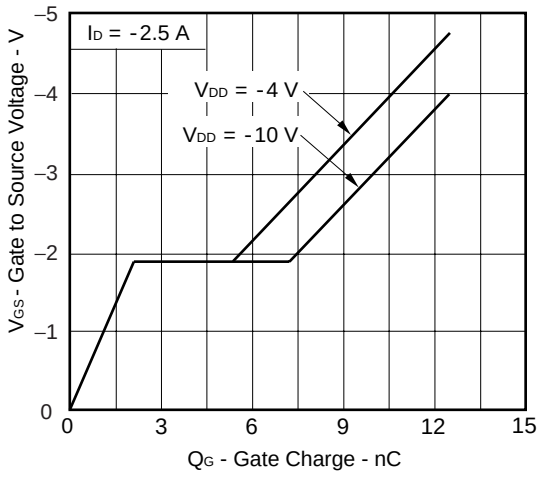
SWITCHING CHARACTERISTICS



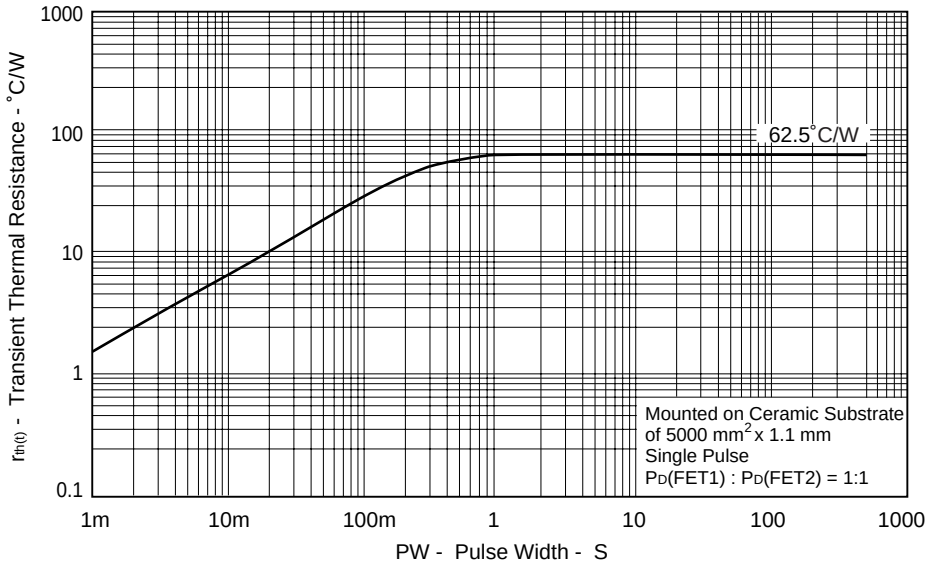
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



[MEMO]

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