Smart Photoflash Capacitor Charger with IGBT Driver

General Description

The RT9591 is a highly integrated photoflash charging solution in digital and film cameras. It is targeted for applications that use either two AA batteries or a single lithium-ion battery.

The RT9591 integrates a constant current controller for charging high voltage photoflash capacitor quickly and efficiently, an IGBT driver for igniting flash tube, and a voltage detector. Only a few external components are used to reduce PCB space and cost.

RT9591 is available in VQFN-16L 3x3 package.

Ordering Information

RT9591 □ □

- Package Type
  QV : VQFN-16L 3x3 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

Features

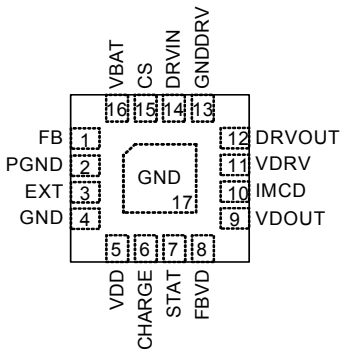
- **1.8V to 6.5V Battery Input Voltage Range**
- **Charges Any Size Photoflash Capacitor**
- **Adjustable Input Current**
- **Uses Standard Transformers**
- **Adjustable Output Voltage**
- **Charge Complete Indicator**
- **Built-in IGBT Driver for IGBT Application**
- **Built-in Voltage Detector**
- **16-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Digital Still Camera
- Film Camera Flash Unit
- Camera Phone Flash

Pin Configurations

(TOP VIEW)



VQFN-16L 3x3

Typical Application Circuit

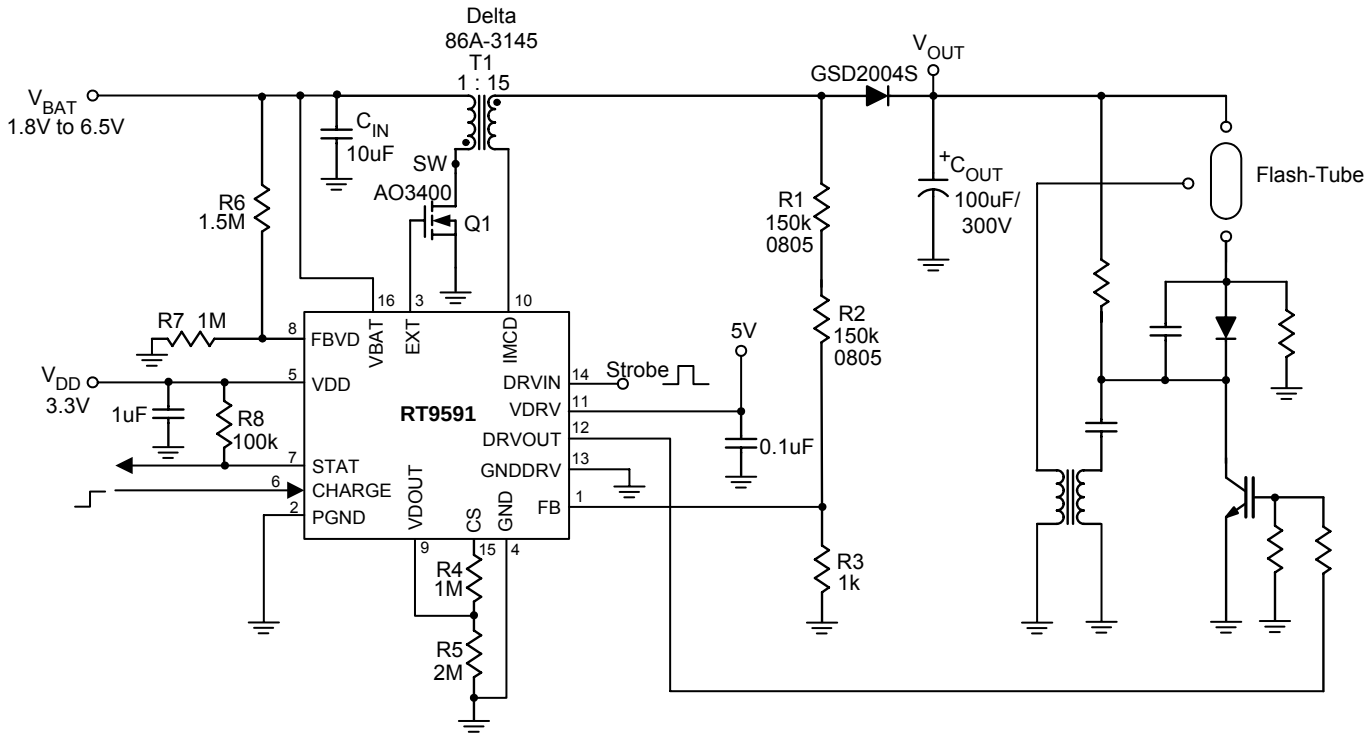


Figure 1. Photoflash Capacitor Charger Application

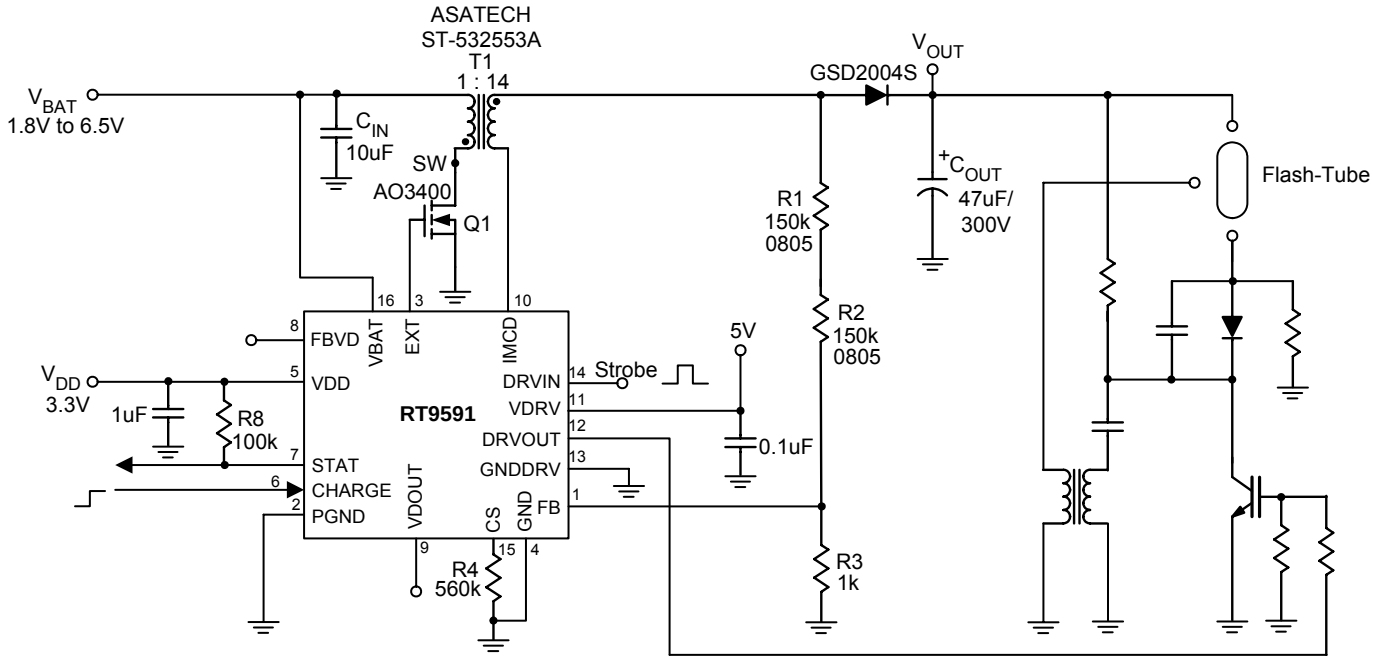


Figure 2. Photoflash Capacitor Charger Application for Low Charging Current

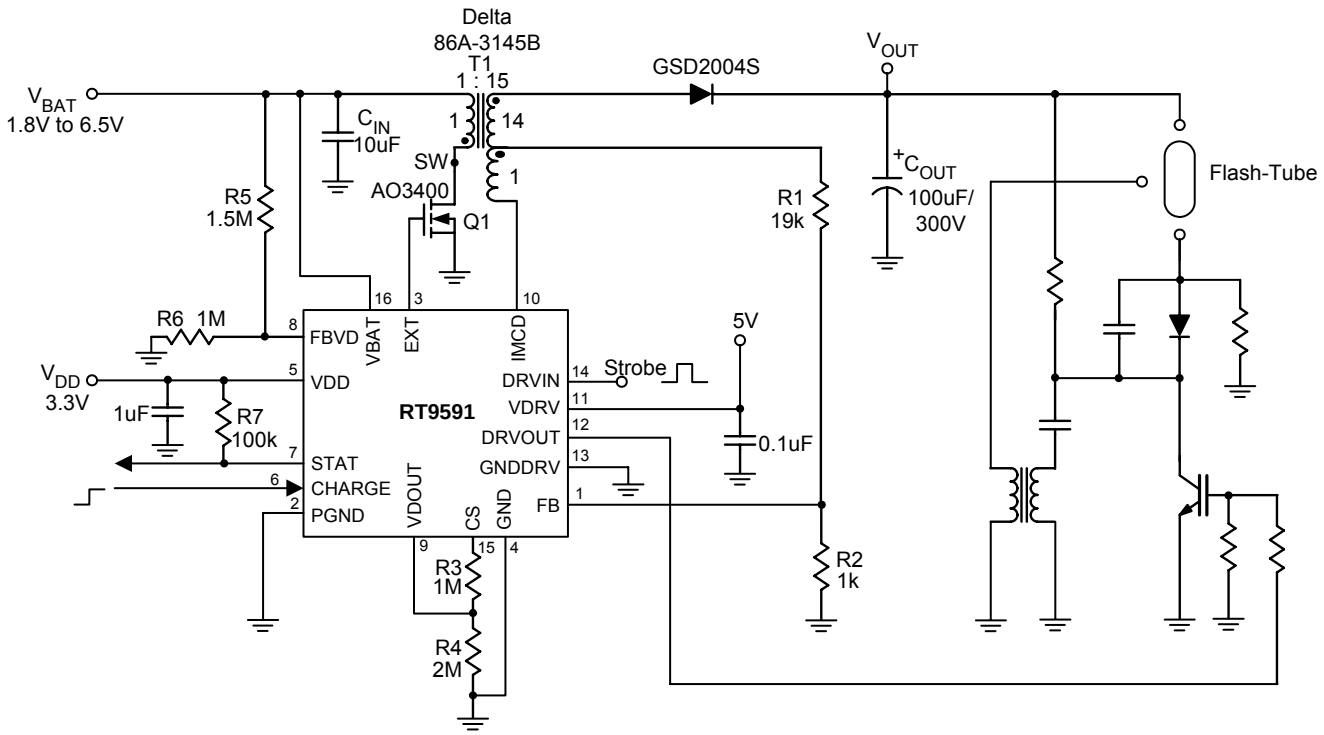
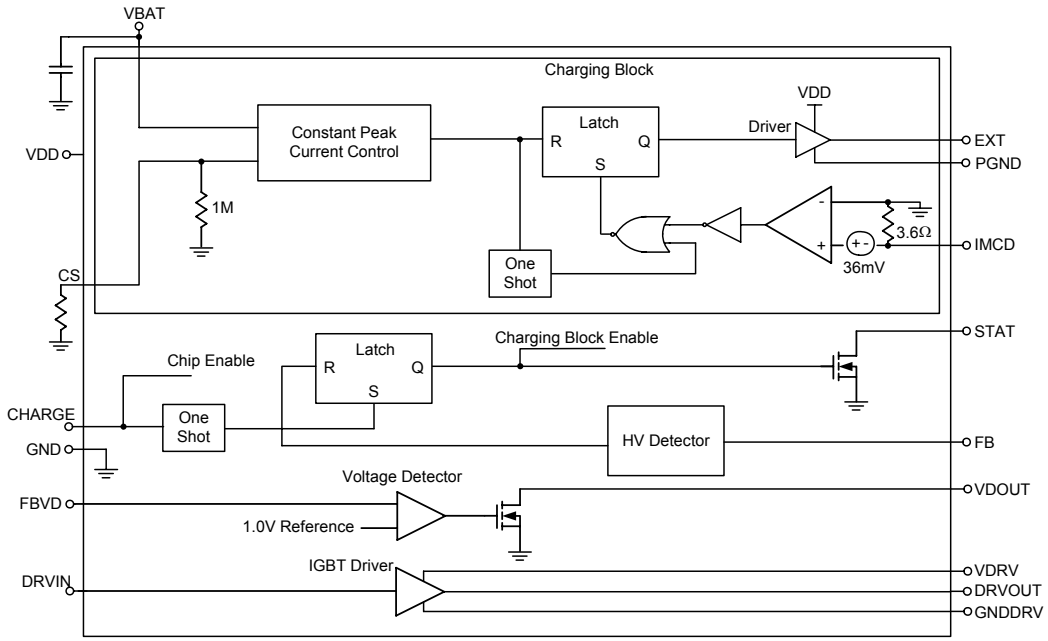


Figure 3. Photoflash Capacitor Charger Application with Center-Tap Transformer

Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Feedback Voltage Pin.
2	PGND	Power Ground.
3	EXT	Output Pin for driving external NMOS on Flyback topology.
4	GND	Ground.
5	VDD	Power Input Pin of RT9591.
6	CHARGE	Charge Enable Pin, the charge function is executed when CHARGE pin is set from Low to High. And the RT9591 gets into Shutdown mode when CHARGE pin is set to Low.
7	STAT	Charge Status Output. Open Drain output. When target output voltage is reached, N-MOSFET turns off. This pin needs a pull up resistor.
8	FBVD	Voltage Detector Feedback Pin.
9	VDOUT	Voltage Detector Output Pin, Open Drain output.
10	IMCD	Minimum Current Detection Pin.
11	VDRV	IGBT Driver Power Pin.
12	DRVOUT	IGBT Driver Output Pin.
13	GNDDRV	IGBT Driver Ground Pin.
14	DRVIN	IGBT Driver Input Pin.
15	CS	Input Current Setting Pin.
16	VBAT	Battery Supply Voltage Input Pin.
Exposed Pad (17)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD}, V_{BAT}, V_{DRV} ---------- –0.3V to 7V
- EXT ---------- –0.3V to (V_{DD} + 0.3V)
- DRVOUT ---------- –0.3V to (V_{DRV} + 0.3V)
- IMCD ---------- –0.5V to 7V
- Other I/O Pin Voltage ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-16L 3x3 ---------- 1.67W
- Package Thermal Resistance
  VQFN-16L 3x3, θ_{JA} ---------- 60°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Electrical Characteristics

(V_{DD} = 3.3V, V_{VDRV} = 3.3V, T_A = 25°C, Unless Otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{DD} Operating Voltage	V_{DD}		1.8	--	6.5	V
V_{DD} UVLO Rising			--	1.6	1.8	V
V_{DD} UVLO Hysteresis			30	60	--	mV
V_{BAT} Voltage Rising	$V_{BAT(MIN)}$		--	1.6	1.81	V
V_{BAT} UVLO Hysteresis			190	300	--	mV
FB Voltage	V_{FB}		0.96	0.98	1	V
Line Regulation	$\lvert \Delta V_{FB} \rvert$	1.8V< V_{DD} < 3V	--	--	8	mV
		3V < V_{DD} < 6.5V	--	--	7	mV
Switch-Off Current	$I_{VDD_SW_OFF}$	V_{FB} = 1.1V	--	1	10	uA
Switch-Off Current	$I_{VBAT_SW_OFF}$	V_{FB} = 1.1V	--	0.01	1	uA
Shutdown Current I_{VDD}+I_{VBAT}	I_{OFF}	Charge pin = 0V, V_{DD} = 4.5V	--	0.01	1	uA
Minimum Current on Secondary Side	I_{IMCD}		8	10	12	mA
EXT On Resistance to V_{DD}		V_{DD} = 3.3V	--	3	6	Ω
EXT On Resistance to GND		V_{DD} = 3.3V	--	3	6	Ω
STAT On Resistance to GND		V_{DD} = 3.3V	--	16	19	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Charge Input High Threshold			--	0.7	1.3	V
Charge Input Low Threshold			0.4	0.7	--	V
Minimum Off Time		V_{BAT} = 1.8V to 6.5V V_{DD} = 1.8V to 6.5V	280	360	430	ns
IGBT Driver						
IGBT Driver Supply Voltage	V_{VDRV}		2.0	--	5.5	V
DRVIN Input High Threshold			--	1.0	1.3	V
DRVIN Input Low Threshold			0.4	1	--	V
DRVOUT On Resistance to V_{VDRV}		V_{VDRV} = 3.3V	--	6	8	Ω
DRVOUT On Resistance to GND		V_{VDRV} = 3.3V	--	6	8	Ω
Propagation Delay (Rising)		V_{BAT} = 1.8V to 6.5V V_{DD} = 1.8V to 6.5V V_{VDRV} = 2V to 6.5V(Note 3)	--	--	20	ns
Propagation Delay (Falling)			--	--	200	ns
Voltage Detector						
Voltage Detector Trip (Falling)	V_{FBVD}	FBVD Falling	0.96	0.99	1.02	V
VDOUT On Resistance to GND		V_{DD} = 3.3V	--	16	19	Ω

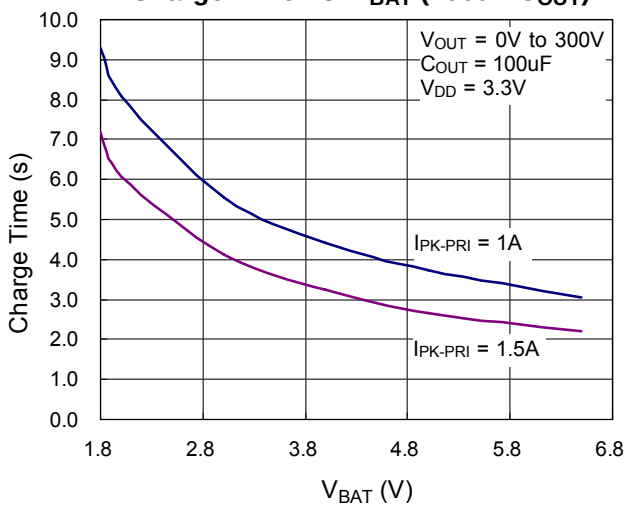
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

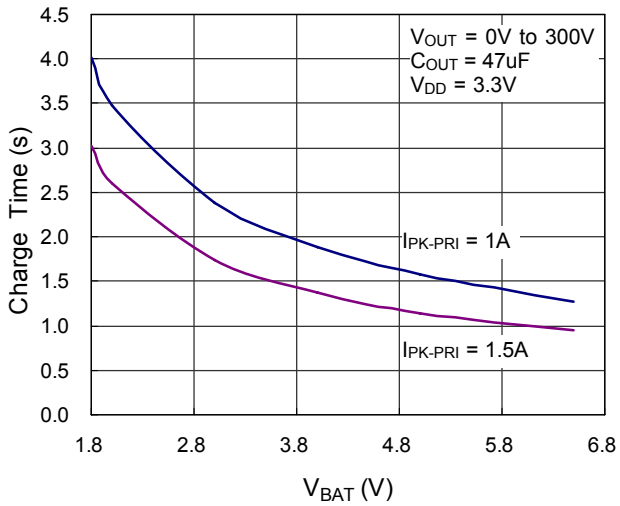
Note 3. VDRV is the IGBT gate driving power. Therefore, setting VDRV voltage must consider IGBT gate threshold voltage, and its driving capability.

Typical Operating Characteristics

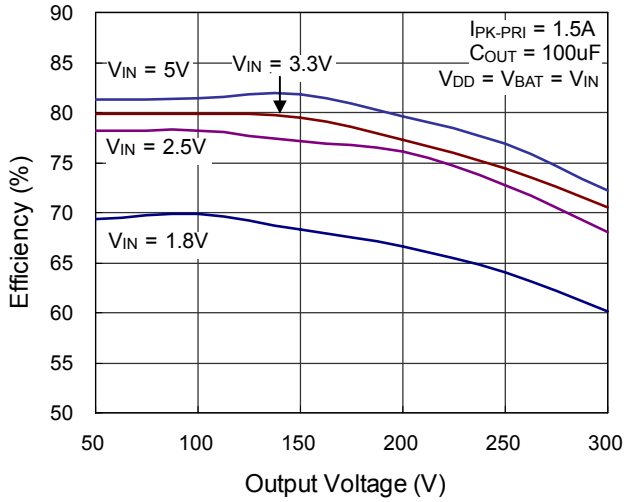
Charge Time vs. V_{BAT} (100uF C_{OUT})



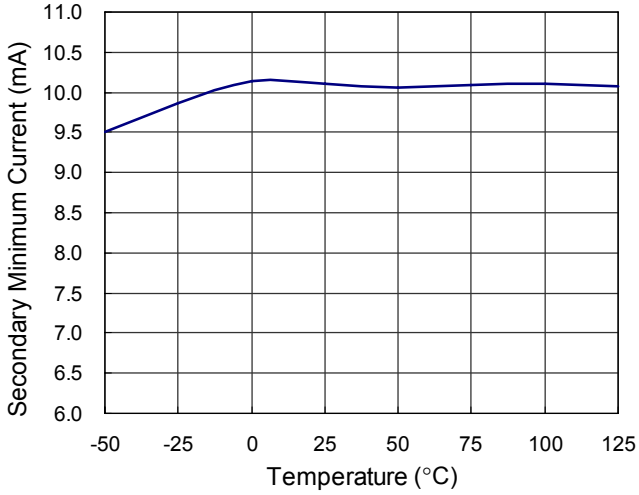
Charge Time vs. V_{BAT} (47uF C_{OUT})



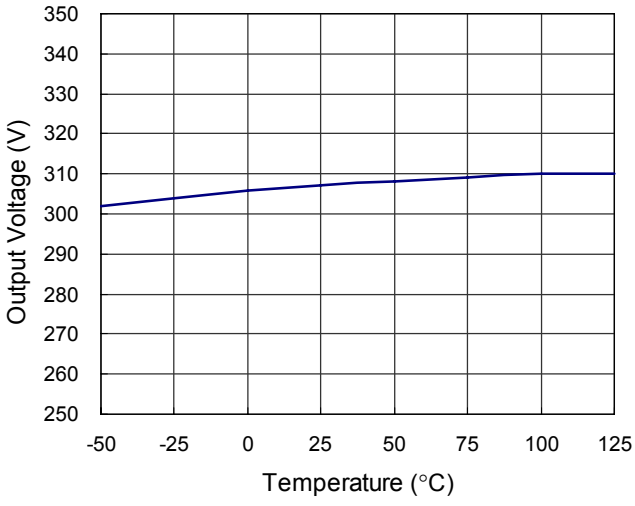
Efficiency vs. Output Voltage



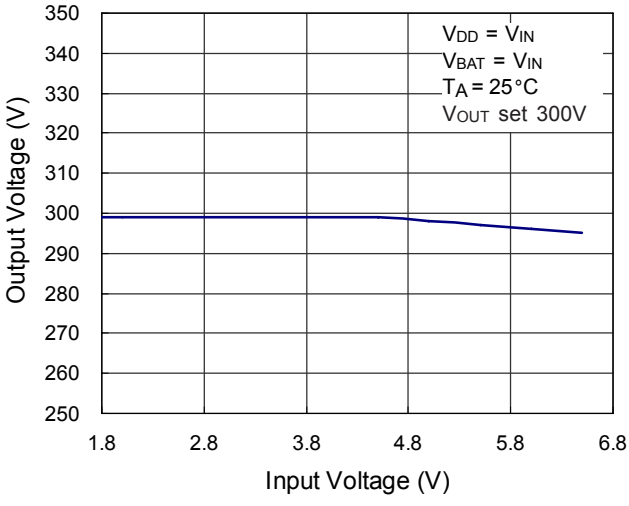
Secondary Minimum Current vs. Temperature



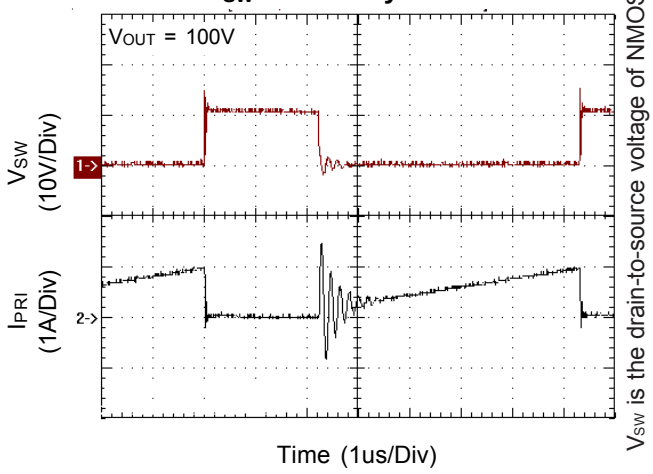
Output Voltage vs. Temperature



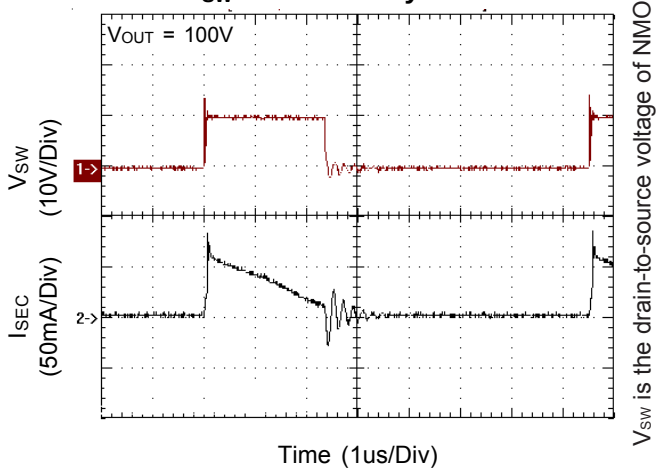
Output Voltage vs. Input Voltage



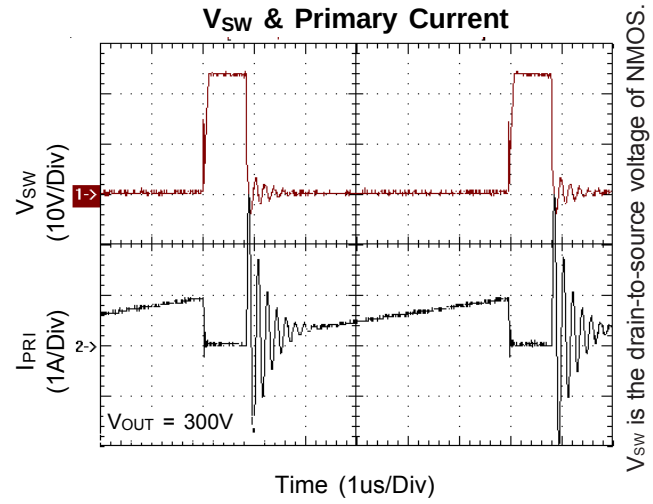
V_{SW} & Primary Current



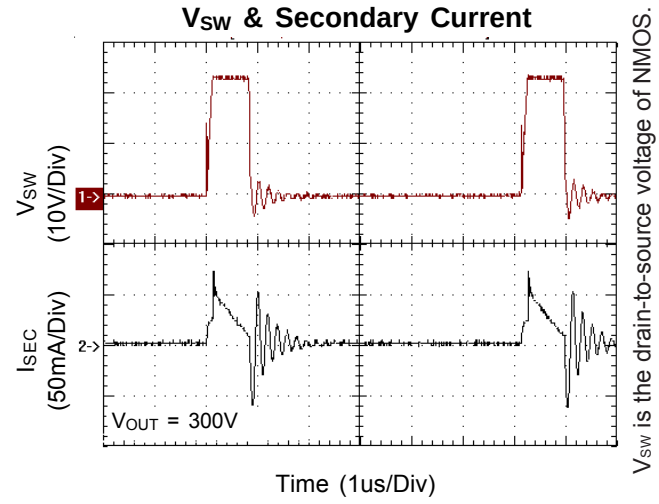
V_{SW} & Secondary Current



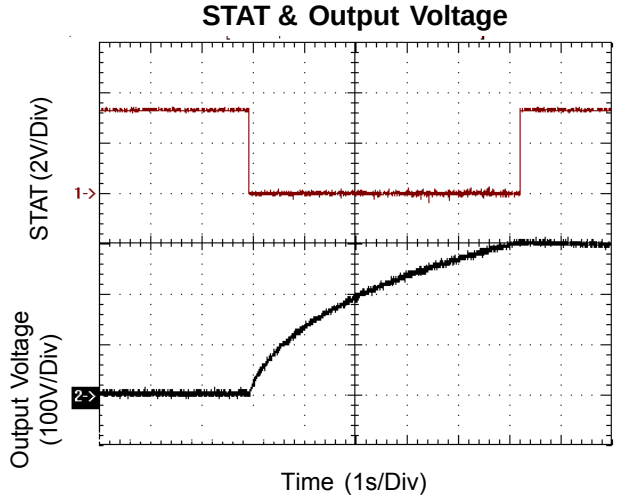
V_{SW} & Primary Current



V_{SW} & Secondary Current



STAT & Output Voltage



Application Information

The RT9591 integrates a constant peak current controller for charging photoflash capacitor, an IGBT driver for igniting flash tube, and a voltage detector with open drain output to provide a cost effective photoflash solution.

The photoflash capacitor charger uses constant primary peak current and constant secondary valley current control to efficiently charge the photoflash capacitor. Pulling the CHARGE pin high initiates the charging cycle. During ON time, the primary current ramps up linearly according to V_{BAT} and primary inductance. A resistor connecting to CS pin determines the ON time of primary NMOS and consequently the primary peak current.

During the OFF time, the energy stored in the flyback transformer is boosted to the output capacitor. The secondary current decreases linearly at a rate determined by the secondary inductance and the output voltage (neglecting the voltage drop of the diode). The secondary current is monitored by the IMCD pin. When the secondary current drops below 10mA, ON time starts again. The charging cycle repeats itself and charges the output voltage.

The output voltage is sensed by a voltage divider connecting to the anode of the rectifying diode. When the output voltage reaches the desired voltage set by resistor divider, the HV detector will terminate the charging cycle, disable the charging block and pull high the STAT pin. The voltage sensing path is cut off when charging completed to minimize the output voltage decay. Both the CHARGE and STAT pins can be easily interfaced to a microprocessor in a digital system.

Transformer

The flyback transformer should be appropriately designed to ensure effective and efficient operation.

1. Turns Ratio

The turns ratio of transformer (N) should be high enough so that the absolute maximum voltage rating for the NMOS drain to source voltage is not exceeded. Choose the minimum turns ratio according to the following formula:

$$N_{(MIN)} \geq \frac{V_{OUT}}{V_{DS(MAX)} - V_{BAT}}$$

V_{OUT}: Target Output Voltage

$V_{DS(MAX)}$: Maximum drain to source voltage of NMOS

2. Primary Inductance

Each switching cycle, energy transferred to the output capacitor is proportional to the primary inductance for a constant primary current. The higher the primary inductance is, the higher the charging efficiency will be. Besides, the RT9591 has a 360ns minimum-off time for correct current and voltage sensing. To ensure the charger operating in continuous conduction mode, the primary inductance should be high enough according to the following formula:

$$L_{PRI} \geq \frac{430 \times 10^{-9} \times V_{OUT}}{N \times I_{PK-PRI}}$$

V_{OUT}: Target Output Voltage

N : Transformer turns ratio

I_{PK-PRI} : Primary peak current

430×10^{-9} : The maximum value of minimum-off time.

3. Leakage Inductance and Parasitic Capacitance

The leakage inductance of the transformer results in the first spike voltage when NMOS turns off as shown in Figure 4. The spike voltage is proportional to the leakage inductance. The spike voltage must not exceed the dynamic rating of the NMOS drain to source voltage. Well-coupling winding design decreases the leakage inductance. However, well-coupling winding design usually results in large parasitic capacitance between windings. The parasitic capacitance consequently causes initial current swing when NMOS turns on as shown in Figure 5. Trade off is necessary between leakage inductance and parasitic capacitance.

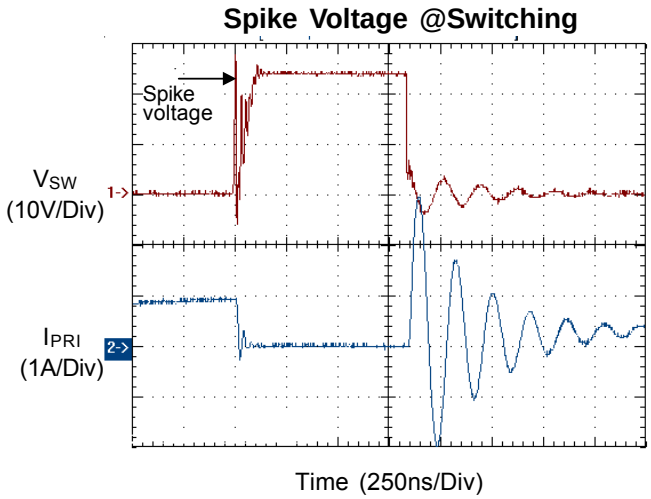


Figure 4

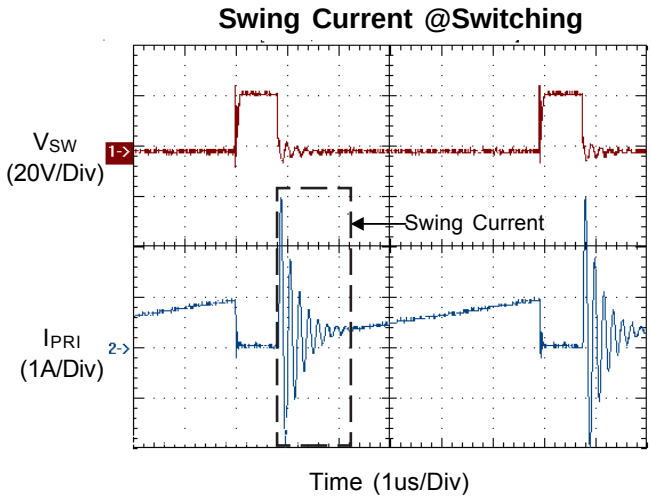


Figure 5

4. Transformer Secondary Capacitance

Any capacitance on the secondary can severely affect the efficiency. A small secondary capacitance is multiplied by N^2 when reflected to the primary side. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary side capacitance should be minimized.

Rectifying Diode

The rectifying diode should be with short reverse recovery time (small parasitic capacitance). Large parasitic capacitance increases switching loss and lowers charging efficiency. In addition, the peak reverse voltage and peak current of the diode should be sufficient.

The peak reverse voltage of the diode is approximately:

$$V_{PK-R} \approx V_{OUT} + (N \times V_{BAT})$$

The peak current of the diode equals primary peak current divide transformer turn ratio as the following equation:

$$I_{PK-SEC} = I_{PK-PRI}/N$$

Note: N is transformer turns ratio.

NMOS

The NMOS is the switching component of the flyback converter. Select adequate drain to source voltage and NMOS turn ON drain current is very important. For the RT9591 typical application circuit,

If V_{OUT} = 300V, V_{BAT} = 6.5V, transformer turn ratio N = 15.

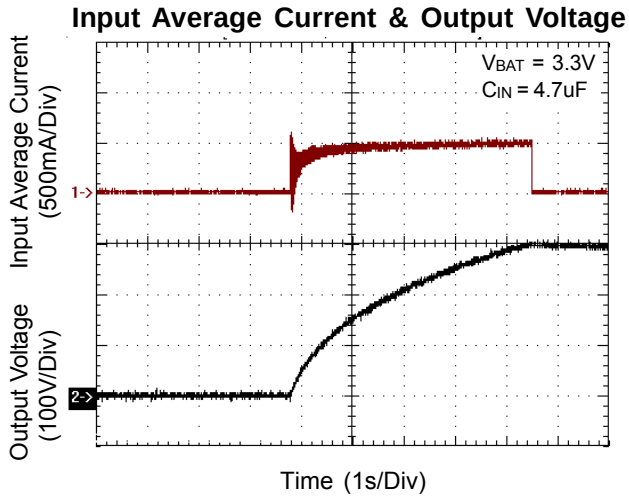
$$V_{DS(MIN)} = 300/15 + 6.5 = 26.5V.$$

The NMOS minimum drain to source voltage should be greater than 26.5V.

In addition, make sure that V_{DD} is higher than $V_{GS(th)}$ (Gate threshold voltage) so as to sufficiently turn on the MOSFET.

Capacitor

X5R ceramic capacitor ≥ 10uF/10V is recommended for input capacitor to well decouple the switching current. Figure 6 and Figure 7 compare the input current waveforms with different input capacitors.



Figuer 6

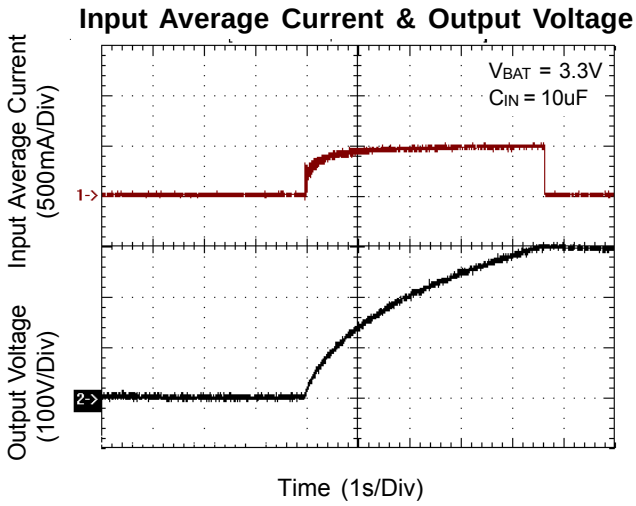


Figure 7

Adjustable Input Current

The RT9591 simply adjusts peak primary current by a resistor R_{CS} connecting to CS pin as shown in Function Block Diagram. R_{CS} paralleled with internal 1MΩ resistor determines the ON time of primary NMOS.

During the ON time, the primary current ramps linearly with a slope = V_{BAT}/L_{PRI}. Consequently, the current setting resister (R_{CS}) could be calculated as:

$$Ra = \frac{(I_{PK-PRI} - 8 \times 10^{-3} \times N) \times L_{PRI}}{30 \times 10^{-12}}$$

$$R_{CS} = \frac{1M \times Ra}{1M - Ra} \ (\Omega)$$

Where I_{PK-PRI} is the primary peak current and N is the turns ratio of transformer.

Users could select appropriate R_{CS} according to the battery capability and required charging time.

Minimum I_{PK-PRI} Limitation

$$\text{The } I_{PK-PRI} \text{ setting must } \geq \frac{430 \times 10^{-9} \times V_{OUT}}{N \times L_{PRI}},$$

where 430×10^{-9} is the maximum value of minimum off time.

If lower I_{PK-PRI} setting limitation is required, you may change transformer to incease N x L_{PRI} product.

Adjustable Output Voltage

The RT9591 senses output voltage by a voltage divider connecting to the anode of the rectifying diode during OFF time. This eliminates power loss at voltage-sensing circuit when charging completed. R3 to (R1+R2) ratio determines the output voltage as shown in the application circuit Figure1. The feedback reference voltage is 0.98V. If V_{OUT} = 300V, in Figure 1 Photoflash Capacitor Charger Application according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + \frac{R1+R2}{R3}), \quad \text{so} \quad \frac{R1+R2}{R3} = 305$$

R3 is recommend 1KΩ; R1 and R2 are used 150KΩ for reducing parasitic capacitance coupling effect of FB pin. R1 and R2 ***MUST*** be greater than 0805 size resister for enduring secondary HV.

Lower Charging Current at Low Battery Voltage

The RT9591 integrates a voltage detector with open drain output. This voltage detector is specially designed for lowering peak primary current and minimizing the impact to battery voltage at low V_{BAT} condition as shown in Figure 8. The voltage detector senses V_{BAT} through a resister divider R6 and R7 and compares it with internal 1V reference voltage. When the sensed voltage is lower than the reference voltage, VDOUT pin goes low and changes the resistance connecting to CS pin and the ON time. For example, if R6 equal 1.5MΩ and R7equal 1MΩ, VDOUT pin change status form open to ground when V_{BAT} voltage under 2.5V. And current setting resister R4 and R5 can set different resistance for different input current when V_{BAT} voltage under detector voltage. Figure 9 shows the lower charging current waveform. When V_{BAT} voltage under 2.5V, the input average current become approximately 600mA to 460mA.

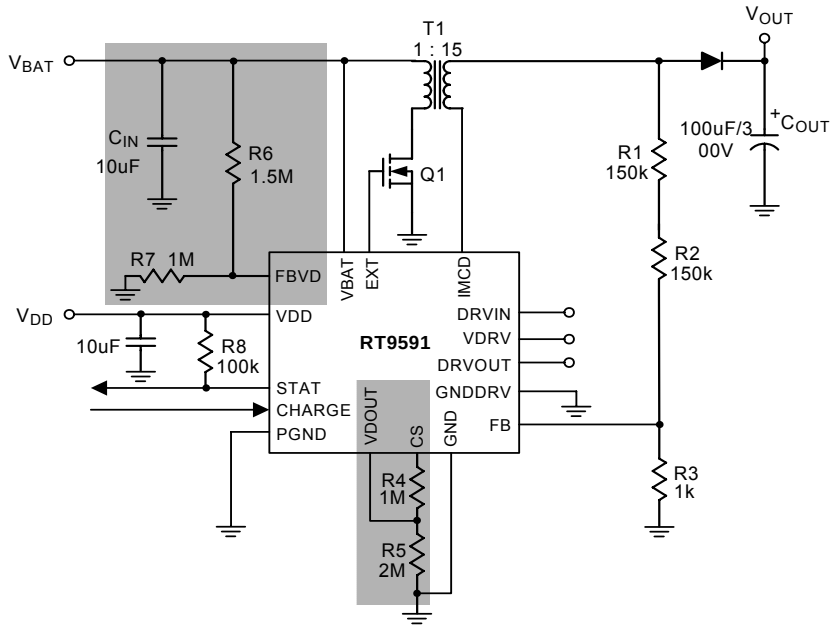


Figure 8. Lower Charging Current Application Circuit

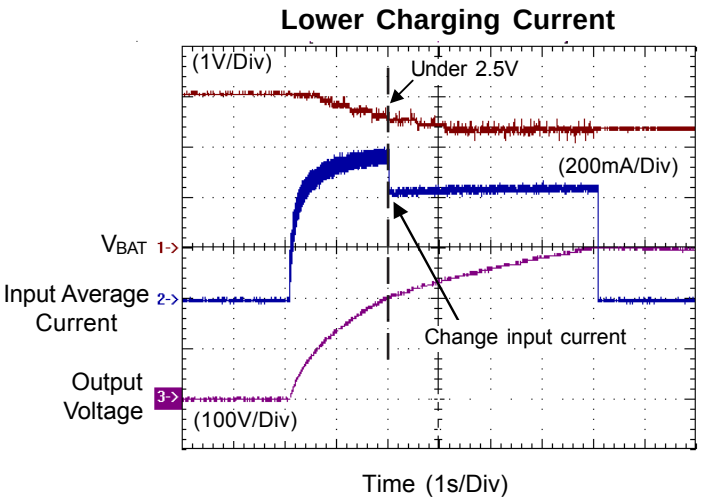


Figure 9

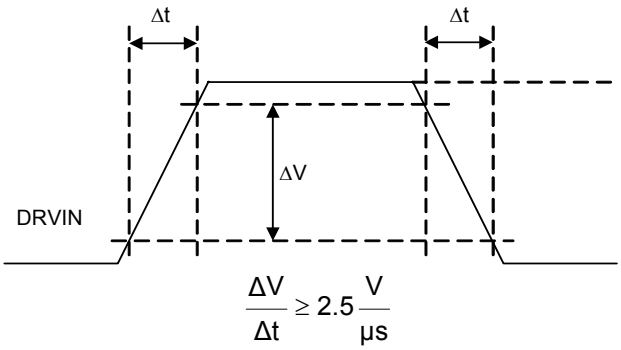


Figure 10. IGBT Driver Input Signal

IGBT Driver Input Signal

The slew rate of IGBT driver input DRVIN should be higher than 2.5V/μs for normally triggering the IGBT as shown in Figure 10.

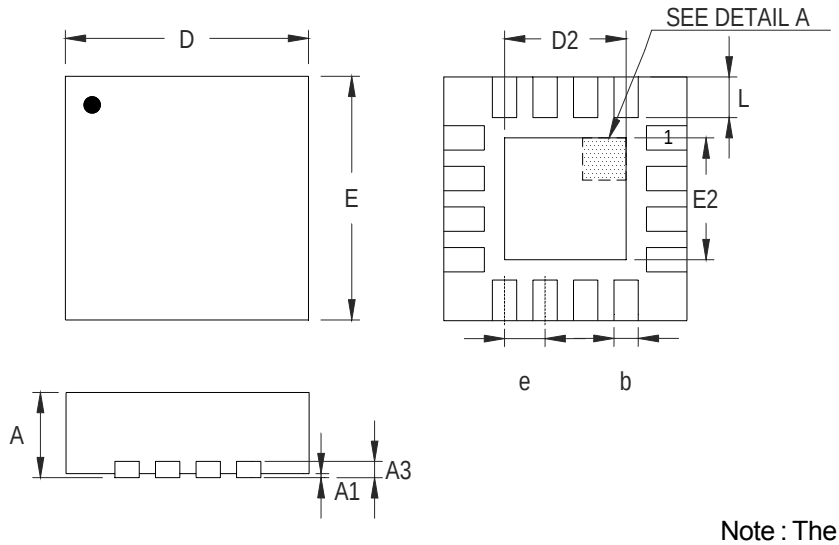
Layout Guide

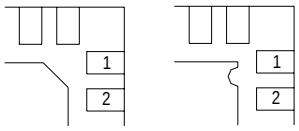
1.Both of primary and the secondary power paths should be as short as possible.

2.Keep FB node area small and far away from nodes with voltage switching to reduce parasitic capacitance coupling effect.

3.The NMOS ground and feedback ground should be connect to V_{BAT} ground for reduce switching noise.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
8F, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com