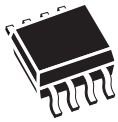
M93S66-125 M93S56-125 M93S46-125

Automotive 4-Kbit, 2-Kbit and 1-Kbit MICROWIRE serial EEPROM with block protection

Datasheet – production data

Features

- Industry standard MICROWIRE™ bus
- Single supply voltage: 2.5 to 5.5 V
- Single organization: by word (x16)
- Programming instructions that work on: word or entire memory
- Self-timed programming cycle with auto-erase
- User-defined write-protected area
- Page Write mode (4 words)
- Ready/$\overline{\text{Busy}}$ signal during programming
- Speed: 2-MHz clock rate, 5 ms write time
- Sequential Read operation
- Enhanced ESD/Latch-up behavior
- More than 1 million Erase/Write cycles
- More than 40-year data retention



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1 Description

The M93S66-125, M93S56-125 and M93S46-125 are a range of 4-Kbit, 2-Kbit, and 1-Kbit serial Electrically Erasable PROgrammable Memory (EEPROM) products. They are collectively referred to as M93Sx6-125.

Figure 1. Logic diagram

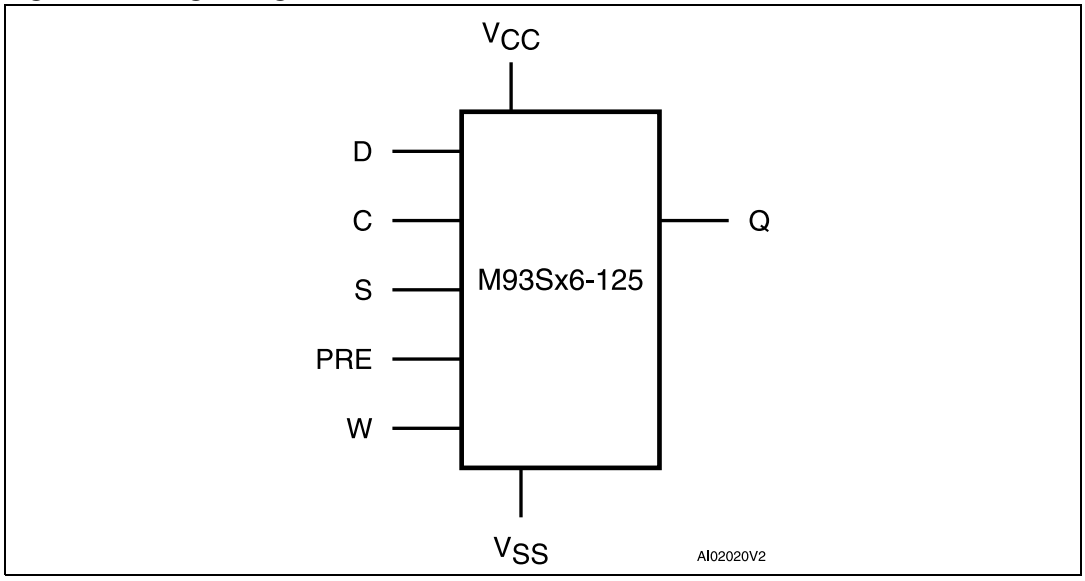


Table 1. Signal names

Signal name	Description
$\overline{S}$	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protection Register Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

The M93Sx6-125 is accessed through a Serial Data Input (D) and Serial Data Output (Q) using the MICROWIRE bus protocol. The memory is divided into 256, 128 and 64 x16-bit words (respectively for M93S66-125, M93S56-125 and M93S46-125).

The M93Sx6-125 is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to set the memory protection. These are summarized in *Table 2* and *Table 3*.

A Read data from memory (READ) instruction loads the address of the first word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the

Chip Select Input ($\overline{S}$) is held High, the M93Sx6-125 can output a sequential stream of data words. In this way, the memory can be read as a data stream from 16 to 4096 bits (for the M93S66-125), or continuously as the address counter automatically rolls over to 00h when the highest address is reached.

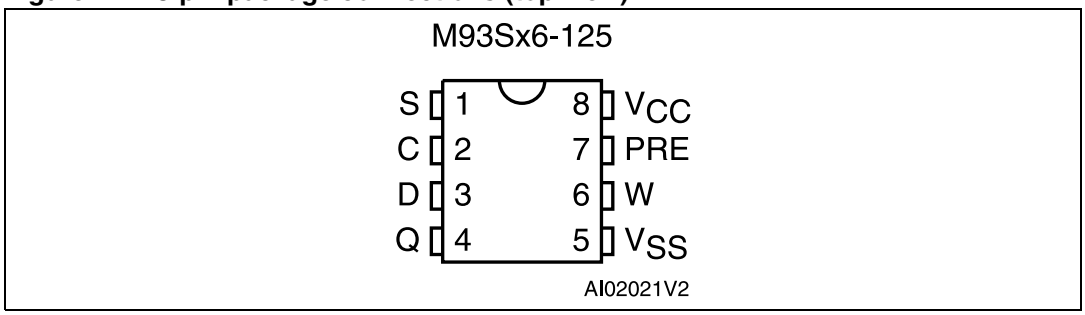
Within the time required by a programming cycle (t_W), up to 4 words may be written with help of the Page Write instruction. the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, a user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protection register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programming (OTP) bit which locks the Protection register content.

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at a time into one of the word locations of the M93Sx6-125, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write protected area. After the start of the programming cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input ($\overline{S}$) is driven High.

An internal *Power-on Data Protection* mechanism in the M93Sx6-125 inhibits the device when the supply is too low.

Figure 2. 8-pin package connections (top view)



Note: See Section 9: Package mechanical data section for package dimensions, and how to identify pin-1.

2 Power-on data protection

To prevent data corruption and inadvertent write operations during power-up, a Power-on Reset (POR) circuit resets all internal programming circuitry, and sets the device in the Write Disable mode.

- At Power-up and Power-down, the device must *not* be selected (that is, Chip Select Input ($\overline{S}$) must be driven Low) until the supply voltage reaches the operating value V_{CC} specified in *Section 8: DC and AC parameters*.
- When V_{CC} reaches its valid level, the device is properly reset (in the Write Disable mode) and is ready to decode and execute incoming instructions.

For the M93Sx6-125, the POR threshold voltage is around 1.5 V.

3 Instructions

The instruction set of the M93Sx6-125 devices contains seven instructions, as summarized in *Table 2* and *Table 3*. Each instruction consists of the following:

- Each instruction is preceded by a rising edge on Chip Select Input ($\overline{S}$) with *Serial Clock* (C) being held Low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two opcode bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the opcode).
- The address bits of the byte or word that is to be accessed. For the M93S46-125, the address is made up of 6 bits (see *Table 2*). For the M93S56-125 and M93S66-125, the address is made up of 8 bits (see *Table 3*).

The M93Sx6-125 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in *Table 9*.

Table 2. Instruction set for the M93S46

Instruction	Description	W	PRE	Start bit	Opcode	Address(1)	Data	Required clock cycles	Additional comments
READ	Read Data from Memory	X	0	1	10	A5-A0	Q15-Q0		
WRITE	Write Data to Memory	1	0	1	01	A5-A0	D15-D0	25	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	1	0	1	11	A5-A0	N x D15-D0	9 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRAL	Write All Memory with same Data	1	0	1	00	01 XXXX	D15-D0	25	Write all data if the Protection Register is cleared
WEN	Write Enable	1	0	1	00	11 XXXX		9	
WDS	Write Disable	X	0	1	00	00 XXXX		9	
PRREAD	Protection Register Read	X	1	1	10	XXXXXX	Q5-Q0 + Flag		Data Output = Protection Register content + Protection Flag bit
PRWRITE	Protection Register Write	1	1	1	01	A5-A0		9	Data above specified address A5-A0 are protected
PRCLEAR	Protection Register Clear	1	1	1	11	111111		9	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protection Register Enable	1	1	1	00	11XXXX		9	
PRDS	Protection Register Disable	1	1	1	00	000000		9	OTP bit is set permanently

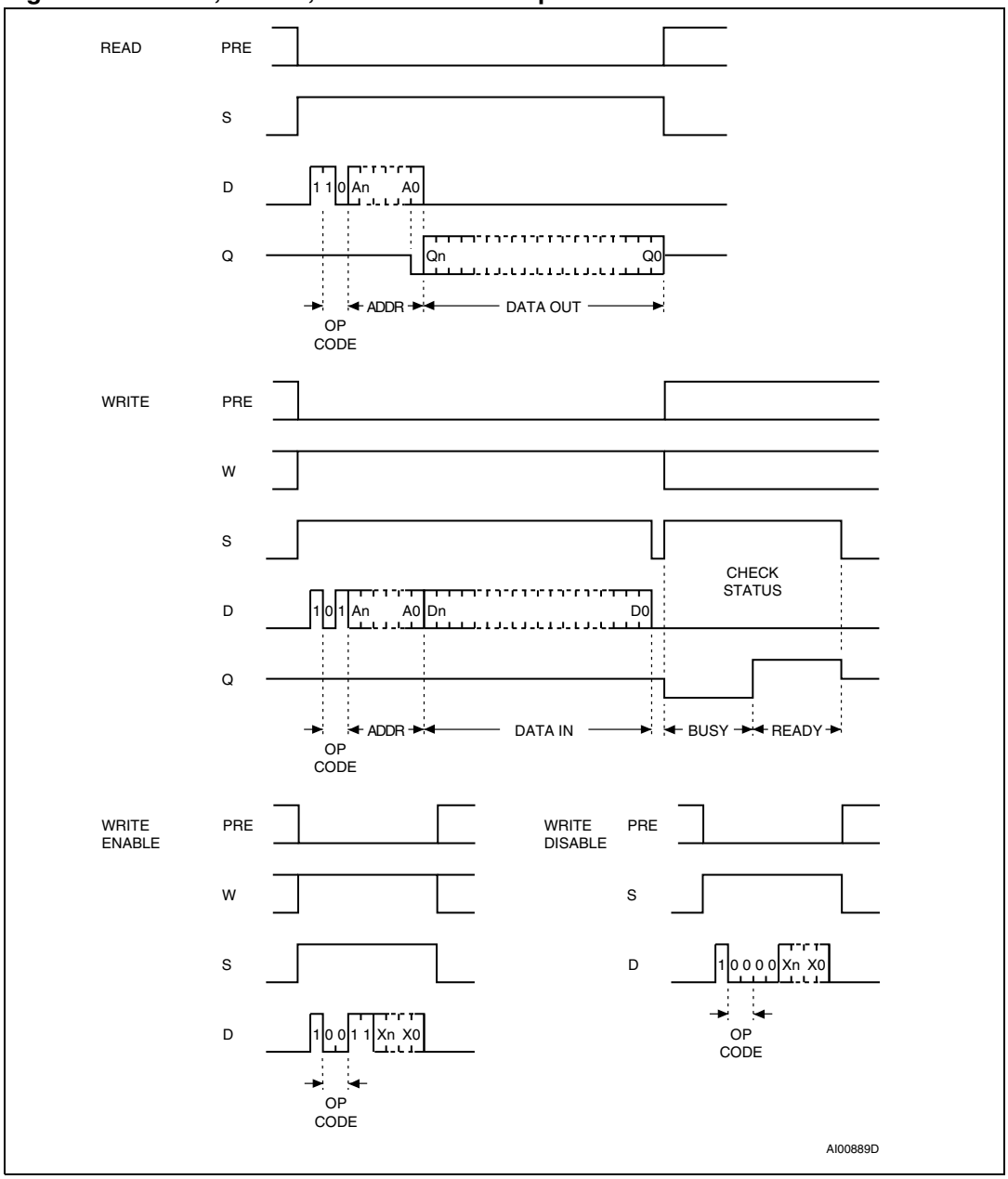
1. X = Don't Care bit.

Table 3. Instruction set for the M93S56, M93S66

Instruction	Description	W	PRE	Start bit	Opcode	Address(1), (2)	Data	Required clock cycles	Additional comments
READ	Read Data from Memory	X	0	1	10	A7-A0	Q15-Q0		
WRITE	Write Data to Memory	1	0	1	01	A7-A0	D15-D0	27	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	1	0	1	11	A7-A0	N x D15-D0	11 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRAL	Write All Memory with same Data	1	0	1	00	01XXXXXX	D15-D0	27	Write all data if the Protection Register is cleared
WEN	Write Enable	1	0	1	00	11XXXXXX		11	
WDS	Write Disable	X	0	1	00	00XXXXXX		11	
PRREAD	Protection Register Read	X	1	1	10	XXXXXXX X	Q7-Q0 + Flag		Data Output = Protection Register content + Protection Flag bit
PRWRITE	Protection Register Write	1	1	1	01	A7-A0		11	Data above specified address A7-A0 are protected
PRCLEAR	Protection Register Clear	1	1	1	11	11111111		11	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protection Register Enable	1	1	1	00	11XXXXXX		11	
PRDS	Protection Register Disable	1	1	1	00	00000000		11	OTP bit is set permanently

1. X = Don't Care bit.
2. Address bit A7 is not decoded by the M93S56-125.

Figure 3. READ, WRITE, WEN and WDS sequences



1. For the meanings of An, Xn, Qn and Dn, see *Table 2* and *Table 3*.

3.1 Read

The Read Data from Memory (READ) instruction outputs serial data on Serial Data Output (Q). When the instruction is received, the opcode and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Sx6-125 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input ($\overline{S}$) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read.

3.2 Write Enable and Write Disable

The Write Enable (WEN) instruction enables the future execution of write instructions, and the Write Disable (WDS) instruction disables it. When power is first applied, the M93Sx6-125 initializes itself so that write instructions are disabled. After a Write Enable (WEN) instruction has been executed, writing remains enabled until a Write Disable (WDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (WDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (WEN) or Write Disable (WDS) instructions.

3.3 Write

The Write Data to Memory (WRITE) instruction is composed of the Start bit plus the opcode followed by the address and the 16 data bits to be written.

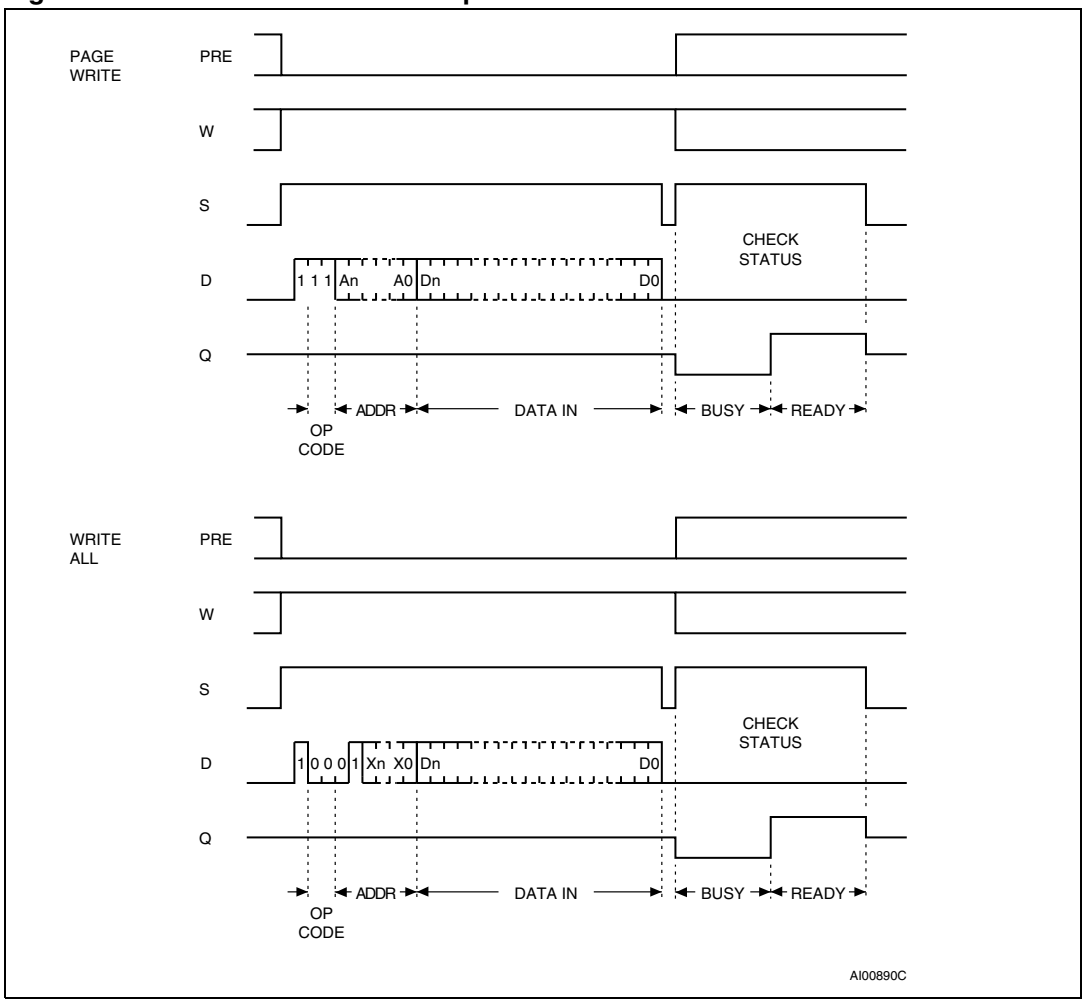
Write Enable ($\overline{W}$) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input ($\overline{S}$) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input ($\overline{S}$) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6-125 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input ($\overline{S}$) can be driven High to monitor the status of the write cycle: Serial Data Output (Q) is driven Low while the M93Sx6-125 is still busy, and High when the cycle is complete, and the M93Sx6-125 is ready to receive a new instruction. The M93Sx6-125 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6-125 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input ($\overline{S}$) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

Figure 4. PAWRITE and WRAL sequence



1. For the meanings of An, Xn and Dn, please see *Table 2* and *Table 3*.

3.4 Page Write

A Page Write to Memory (PAWRITE) instruction contains the first address to be written, followed by up to 4 data words.

After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits remaining unchanged (A7-A2 for M93S66-125, M93S56-125; A5-A2 for M93S46-125). Users must take care, in the software, to ensure that the last word address has the same upper order address bits as the initial address transmitted to avoid address roll-over.

The Page Write to Memory (PAWRITE) instruction will not be executed if any of the 4 words addresses the protected area.

Write Enable ($\overline{W}$) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input ($\overline{S}$) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input ($\overline{S}$) is brought Low before or

after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6-125 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input ($\overline{S}$) can be driven High to monitor the status of the write cycle: Serial Data Output (Q) is driven Low while the M93Sx6-125 is still busy, and High when the cycle is complete, and the M93Sx6-125 is ready to receive a new instruction. The M93Sx6-125 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6-125 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input ($\overline{S}$) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

3.5 Write All

The Write All Memory with same Data (WRAL) instruction is valid only after the Protection Register has been cleared by executing a Protection Register Clear (PRCLEAR) instruction. The Write All Memory with same Data (WRAL) instruction simultaneously writes the whole memory with the same data word given in the instruction.

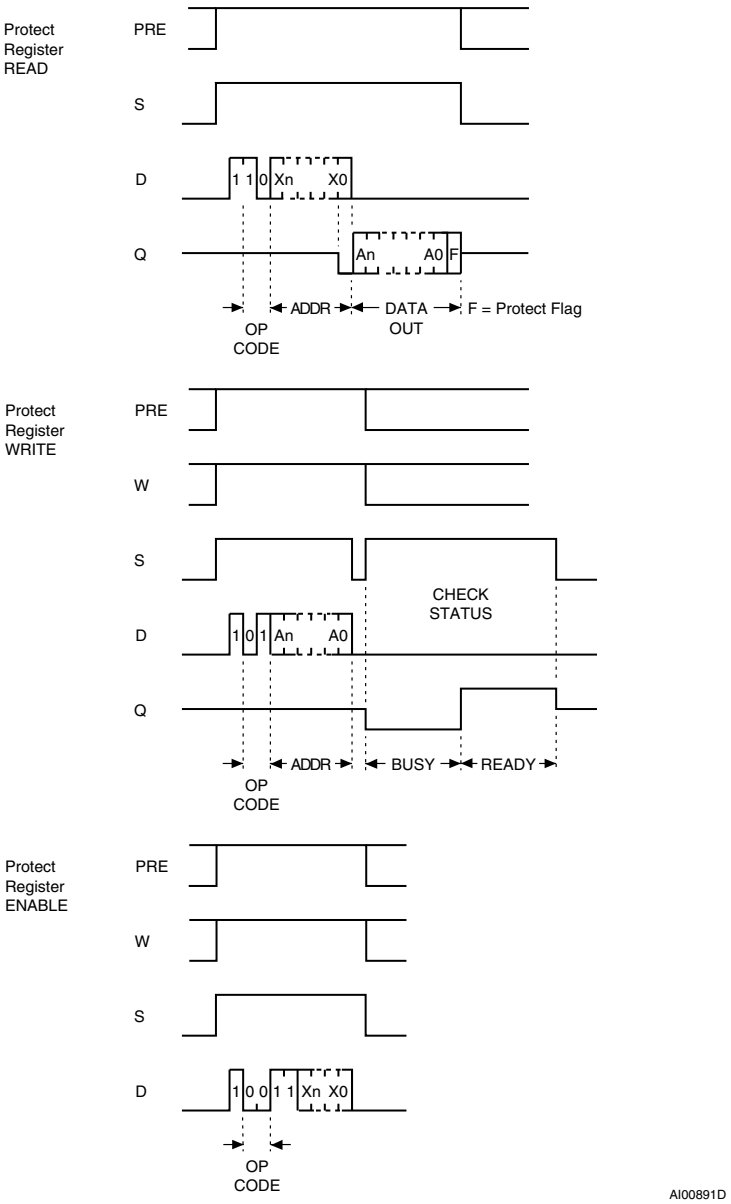
Write Enable ($\overline{W}$) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input ($\overline{S}$) must be taken Low before the next rising edge of Serial Clock (C).* If Chip Select Input ($\overline{S}$) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6-125 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input ($\overline{S}$) can be driven High to monitor the status of the write cycle: Serial Data Output (Q) is driven Low while the M93Sx6-125 is still busy, and High when the cycle is complete, and the M93Sx6-125 is ready to receive a new instruction. The M93Sx6-125 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6-125 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input ($\overline{S}$) is brought Low.

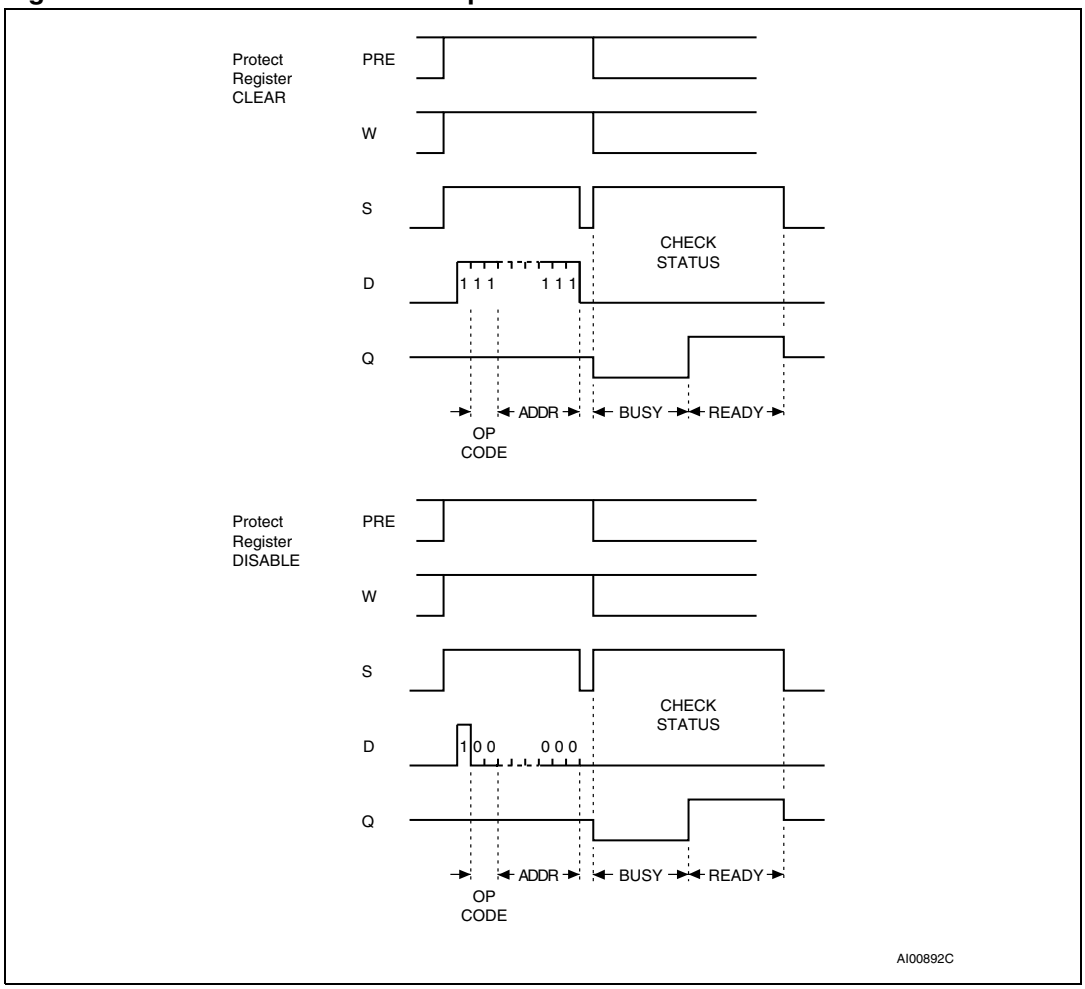
Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

Figure 5. PREAD, PRWRITE and PREN sequences



1. For the meanings of An, Xn and Dn, please see *Table 2* and *Table 3*.

Figure 6. PRCLEAR and PRDS sequences



1. For the meanings of An, Xn and Dn, please see *Table 2* and *Table 3*.

4 Write protection and the Protection Register

The Protection Register on the M93Sx6-125 is used to adjust the amount of memory that is to be write protected. The write protected area extends from the address given in the Protection Register, up to the top address in the M93Sx6-125 device.

Two flag bits are used to indicate the Protection Register status:

- Protection Flag: this is used to enable/disable protection of the write-protected area of the M93Sx6-125 memory
- OTP bit: when set, this disables access to the Protection Register, and thus prevents any further modifications to the value in the Protection Register.

The lower-bound memory address is written to the Protection Register using the Protection Register Write (PRWRITE) instruction. It can be read using the Protection Register Read (PRREAD) instruction.

The Protection Register Enable (PREN) instruction must be executed before any PRCLEAR, PRWRITE or PRDS instruction, and with appropriate levels applied to the Protection Enable (PRE) and Write Enable ($\overline{W}$) signals.

Write-access to the Protection Register is achieved by executing the following sequence:

- Execute the Write Enable (WEN) instruction
- Execute the Protection Register Enable (PREN) instruction
- Execute one PRWRITE, PRCLEAR or PRDS instructions, to set a new boundary address in the Protection Register, to clear the protection address (to all 1s), or permanently to freeze the value held in the Protection Register.

4.1 Protection Register Read

The Protection Register Read (PRREAD) instruction outputs, on Serial Data Output (Q), the content of the Protection Register, followed by the Protection Flag bit. The Protection Enable (PRE) signal must be driven High before and during the instruction.

As with the Read Data from Memory (READ) instruction, a dummy 0 bit is output first. Since it is not possible to distinguish between the Protection Register being cleared (all 1s) or having been written with all 1s, the user must check the Protection Flag status (and not the Protection Register content) to ascertain the setting of the memory protection.

4.2 Protection Register Enable

The Protection Register Enable (PREN) instruction is used to authorize the use of instructions that modify the Protection Register (PRWRITE, PRCLEAR, PRDS). The Protection Register Enable (PREN) instruction does not modify the Protection Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protection Register Enable (PREN) instruction. Both the Protection Enable (PRE) and Write Enable ($\overline{W}$) signals must be driven High during the instruction execution.

4.3 Protection Register Clear

The Protection Register Clear (PRCLEAR) instruction clears the address stored in the Protection Register to all 1s, so that none of the memory is write-protected by the Protection Register. However, it should be noted that all the memory remains protected, in the normal way, using the Write Enable (WEN) and Write Disable (WDS) instructions.

The Protection Register Clear (PRCLEAR) instruction clears the Protection Flag to 1. Both the Protection Enable (PRE) and Write Enable ($\overline{W}$) signals must be driven High during the instruction execution.

Note: A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Clear (PRCLEAR) instruction.

4.4 Protection Register Write

The Protection Register Write (PRWRITE) instruction is used to write an address into the Protection Register. This is the address of the first word to be protected. After the Protection Register Write (PRWRITE) instruction has been executed, all memory locations equal to and above the specified address are protected from writing.

The Protection Flag bit is set to 0, and can be read with Protection Register Read (PRREAD) instruction. Both the Protection Enable (PRE) and Write Enable ($\overline{W}$) signals must be driven High during the instruction execution.

Note: A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Write (PRWRITE) instruction, but it is not necessary to execute first a Protection Register Clear (PRCLEAR).

4.5 Protection Register Disable

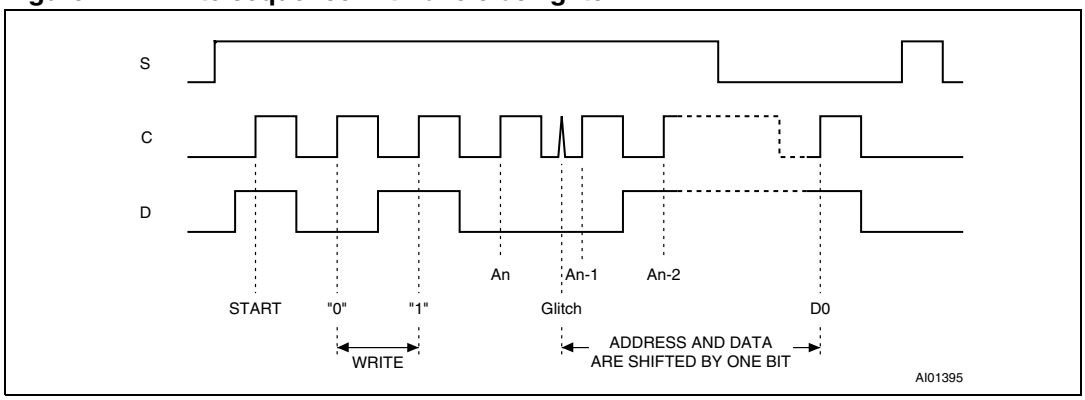
The Protection Register Disable (PRDS) instruction sets the One Time Programmable (OTP) bit. This instruction is a ONE TIME ONLY instruction which latches the Protection Register content, this content is therefore unalterable in the future. Both the Protection Enable (PRE) and Write Enable ($\overline{W}$) signals must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protection Register, using the Protection Register Read (PRREAD) instruction, then by writing this same value back into the Protection Register, using the Protection Register Write (PRWRITE) instruction. When the OTP bit is set, the Ready/Busy status cannot appear on Serial Data Output (Q). When the OTP bit is not set, the Busy status appears on Serial Data Output (Q).

Note: A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Disable (PRDS) instruction.

5 Common I/O operation

Serial Data Output (Q) and Serial Data Input (D) can be connected together, through a current limiting resistor, to form a common, single-wire data bus. Some precautions must be taken when operating the memory in this way, mostly to prevent a short circuit current from flowing when the last address bit (A0) clashes with the first data bit on Serial Data Output (Q). Please see *AN394 (Microwire EEPROM common I/O operation application note)* for details.

Figure 7. Write sequence with one clock glitch



6 Clock pulse counter

In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the Bus Master (the microcontroller). This can lead to a misalignment of the instruction of one or more bits (as shown in *Figure 7*) and may lead to the writing of erroneous data at an erroneous address.

To combat this problem, the M93Sx6-125 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input ($\overline{S}$). If the number of clock pulses received is not the number expected, the WRITE, PAWRITE, WRALL, PRWRITE or PRCLEAR instruction is aborted, and the contents of the memory are not modified.

The number of clock cycles expected for each instruction, and for each member of the M93Sx6-125 family, are summarized in *Table 2* to *Table 3*. For example, a Write Data to Memory (WRITE) instruction on the M93S56 (or M93S66) expects 27 clock cycles from the start bit to the falling edge of Chip Select Input ($\overline{S}$).

For example:

1 Start bit

+ 2 Op-code bits

+ 8 Address bits

+ 16 Data bits

7 Maximum rating

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	See note (1)		°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)	–0.50	V_{CC}+0.5	V
V_{IN}	Input range	–0.50	V_{CC}+1	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. Operating conditions (M93Sx6-W, device grade 3)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	125	°C

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Table 6. AC measurement conditions (M93Sx6-W, device grade 3)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Figure 8. AC testing input output waveforms

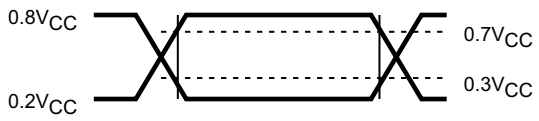


Table 7. Capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF

1. Sampled only, not 100% tested, at T_A=25°C and a frequency of 1 MHz.

Table 8. DC characteristics (M93Sx6-W, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \leq V_{IN} \leq V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \leq V_{OUT} \leq V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz		2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz		1	mA
I_{CC1}	Supply current (stand-by)	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}		5	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5 V, I_{OH} = –100µA	V_{CC}–0.2		V

Table 9. AC characteristics (M93Sx6-W, device grade 3)

Test conditions specified in *Table 5* and *Table 6*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock Frequency	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		ns
t_{SLCH}		Chip Select Low to Clock High	50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select Low to Chip Select High	200		ns
t_{CHCL}(2)	t_{SKH}	Clock High Time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock Low Time	200		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	50		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		200	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to Output Low		200	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		200	ns
t_W	t_{WP}	Erase/Write Cycle time		5	ms

1. Chip Select Input ($\overline{S}$) must be brought Low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Figure 9. Synchronous timing (START and OPCODE INPUT)

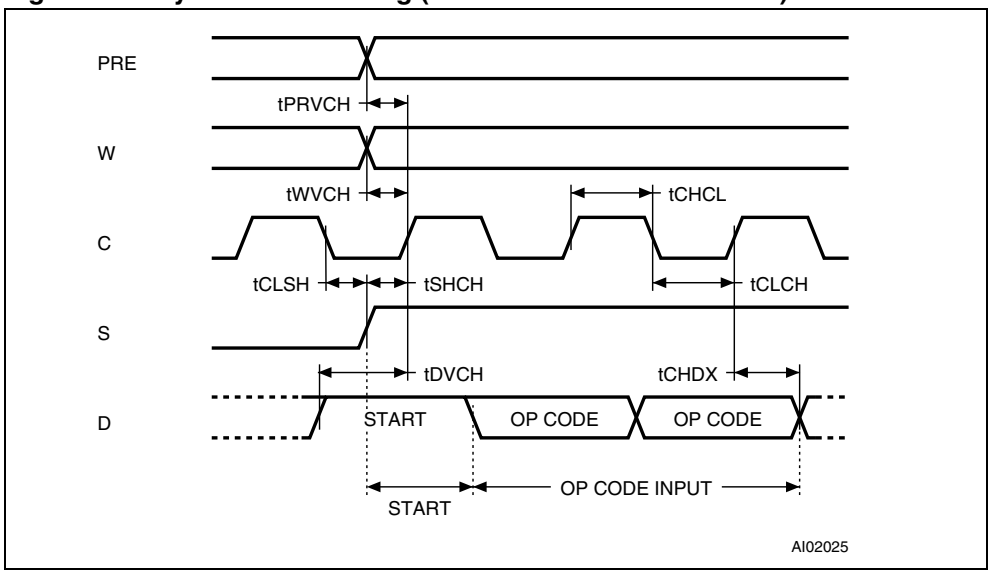


Figure 10. Synchronous timing (READ)

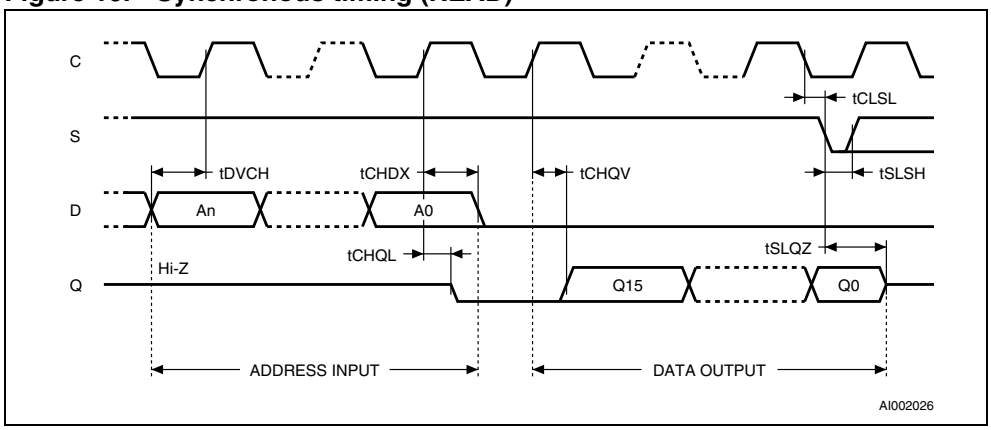
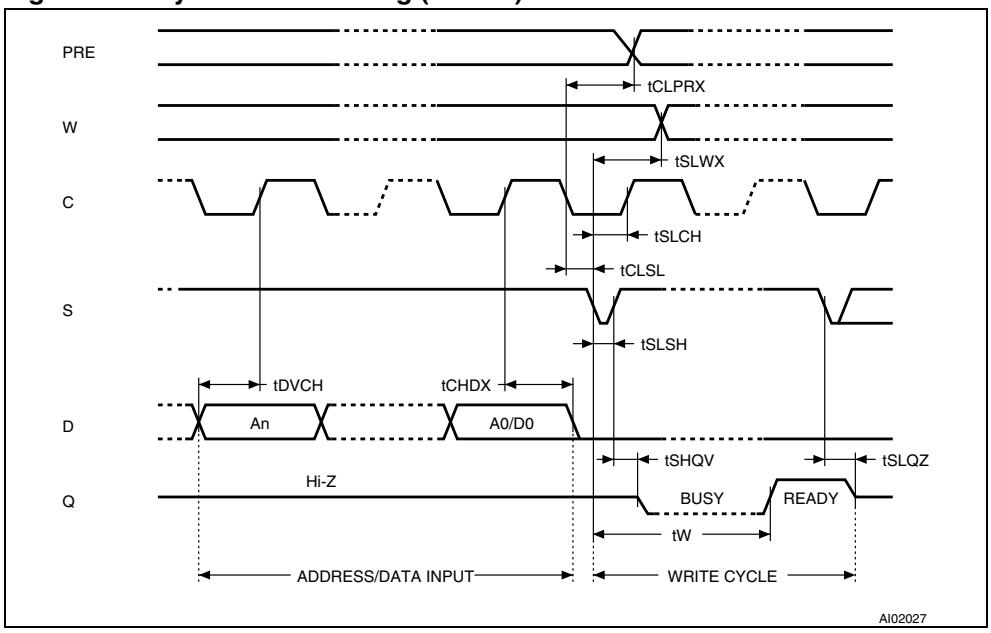


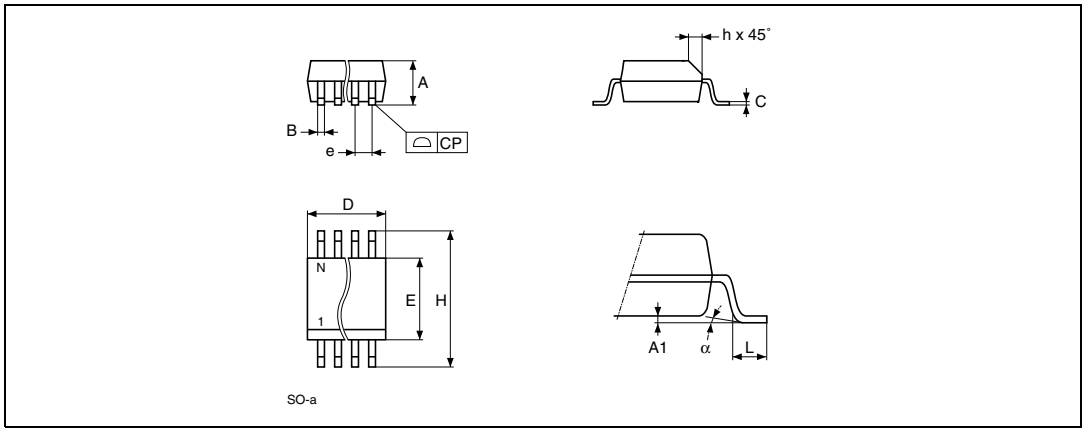
Figure 11. Synchronous timing (WRITE)



9 Package mechanical data

In order to meet environmental requirements, ST offers the M93Sx6-125 devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 12. SO8 narrow – 8-lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 10. SO8 narrow – 8 lead plastic small outline, 150 mils body width, mechanical data

Symbol	mm			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
a		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

1. Values in inches are converted from mm and rounded to 4 decimal digits.

10 Part numbering

Table 11. Ordering information scheme

Example: M93S66 – W MN 3 T P /S

Device type

M93 = MICROWIRE serial access EEPROM (x16) with block protection

Device function

66 = 4 Kbit (256 x 16)

56 = 2 Kbit (128 x 16)

46 = 1 Kbit (64 x 16)

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

Package

MN = SO8 (150 mil width)

Device grade

3 = Automotive: device tested with High Reliability Certified Flow over –40 to 125°C

Option

blank = Standard packing

T = Tape & reel packing

Plating technology

blank = Standard SnPb plating

P = Lead-free and RoHS compliant

Process

/S = Manufacturing technology code

Devices are shipped from the factory with the memory content set at all 1s (FFh).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

11 Revision history

Table 12. Document revision history

Date	Revision	Changes
14-Mar-2012	1	Initial release.

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