DATA SHEET

GPLB62P100UA1

8-Bit LCD Controller/Driver with SPU

Jul 28, 2016

Version 1.2

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8-Bit LCD CONTROLLER/DRIVER WITH SPU

1. GENERAL DESCRIPTION

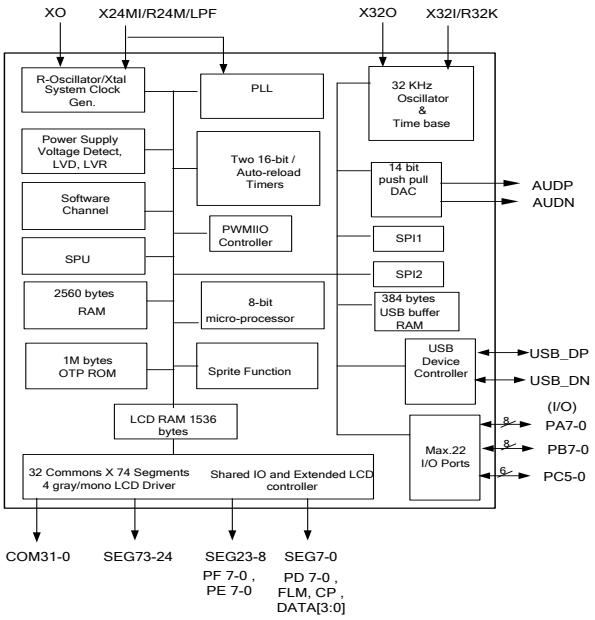
The GPLB62P100UA1, an 8-bit microprocessor for handheld LCD product, features 2M bytes OTP ROM, 2560 bytes working RAM,1536 bytes LCD RAM, 22 I/Os, two 16-bit timers, two SPI interfaces, and automatic display controller/ driver for mono/ 4-gray-level LCD.

In graphic features, GPLB62P100UA1 contains up to 74 segments and 32 commons, forming a maximum of 2,368 dots LCD resolution. Besides the built-in driver function, the common/segment could be extended with external drivers such as GPLD2080A and GPLD2120A. A LCD sprite function is included in GPLB62P100UA1; it is capable of operating over a wide voltage range from 2.3V through 5.5V, and Low Voltage Reset function to keep system operating properly when power drops below certain level.

The GPLB62P100UA1 carries a high performance SPU voice engine to achieve 8-channel ADPCM/PCM high quality voice. Plus, it features one 14-bit DAC with push-pull amplifier to drive speaker directly. Its large memory area allows user to store both program and audio data in one place. The USB device function assures data transmitted in super high speed with reliability as well. There is a Serial Peripheral Interface (SPI) controller built-in to facilitate communicating with other devices. Furthermore, a SLEEP (power-down) function is also built-in to extend battery life.

2. BLOCK DIAGRAM

2.1. GPLB62P100UA1



3. FEATURES

- 8-bit micro-processor
- 1M bytes OTP ROM
- 2560-byte SRAM
- 1536-byte LCD RAM
- Operating voltage: 2.3V – 5.5V
- Max. CPU operating speed:
  - 12.0MHz @ 2.7V – 5.5V
  - 8.0MHz @ 2.3V – 3.6V
- Programmable CPU clock: /2, /4, /8, /16, /32, /64 and /128 clock frequency
- Six wake-up sources
- 23 IRQs & 4 NMI Interrupts
- Internal built-in regulator to supply core power (3.3V, for 3-battery application). Also internal built-in regulator can be turned off and external 3.6V power is used to supply core power (for 2-battery application).
- Supports USB 2.0 full speed (12MHz) compliant device with built-in transceiver
- SPU(Sound Processing Unit) engine with 8 voice channels
  - Supports 4/5 bit ADPCM and 8/16 bit PCM data format
  - Transform 4/5 bit ADPCM data to 14 bit data to play high quality sound

- Supports special tag such as Silence Tag, Event tag

- One software channel with noise filter to play high quality sound.
- LCD sprite function
  - Supports special function such as PIP, data shift, and write back etc.
- Programmable LCD driver
  - Up to 74 segments and 32 commons, forming a maximum of 2368 dots LCD resolution
  - The segment could be further extended with external drivers such as GPLD2080A and GPLD2120A.
  - Supports up to 32 x 192 gray level LCD panel with two GPLD2080.
  - Supports up to 32 x 384 mono level LCD panel with four GPLD2080.
  - Supports from 1/2 duty up to 1/32 duty
  - 1536 bytes dedicated LCD RAM
  - Supports normal type-B and type-C LCD waveform with or without key scan
  - Built-in voltage regulator to generate VLCD for LCD driver
  - 46-level contrast control (VLCD=3.5V~8V)
  - Power saving SLEEP mode
- Low Voltage Detector
  8-level (2.3V/2.4V/2.6V/2.9V/3.0V/3.3V/3.6V/4.0V) voltage detector
- Low Voltage Reset
- Peripherals
  - Max. 46 I/O pins (PA[7:0], PB[7:0], PC[5:0], PD[7:0], PE[7:0] , PF[7:0])
    Dedicated I/Os: PA[7:0], PB[7:0], PC[5:0]
    Shared pin I/Os:
    PD[3:0]/SEG[3:0]/LCDDI[3:0]
    PD[4]/SEG[4]/LCDCP
    PD[5]/SEG[5]/LCDLP
    PD[6]/SEG[6]/LCDM
    PD[7]/SEG[7]/LCDFLM
    PE[7:0]/SEG[15:8]
    PF[7:0]/SEG[23:16]
  - Eight I/Os with high sink current for LED application
  - Key wakeup/interrupt function
  - Built-in 32.768KHz oscillator circuit for real time clock function (X'tal or R-osc)
  - Built-in R-oscillator (external resistor is needed) or X'tal or PLL for system operating clock
  - Internal time base generator
  - Two 16-bit reloadable timer/counters
  - Watchdog timer
  - 14-bit DAC with push-pull amplifier for driving speaker directly
  - IR output
  - Hardware PWMIO
  - Two SPI serial interface I/Os
- Powerful 8-ch Sound Processing Unit (SPU)
  - Variable tone-color sampling rate: max = 96KHz @ SPU_clock = 24MHz
  - 8-voice polyphony
  - Supports PCM/ADPCM tone-color table

4. APPICATION FIELD

- Handheld LCD game
- Educational toys (Electronic Learning Aids)
- Data bank
- Dictionary
- Translator

5. SIGNAL DESCRIPTIONS

5.1. Main Function PIN

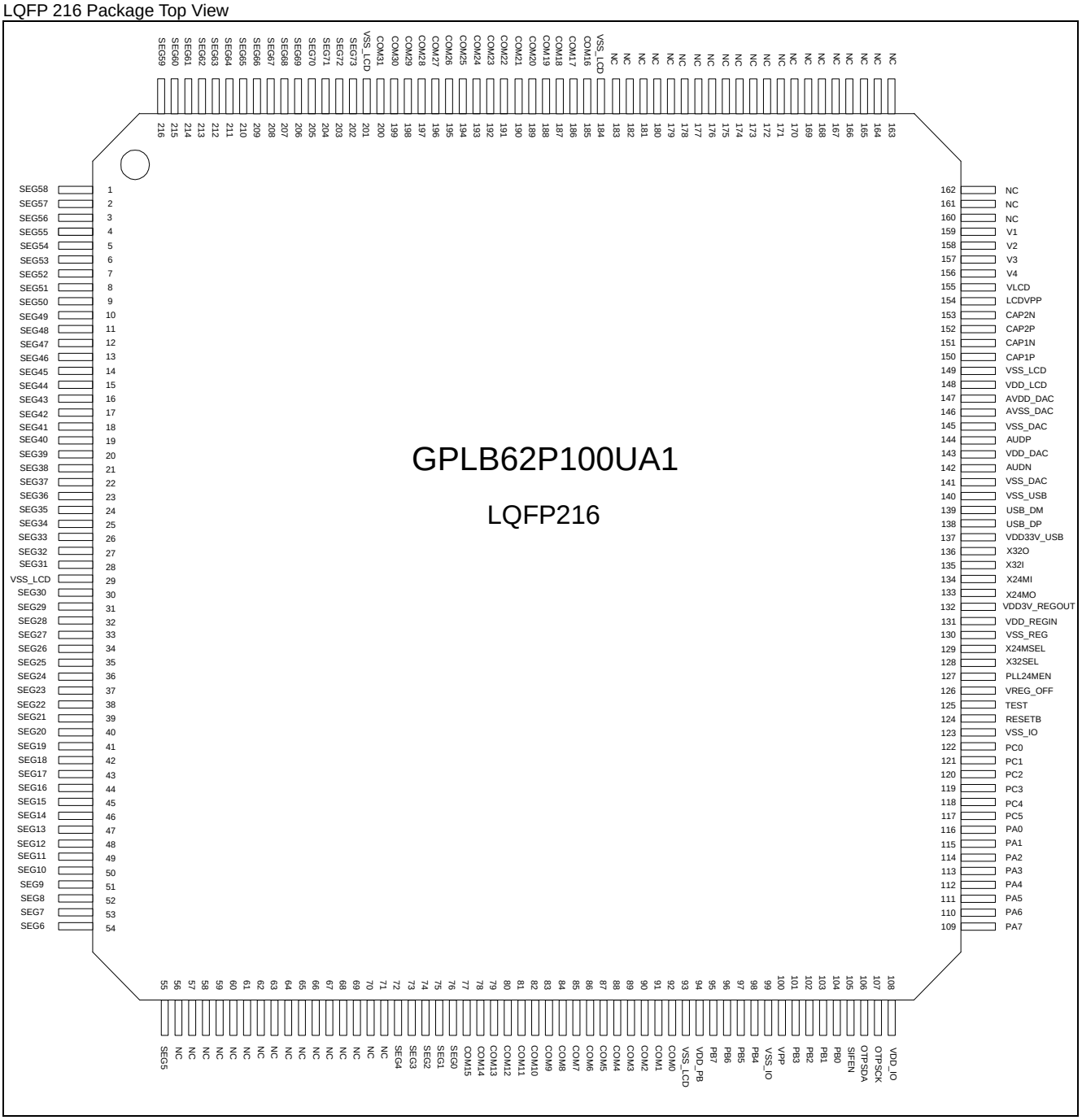
Mnemonic	PIN No.	Type	Description
SEG0/PD0/LCDDI0	61	O	LCD driver segment output. SEG0 shared pin with PD0 and LCDDI0
SEG1/PD1/LCDDI1	60	O	LCD driver segment output. SEG1 shared pin with PD1 and LCDDI1
SEG2/PD2/LCDDI2	59	O	LCD driver segment output. SEG2 shared pin with PD2 and LCDDI2
SEG3/PD3/LCDDI3	58	O	LCD driver segment output. SEG3 shared pin with PD3 and LCDDI3
SEG4/PD4/LCDCP	57	O	LCD driver segment output. SEG4 shared pin with PD4 and LCDCP
SEG5/PD5/LCDLP	56	O	LCD driver segment output. SEG5 shared pin with PD5 and LCDLP
SEG6/PD6/LCDM	55	O	LCD driver segment output. SEG6 shared pin with PD6 and LCDM
SEG7/PD7/LCDFLM	54	O	LCD driver segment output. SEG7 shared pin with PD7 and LCDFLM
SEG15 - 8 /PE7-0	46~53	O	LCD driver segment output. SEG15 - 8 shared pin with PE7-0
SEG23 - 16/PF7-0	38~45	O	LCD driver segment output. SEG23 - 16 shared pin with PF7-0
SEG73 - 24	163~176,1~29, 31~37	O	LCD driver segment output.
COM16-31/SEG89– 74	146~161	O	LCD driver segment output shared with comment output.
COM0- 15	77~62	O	LCD driver common output.
PA0/IRO/EXT1	101	I/O	PA0 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with IRO (IR output) and external interrupt 1.
PA1/EXT2	100	I/O	PA1 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with external interrupt 2.
PA3 - 2	98,99	I/O	PA3-2 is a bi-directional I/O port, which can be software programmed as wakeup I/O.
PA4/ PWMIO0	97	I/O	PA4 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with PWMIO0.
PA5/ PWMIO1	96	I/O	PA5 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with PWMIO1.
PA6/ PWMIO2	95	I/O	PA6 is a bi-directional I/O port, which can be software programmed as wake up I/O and is shared with PWMIO2.
PA7/PWMIO3	94	I/O	PA7 is a bi-directional I/O port, which can be software programmed as wakeup I/O and is shared with PWMIO3.
PB0/SPI2_CSN/IISCKO	89	I/O	PB0 is shared with SPI2_CSN and IISCKO
PB1/ SPI2_SCK//IISDAO	88	I/O	PB1 is shared with SPI2_SCK and IISDAO
PB2/ SPI2_SDO/IISWSO	87	I/O	PB2 is shared with SPI2_SDO and IISWSO
PB3/ SPI2_SDI	86	I/O	PB3 is shared with SPI2_SDI.
PB4/SPI1_CSN/ PWMIO0	83	I/O	PB4 is shared with SPI1_CSN and shared with PWMIO0and is a high drive IO.
PB5/SPI1_SCK/ PWMIO1/IISCKI	82	I/O	PB5 is shared with SPI1_SCK and IISCKI and shared with PWMIO1 and is a high drive IO.
PB6/SPI1_SDO/ PWMIO2/IISDAI	81	I/O	PB[6:5] is shared with SPI1_SDO and IISDAI and shared with PWMIO2 and is a high drive IO.
PB7/ SPI1_SDI/ PWMIO3/IISWSI	80	I/O	PB7 is shared with SPI1_SDI and IISWSI and shared with PWMIO3 and is a high drive IO.
PC0 -5	107~102	I/O	PC[0:5] is a bi-directional I/O port
X24MI/R24M/LPF	119	I	Crystal input or ROSC input connected to VDD33V_REGOUT through a resistor, or RC low pass filter connection for PLL(Mask option).

Mnemonic	PIN No.	Type	Description
X24MO	118	O	Crystal output
RESETB	109	I	System reset input, low active, internal pull high.
AUDP, AUDN	129,127	O	Audio output of push pull DAC
X32I/R32K	120	I	32.768KHz crystal input or connects to VDD33V_REGOUT through a resistor (option).
X32O	121	O	32.768KHz crystal output
SIFEN	90	I	OTP serial interface enable, input pin with pull high
OTPSCK	92	I	OTP serial interface clock, input pin with pull low
OTPSDA	91	I/O	OTP serial interface data
VREG_OFF	111	I	Regulator on/off selection, input pin with floating. 0:on, 1: off
PLL24MEN	112	I	Main clock selection, input pin with floating, 1: clock source selected from PLL24MHZ, 0: clock source selected from Crystal, or R-osc.
X24MSEL	114	I	Main clock selection, input pin with floating. 0:R-osc; 1:Crystal 24MHz
X32SEL	113	I	32KHz oscillator selection, input pin with floating. 0:R-osc; 1:Crystal
TEST	110	I	Test input, internal pull low
CAP1P, CAP1N	135,136	P	LCD voltage generation. Charge pump capacitor interconnection pins.
CAP2P, CAP2N	137,138	P	LCD voltage generation. Charge pump capacitor interconnection pins.
LCDVPP	139	P	LCD voltage generation. Voltage generated by charge pump.
VPP	85	P	OTP program power, high voltage pin is used in user mode operating at 7.5V during program cycle and 3.3V in read cycle
V4	141	P	LCD voltage generation
V3	142	P	LCD voltage generation
V2	143	P	LCD voltage generation
V1	144	P	LCD voltage generation
VLCD	140	P	LCD voltage generation. The highest Voltage for LCD display.
VDD_REGIN	116	P	Power for Regulator
VSS_REG	115	P	Ground for Regulator
VDD33V_REGOUT	117	P	3.3V power output from regulator (regulator can be off when external 3V is supplied).
VDD_LCD	133	P	Power for LCD driver
VSS_LCD4,VSS_LCD5,VSS_LCD1,VSS_LCD2,VSS_LCD3	30,78,134,145,162	P	Ground for LCD driver
VDD_IO	93	P	Power for PA, PC, PD, PE, PF
VSS_IO1,VSS_IO2	84,108	P	Ground for PA, PB, PC, PD, PE, PF
VDD_PB	79	P	Power for PB
VDD_DAC	128	P	Power for push pull DAC driver
VSS_DAC	126	P	Ground for push pull DAC driver
AVDD_DAC	132	P	Analog ground for push pull DAC
AVSS_DAC	131	P	Analog power for push pull DAC
USB_DP	123	I/O	USB_DP pin of USBPHY
USB_DM	124	I/O	USB_DN pin of USBPHY
VDD33V_USB	122	P	Power for USB
VSS_USB	125	P	Ground for USB

Legend: I = Input, O = Output, P = Power

5.2. PIN Map

LQFP 216 Package Top View



6. FUNCTIONAL DESCRIPTIONS

6.1. Memories

GPLB62P100UA1 contains 2560-byte SRAM, 1536-byte LCD RAM and works with 1M bytes OTP ROM.

6.2. Operating States

There are three operation modes involved in GPLB62P100UA1: standby, halt and operating. The following table shows the differences between these modes.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768Hz Oscillator	ON	ON	OFF
LCD Driver	ON	ON/OFF	OFF

6.2.1. Operating Mode

In operating state, all functions (CPU, 32768Hz oscillator, timer/counter, LCD driver…) are activated.

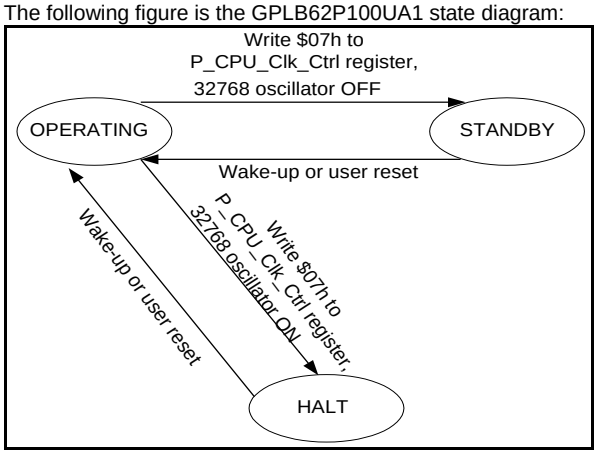
6.2.2. Standby Mode

Turn off 32768Hz oscillator and write “07H” to P_CLK_CPU_Ctrl Register ($3006) to activate standby mode. The standby mode is a mode that the device is placed in its lowest current consumption state. In standby mode, all functions are turned off; in addition, RAM and I/Os will remain in their previous states.

6.2.3. Halt Mode

Write “07H” to P_CLK_CPU_Ctrl Register ($3006) but still keeps 32768Hz oscillator running to enter halt mode. In halt mode, CPU clock halts and waits for an event (e.g. key press, timer overflow) to wake up. The 32768Hz related functions, such as timer/counter and LCD driver, may remain active in the halt mode.

The following figure is the GPLB62P100UA1 state diagram:



GPLB62P100UA1 State Diagram

6.3. Speech and Melody, and DAC

The GPLB62P100UA1 uses a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM code. The SPU also supports automatic zero-crossing concatenating function. A hardware multiplier is also embedded in this SPU for software use. The fixed addresses of RAM area $0000 - $009F is designed as address pointers and a data buffer for the 8-channel speech/melody generation. Moreover, one 14-bit software channel with noise filter is also supported. There is one 14-bit DAC with push-pull amplifier for direct audio output.

6.4. Hardware PWMIO

Hardware PWMIO supports 4 LED outputs with brightness control of 256 levels. The clock source of PWMIO is selective by user’s request.

6.5. LCD Controller/Driver

GPLB62P100UA1 has a built-in LCD driver and support monochrome and 4-gray-level LCD control. The LCD driver can support up to 32COM * 74SEG, and it also can cascade external LCD SEG driver that can extend LCD resolution up to 32COM * 192SEG with gray level or up to 32COM * 384SEG with mono level. Programmers are able to define the LCD configuration by setting up the LCD Control Register. Once the LCD configuration is completed, the desired pattern can be displayed by filling the LCD buffer with proper data. The LCD driver can also operate in halt mode by keeping 32768Hz oscillator running. The LCD driver in GPLB62P100UA1 supports 1/2 – 1/32 duty and 1/3 - 1/7 bias.

6.6. LCD Voltage Generator

To achieve highly integrated circuit and save external components, GPLB62P100UA1 has built-in charge-pump circuit to generate LCD’s bias voltages VLCD, V4, V3, V2 and V1. The level of VLCD can be adjusted by software. It is suggested that VLCD must be higher than VDD_IO or abnormal operation will occur.

6.7. LCD Sprite Function

The GPLB62P100UA1 also supports special functions such as PIP, data shift, and write back, etc. User can implement sprite function easily.

6.8. USB Device Function

The GPLB62P100UA1 provides the device function which is compatible with USB 2.0 full-speed standard. A USB transceiver is also built-in.

6.9. Low Voltage Detection

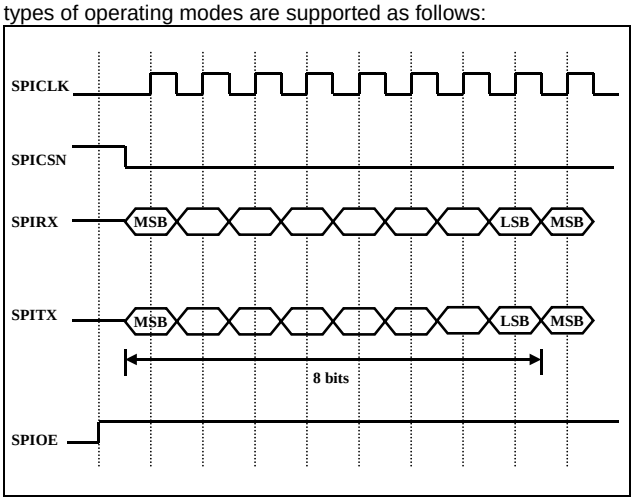
The GPLB62P100UA1 equips an 8-level (software programmable) low voltage detector to detect low voltage events. Users can turn on the low voltage detection that monitors VDD_REGIN periodically to check whether it is lower than the given value. In addition, if LV NMI is enabled, an NMI will be issued to notify CPU if power voltage drops below the given value. Also, the voltage detector will generate a system reset if power supply voltage drops too low.

6.10. Watchdog Timer (WDT)

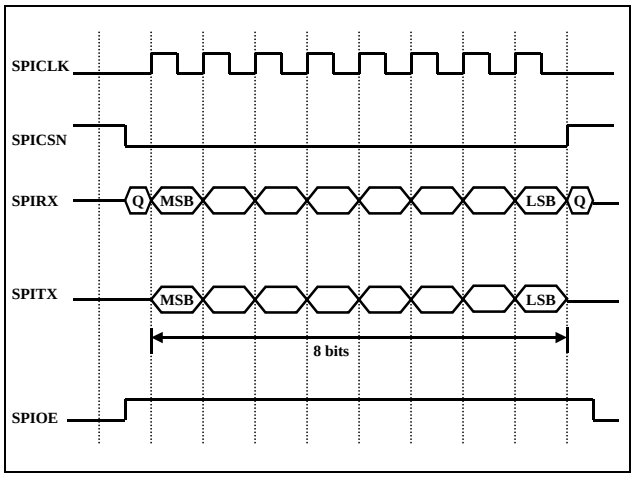
An on-chip watchdog timer is also available in the GPLB62P100UA1. The WDT is designed to recover the system from unexpected operations. In some cases, if WDT is not cleared within one second, the WDT will generate a system reset to restart system. If WDT is enabled, the WDT should be cleared periodically to avoid accidental reset. The WDT can be cleared through software programming. Note that the WDT only works when 32768Hz clock is activated.

6.11. SPI Controller

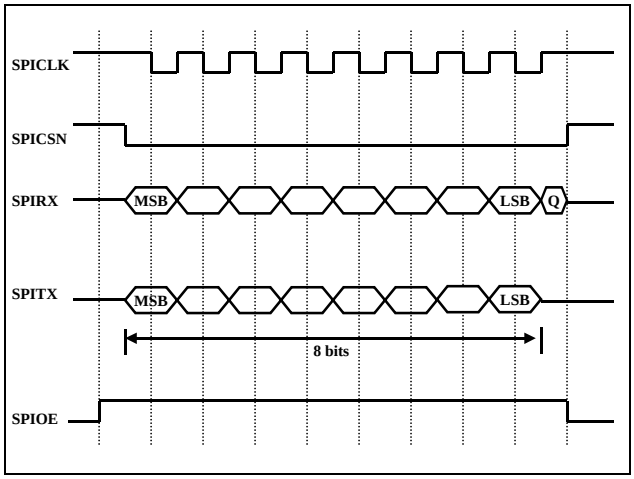
Two Serial Peripheral Interface (SPI) controllers are built-in to enable synchronous serial communication with master/slave peripherals. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO). The four signals of SPI1 are shared with PB4, PB5, PB6 and PB7. The four signals of SPI2 are shared with PB0, PB1, PB2 and PB3. While SPI module is enabled by corresponding control bit, these four pins cannot be used as GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of operating modes are supported as follows:



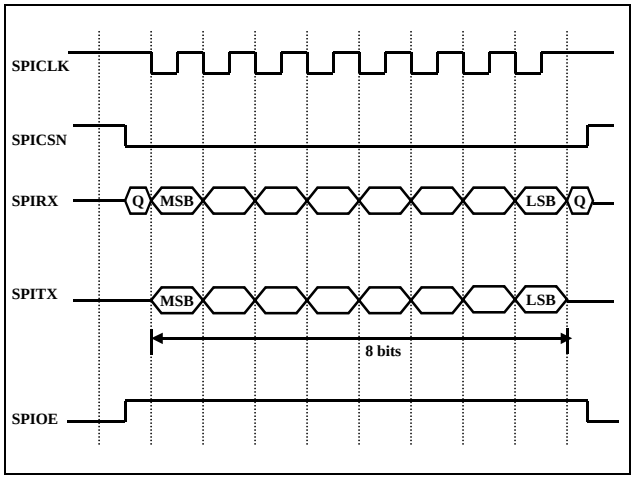
Master Mode, Polarity = 0, Phase=0



Master Mode, Polarity = 0, Phase=1



Master Mode, Polarity = 1, Phase=0



Master Mode, Polarity = 1, Phase=1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD_REGIN=4.5V, for 3-battery Application, Internal Regulator Enabled Output, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN	2.7	-	5.5	V	For 3-battery
Operating Current	I_{OP1}	-	7	9	mA	F_{CPU} = 8.0MHz @ 4.5V F_{XTAL} = 16.0MHz, no load, DAC disabled.
	I_{OP2}	-	8.2	12	mA	F_{CPU} = 12.0MHz @ 4.5V F_{ROSC} = 24.0MHz, no load, DAC disabled.
Halt Current	I_{HALT}	-	50	70	μA	VDD_REGIN = 4.5V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=7.1 V, no LCD panel
Standby Current (Regulator on)	I_{STBYR}	-	-	10	μA	VDD_REGIN = 4.5V, internal regulator on, all off.
Input High Level(PA/PB/PC) (PD/PE/PF)	V_{IH1} V_{IH2}	-	2.5 2	-	V	VDD_ IO = 4.5V
Input Low Level(PA/PB/PC) (PD/PE/PF)	V_{IL1} V_{IL2}	-	1.8 1.9	-	V	VDD_ IO = 4.5V
Output High Current (I/O) PA PB4~PB7 PB0~PB3/PC PD/PE/PF	 I_{OH1} I_{OH2} I_{OH3} I_{OH4}	 9.1 11.2 7 4.2	 13 16 10 6	 16.9 20.8 13 7.8	mA	VDD_ IO = 4.5V, V_{OH} = 3.15V
Output Sink Current (I/O) PA4~PA7 PB4~PB7 PA0~PA3/PB0~PB3 PD/PE/PF	 I_{OL1} I_{OL2} I_{OL3} I_{OL4}	 25 15 5.6 4.9	 50 30 8 7	 75 45 10.4 9.1	mA	VDD_ IO = 4.5V, V_{OL} = 1.35V
Input Pull-Low Resistor PA(weak pull) PA(strong pull) PB~PF	R_{PL}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 4.5V
Input Pull-High Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PH}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 0V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	3.5	-	8	V	VDD_REGIN = 4.5V, no load
OSC Resistor	R_{OSC}	-	22	-	KΩ	F_{OSC} = 24MHz @ 4.5V
OSC32K Resistor	R_{OSC32k}	-	3	-	MΩ	F_{OSC32} = 32768Hz @ 4.5V
CPU Clock	F_{CPU}	-	-	12	MHz	F_{CPU} = F_{OSC}/2 @ 2.7V

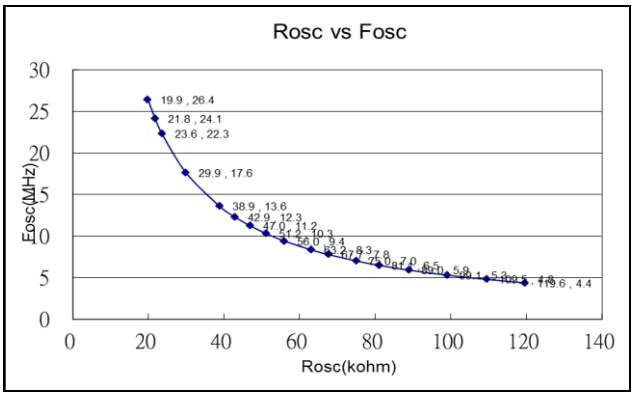
Note: V_{LCD} should be higher than VDD_IO to prevent abnormal functions.

7.3. DC Characteristics(VDD_REGIN= 3.0V, 2-battery Application, Internal Regulator Output Disabled, TA=25℃)

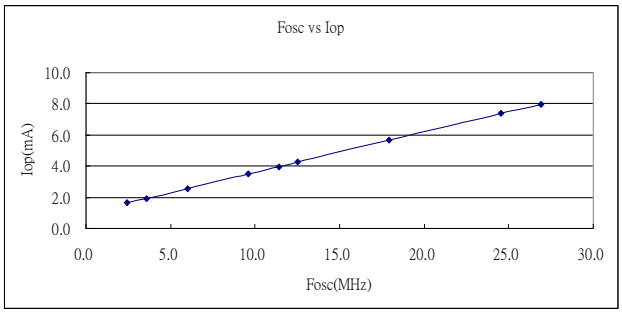
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD_REGIN	2.3	-	3.6	V	For 2-battery
Operating Current	I_{OP1}	-	5	8	mA	F_{CPU} = 8.0MHz @ 3.0V F_{XTAL} = 16.0MHz, no load, DAC disabled.
	I_{OP2}	-	7	10	mA	F_{CPU} = 12.0MHz @ 3.0V F_{ROSC} = 24.0MHz, no load, DAC disabled.
Halt Current	I_{HALT}	-	40	65	μA	VDD_REGIN = 3.3V, 32K X'tal ON, Strobe off, LCD ON, 1/7 Bias, VLCD=7.06 V, no LCD panel
Standby Current (Regulator off)	I_{STBY}	-	1	5	μA	VDD_REGIN = 3.0V, all off
Input High Level(PA/PB/PC) (PD/PE/PF)	V_{IH1} V_{IH2}	-	1.8 1.5	-	V	VDD_IO = 3.0V
Input Low Level(PA/PB/PC) (PD/PE/PF)	V_{IL1} V_{IL2}	-	1.2 1.4	-	V	VDD_ IO = 3.0V
Output High Current (I/O) PA PB4~PB7 PB0~PB3/PC PD/PE/PF	 I_{OH1} I_{OH1} I_{OH2} I_{OH3}	 4.2 5.6 3.5 2.1	 6 8 5 3	 7.8 10.4 6.5 3.9	mA	VDD_ IO = 3.0V, V_{OH} = 2.1V
Output Sink Current (I/O) PA4~PA7 PB4~PB7 PA0~PA3/PB0~PB3 PD/PE/PF	 I_{OL1} I_{OL2} I_{OL3} I_{OL4}	 13 8 3.2 3.5	 25 16 4.5 5	 37 24 5.9 6.5	mA	VDD_ IO = 3.0V, V_{OL} = 0.9V
Input Pull-Low Resistor PA(weak pull) PA(strong pull) PB~PF	R_{PL}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 3.0V
Input Pull-High Resistor PA(weak pull) PA(strong pull) PB,PC	R_{PH}	 100 35 35	 150 50 50	 200 65 65	KΩ	V_{IN} = 0V
LCD Driver Voltage (V_{LCD} - VSS)	V_{LCD}	3.5	-	8	V	VDD_ IO = 3.0V
OSC Resistor	R_{OSC}	-	33	-	KΩ	F_{OSC} = 16MHz @ 3.0V
OSC32K Resistor	R_{OSC32k}	-	3	-	MΩ	F_{OSC32} = 32768Hz @ 3.0V
CPU Clock	F_{CPU}	-	-	8	MHz	F_{CPU} = F_{OSC}/2 @ 2.3V

Note: V_{LCD} should be higher than VDD to prevent abnormal functions.

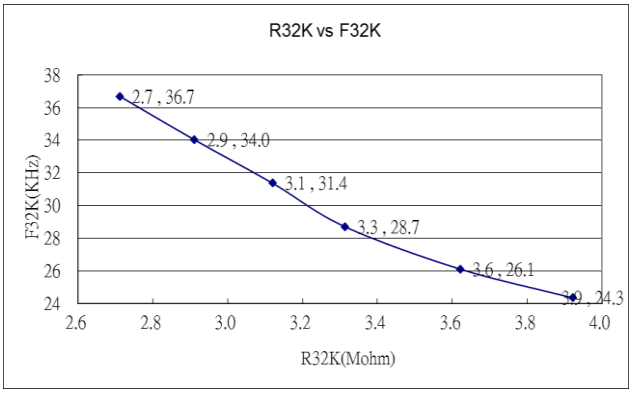
7.4. The Relationship between the R_{OSC} and the F_{OSC}



7.6. The Relationship between the F_{CPU} and the I_{OP}



7.5. The Relationship between the R32K and the F32K



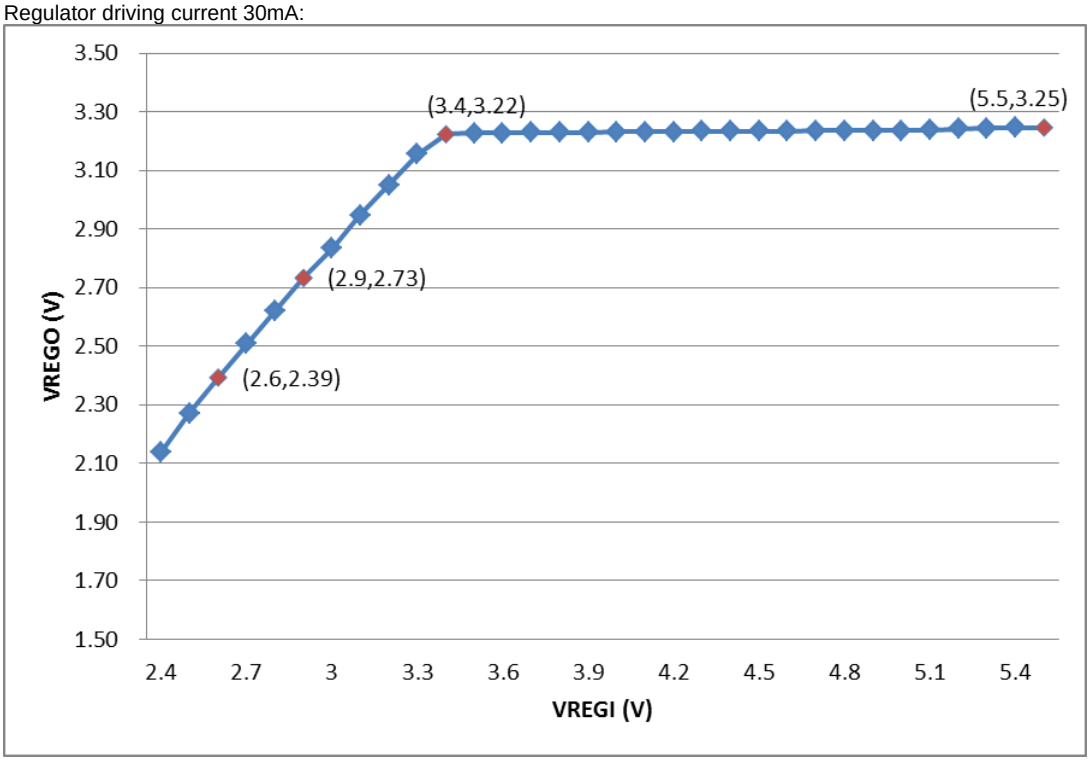
7.7. DAC Characteristics (VDD_REGIN = 5.0V, TA = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n (5V@0.45W)	-	-	0.18	-	%
Noise at No Signal	-	-	-64	-	dBr A
Dynamic Range(-60dB)	-	-	-64	-	dBr A

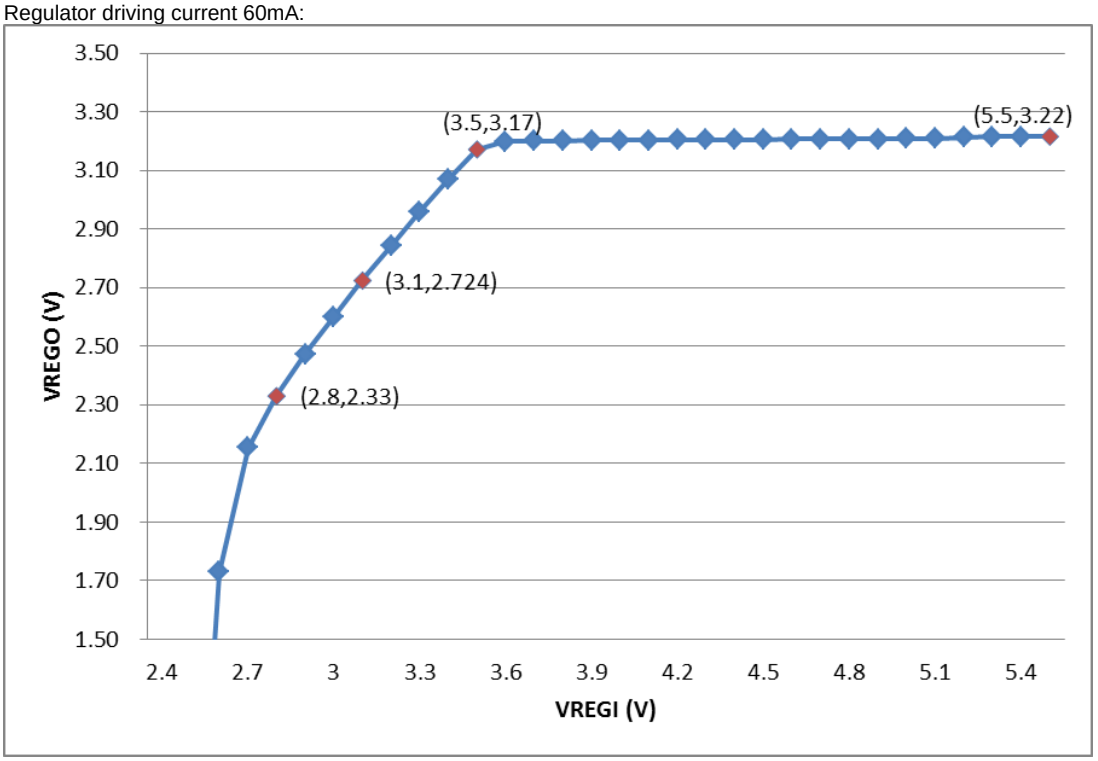
7.8. Regulator Characteristics (TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VREGI	2.3	4.5	5.5	V	
Maximum Current Output	IREGO	-	-	60	mA	VDD_REGIN = 4.5V, △VDD33V_REGOUT < 220 mV
Output Voltage	VREGO	3.135	3.3	3.465	V	VREGI > 3.5V
Standby Current	IRGES	-	2.5	-	uA	

Regulator driving current 30mA:

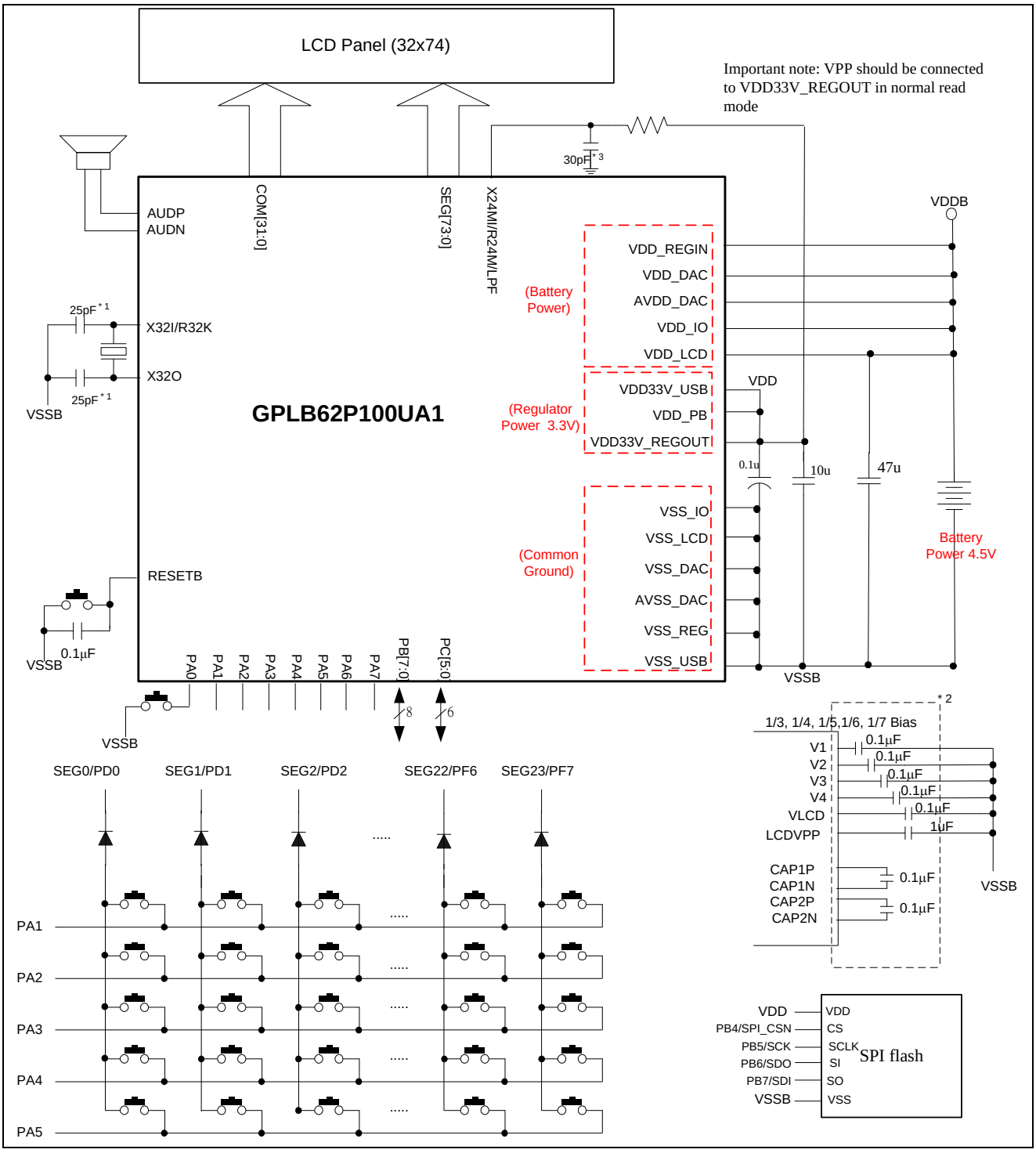


Regulator driving current 60mA:



8. APPLICATION CIRCUITS

8.1. 2,368 Dots LCD Driver, 74 Segments × 32 Commons, 3-battery Application, Internal 3.3V Regulator Enabled, ROSC24M XTAL32K Selected, PB[4:7] Connected to 3.3V SPI Flash using Internal 3.3V Regulator Power - (1)

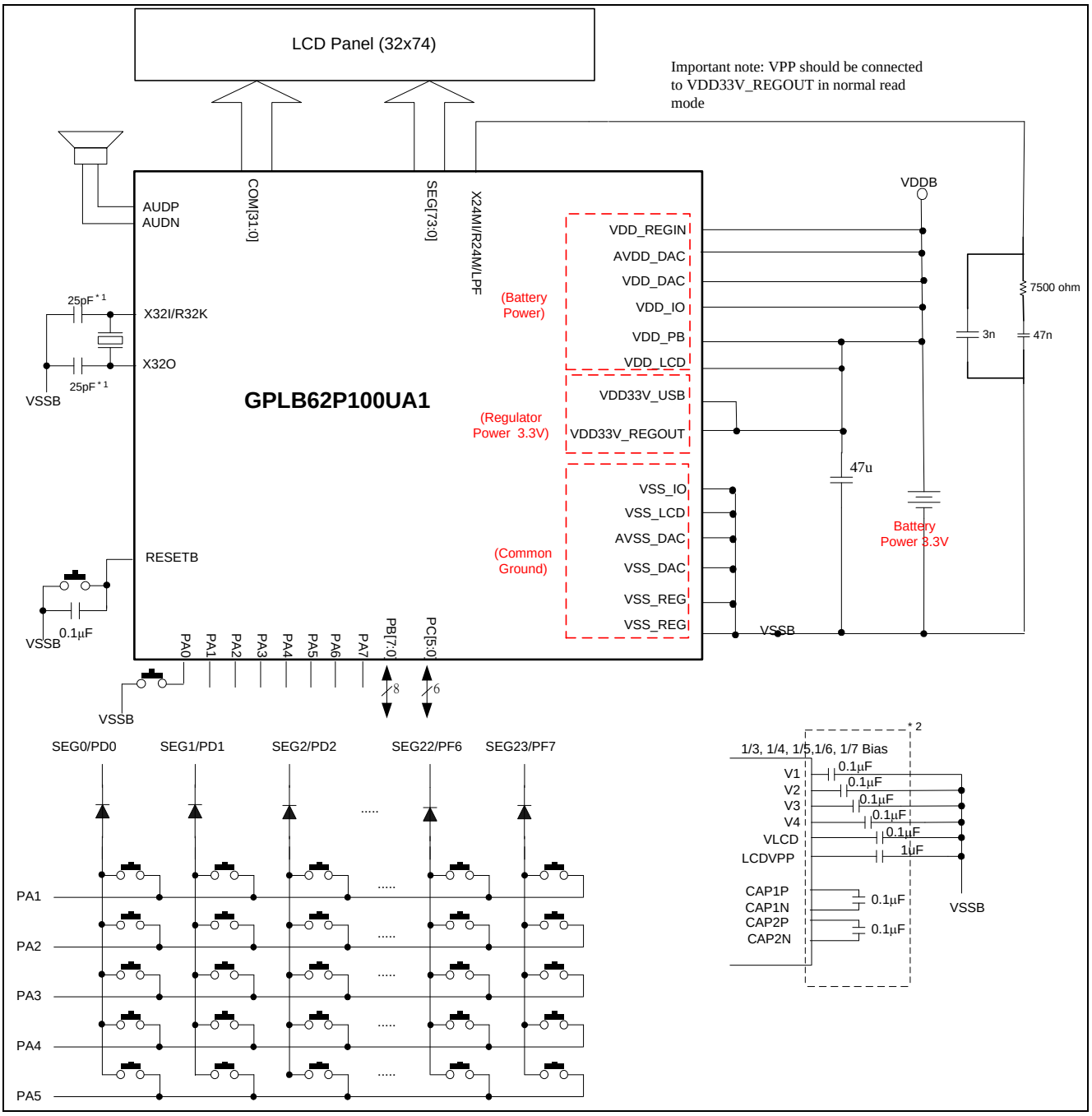


Note*1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).

Note*2: These capacitor values are for design guidance only. The ratio of LCDVPP capacitance to CAP1N/CAP1P/CAP2N/CAP2P capacitance is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. In a large LCD panel, the followings are recommended: 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for LCDVPP and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N.

Note*3: This capacitor can be removed if this node is immune from noise.

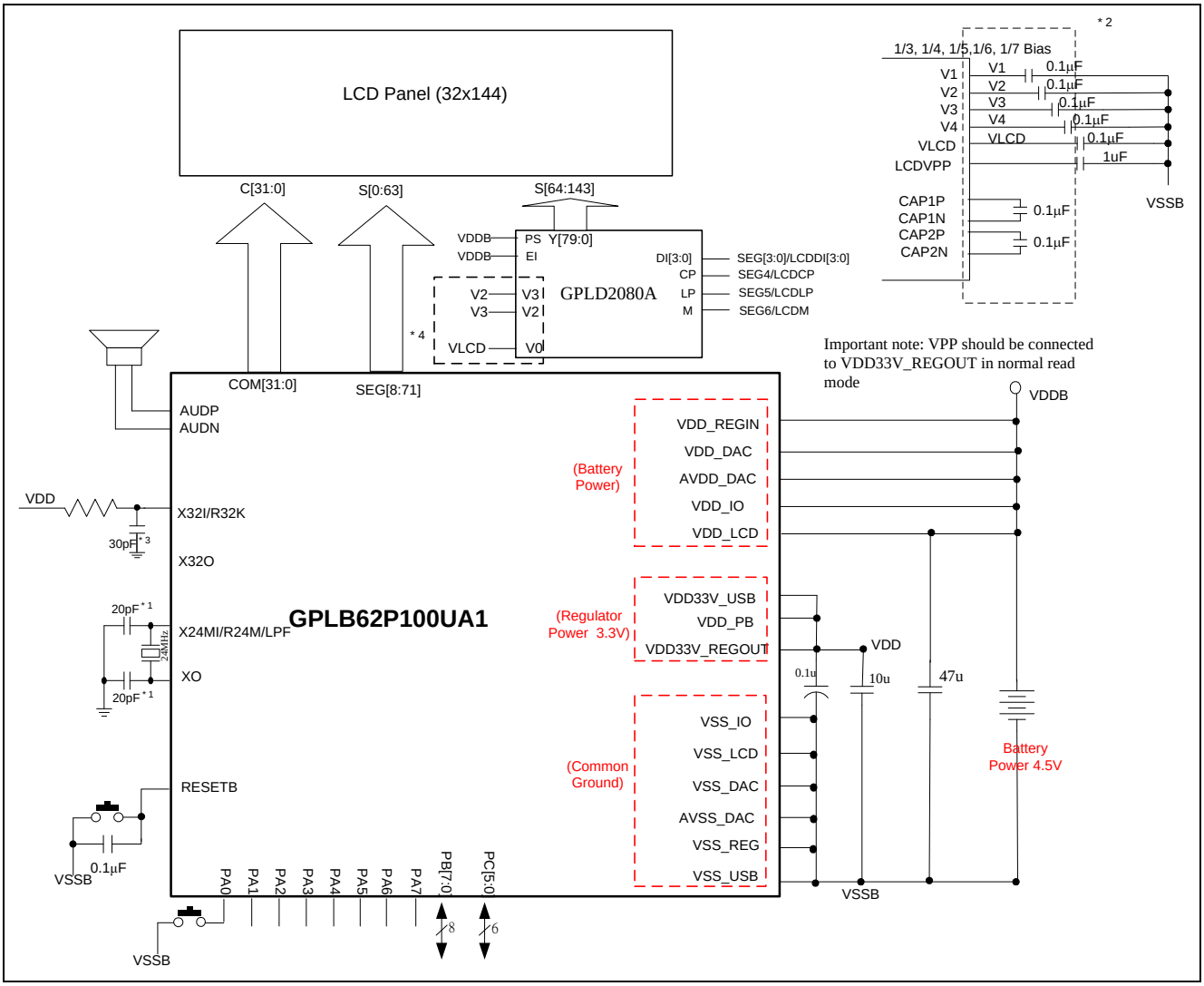
8.2. 2,368 Dots LCD Driver, 74 Segments × 32 Commons, Internal 3.3V Regulator Disabled, 2-battery Application, System PLL XTAL32K Selected - (2)



Note*1: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and CL1=CL2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF).

Note*2: These capacitor values are for design guidance only. The ratio of LCDVPP capacitance to CAP1N/CAP1P/CAP2N/CAP2P capacitance is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. In a large LCD panel, the followings are recommended: 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for LCDVPP and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N.

8.3. 4,608 Dots LCD, Extended LCD Driver Enabled, Connected to GPLD2080A, 144 Segments (Internal 64 Segments + External 80 Segments) × 32 Commons, 3-battery Application, Internal 3.3V Regulator Enabled, XTAL24M ROSC32K Selected - (3)



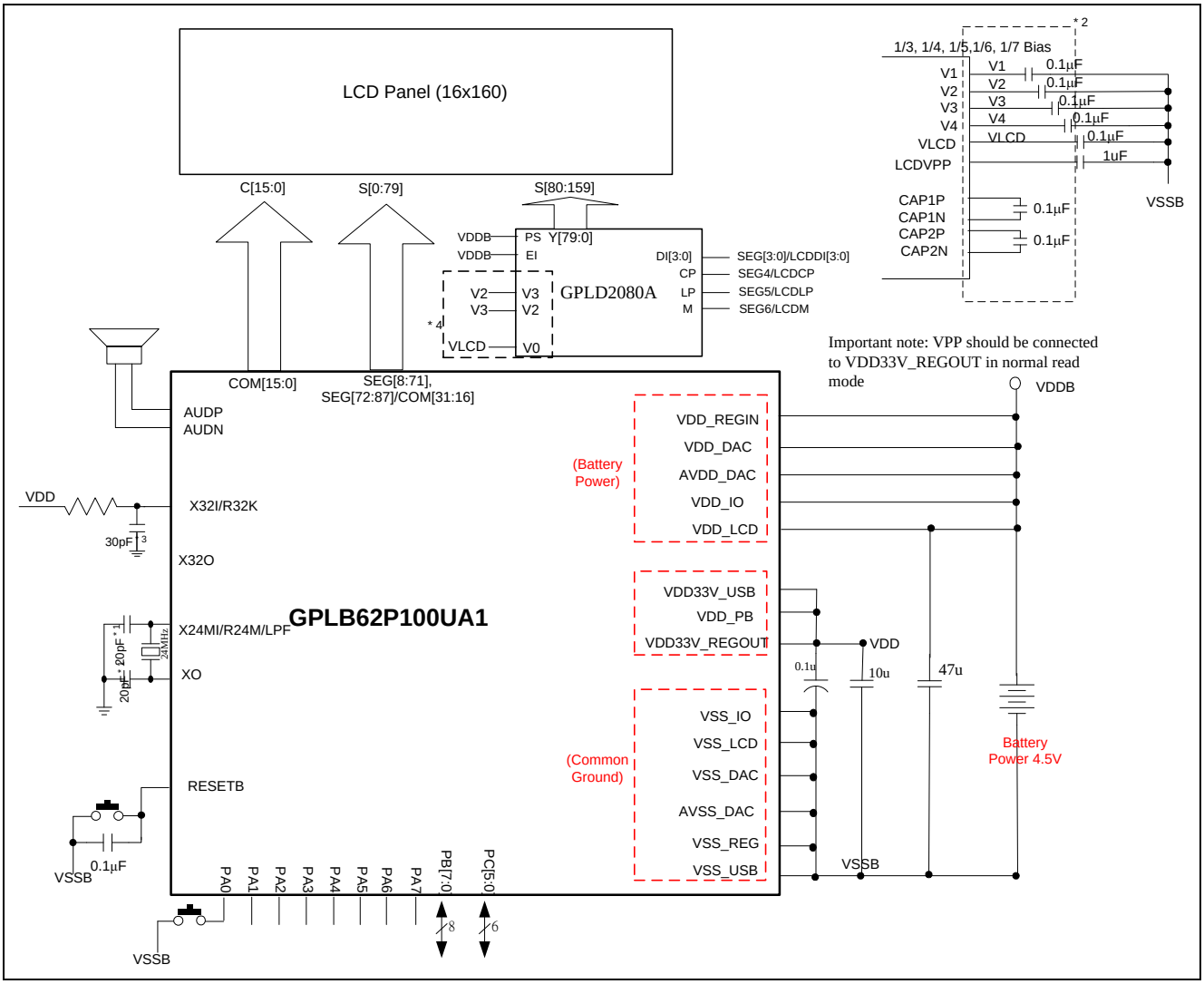
Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. The ratio of LCDVPP capacitance to CAP1N/CAP1P/CAP2N/CAP2P capacitance is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. In a large LCD panel, the followings are recommended: 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for LCDVPP and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N.

Note*3: This capacitor can be removed if this node is immune from noise.

Note*4: Take care of the LCD power pin connection. GPLB62P100UA1's VLCD connects to GPLD2080A's V0. GPLB62P100UA1's V3 connects to GPLD2080A's V2. GPLB62P100UA1's V2 connects to GPLD2080A's V3.

8.4. 2,560 Dots LCD, Extended LCD Driver Enabled, Connected to GPLD2080A, 160 Segments (Internal 80 Segments + External 80 Segments) × 16 Commons, 3-battery Application, Internal 3.3V Regulator Enabled, XTAL24M ROSC32K Selected - (4)



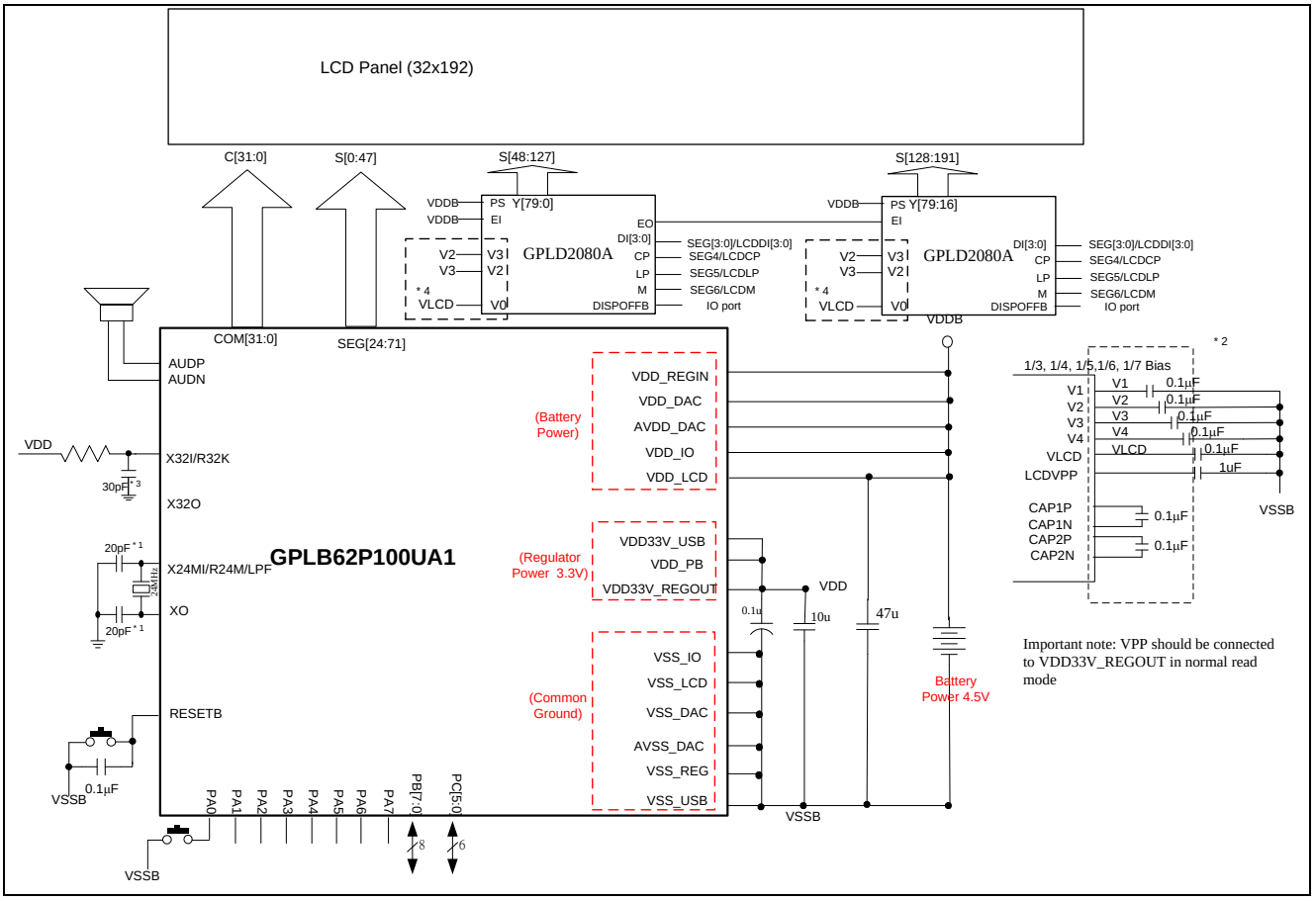
Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. The ratio of LCDVPP capacitance to CAP1N/CAP1P/CAP2N/CAP2P capacitance is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. In a large LCD panel, the followings are recommended: 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for LCDVPP and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N.

Note*3: This capacitor can be removed if this node is immune from noise.

Note*4: Take care of the LCD power pin connection. GPLB62P100UA1's VLCD connects to GPLD2080A's V0. GPLB62P100UA1's V3 connects to GPLD2080A's V2. GPLB62P100UA1's V2 connects to GPLD2080A's V3.

8.5. 6144 Dots LCD, Extended LCD Driver Enabled, Connected to two GPLD2080A, 192 Segments (Internal 48 Segments + External 144 Segments) × 32 Commons, 3-battery Application, Internal 3.3V Regulator Enabled, XTAL24M ROSC32K Selected - (5)



Note*1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

Note*2: These capacitor values are for design guidance only. The ratio of LCDVPP capacitance to CAP1N/CAP1P/CAP2N/CAP2P capacitance is recommended to be 10:1. Generally, capacitance of VLCD and V1~V4 is 0.1uF and cannot be larger than capacitance of LCDVPP. In a large LCD panel, the followings are recommended: 1uF capacitance for VLCD and V1~V4, 2.2uF capacitance for LCDVPP and 0.22uF capacitance for CAP1P/CAP1N/CAP2P/CAP2N.

Note*3: This capacitor can be removed if this node is immune from noise.

Note*4: Take care of the LCD power pin connection. GPLB62P100UA1's VLCD connects to GPLD2080A's V0. GPLB62P100UA1's V3 connects to GPLD2080A's V2. GPLB62P100UA1's V2 connects to GPLD2080A's V3.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPLB62P100UA1 - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Jul. 28, 2016	1.2	update IOH/IOL variation range	11-13
Aug. 12, 2014	1.1	update DC and regulator characteristic and its application circuit.	
May. 16, 2013	1.0	Original	22