

Multi-Phase 6-Core Step-Down Converter

Check for Samples: [LP8755](#)

FEATURES

- **Six High-Efficiency Step-Down DC/DC Converter Cores:**
 - **Max Output Current 15A**
 - **Cores Bundled to a 6-Phase Converter**
 - **Load Current Reporting**
 - **Programmable Over-Current Protection (OCP)**
 - **Auto PWM/PFM and Forced-PWM Operations and Automatic Low Power-Mode Setting**
 - **Auto Phase Adding/Shedding**
 - **Remote Differential Feedback Voltage Sensing**
 - **Ramp Control**
 - **V_{OUT} Range = 0.6V to 1.67V**
- **I²C-Compatible Interface which Supports Standard (100 kHz), Fast (400 kHz), and High-Speed (3.4 MHz) Modes**
- **Four Pin-Selectable I²C Addresses**
- **Interrupt Function with Programmable Masking**
- **Output Short-Circuit and Input Over-voltage Protection**
- **Spread Spectrum for EMI Reduction**
- **Over-Temperature Protection (OTP)**
- **Under-Voltage Lock-out (UVLO)**
- **49-Bump 0.4 mm Pitch DSBGA Package, 2.99 mm x 2.85 mm**

APPLICATIONS

- **Smart Phones, eBooks and Tablets**
- **GSM, GPRS, EDGE, LTE, CDMA and WCDMA Handsets**
- **Gaming Devices**

DESCRIPTION

The LP8755 is designed to meet the power management requirements of the latest applications processors in mobile phones and similar portable applications. The device contains six step-down DC/DC converter cores, which are bundled together in a 6-phase buck converter. The device is fully controlled by a SmartReflex™-compatible interface or an I²C-compatible serial interface.

The LP8755 focuses on high-efficiency, step-down conversion over a wide output current range. The step-down converter enters a low-power mode at light load for maximum efficiency. The regulator supports remote differential voltage sensing to compensate I*R drop between the regulator output and the load. A selectable spread spectrum mode reduces radiated emissions.

The protection features include short-circuit protection, current limits, output OVP, input OVP, UVLO, temperature warning, and shutdown functions. Several error flags are provided for status information of the IC. In addition, I²C read-back includes total load current and load current for each buck core: The LP8755 has the ability to sense current being delivered to the load without the addition of current sense resistors. During startup, the device controls the output slew rate to minimize output voltage overshoot and the inrush current.



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Typical Application Circuit

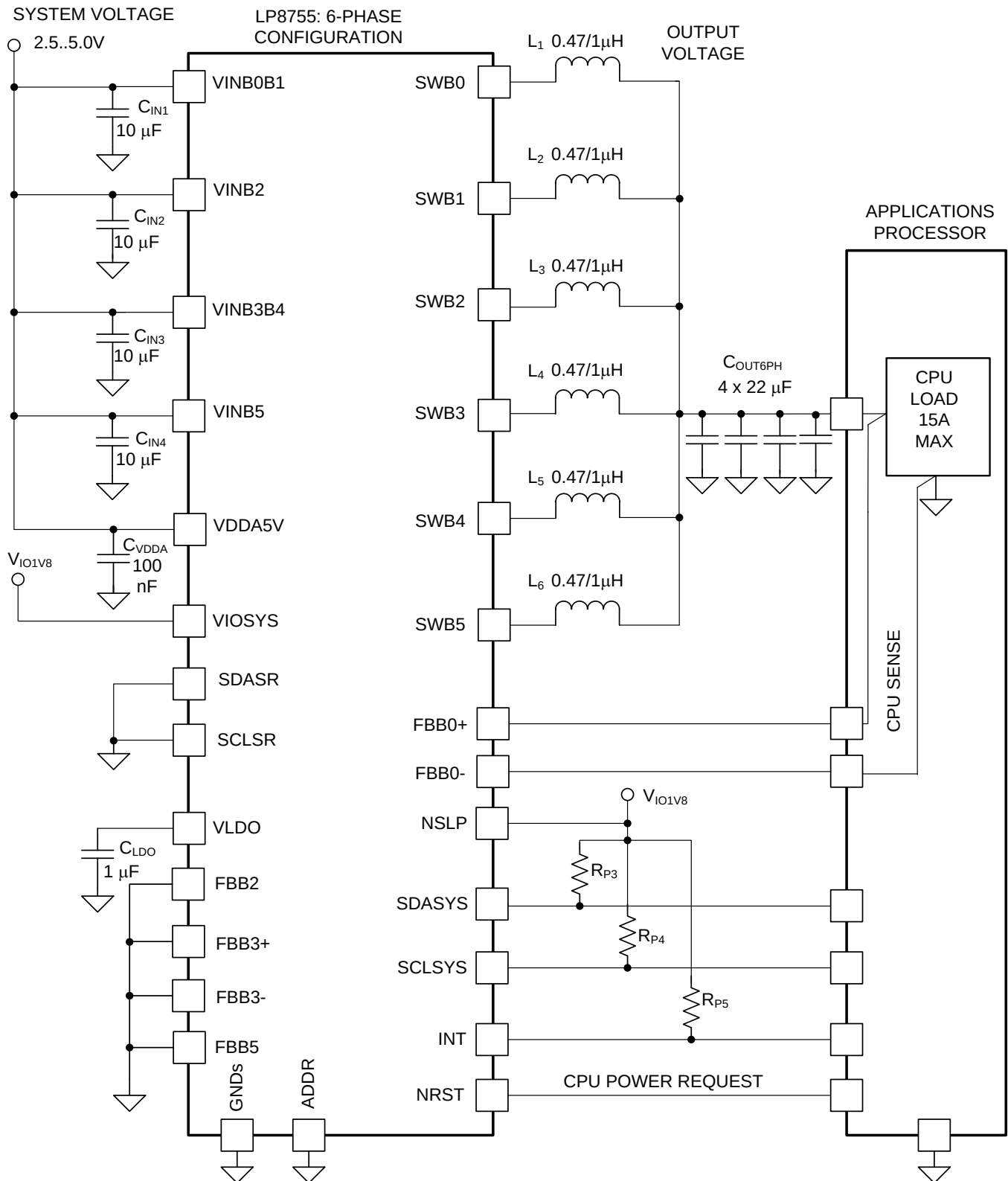


Figure 1.

Pin Assignments

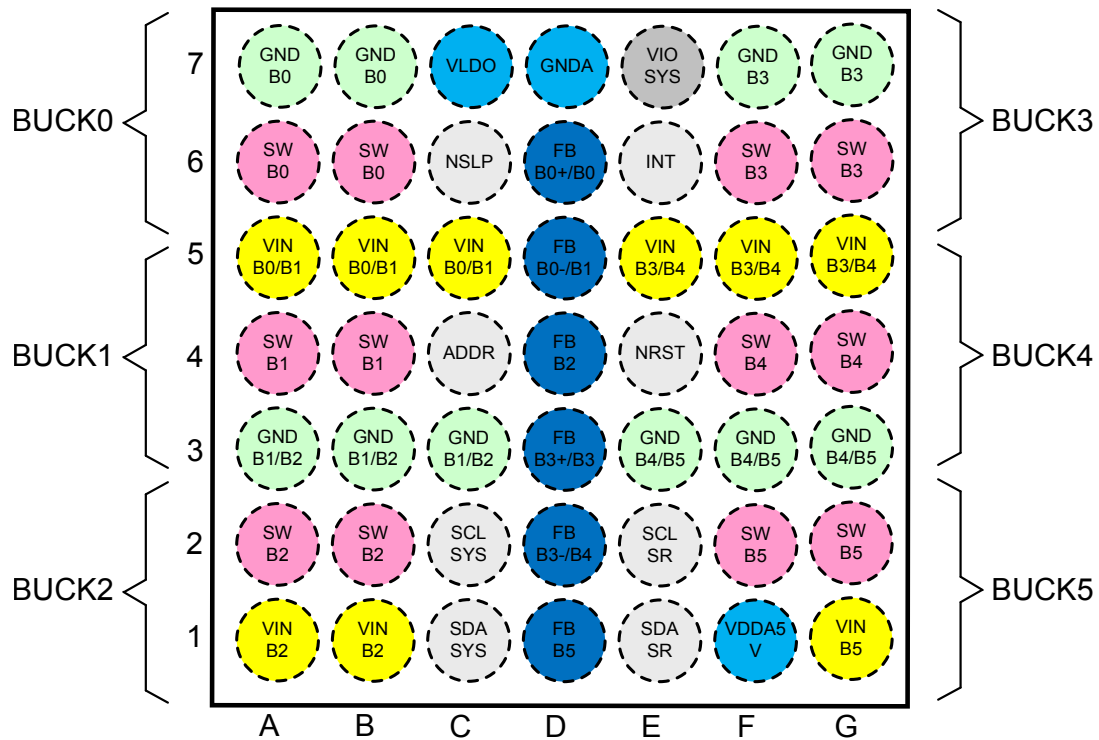


Figure 2. Top View

Table 1. Pin Descriptions

Pin(s)	Name	Type ⁽¹⁾	Function
A1, B1	VINB2	P	Input for Buck 2. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A2, B2	SWB2	A	Buck 2 switch node
A3, B3, C3	GNDB1/B2	G	Power Ground for Buck 1 and Buck 2
A4, B4	SWB1	A	Buck 1 switch node
A5, B5, C5	VINB0/B1	P	Input for Buck 0 and Buck 1. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A6, B6	SWB0	A	Buck 0 switch node
A7, B7	GNDB0	G	Power Ground for Buck 0
C1	SDASYS	DI/O	Serial interface data input and output for system access. Connect a pull-up resistor.
C2	SCLSYS	DI	Serial interface clock input for system access. Connect a pull-up resistor.
C4	ADDR	DI	Serial bus address selection. Connect to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h) or SCLSYS (addr = 63h).
C6	NSLP	DI	Full Power to Low Power state transition control signal (active LOW)
C7	VLDO	A	Internal supply voltage capacitor pin. A ceramic low ESR 1.0 μ F capacitor should be connected from this pin to GND. The LDO voltage is generated internally, do NOT supply or load this pin externally.
D1	FBB5	A	N/A for six-phase converter. Connect to GND.
D2	FBB3-/B4	A	N/A for six-phase converter. Connect to GND.
D3	FBB3+/B3	A	N/A for six-phase converter. Connect to GND.
D4	FBB2	A	N/A for six-phase converter. Connect to GND.
D5	FBB0-/B1	A	Remote sensing (negative). Connect to the respective sense pin of the processor or to the negative power supply trace of the processor as close as possible to the processor.
D6	FBB0+/B0	A	Remote sensing (positive). Connect to the respective sense pin of the processor or to the positive power supply trace of the processor as close as possible to the processor.
D7	GNDA	G	Ground
E1	SDASR	DI/O	Serial Interface data input and output for Dynamic Voltage Scaling (DVS). Connect a pull-up resistor / connect to GND if not used.
E2	SCLSR	DI	Serial Interface clock input for Dynamic Voltage Scaling (DVS). Connect a pull-up resistor / connect to GND if not used.
E3, F3, G3	GNDB4/B5	G	Power Ground for Buck 4 and Buck 5
E4	NRST	A	Reference input for Dynamic Voltage Scaling (DVS) interface. Setting NRST input HIGH triggers startup sequence.
E5, F5, G5	VINB3/B4	P	Input for Buck 3 and Buck 4. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
E6	INT	DO	Open-drain interrupt output. Active LOW.
E7	VIOSYS	A	This pin shall be tied to the system I/O-voltage. Bias supply voltage for the device. Enables the I/O interface: All registers are accessible via serial bus interface when this pin is pulled high. An internal power-on reset (POR) occurs when VIOSYS is toggled low/high. The I ² C host should allow at least 500 μ s before sending data to the LP8755 after the rising edge of the VIOSYS line.
F1	VDDA5V	P	Input for Analog blocks
F2, G2	SWB5	A	Buck 5 switch node
F4, G4	SWB4	A	Buck 4 switch node
F6, G6	SWB3	A	Buck 3 switch node
F7, G7	GNDB3	G	Power Ground for Buck 3
G1	VINB5	P	Input for Buck 5. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.

(1) P = Power Connection Pin, A = Analog Pin, G = Ground Pin, DI/O = Digital Input/Output Pin, DI = Digital Input Pin, DO = Digital Output Pin



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

INPUT VOLTAGE		
Voltage on Power Connections (VIO SYS, VDDA5V, VINBxx)		–0.3V to +6.0V
Voltage on Logic Pins (Input or Output Pins) (SCL SYS, SDASYS, NRST, NSLP, ADDR, INT, SCLSR, SDASR)		–0.3V to +6.0V
Buck switch nodes (SWBxx)		(GND–0.2V) to (VINBxx + 0.2V) with +6.0V max
VLDO, FBB0+/B0, FBB0–/B1, FBB2, FBB3+/B3, FBB3–/B4, FBB5		–0.3V to +2.0V
All other analog pins		–0.3V to +6.0V
TEMPERATURE		
Junction Temperature (T _{J-MAX})		+150°C
Storage Temperature Range		–65°C to +150° C
Maximum Lead Temperature (Soldering, 10 sec.) ⁽³⁾		260°C
ESD RATING ⁽⁴⁾		
All Pins	Human Body Model	1 kV
	Charge Device Model	250V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (2) All voltage values are with respect to network ground terminal.
- (3) For detailed soldering specifications and information, please refer to [Application Note 1112](#): DSBGA Wafer Level chip Scale Package (AN-1112)
- (4) The Human Body Model applicable standard JESD22–A114C, and Charge Device Model applicable standard JESD22–C101.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		LP8755	UNITS
		YFQ	
		49 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	49.2	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	0.2	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	6.6	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	2.9	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	6.5	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS ⁽¹⁾⁽²⁾

INPUT VOLTAGE	
Voltage on Power Connections (VDDA5V, VINBxx)	2.5V to 5.0V
Voltage on VIOSYS	1.8V to smaller of 3.3V or VINBxx
SCLSYS, SDASYS, ADDR	0V to voltage on VIOSYS
SCLSR, SDASR, NSLP, INT	0V to voltage on NRST
NRST	0V to 1.8V
TEMPERATURE	
Junction Temperature (T _j)	–40°C to +125°C
Ambient Temperature (T _A) ⁽³⁾	–40°C to +85°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (2) All voltage values are with respect to network ground terminal.
- (3) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

GENERAL ELECTRICAL CHARACTERISTICS ⁽¹⁾⁽²⁾

Typical values and limits appearing in normal type apply for T_A = +25°C. Unless otherwise noted, V_{DDA5V} = V_{INBxx} = 3.7V; V_{IOSYS} = 1.8V. Limits appearing in boldface type apply over the entire ambient temperature range T_A = –40°C to +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CURRENTS						
I _{SHDN}	Shutdown Supply Current. Total current into power connections VDDA5V and VINBxx	V _{IOSYS} = 0V, NRST = 0V		0.1	2	μA
I _{STBY}	Standby Mode Supply Current. Total current into power connections VDDA5V and VINBxx	V _{IOSYS} = 1.8V, NRST = 0V		80		μA
I _{Active}	Active mode current consumption. Total current into power connections VDDA5V and VINBxx	PFM Mode, no load, one core active		0.4		mA
		Forced PWM Mode, no load, one core active		14.5		mA
LOGIC AND CONTROL INPUTS SCLSYS, SDASYS, ADDR						
V _{IL}	Input Low Level	V _{IOSYS} = 1.8V to 3.3V			0.3 x V _{IOSYS}	V
V _{IH}	Input High Level	V _{IOSYS} = 1.8V to 3.3V	0.7 x V _{IOSYS}			V
V _{hys}	Hysteresis of Schmitt trigger inputs (SCLSYS, SDASYS)		0.1 x V _{IOSYS}			V
C _i	Capacitance of pins	Note ⁽³⁾			4	pF
LOGIC AND CONTROL INPUTS SCLSR, SDASR, NSLP, NRST						
V _{IL}	Input Low Level	V _{NRST} = 1.8V			0.3 x V _{NRST}	V
V _{IH}	Input High Level	V _{NRST} = 1.8V	0.7 x V _{NRST}			V
V _{hys}	Hysteresis of Schmitt trigger inputs (SCLSR, SDASR)		0.1 x V _{NRST}			V
C _i	Capacitance of SCLSR and SDASR pins				4	pF
R _{IN}	Input Resistance	NRST Pull-down Resistor to GND		1200		kΩ

- (1) All voltage values are with respect to network ground terminal.
- (2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ.) numbers are not ensured, but do represent the most likely norm.
- (3) Maximum capacitance of SCLSYS or SDASYS line is 8 pF, if ADDR pin is connected to line for serial bus address selection.

GENERAL ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾ (continued)

Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBxx} = 3.7\text{V}$; $V_{IOSYS} = 1.8\text{V}$. Limits appearing in boldface type apply over the entire ambient temperature range $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL_NRST}	Input Low Level NRST				0.54	V
V_{IH_NRST}	Input High Level NRST		1.3			V
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output Low Level	Voltage on INT-pin, $I_{SINK} = 3\text{mA}$, $V_{NRST} = V_{IOSYS} = 1.8\text{V}$			0.4	V
		Voltage on SDASYS, SDASR, $I_{SINK} = 3\text{mA}$, $V_{NRST} = V_{IOSYS} = 1.8\text{V}$			0.36	
R_P	External Pull-up Resistor for INT	To I/O Supply		10		k Ω
ALL LOGIC AND CONTROL INPUTS						
I_{LEAK}	Input Current	All Logic Inputs over pin voltage range. Note that NRST pin does have an 1.2 M Ω internal pull-down resistor and current through this resistor is not included into I_{LEAK} rating.	-1		+1	μA

6-PHASE BUCK ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBxx} = 3.7\text{V}$; $V_{IOSYS} = V_{NRST} = 1.8\text{V}$; $V_{OUT} = 1.1\text{V}$. Unless otherwise noted, specifications apply to the [Figure 34](#). Limits appearing in boldface type apply over the entire ambient temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. ⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage ⁽³⁾⁽⁴⁾	PWM Mode, $V_{OUTSET} = 0.6\text{V}$ to 1.67V , $I_{OUT} \leq 15\text{A}$ ⁽⁵⁾	0.975 x V_{OUTSET}	V_{OUTSET}	1.025 x V_{OUTSET}	V
		PFM Mode, $V_{OUTSET} = 0.6\text{V}$ to 1.67V , $I_{OUT} \leq 375\text{mA}$	0.975 x V_{OUTSET}	V_{OUTSET}	1.025 x V_{OUTSET}	V
		Low Power Mode, $V_{OUT} = 0.6\text{V}$ to 1.67V , $I_{OUT} \leq 30\text{mA}$	0.97 x V_{OUTSET}	V_{OUTSET}	1.03 x V_{OUTSET}	V
I_{LIMITP}	High Side Switch Current Limit	3.0A register setting ⁽⁴⁾	2700	3200	3700	mA
I_{LIMITN}	Low Side Switch Current Limit	Reverse current ⁽⁴⁾	650	850	1050	mA
V_{OUT}	Output voltage range	Programmable by register setting	0.6	1.0	1.67	V
f_{SW}	Switching Frequency	$2.5\text{V} \leq V_{INBxx} \leq 5.0\text{V}$, $0.6\text{V} \leq V_{OUTSET} < 0.8\text{V}$ ⁽⁴⁾	2.7	3.0	3.4	MHz
		$2.5\text{V} \leq V_{INBxx} \leq 5.0\text{V}$, $0.8\text{V} \leq V_{OUTSET} \leq 1.67\text{V}$ ⁽⁴⁾	3.6	4.0	4.5	
$R_{DS(on)_P}$	Pin-Pin Resistance for PFET	Test Current = 200 mA; Split FET		120		m Ω
		Test Current = 200 mA; Full FET		60		

- (1) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
- (2) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8755 device depends greatly on the care taken in designing the Printed Wiring Board (PWB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
- (3) Due to the nature of the converter operating in PFM mode/Low-Power Mode, the Feedback Voltage accuracy specification is for the lower point of the ripple. Thus the converter will position the average output voltage typically slightly above the nominal PWM-mode output voltage.
- (4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
- (5) The power switches in the LP8755 are designed to operate continuously with currents up to the switch current limit thresholds. However, when continuously operating at high current levels there will be significant heat generated within the IC and thus sustained total DC current which the device can support is typically limited by thermal constraints. Thermal issues will become extremely important when designing PWB and the thermal environment of the LP8755. PWB with high thermal efficiency is required to ensure the junction temperature is kept below $+125^\circ\text{C}$. Completing thermal analyses in early stages of the product design process is highly recommended to predict thermal performance at board level. Under high current load conditions the serial bus master device must monitor the temperature of the converter using the Thermal warning feature, see [PROTECTION FEATURES CHARACTERISTICS](#). If the 2nd thermal warning is triggered at 120°C , the application must quickly decrease the load current to keep the converter within its recommended operating temperature.

6-PHASE BUCK ELECTRICAL CHARACTERISTICS (continued)

Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBxx} = 3.7\text{V}$; $V_{IOSYS} = V_{NRST} = 1.8\text{V}$; $V_{OUT} = 1.1\text{V}$. Unless otherwise noted, specifications apply to the [Figure 34](#). Limits appearing in **boldface** type apply over the entire ambient temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. ⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$R_{\text{DS(on)N}}$	Pin-Pin Resistance for NFET	$I_{\text{OUT}} = -200\text{ mA}$		50		mΩ
$I_{\text{LK_HS}}$	High-side Leakage Current	$V_{\text{SW}} = 0\text{V}$, Per Buck Core			2	μA
$I_{\text{LK_LS}}$	Low-side Leakage Current	$V_{\text{SW}} = 3.7\text{V} = V_{\text{INBxx}}$, Per Buck Core			2	μA
R_{PD}	Pull-down Resistor	Enabled via control register, Only active when converter disabled, Per Buck Core		250		Ω
$R_{\text{IN_FB}}$	Differential Feedback Input Resistance	Note ⁽⁶⁾	200	300	400	kΩ

(6) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

6-PHASE BUCK SYSTEM CHARACTERISTICS

These specification limits are ensured by design proving the component values in the [Figure 34](#) are used. Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBxx} = 3.7\text{V}$; $V_{IOSYS} = V_{NRST} = 1.8\text{V}$, $V_{OUT} = 1.1\text{V}$. Limits appearing in **boldface** type apply over the entire ambient temperature range for operation, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
K_{RAMP}	Ramp timer	Programmable via control register, Note ⁽⁴⁾				mV/μs
		RAMP_B0[2:0] = 000		30		
		RAMP_B0[2:0] = 001		15		
		RAMP_B0[2:0] = 010		7.5		
		RAMP_B0[2:0] = 011		3.8		
		RAMP_B0[2:0] = 100		1.9		
		RAMP_B0[2:0] = 101		0.94		
		RAMP_B0[2:0] = 110		0.47		
		RAMP_B0[2:0] = 111		0.23		
T_{START}	Startup Time	Time from NRST-HIGH to start of switching		25		μs
T_{RAMP}	V_{OUT} Rise Time	Time to ramp from 5% to 95% of V_{OUT}		20		μs

- (1) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
- (2) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8755 device depends greatly on the care taken in designing the Printed Wiring Board (PWB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
- (3) Specifications listed in this table are for 6-phase configuration only. Besides the default 6-phase, single-output voltage rail configuration, the 6 switcher cores can be bundled to a variety of different grouping configurations. For applications requiring other DC/DC converter configuration(s), please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) In the real application, achievable output voltage ramp profiles are influenced by a number of factors, including the amount of output capacitance, the load current level, the load characteristic (either resistive or constant-current), and the voltage ramp amplitude.

6-PHASE BUCK SYSTEM CHARACTERISTICS (continued)

These specification limits are ensured by design proving the component values in the [Figure 34](#) are used. Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBXX} = 3.7\text{V}$; $V_{IOSYS} = V_{NRST} = 1.8\text{V}$, $V_{OUT} = 1.1\text{V}$. Limits appearing in **boldface** type apply over the entire ambient temperature range for operation, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{\text{PFM-PWM}}$	PFM to PWM Switch-Over Current Threshold	Average output current, Programmable via control register, $V_{OUT} = 1.1\text{V}$, Note ⁽⁵⁾				mA
		PFM_EXIT_B0[2:0] = 000		100		
		PFM_EXIT_B0[2:0] = 001		125		
		PFM_EXIT_B0[2:0] = 010		150		
		PFM_EXIT_B0[2:0] = 011		175		
		PFM_EXIT_B0[2:0] = 100		225		
		PFM_EXIT_B0[2:0] = 101		275		
		PFM_EXIT_B0[2:0] = 110		325		
		PFM_EXIT_B0[2:0] = 111		375		
$I_{\text{PWM-PFM}}$	PWM to PFM Switchover Current Threshold	Average output current, Programmable via control register, $V_{OUT} = 1.1\text{V}$, Note ⁽⁵⁾				mA
		PFM_ENTRY_B0[2:0] = 000		50		
		PFM_ENTRY_B0[2:0] = 001		75		
		PFM_ENTRY_B0[2:0] = 010		100		
		PFM_ENTRY_B0[2:0] = 011		125		
		PFM_ENTRY_B0[2:0] = 100		175		
		PFM_ENTRY_B0[2:0] = 101		225		
		PFM_ENTRY_B0[2:0] = 110		275		
		PFM_ENTRY_B0[2:0] = 111		325		
I_{ADD}	Phase adding level	ADD_PH_B0[2:0] = 001		400		mA
		ADD_PH_B0[2:0] = 010		500		
		ADD_PH_B0[2:0] = 011		600		
		ADD_PH_B0[2:0] = 100		700		
		ADD_PH_B0[2:0] = 101		800		
		ADD_PH_B0[2:0] = 110		900		
		ADD_PH_B0[2:0] = 111		1000		
I_{SHED}	Phase shedding level	SHED_PH_B0[2:0] = 000		300		mA
		SHED_PH_B0[2:0] = 001		400		
		SHED_PH_B0[2:0] = 010		500		
		SHED_PH_B0[2:0] = 011		600		
		SHED_PH_B0[2:0] = 100		700		
		SHED_PH_B0[2:0] = 101		800		
		SHED_PH_B0[2:0] = 110		900		
ΔV_{OUT}	Line Regulation	$2.5\text{V} \leq V_{\text{INBXX}} \leq 5.0\text{V}$ $I_{\text{LOAD}} = 1\text{A}$, forced PWM		0.05		%/V
	Load Regulation in PWM mode of operation	$100\text{ mA} \leq I_{\text{LOAD}} \leq 10\text{A}$, Differential sensing enabled		0.2		%/A
	Transient load step response	AUTO (no ECO) mode, $I_{\text{OUT}} 0.5\text{ mA} \rightarrow 500\text{ mA} \rightarrow 0.5\text{ mA}$, 100 ns load step		± 30		mV
		PWM mode, $I_{\text{OUT}} 0.6\text{A} \rightarrow 2\text{A} \rightarrow 0.6\text{A}$, 400 ns load step		± 20		mV
		PWM mode, $I_{\text{OUT}} 1\text{A} \rightarrow 8\text{A} \rightarrow 1\text{A}$, 400 ns load step		± 60		mV
	Transient Line Response	V_{INBXX} stepping $3.3\text{V} \leftrightarrow 3.8\text{V}$, $t_r = t_f = 10\text{ }\mu\text{s}$, $I_{\text{OUT}} = 2000\text{ mA DC}$		± 15		mV

(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage, and the inductor current level.

6-PHASE BUCK SYSTEM CHARACTERISTICS (continued)

These specification limits are ensured by design proving the component values in the [Figure 34](#) are used. Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBxx} = 3.7\text{V}$; $V_{IOSYS} = V_{NRST} = 1.8\text{V}$, $V_{OUT} = 1.1\text{V}$. Limits appearing in **boldface** type apply over the entire ambient temperature range for operation, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	Output Current	DC load each phase			2500	mA
		Six phases combined ⁽⁶⁾			15000	
C_{OUT}	Output Capacitance	Effective capacitance during operation, $V_{OUT} = 0.6\text{V}$ to 1.67V , Min value over $T_A -40^\circ\text{C}$ to $+85^\circ\text{C}$	30	50		μF
C_{IN}	Input Capacitance on each input voltage rail ⁽⁷⁾	Effective capacitance during operation, $2.5\text{V} \leq V_{INBxx} \leq 5.0\text{V}$, Min value over $T_A -40^\circ\text{C}$ to $+85^\circ\text{C}$	2.5	10		μF
L	Output Inductance	Effective inductance during operation	0.25	0.47	1.0	μH
$I_{BALANCE}$	Current Balancing Accuracy	$I_{OUT} \geq 1000\text{ mA}$		< 10		%
GBW	Gain Bandwidth			1.2		MHz
V_{RIPPLE_PWM}	Output Voltage Ripple PWM Mode, One phase active ⁽⁸⁾	C_{OUT} ESR = 10 m Ω PWM mode, $I_{OUT} = 200\text{ mA}$ Switching Frequency = 4.0 MHz		7		mV _{PP}
V_{RIPPLE_PFM}	Output Voltage Ripple PFM Mode ⁽⁸⁾	C_{OUT} ESR = 10 m Ω PFM mode $I_{OUT} = 100\text{ }\mu\text{A}$		8		mV _{PP}
V_{RIPPLE_LP}	Output Voltage Ripple Low Power ⁽⁸⁾	C_{OUT} ESR = 10 m Ω PFM Low Power mode $I_{OUT} = 100\text{ }\mu\text{A}$		8		mV _{PP}

- (6) The power switches in the LP8755 are designed to operate continuously with currents up to the switch current limit thresholds. However, when continuously operating at high current levels there will be significant heat generated within the IC and thus sustained total DC current which the device can support is typically limited by thermal constraints. Thermal issues will become extremely important when designing PWB and the thermal environment of the LP8755. PWB with high thermal efficiency is required to ensure the junction temperature is kept below $+125^\circ\text{C}$. Completing thermal analyses in early stages of the product design process is highly recommended to predict thermal performance at board level. Under high current load conditions the serial bus master device must monitor the temperature of the converter using the Thermal warning feature, see [PROTECTION FEATURES CHARACTERISTICS](#). If the 2nd thermal warning is triggered at 120°C , the application must quickly decrease the load current to keep the converter within its recommended operating temperature.
- (7) In addition to these capacitors, at least one higher value capacitor like 22 μF should be placed close to the power pins. Note that cores B0-B1 and B3-B4 do have combined power input pins
- (8) Ripple voltage should be measured at C_{OUT} electrode on a well-designed PC board, using suggested inductors and capacitors and with a high-quality scope probe.

PROTECTION FEATURES CHARACTERISTICS

Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{\text{DDA5V}} = V_{\text{INBxx}} = 3.7\text{V}$; $V_{\text{IOSYS}} = V_{\text{NRST}} = 1.8\text{V}$. Unless otherwise noted, specifications apply to the [Figure 34](#). Limits appearing in boldface type apply over the entire ambient temperature range $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. ⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOLTAGE MONITORING						
V _{PG}	Power Good Threshold Voltage	Power good threshold for voltage decreasing, % of setting, V _{OUT} = 1.1V		90		%
V _{OVP}	Input Over-voltage Protection Trigger Point ⁽³⁾⁽⁴⁾	VIN rising. Voltage monitored on VDDA5V Power Bump	5.15	5.30	5.45	V
V _{UVLO}	Input Under-voltage Lockout (UVLO) turn-on threshold ⁽³⁾	VIN falling. Voltage monitored on VDDA5V Power Bump	2.15	2.25	2.35	V
V _{SCP}	Output short-circuit fault threshold	Detected by sensing the voltage on converter output with respect to GND		400		mV
t _{MASKSCP}	SCP masking time	Triggered by converter startup, Specified by design		400		μs
t _{MASKPG}	Power Good masking time	Triggered by converter startup, Specified by design		400		μs
		Triggered by VSET transition, Specified by design				
		Slew Rate setting mV/μs				
		30		50		μs
		15		100		
		7.5		200		
		3.8		400		
		1.9		800		
		0.94		1600		
		0.47		3200		
0.23		6400				
THERMAL SHUTDOWN AND MONITORING						
T _{SHUT}	Thermal Shutdown (TSD)	Threshold, Temperature rising		150		°C
		Hysteresis		25		
T _{WARN}	Thermal warning	Temperature rising, 1 st warning, Interrupt only		85		
		Hysteresis		10		
	Thermal warning prior to TSD	Temperature rising, 2 nd warning, Interrupt and flag set		120		
		Hysteresis		10		

- (1) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
- (2) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8755 device depends greatly on the care taken in designing the Printed Wiring Board (PWB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
- (3) Under-voltage lock-out (UVLO) and over-voltage protection (OVP) circuits shut down the LP8755 when the system input voltage is outside the desired operating range.
- (4) Limits for OVP trigger points apply when V_{IOSYS} is high. False OVP alarm may occur, if the input voltage rises close to 5V while V_{IOSYS} is low.

I²C-COMPATIBLE SERIAL BUS INTERFACE

Serial bus address is selected by the ADDR pin. Connect the pin to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h), or SCLSYS (addr = 63h). Both of the serial buses share the same address; that is, if addr = 60h is selected for the system bus, the SmartReflex bus will respond to the same address. Start conditions are used to secure the I²C slave address. During the I²C bus start condition, it is detected whether the ADDR is connected to SDASYS, SCLSYS, GND, or VIOSYS. The I²C host should allow at least 500 μ s before sending data to the LP8755 after the rising edge of the VIOSYS line.

These specifications are ensured by design. Typical values and limits appearing in normal type apply for $T_A = +25^\circ\text{C}$. Unless otherwise noted, $V_{DDA5V} = V_{INBxx} = 3.7\text{V}$; $V_{IOSYS} = V_{NRST} = 1.8\text{V}$. Limits appearing in **boldface** type apply over the entire ambient temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

Symbol	Parameter (See Figure 3 for Timing Diagram)	Conditions	Min	Typ	Max	Units
DIGITAL TIMING SPECIFICATIONS (SCL, SDA)⁽¹⁾⁽²⁾⁽³⁾						
f_{CLK}	Serial Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
		High-speed Mode, $C_b = 100\text{ pF (max)}$			3.4	MHz
		High-speed Mode, $C_b = 400\text{ pF (max)}^{(4)}$			1.7	MHz
t_{LOW}	SCL Low Time	Standard Mode	4.7			μ s
		Fast Mode	1.3			
		High-speed Mode, $C_b = 100\text{ pF (max)}$	160			ns
		High-speed Mode, $C_b = 400\text{ pF (max)}^{(4)}$	320			
t_{HIGH}	SCL High Time	Standard Mode	4.0			μ s
		Fast Mode	0.6			
		High-speed Mode, $C_b = 100\text{ pF (max)}$	60			ns
		High-speed Mode, $C_b = 400\text{ pF (max)}^{(4)}$	120			
$t_{\text{SU;DAT}}$	Data Setup Time	Standard Mode	250			ns
		Fast Mode	100			
		High-speed Mode	10			
$t_{\text{HD;DAT}}$	Data Hold Time	Standard Mode	0		3.45	μ s
		Fast Mode	0		0.9	
		High-speed Mode, $C_b = 100\text{ pF (max)}$	0		70	ns
		High-speed Mode, $C_b = 400\text{ pF (max)}^{(4)}$	0		150	
$t_{\text{SU;STA}}$	Setup time for a repeated start condition	Standard Mode	4.7			μ s
		Fast Mode	0.6			
		High-speed Mode	160			ns
$t_{\text{HD;STA}}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			μ s
		Fast Mode	0.6			
		High-speed Mode	160			ns
t_{BUF}	Bus free time between a stop and start condition	Standard Mode	4.7			μ s
		Fast Mode	1.3			
$t_{\text{SU;STO}}$	Setup time for a stop condition	Standard Mode	4.0			μ s
		Fast Mode	0.6			
		High-speed Mode	160			ns

(1) Unless otherwise stated, 'SDA' in this paragraph refers to both of the SDASR and SDASYS signals, and respectively 'SCL' refers to SCLSR and SCLSYS signals.

(2) C_b refers to the capacitance of one bus line. C_b is expressed in pF units. The specification table provided applies to both of the interfaces; SmartReflex™ and System interface.

(3) The power-on default setting for the system bus and the SmartReflex bus is High-speed-enabled, there is no handshaking required to initiate High speed. Handshake phase and 50 ns filter setting can be enabled via register if strict I²C compatibility and handshaking is required.

(4) For bus line loads C_b between 100 pF and 400 pF the timing parameters must be linearly interpolated.

I²C-COMPATIBLE SERIAL BUS INTERFACE (continued)

Serial bus address is selected by the ADDR pin. Connect the pin to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h), or SCLSYS (addr = 63h). Both of the serial buses share the same address; that is, if addr = 60h is selected for the system bus, the SmartReflex bus will respond to the same address. Start conditions are used to secure the I²C slave address. During the I²C bus start condition, it is detected whether the ADDR is connected to SDASYS, SCLSYS, GND, or VIOSYS. The I²C host should allow at least 500 µs before sending data to the LP8755 after the rising edge of the VIOSYS line.

These specifications are ensured by design. Typical values and limits appearing in normal type apply for T_A = +25°C. Unless otherwise noted, V_{DDA5V} = V_{INBXX} = 3.7V; V_{IOSYS} = V_{NRST} = 1.8V. Limits appearing in **boldface** type apply over the entire ambient temperature range, T_A = –40°C to +85°C.

Symbol	Parameter (See Figure 3 for Timing Diagram)	Conditions	Min	Typ	Max	Units
t _{rDA}	Rise time of SDA signal	Standard Mode			1000	ns
		Fast Mode	20		300	ns
		High-speed Mode, C _b = 100 pF (max)	10		80	ns
		High-speed Mode, C _b = 400 pF (max) ⁽⁴⁾	20		160	ns
t _{fDA}	Fall time of SDA signal	Standard Mode			300	ns
		Fast Mode	6.5		300	ns
		High-speed Mode, C _b = 100 pF (max)	10		80	ns
		High-speed Mode, C _b = 400 pF (max) ⁽⁴⁾	20		160	ns
t _{rCL}	Rise time of SCL signal	Standard Mode			1000	ns
		Fast Mode	20		300	ns
		High-speed Mode, C _b = 100 pF (max)	10		40	ns
		High-speed Mode, C _b = 400 pF (max) ⁽⁴⁾	20		80	ns
t _{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	High-speed Mode, C _b = 100 pF (max)	10		80	ns
		High-speed Mode, C _b = 400 pF (max) ⁽⁴⁾	20		160	ns
t _{fCL}	Fall time of a SCL signal	Standard Mode			300	ns
		Fast Mode	6.5		300	ns
		High-speed Mode, C _b = 100 pF (max)	10		40	ns
		High-speed Mode, C _b = 400 pF (max) ⁽⁴⁾	20		80	ns
C _b	Capacitive load for each bus line (SCL and SDA)				400	pF
t _{SP}	Pulse width of spike suppressed ⁽⁵⁾	Fast mode			50	ns
		High-speed mode			10	

(5) Spike suppression filtering on SCL, SCLSR, SDA and SDASR will suppress spikes that are less than the indicated width.

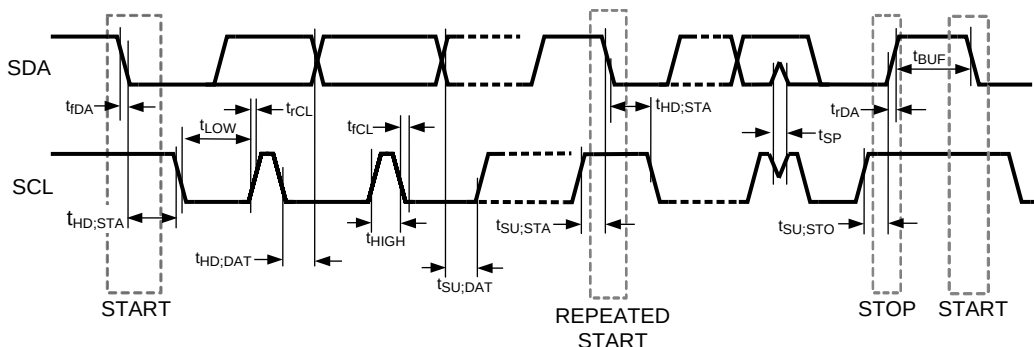


Figure 3. I²C Timing

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $V_{DDA5V} = V_{INBxx} = 3.7V$

Table 2. Table of Graphs

Item		FIGURE
Efficiency	vs Load current	4, 5, 6
	vs Input voltage	7, 8, 9
DC output voltage	vs Load current (low-power mode / PFM / PWM)	10
	vs Temperature	11
Line Regulation		12
Phase adding	vs Load current	13
Phase shedding	vs Load current	14
PFM Mode Current Consumption	vs Input voltage	15
PWM Mode Current Consumption	vs Input voltage	16
Phase Currents and Current Balancing		17, 18
Load Current Measured by LP8755	Compared with the real load current	19, 20
Transient load response		21, 22, 23
Transient line response	PWM	24
Output Voltage Ripple		25, 26
Startup	No load, 3A load	27, 28
Shut-down	No load	29
DC load ramp		30
Voltage transitions	vs Ramp settings	31
Not Power Good (nPG) Event		32
VOUT Short		33

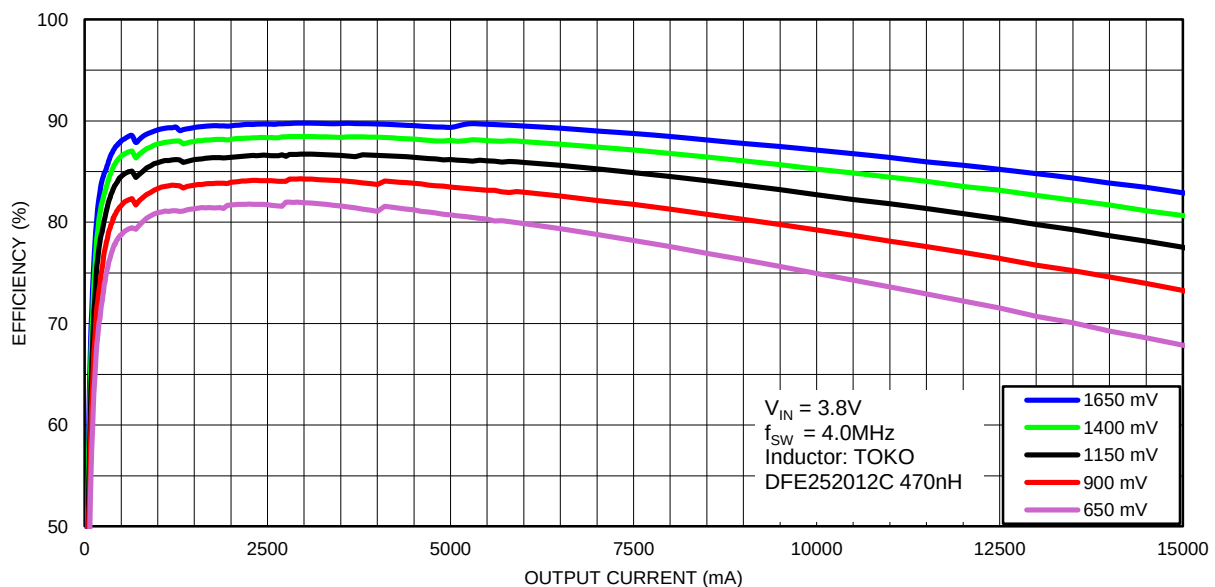


Figure 4. Efficiency vs Load Current in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

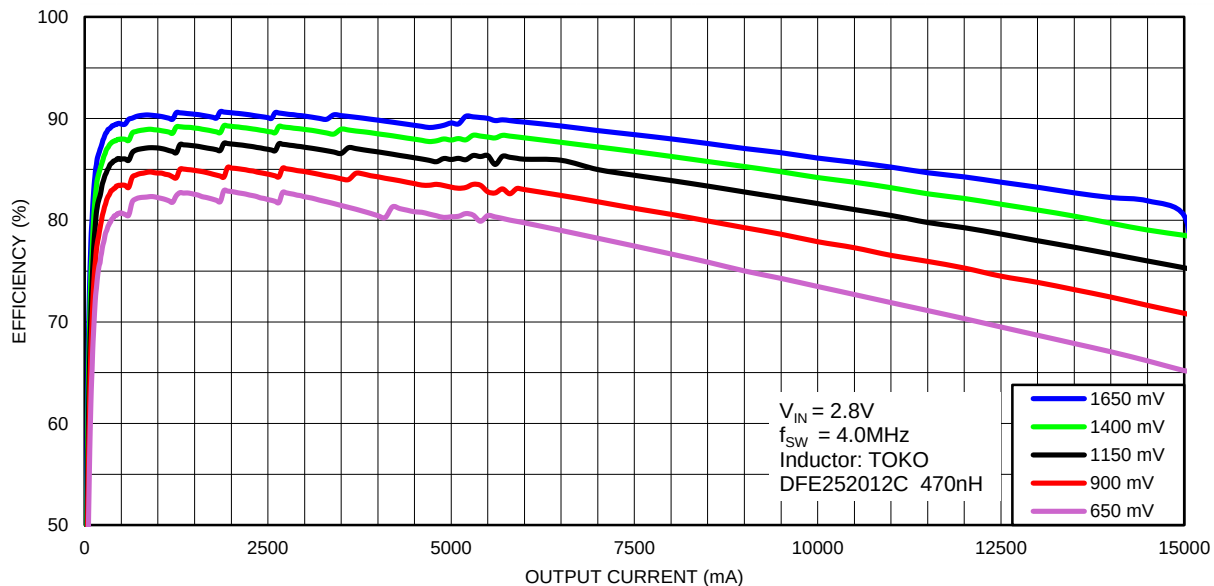


Figure 5. Efficiency vs Load Current in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

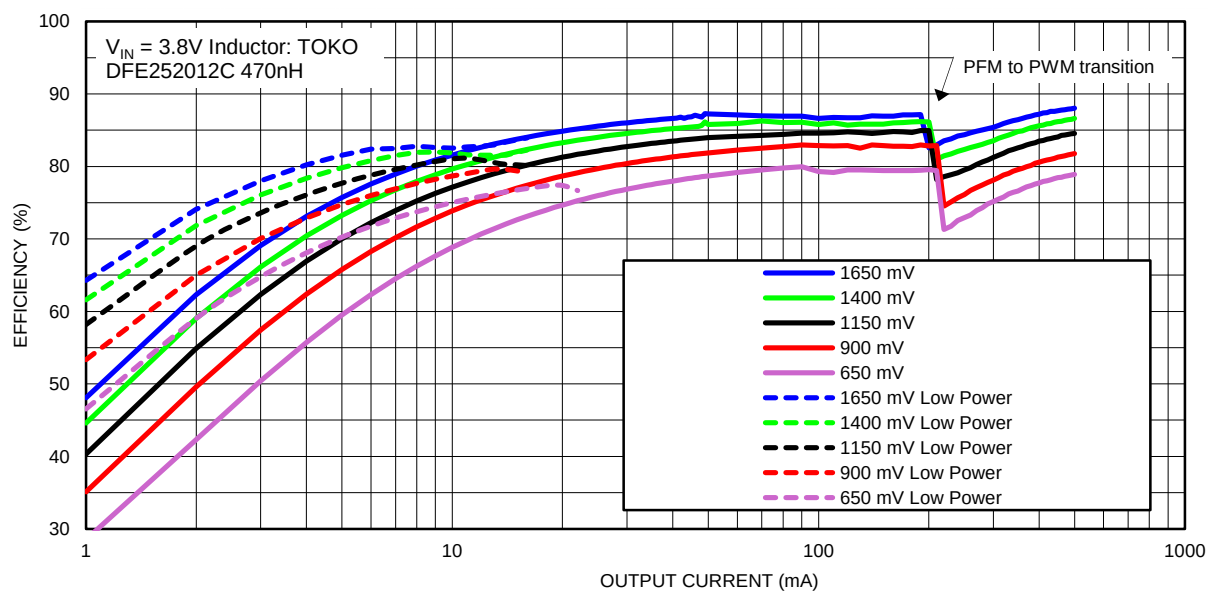


Figure 6. Light Load Efficiency, PFM and Low Power Mode Enabled; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV. PFM_EXIT_B0[2:0] = 100b (225 mA)

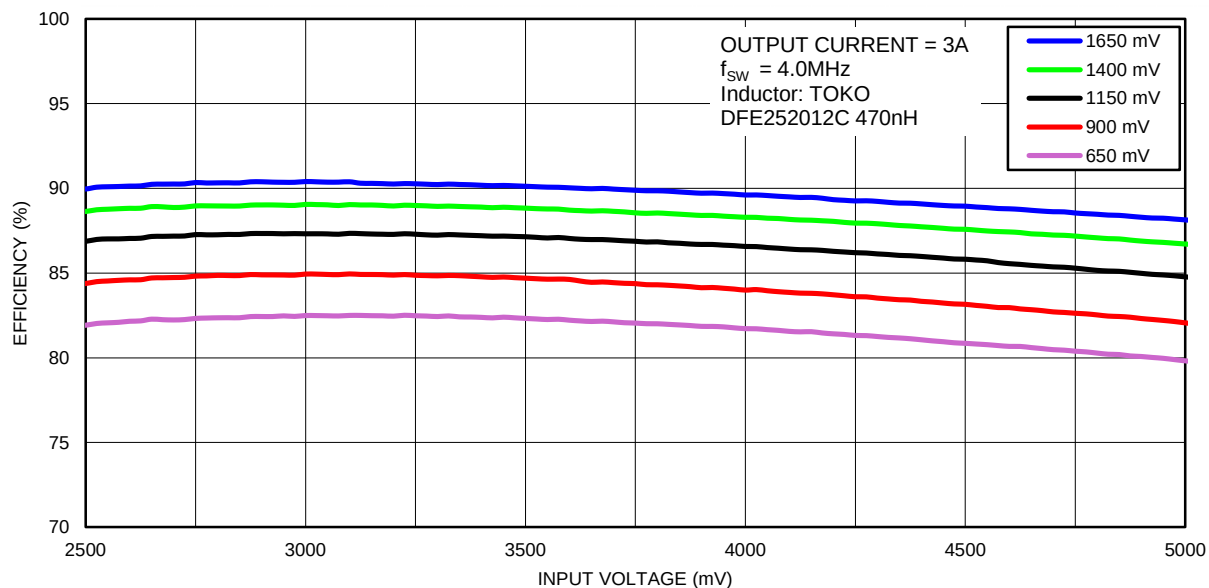


Figure 7. Efficiency vs Input Voltage in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

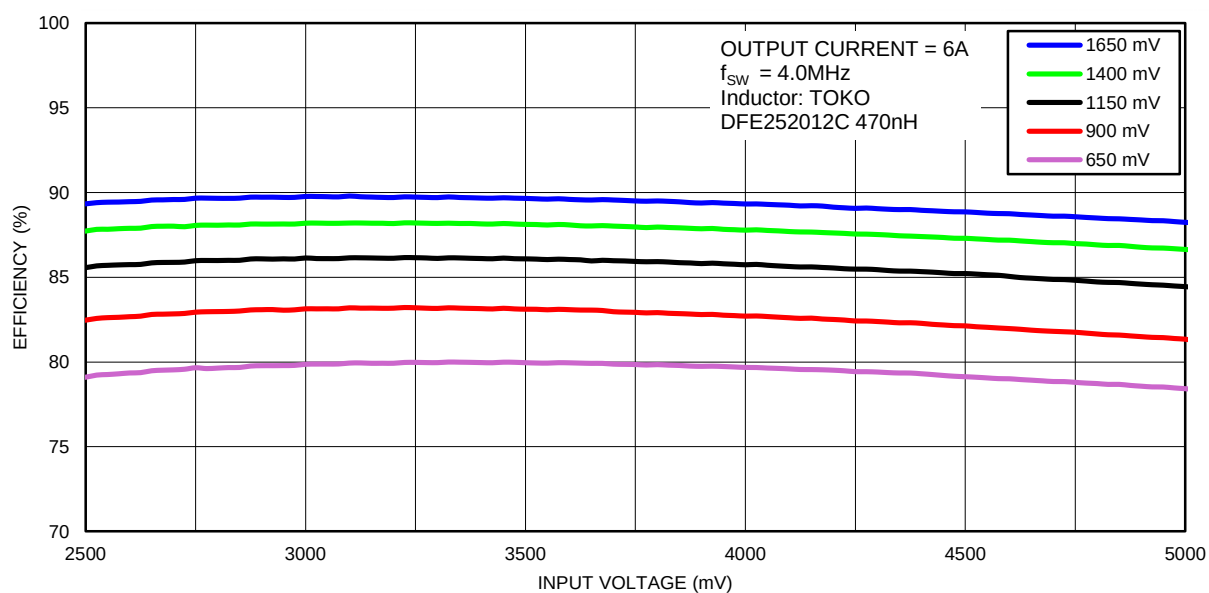


Figure 8. Efficiency vs Input Voltage in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

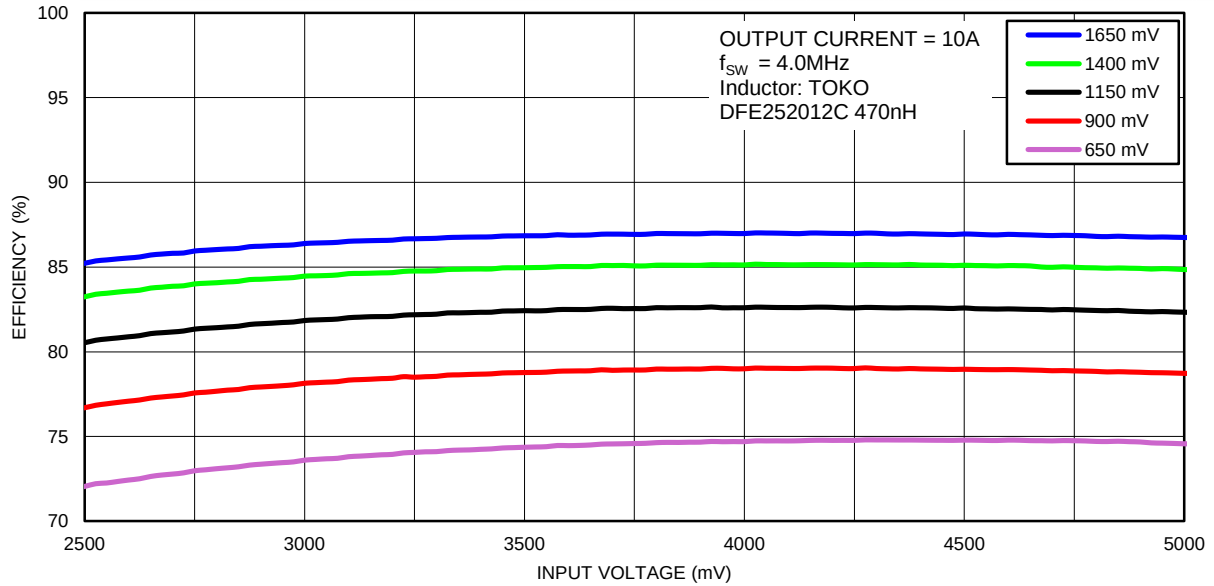


Figure 9. Efficiency vs Input Voltage in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

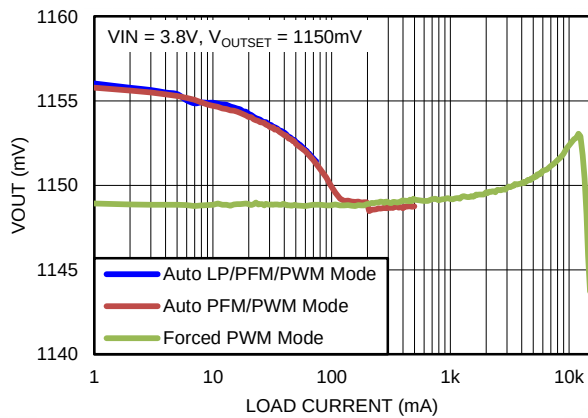


Figure 10. Output Voltage vs Load Current in Different Modes

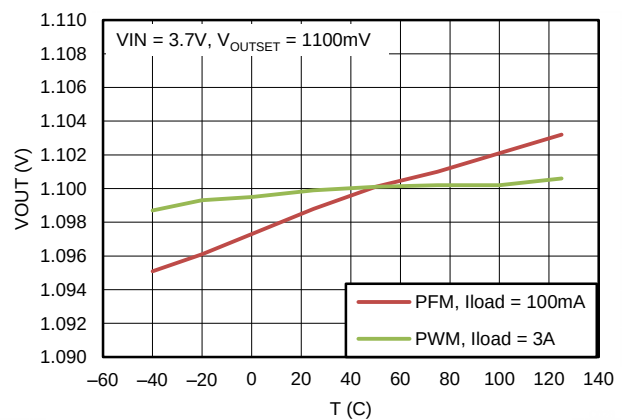


Figure 11. Output Voltage vs Temperature

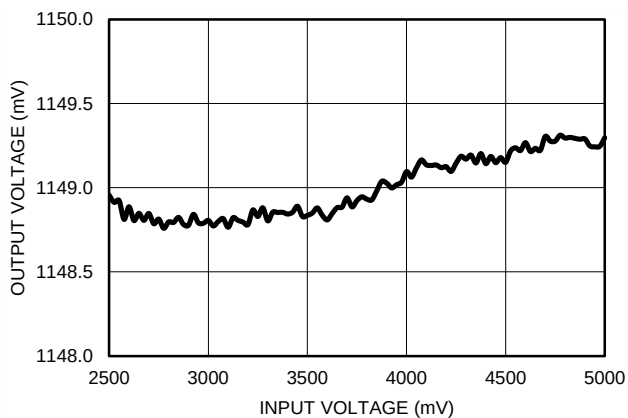


Figure 12. Line Regulation; $I_{LOAD} = 1.0A$; $V_{OUTSET} = 1150$ mV

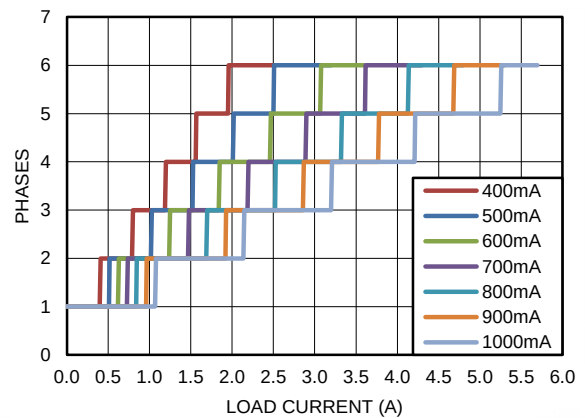


Figure 13. Phase Adding vs Load Current in Different ADD_PH_B0 Settings

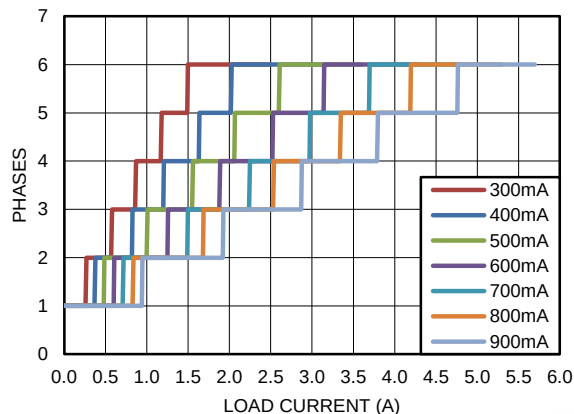


Figure 14. Phase Shedding vs Load Current in Different SHED_PH_B0 Settings

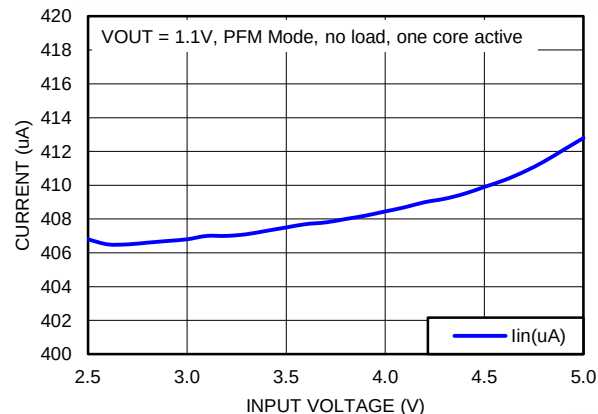


Figure 15. PFM Mode Current Consumption vs V_{IN}

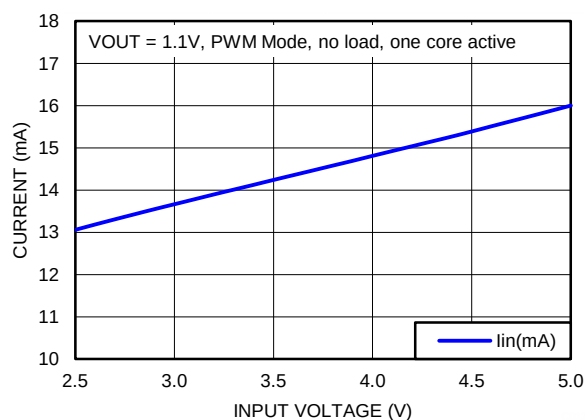


Figure 16. PWM Mode Current Consumption vs V_{IN}

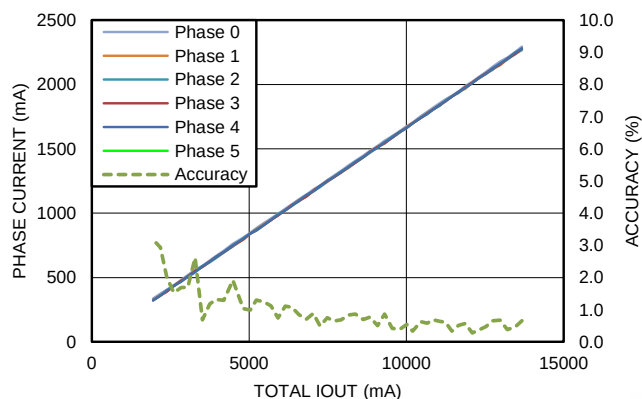


Figure 17. Phase Currents and Current Balancing Accuracy, 6 Phases Active (Currents measured by LP8755)

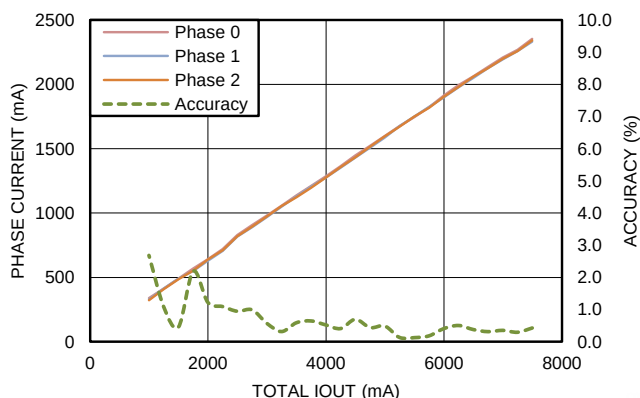


Figure 18. Phase Currents and Current Balancing Accuracy, 3 Phases Active (Currents measured by LP8755)

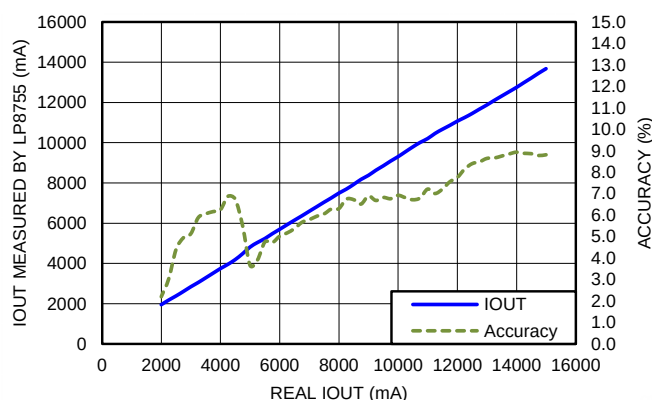


Figure 19. Load Current Measured by LP8755 vs Real Load Current, 6 Phases Active

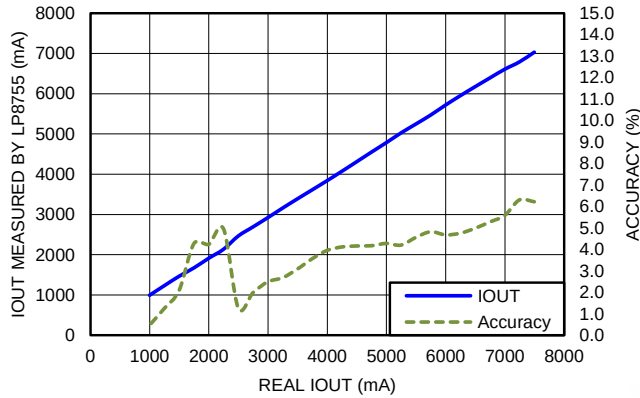


Figure 20. Load Current Measured by LP8755 vs Real Load Current, 3 Phases Active

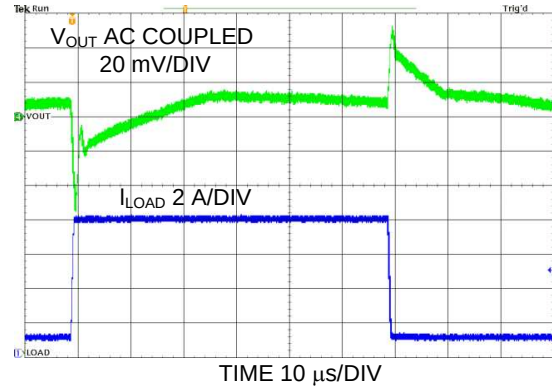


Figure 21. Transient Load Step Response; PWM mode, I_{OUT} 1 A → 8 A → 1 A, $t_{RISE} = t_{FALL} = 400$ ns

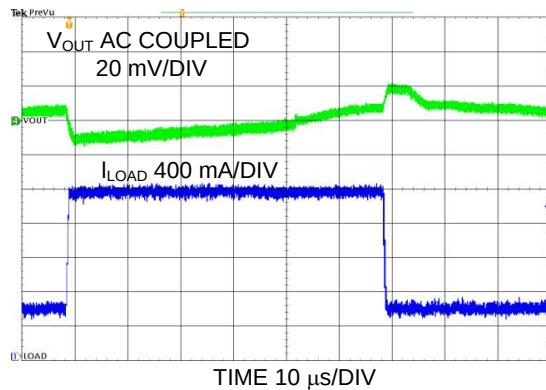


Figure 22. Transient Load Step Response; PWM mode, I_{OUT} 0.6 A → 2 A → 0.6 A, $t_{RISE} = t_{FALL} = 400$ ns

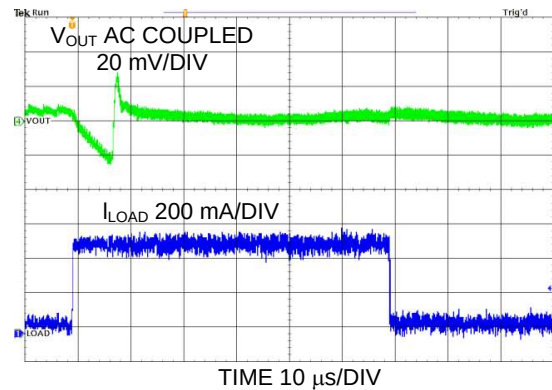


Figure 23. Transient Load Step Response; AUTO mode, I_{OUT} 0.5 mA → 500 mA → 0.5 mA, $t_{RISE} = t_{FALL} = 100$ ns

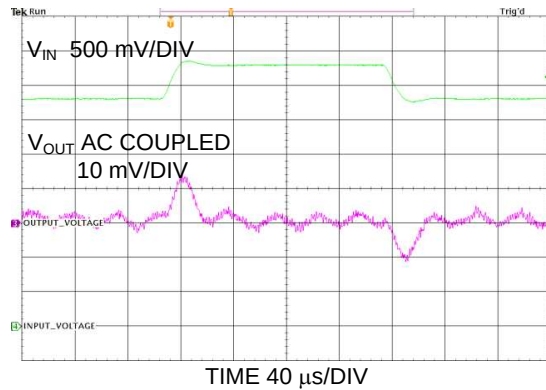


Figure 24. Transient Line Response; $I_{OUT} = 2000$ mA DC

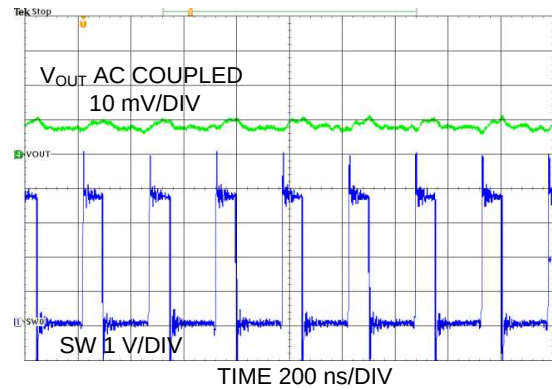


Figure 25. Output Voltage Ripple, PWM Mode. $I_{OUT} = 200$ mA; One Phase Active

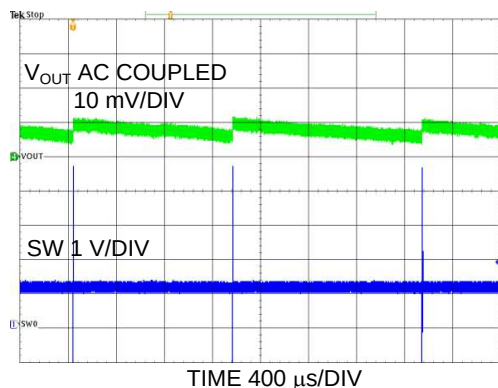
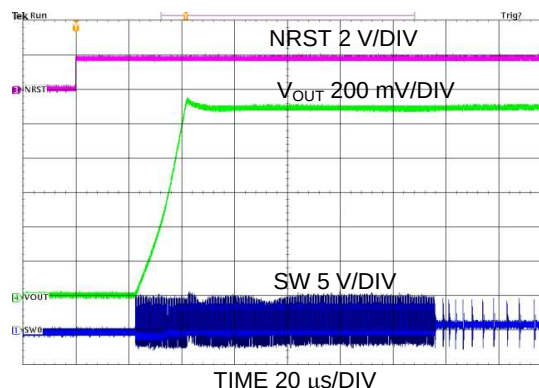
Figure 26. Output Voltage Ripple, PFM Mode. $I_{OUT} = 100 \mu A$ 

Figure 27. Startup with NRST, No Load

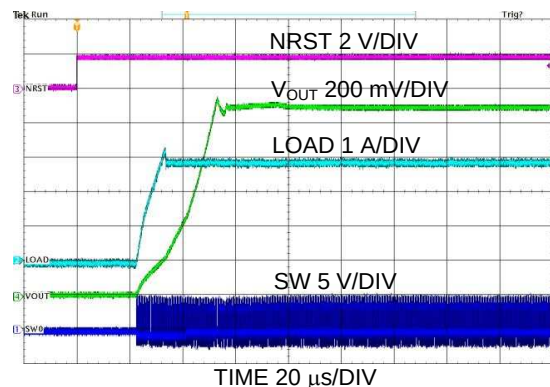


Figure 28. Startup with NRST, 3A Load

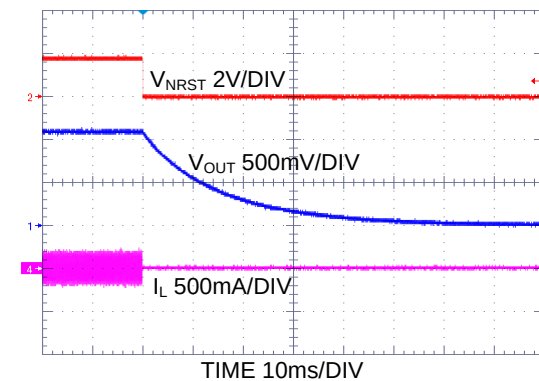
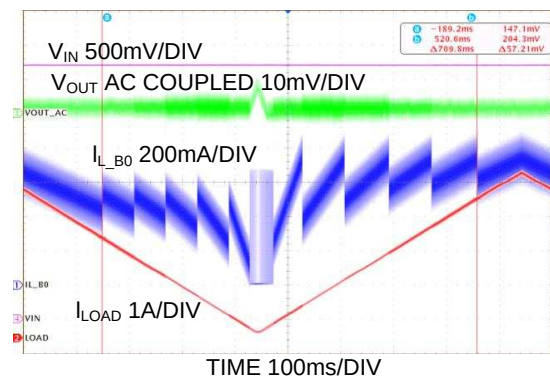
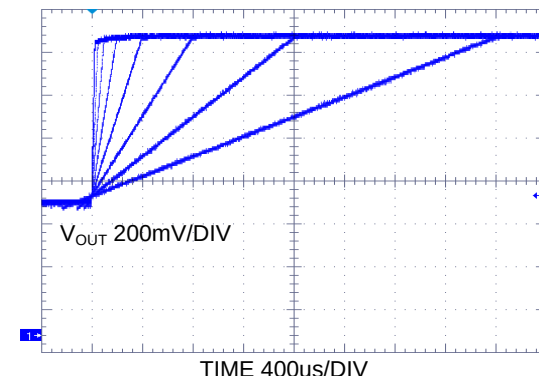
Figure 29. Shutdown with NRST, $V_{IN} = 3.7V$, $V_{OUT} = 1.1V$, No Load, Forced PWM

Figure 30. Load ramp 4.5A → 0A → 4.5A

Figure 31. V_{OUT} Transition from 0.6V to 1.4V with Different Ramp Settings, $V_{IN} = 3.7V$

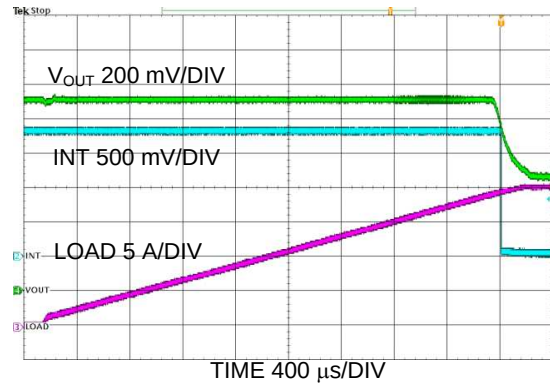


Figure 32. Interrupt Line Going Low with Not Power Good Activation

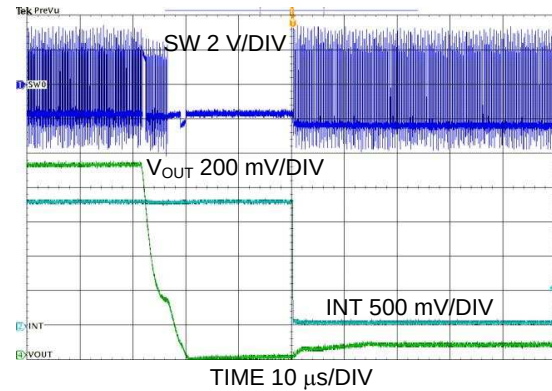


Figure 33. Metallic Short Applied at V_{OUT}

PARAMETER MEASUREMENT INFORMATION

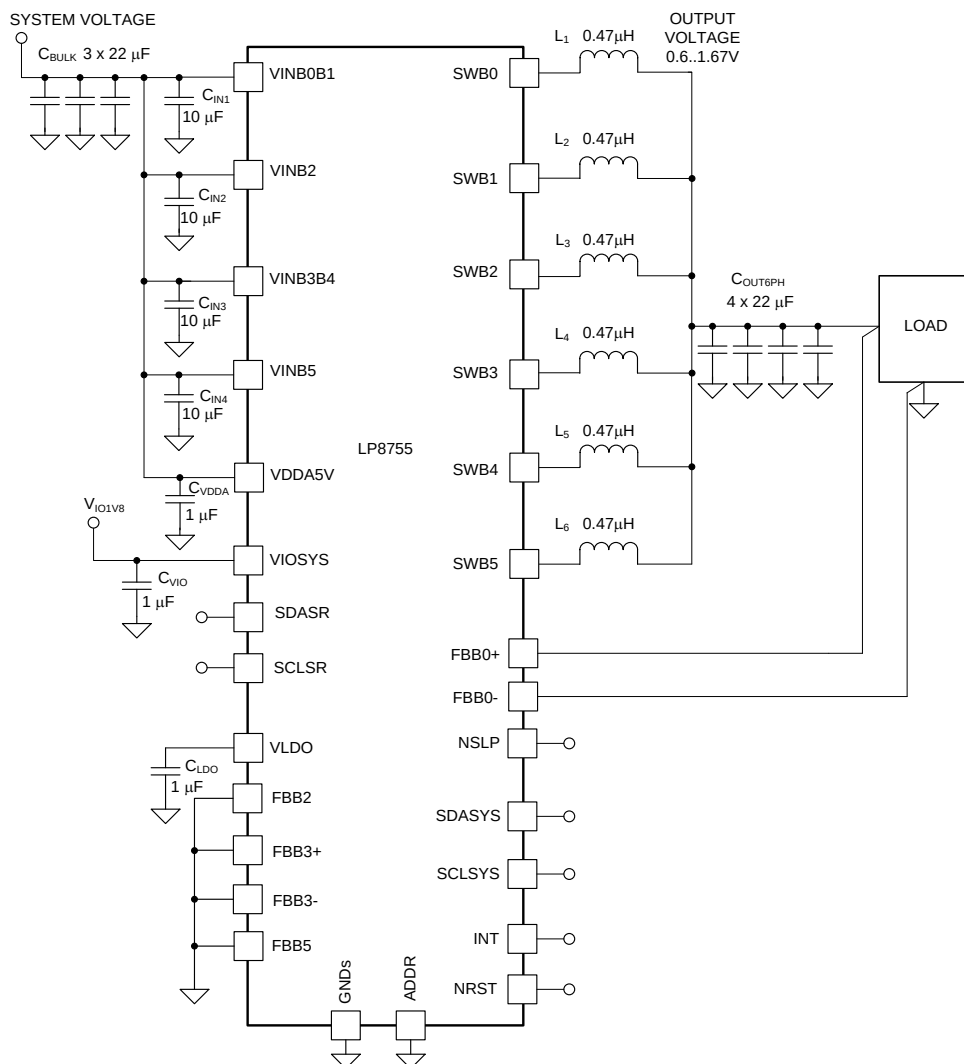
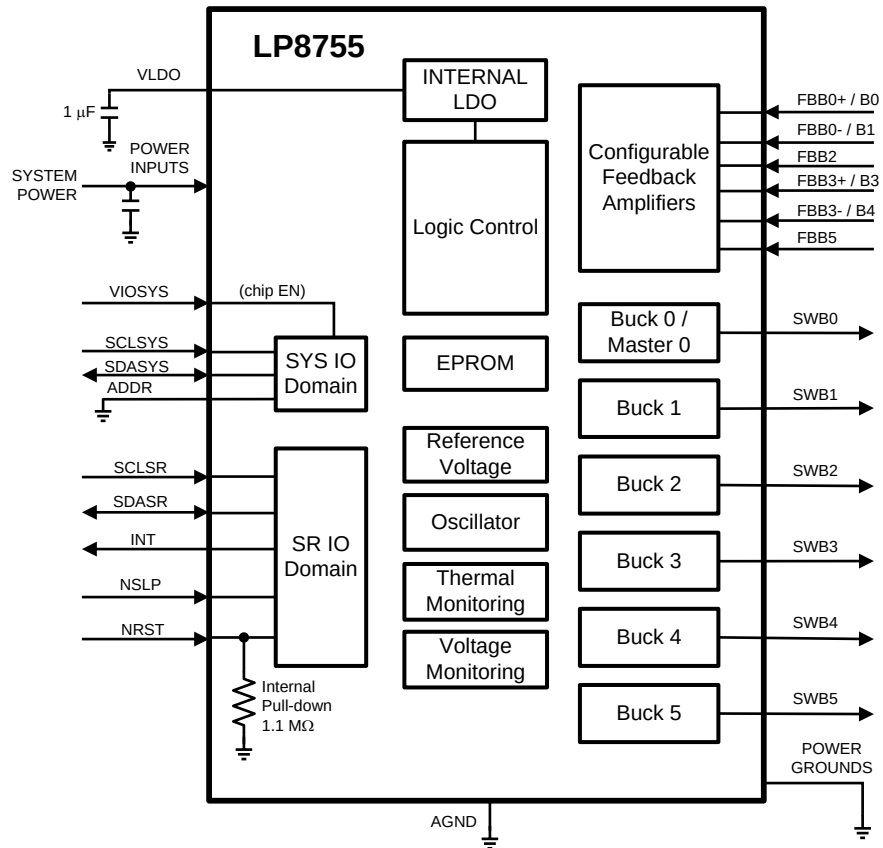


Figure 34. Parameter Measurement Circuit

Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER, TYPE
LP8755	LP8755 Multi-phase 6-Core Step-Down Converter	Texas Instruments
L ₁ , L ₂ , L ₃ , L ₄ , L ₅ , L ₆	Inductor 0.47 μH, 2520 footprint	TOKO DFE252012C
C _{IN1} , C _{IN2} , C _{IN3} , C _{IN4}	Capacitor Ceramic, 10 μF, 6.3V, ±20%, X5R, 0603	Murata GRM188R60J106ME84, High-performance Type
C _{VIO} , C _{VDDA} , C _{LDO}	Capacitor Ceramic, 1 μF, 6.3V, ±20%, X5R, 0201	Samsung CL03A105MQ3CSNH
C _{OUT6PH} , C _{BULK}	Capacitor Ceramic, 22 μF, 10V, ±20%, X5R, 0603	Samsung CL10A226MP8NUNE

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Overview

The LP8755 is a high-efficiency, high-performance power supply IC with six step-down DC-DC converter cores. It delivers 0.6V to 1.67V regulated voltage rail from either a single Li-Ion or three cell NiMH/NiCd batteries to portable devices such as cell phones and PDAs.

There are three modes of operation for the 6-phase converter, depending on the output current required: PWM (Pulse Width Modulation), PFM (Pulse-Frequency Modulation), and Low-Power PFM. Converter operates in PWM mode at high load currents of approximately 100 mA or higher, depending on register setting. Lighter output current loads will cause the converter to automatically switch into PFM or Low-Power PFM mode for reduced current consumption and a longer battery life. Forced PWM is also available for highest transient performance.

Under no-load conditions the device can be set to Standby or Shutdown. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHDN} = 0.1 \mu A$ typ.). Additional features include soft-start, under-voltage lockout, over-voltage protection, current overload protection, thermal warning, and thermal shutdown.

Buck Information

The LP8755 has six integrated high-efficiency buck converter cores. The cores are designed for flexibility; most of the functions are programmable, thus allowing optimization of the SMPS operation for each application. The cores are bundled together to establish a multi-phase converter. This is shown in [Figure 1](#).

OPERATING MODES:

- OFF: Output is isolated from the input voltage rail in this mode. Output has an optional pull-down resistor.
- PWM: Converter operates in buck configuration. Average switching frequency is constant.
- PFM: Converter switches only when output voltage decreases below programmed threshold. Inductor current is discontinuous.
- Low-Power PFM: This mode is similar to PFM mode, but some of the internal blocks are turned off between the PFM pulses. Load transient response is compromised due to the wake-up time.

FEATURES:

- DVS support; SmartReflex functionality
- Automatic mode control based on the loading
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Power good flag with maskable interrupt
- Over-voltage comparator
- Phase control for optimized EMI
- Average output current sensing (for PFM/PWM entry/exit, phase adding/shedding, and load current reporting)
- Current balancing between the phases of the converter
- Differential voltage sensing
- Dynamic phase adding/shedding, each output being phase shifted
- Spread spectrum technique to reduce EMI

PROGRAMMABILITY (The following parameters can be programmed via registers):

- Output voltage
- Forced PWM operation
- Switch current limits for both high and low side
- PWM/PFM mode entry and exit (based on average output current)
- Output voltage slew rate

The LP8755 has an integrated OTP (One-Time-Programmable) memory for storing the default values for some programmable parameters. The OTP is programmed during manufacturing, before the final testing. The following parameters are pre-programmed in the fab but can be re-programmed in the field via the serial bus. Because the parameters strongly affect the converter performance, altered settings must be carefully evaluated before being implemented. Also, these parameters are secured by a lock code to prevent unwanted re-programming:

- Switching frequency
- Loop compensation. Both integral and proportion terms are programmable

Modes of Operation

SHUTDOWN: All switch, reference, control and bias circuitry of the LP8755 are turned off. The main battery supply voltage is high enough to start the buck power-up sequence but VIOSYS and NRST are LOW.

STANDBY: Setting VIOSYS HIGH (>1.8V) enables standby-operation. All registers can be read or written by the system master via the system serial interface. Recovery from UVLO, TSD, or OVP event also leads to standby.

ACTIVE: Regulated DC/DC converters are on or can be enabled with full current capability. In this mode, all features and control registers are available via the system serial bus and via SmartReflex interface.

LOW-POWER: At light loads (less than ~30 mA), and when the load does not require highest level of transient performance, the device enters automatically Low-Power mode. In this mode the part operates at low Iq. Conditions entering and exiting Low-Power mode are shown in Figure 35.

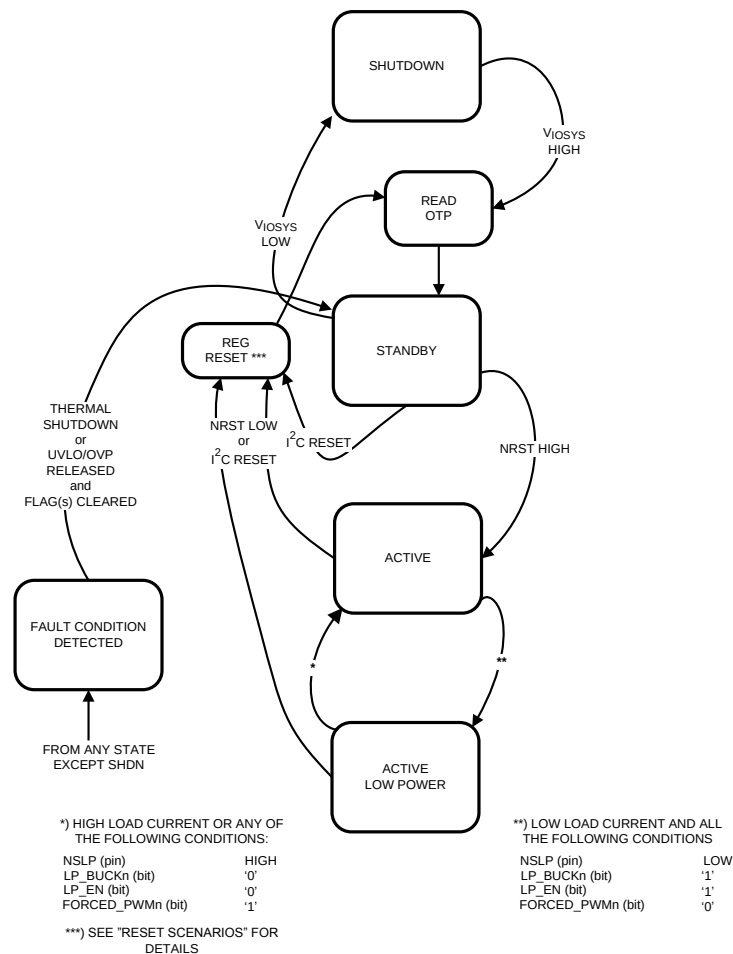


Figure 35. Device Operation Modes

Multi-Phase DC/DC Converters

Overview

A multi-phase synchronous buck converter offers several advantages over a single power-stage converter. For application processor power delivery, lower ripple on the input and output currents and faster transient response to load steps are the most significant advantages. Also, since the load current is evenly shared among multiple channels, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. Physical size of the output inductor shrinks significantly for the similar reason. Interleaving switching action of the converters and channels for a typical application (shown in [Figure 1](#)) is illustrated in [Figure 38](#).

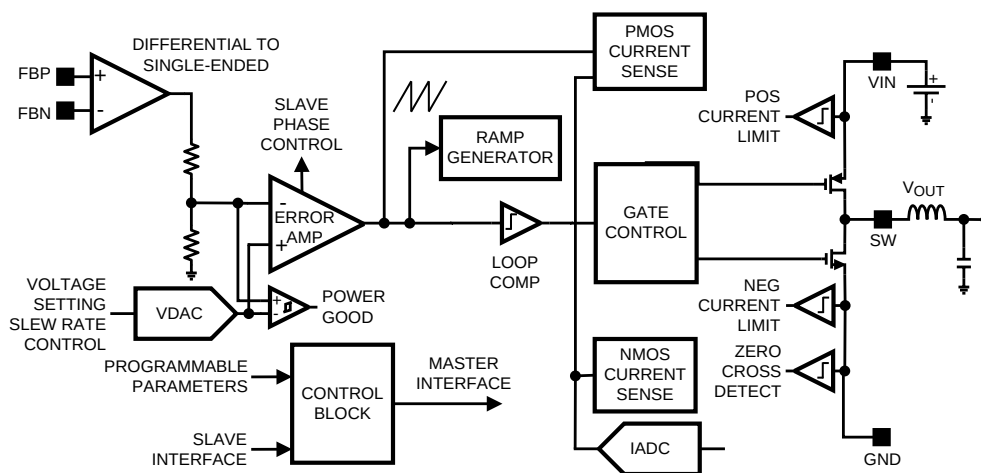


Figure 36. Detailed Block Diagram Showing One Core

Multi-Phase Operation and Phase-Shedding

Under heavy load conditions, the 6-phase converter switches each channel 60° apart. As a result, the 6-phase converter has an effective ripple frequency six times greater than the switching frequency of any one phase. However, the parallel operation decreases the efficiency at light load conditions. In order to overcome this operational inefficiency, the LP8755 can change the number of active phases to optimize efficiency for the variations of the load. This is called phase-shedding. The concept is illustrated below in [Figure 37](#).

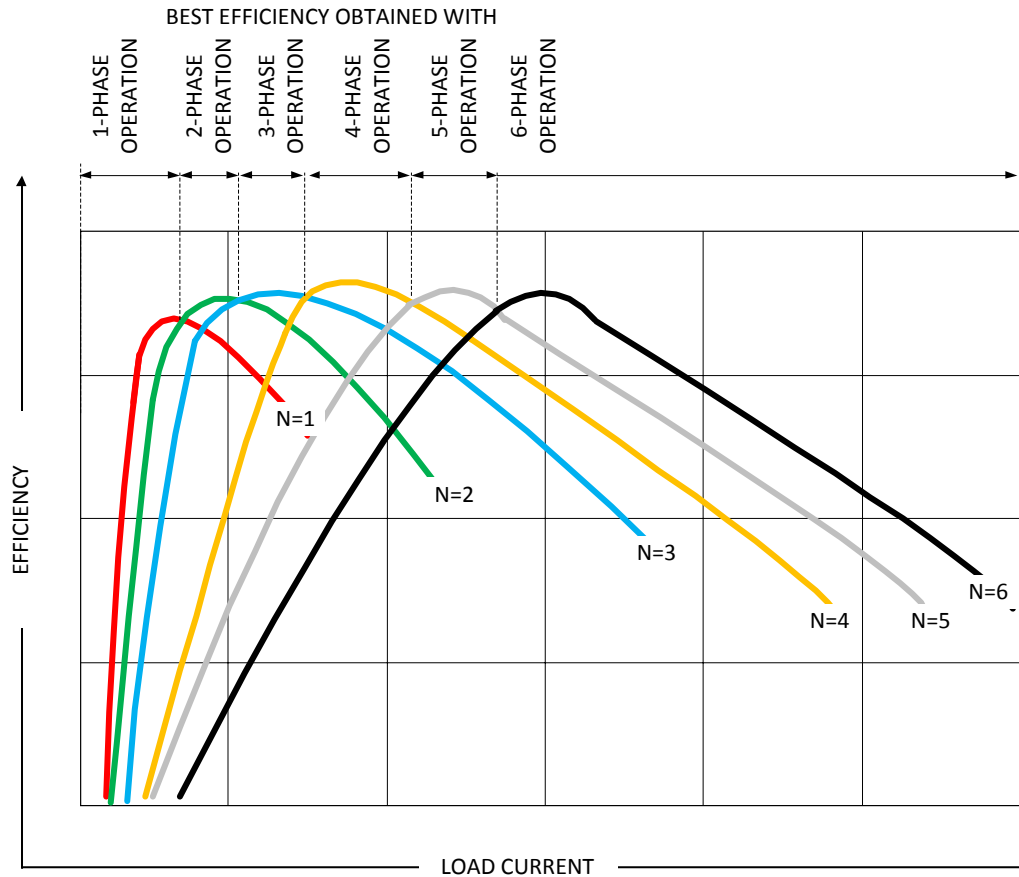
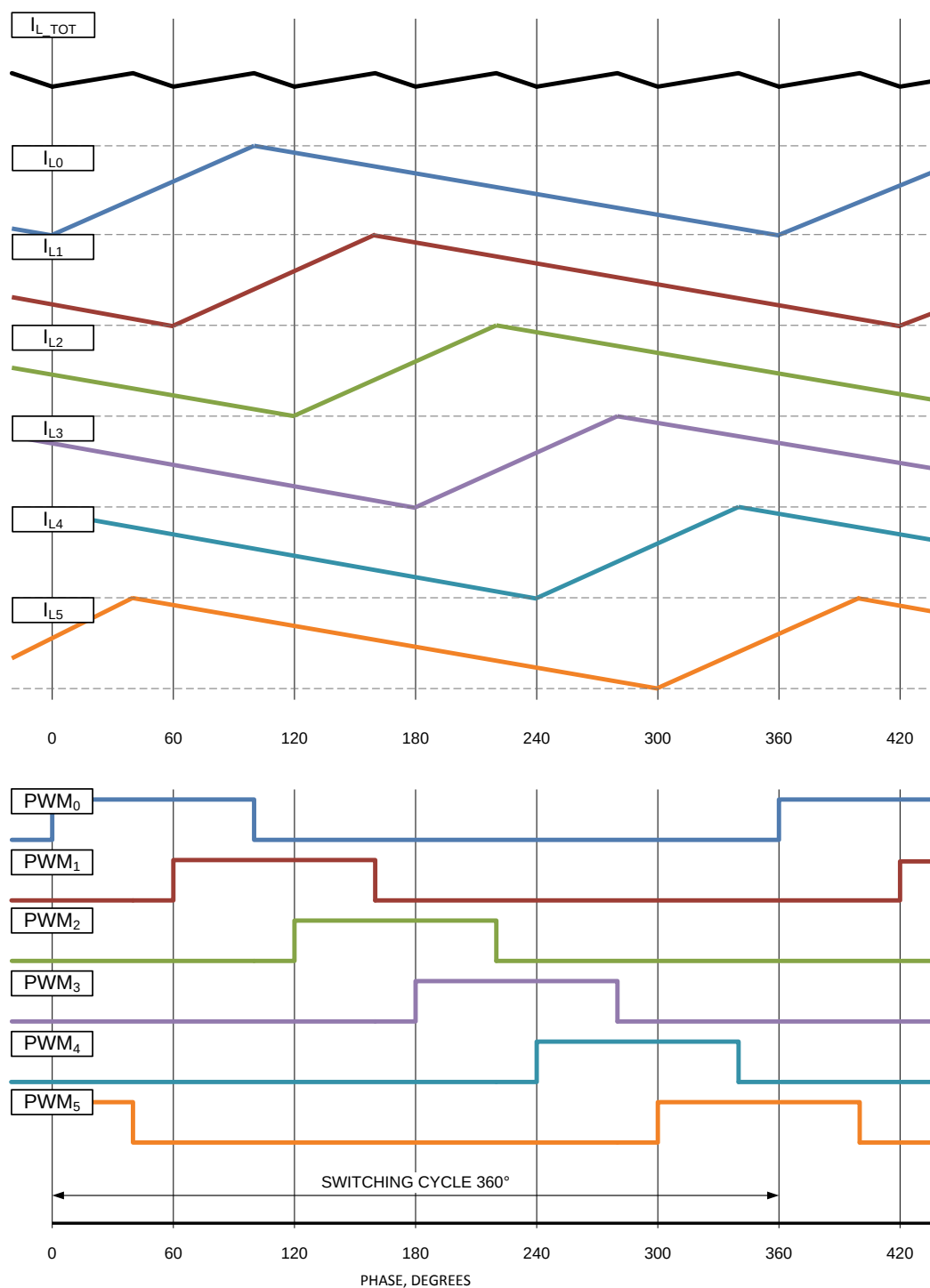


Figure 37. Multi-phase Buck Converter Efficiency vs Number of Phases; All Converters in PWM Mode ⁽¹⁾

(1) Graph is not to scale and is for illustrative purposes only.

Figure 38. PWM Timings and Inductor Current Waveforms ⁽²⁾

(2) Graph is not to scale and is for illustrative purposes only.

Transition between PFM and PWM, Low-Power Mode

Normal PWM-mode operation with phase-shedding can optimize efficiency at mid-to-full load, but this is usually at the expense of light-load efficiency. The LP8755 converter operates in PWM mode at a load current of 100 to 375 mA or higher; this mode transition trip-point is set by register. Lighter load current causes the device to automatically switch into PFM mode for reduced current consumption. By combining PFM and PWM modes in the same regulator and providing automatic switching, high efficiency can be achieved over a wide output load current range.

Efficiency is further enhanced when the converter enters Low-Power PFM mode. The LP8755 includes Low-Power mode function for low-current consumption. In this mode most of the internal blocks are disabled between the inductor current ramp up and ramp down phases to reduce the operating current. However, as a result, the transient performance of the converter will be compromised. The Low-Power mode can be enabled by control register setting. Also, the application processor or the PMIC may provide a HW signal (NSLP) to the LP8755's input to indicate when the processor has entered a low-power state. When the signal is asserted, the LP8755's Low-Power PFM function will be enabled, and the LP8755 will run with a reduced input current. The right timing of the NSLP signal from the system is important for best load-transient performance. The NSLP signal should be asserted only when load current is stable and below 30 mA. Before the load current increases above 30 mA, the NSLP signal should be de-asserted 100 μ s (minimum) prior to a load step to prepare the converter for the higher load current.

Buck Converter Load Current

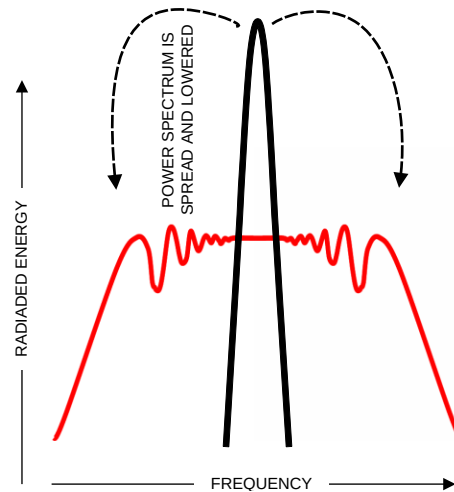
The buck load current can be monitored via I²C registers. Current of different buck converter cores or the total load current of the master can be selected from register 0x21 (see [Buck converter configuration load current selection](#)). A write to this selection register starts a current measurement sequence. The measurement sequence is a minimum of 50 μ s long. When a measurement sequence starts, the I_LOAD_READY bit in register 0x0E is set to '0'. After the measurement sequence is finished, the I_LOAD_READY bit is set to '1'. (Note that by default this bit is '0'.) The measurement result can be read from registers 0x22 and 0x21. Register 0x22 bits [7:0] give out the LSB bits, and register 0x21 bits [6:4] give out MSB bits. The measurement result [10:0] LSB is 10 mA, and the maximum value of the measurement is 20A. The LP8755 can be configured to give out an interrupt after the load current measurement sequence is finished. Load current measurement interrupt can be masked with Register INT_MASKS_2 (0x2E) bit [3] (MASK_I_LOAD_READY).

Table 4. Buck Converter Configuration Load Current Selection

Register 0x21 bits	Buck converter configuration
000	Buck converter 0 load current
001	Buck converter 1 load current
010	Buck converter 2 load current
011	Buck converter 3 load current
100	Buck converter 4 load current
101	Buck converter 5 load current
110	Master load currents. Sum of the slaves' current.

Spread Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP8755's register-selectable spread spectrum mode minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies randomly around the center frequency, reducing the EMI emissions radiated by the converter, associated passive components, and PWB traces. See [Figure 39](#).



Where a fixed-frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP8755 spreads that energy over a large bandwidth.

Figure 39. Spread Spectrum Modulation

Power-Up and Output Voltage Sequencing

The power-up sequence for the LP8755 is as follows:

- VINBxx and VDDA5V reach min recommended levels.
- VIOSYS set high. Enables the system I/O interface. For power-on-reset (POR), the I²C host should allow at least 500 μ s before sending data to the LP8755 after the rising edge of the VIOSYS line.
- VLDO voltage is raising. The LDO voltage is generated internally. The internal POR signal is activated.
- Internal POR deasserted, OTP read.
- Device enters standby mode.
- DC/DC enable, output voltage, voltage slew rate programmed over I²C as needed by the application.
- NRTS set high. Once the DC/DC converter is started, it can be enabled or disabled by EN/DIS bit.

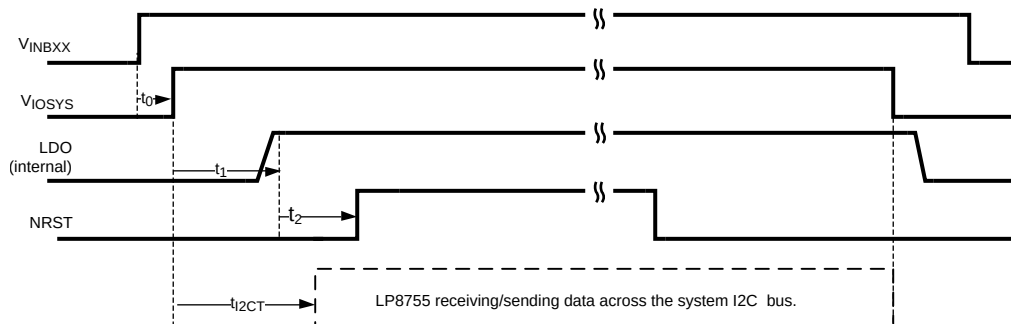


Figure 40. Timing Diagram for the Power-Up Sequence

Table 5. Power-Up Sequence

SYMBOL	PARAMETER	CONDITION ⁽¹⁾	MIN	TYP	MAX	UNIT
t_0	V_{INBXX} to V_{IOSYS} assertion		0			μ s
t_1	LDO _{ON} Delay Time	$C_{LDO} = 1 \mu$ F		<100	150	μ s
t_2	LDO _{ON} to NRST HIGH		0			μ s
t_{I2CT}	Device ready for I ² C data transfer		500			μ s

(1) These specification table entries are ensured by design. The power input lines V_{INBXX} , V_{DDA5V} and V_{IOSYS} must be stable before the NRST line goes High. Also, the VLDO line must be stable 1.8V before the NRST line goes High.

Device Reset Scenarios

There are three reset methods implemented on the LP8755:

- Software reset
- Hardware reset
- Power-on reset (POR)

An SW-reset occurs when the reset register is written first with 01H, followed by a 00H right after that. This event resets the control registers shown in Table 6 to the default values. The temperature, power good, and other faults are persistent over the SW reset to allow for the system to identify to cause of the failure.

An internal power-on reset (POR) occurs when the supply voltage (V_{DDA5V}) transitions above the POR threshold or V_{IOSYS} is toggled low/high. Each of the registers contain a factory-defined value upon POR, and this data remains there until any of the following occurs:

- Device sets a Flag bit, causing the Status register to be updated. The other registers remain untouched.
- A different data word is written to a writable register.

The internal registers will lose their contents if the supply voltage (V_{DDA5V}) goes below 1V (typ.).

A hardware reset is accomplished by NRST low. This event resets the control registers shown in Table 6 to the default values.

Under OVP, UVLO, TSD, or V_{IOSYS} low (while NRST still high) conditions, a Fast Power-Down sequence is launched.

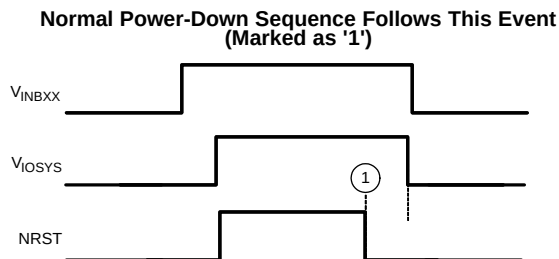


Figure 41. The External Power Control System De-asserts NRST

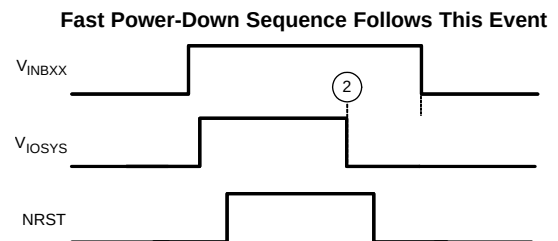
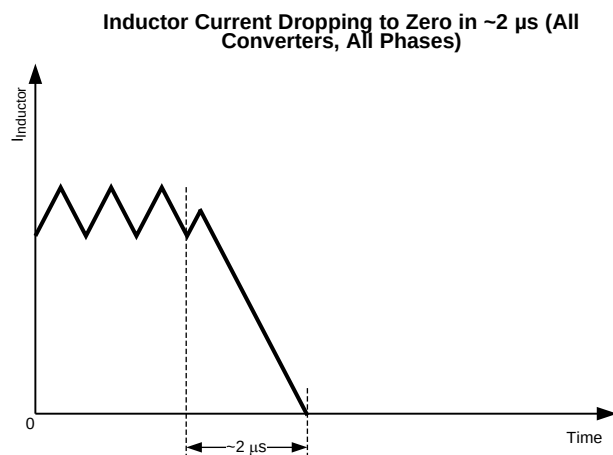
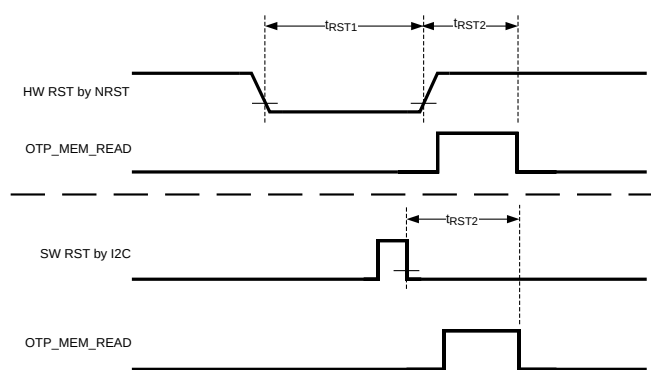


Figure 42. NRST Stays HIGH While VIOSYS Transition from HIGH to LOW Happens (Marked as '2')

**Figure 43. Fast Power-Down Sequence****Figure 44. Reset Timings**

SYMBOL	PARAMETER	LIMIT
t_{RST1}	NRST active low pulse width	1 μ s min + value on DELAY register.
t_{RST2}	NRST inactive or I ² C reset event to MEMORY READ end	25 μ s max

Table 6. Hardware Reset, Power-On Reset (POR) and Software Reset: Registers After Reset

Hex Address	Register	Software Reset I ² C RESET	Hardware Reset NRST LOW ⁽¹⁾	Power-On Reset VIOSYS LOW
0x00	VSET_B0	All bits retained	All bits retained	All bits cleared
0x06	FPWM	All bits cleared	All bits cleared	All bits cleared
0x07	BUCK0_CTRL	All bits cleared	All bits cleared	All bits cleared
0x0D	FLAGS_0	All bits retained	All bits retained	All bits cleared
0x0E	FLAGS_1	All bits retained	All bits retained	All bits cleared
0x0F	INT_MASK0	All bits cleared	All bits cleared	All bits cleared
0x010	GENERAL	All bits cleared	All bits cleared	All bits cleared
0x011	RESET	N/A	All bits cleared	All bits cleared
0x012	DELAY_BUCK0	All bits cleared	All bits cleared	All bits cleared
0x018	CHIP_ID	Read Only		
0x019	PFM_LEV_B0	All bits cleared	All bits cleared	All bits cleared
0x01F	PHASE_LEV_B0	All bits cleared	All bits cleared	All bits cleared
0x21	SEL_I_LOAD	All bits retained	All bits retained	All bits cleared
0x22	LOAD_CURR	Read Only		
0x2E	INT_MASK_2	All bits cleared	All bits cleared	All bits cleared
0xDD	LOCK_REG	All bits retained	All bits retained	All bits cleared

(1) Reset will take effect upon complete of the power-down sequence.

Diagnosis and Protection Features

The LP8755 is capable of providing two levels of protection features: Warnings for diagnosis and faults which are causing the converters to shut down. When the device detects warning or fault conditions, the LP8755 sets the flag bits indicating which fault or warning conditions have occurred; the INT pin will be pulled low. INT will be released again after a clear of flags is complete. The flag bits are persistent over reset to allow for the system to identify what was causing the interrupt and/or converter shutdown.

Also, the LP8755 has a soft-start circuit that limits in-rush current during startup. The output voltage increase rate is 30 mV/ μ sec (default) during soft-start.

Table 7. Summary of exceptions and interrupt signals

Event	Register/bit	Interrupt Signal Produced?	INT mask available?
SCP triggered	FLAGS_1/SCP	Yes	Yes
Not PowerGood	FLAGS_0/nPG	Yes	Yes
TEMP status change	FLAGS_0/TEMP	On any temperature change except for the case when TEMP[1:0] = 0b11	Yes
Thermal warning	FLAGS_1/T_WARNING	Yes	Yes
Thermal shutdown	FLAGS_1/THSD	Yes	No
OVP triggered	FLAGS_1/OVP	Yes	Yes
Load current measurement ready	FLAGS_1/I_LOAD_READY	Yes	Yes
UVLO triggered	FLAGS_1/UVLO	Yes	Yes

Warnings for Diagnosis (No Power Down)

Short-Circuit Protection

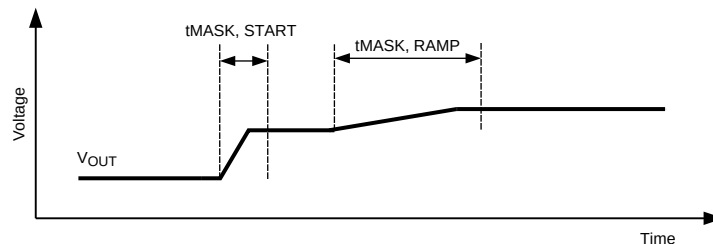
A short-circuit protection feature allows the LP8755 to protect itself and external components during overload conditions. The output short-circuit fault threshold is 400 mV (typ.) .

Power Good Monitoring

When the converter's feedback-pin voltage falls lower than 90% (typ.) of the set voltage, the nPG flag is set. To prevent a false alarm, the power good circuit is masked during converter startup and voltage transitions. The duration of the power good mask is set to 400 μ s for converter startup. For voltage ramps the masking time is extended by an internal logic circuit up to 6.4 ms. (See [PROTECTION FEATURES CHARACTERISTICS](#).)

Thermal Warnings

Prior to the thermal shutdown, thermal warnings are set. The first warning is set at +85°C (INT pin low), and the second at 120°C (INT pin pulled low and TWARNING flag set). If the chip temperature crosses any of the thresholds of 85°C, 120°C, or 150°C (see FLAGS_0 register) the INT pin will be triggered. INT will be cleared upon read of TEMP[1:0] bits except if TEMP [1:0] = 0b11, which is a thermal fault event.



Masking time for startup is constant 400 μ s (typ.). Masking time for voltage transitions depends on the selected ramp rates.

Figure 45. Power Good Masking Principle

Faults (Fault State and Fast Power-Down)

Under-Voltage Lock-out

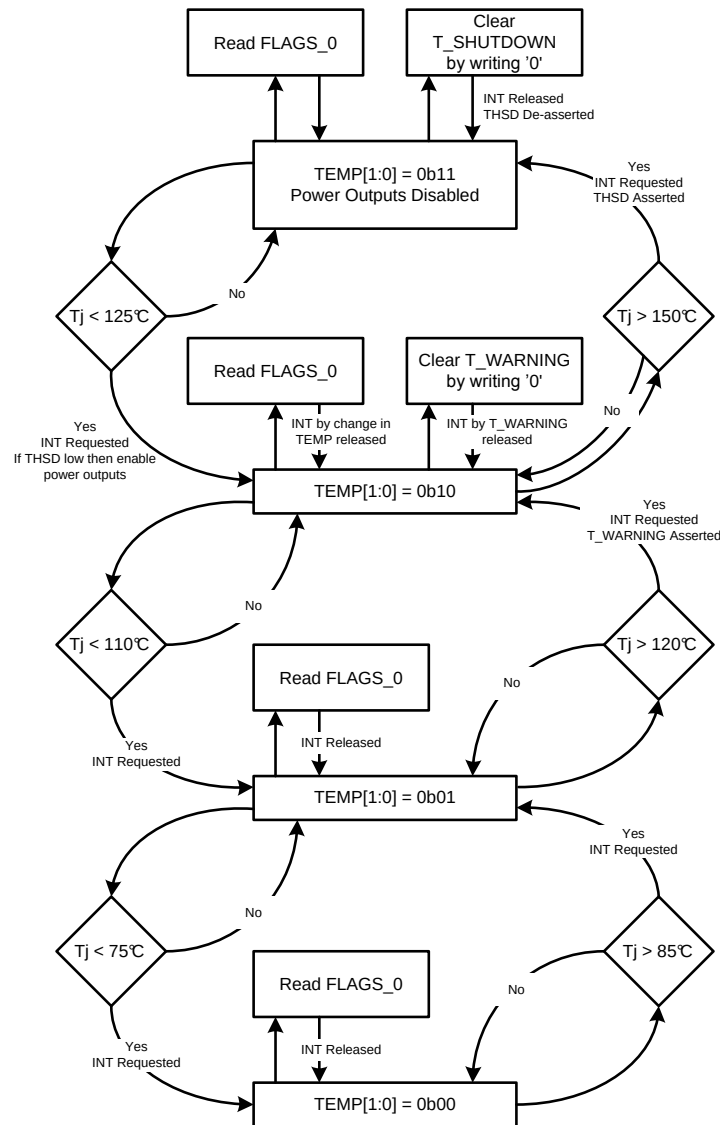
When the input voltage falls below 2.25V (typ.) at the VDDA5V pin, the LP8755 indicates a fault by activating the UVLO flag. The buck converter shut down without a power-down sequence (Fast Power-Down). The flag will remain active until the input voltage is raised above the UVLO threshold. If the flag is cleared while the fault persists, the flag is immediately re-asserted, and interrupt remains active.

Over-Voltage Protection

When an input voltage greater than 5.3V (typ.) is detected at the VDDA5V pin, the LP8755 indicates a fault by activating the OVP flag. The buck converter shut down without power-down sequence (Fast Power-Down). The flag will remain active until the input voltage is below the OVP threshold. If the flag is cleared while the fault persists, the flag is immediately re-asserted and interrupt remains active.

Thermal Shutdown

The LP8755 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device enters shutdown via fault-state. INT will be cleared upon write of the THSD flag. See Figure 46 for LP8755 thermal diagnosis and protection features.



Note that INT is asserted whenever any of the thermal thresholds is crossed. Note also the 10°C Hysteresis on the T_j Thresholds.

Figure 46. Thermal Warnings and Thermal Shutdown Flow

I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. Note: CLK pin is not used for serial bus data transfer. There are two buses implemented: the System I²C bus and the SmartReflex bus. In the following paragraphs, SCL refers to both SCLSYS and SCLSR, and SDA refers to SDASYS and SDASR. The LP8755 supports fast mode (400 kHz) and high-speed mode (3.4 MHz).

Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW.

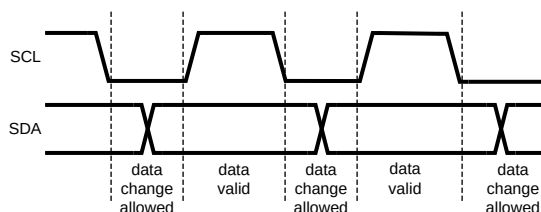


Figure 47. Data Validity Diagram

Start and Stop Conditions

The LP8755 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

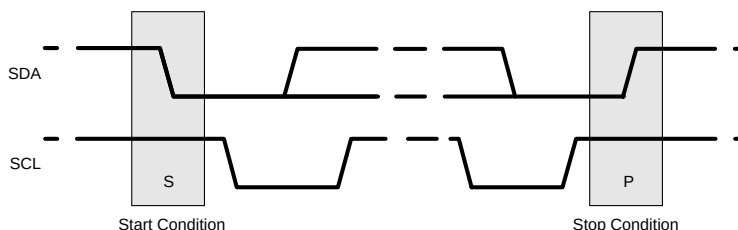


Figure 48. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. [Figure 3](#) shows the SDA and SCL signal timing for the I²C-Compatible Bus. See the [I²C-COMPATIBLE SERIAL BUS INTERFACE](#) for timing values.

Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP8755 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP8755 generates an acknowledge after each byte has been received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

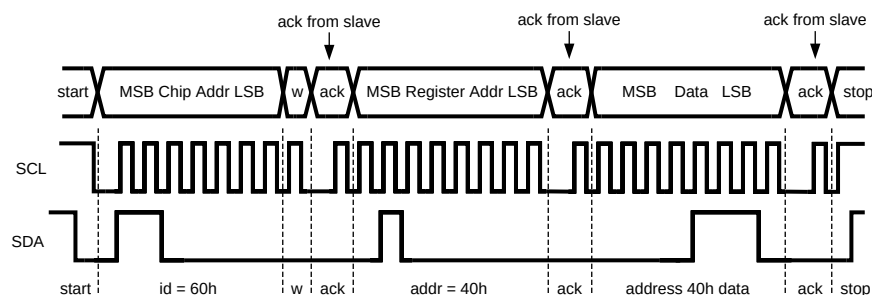
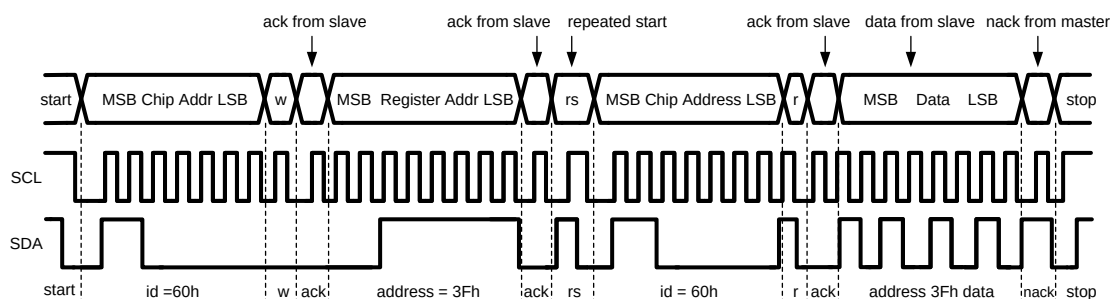


Figure 49. Write Cycle (w = write; SDA = '0'), id = device address = 60Hex for LP8755

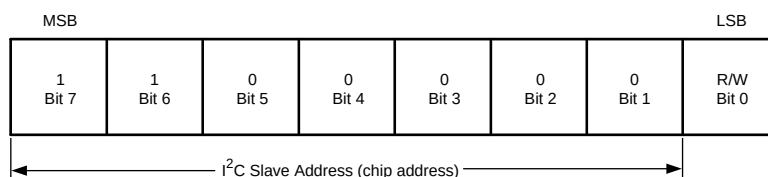


When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 50. Read Cycle (r = read; SDA = '1'), id = device address = 60Hex for LP8755.

I²C-Compatible Chip Address

The device address for the LP8755 is 0x60 (ADDR pin tied to the GND). After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



A. Here device address is 1100000Bin = 60Hex.

Figure 51. Device Address

Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP8755, the internal address index counter will be incremented by one, and the next register will be written. [Table 8](#) below shows writing sequence to two consecutive registers. Note: the auto-increment feature does not work for read.

Table 8. Auto-Increment Example

Master Action	Start	Device Address = 60H	Write		Register Address		Data		Data		Stop
LP8755 Action				ACK		ACK		ACK		ACK	

Register Descriptions

The LP8755 is controlled by a set of registers through the system serial interface port or through the SmartReflex-compatible interface. [Table 9](#) below lists device registers, their addresses and their abbreviations. A more detailed description is given in the [Control Register Details](#) section.

Table 9.

Hex Add	Register	Read / Write	MSB	Data						LSB
			D7	D6	D5	D4	D3	D2	D1	D0
0x00	VSET_B0	R/W	EN_DISB0	VSET_B0[6:0]						
0x06	FPWM	R/W								FPWM_B0
0x07	BUCK0_CTRL	R/W	OC_LEV_B0[1:0]		LP_B0	RDIS_B0	RESERV	RAMP_B0[2:0]		
0x0D	FLAGS_0	R/W						nPG	TEMP[1:0]	
0x0E	FLAGS_1	R/W			I_LOAD_READY	UVLO	T_WARNING	THSD	OVP	SCP
0x0F	INT_MASK_0	R/W						MASK_nPG	MASK_OVP	MASK_SCP
0x10	GENERAL	R/W			EN_SS		DIS_DIF	F_SLP	SLP_POL	LP_EN
0x11	RESET	R/W								SW_RESET
0x12	DELAY_BUCK0	R/W	DELAY_B0[7:0]							
0x18	CHIP_ID	R	VENDOR[1:0]	ALL_LAYER[1:0]			METAL_LAYER[3:0]			
0x19	PFM_LEV_B0	R/W		PFM_ENTRY_B0[0:2]				PFM_EXIT_B0[0:2]		
0x1F	PHASE_LEV_B0	R/W		ADD_PH_B0				SHED_PH_B0		
0x21	SEL_I_LOAD	R/W		BUCK_LOAD_CURR				LOAD_CURRENT_SOURCE		
0x22	LOAD_CURR	R	BUCK_LOAD_CURR							
0x2E	INT_MASK_2	R/W					MASK_ILOAD_READY	MASK_UVLO	MASK_TWARNING	MASK_TEMP
0xDD	LOCK_REG	R/W	LOCK_WORD							

Control Register Details

Register Address (Hex)	Register Name	Bit(s)	Read/Write	Default Value After Reset (Bin)	Bit Mnemonic and Description
0x00	VSET_B0	[7]	R/W	1	EN_DISB0 DC/DC converter Buck0 Enable/Disable. The Enable of the master Buck0 controls the operation of the slave bucks. 0 = Converter disabled 1 = Converter enabled Note: When a disable request is received the converter is disabled immediately.
		[6:0]	R/W	0111100	VSET_B0 Sets the output voltage. Defined by: $V_{OUT} = 0.5V + 10\text{ mV} * VSET_B0$ V_{OUT} range = 0.6 V to 1.67V NOTE: Do not use VSET_B0 values < 0001010 (10 dec) = 0.6V. NOTE: Register settings starting from 1110110 up to 1111111 are clamped to 1.67V.
0x06	FPWM	[0]	R/W	0	FPWM_B0 Force PWM mode of operation, Buck regulator 0 (Master). The setting of the master controls the operation of the slave bucks. 0 = PWM, PFM or Low-Power PFM operation mode. 1 = This will force the master converter and the slaves to operate always in the PWM mode of operation.
0x07	BUCK0_CTRL	[7:6]	R/W	11	OC_LEV_B0 Inductor positive current limit 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
0x07	BUCK0_CTRL	[5]	R/W	0	LP_B0 Allows converter to be placed into Low-Power mode. 1 = Entering to Low-Power PFM mode is allowed. 0 = Entering to Low-Power PFM more is not allowed.
0x07	BUCK0_CTRL	[4]	R/W	1	RDIS_B0 Enables the output discharge resistors when the V_{OUT} supply has been disabled. 1 = Enable pull-down 0 = Disable pull-down
0x07	BUCK0_CTRL	[2:0]	R/W	001	RAMP_B0 This set the output voltage change ramp as follows: 000 = 30 mV/ μ s 001 = 15 mV/ μ s 010 = 7.5 mV/ μ s 011 = 3.8 mV/ μ s 100 = 1.9 mV/ μ s 101 = 0.94 mV/ μ s 110 = 0.47 mV/ μ s 111 = 0.23 mV/ μ s
0x0D	FLAGS_0	[2]	R/W	0	nPG Flag Bit Power good fault flag for V_{OUT} rail 1 = Power fault detected 0 = Power good ⁽¹⁾
0x0D	FLAGS_0	[1:0]	R	00	TEMP indicates the die temperature as follows: 00: die temperature lower than 85°C 01: 85°C ≤ die temperature < 120°C 10: 120°C ≤ die temperature < 150°C 11: die temperature 150°C or higher

(1) The flag bit(s) can be cleared only by writing a zero to the associated register bit(s) or power cycling the device (V_{IOSYS} to LOW). Reading or RESET does not clear the flag bits. After clearing, the OVP, SCP, nPG fault flag(s) will be raised again '1' if the fault condition persists. The THSD flag will remain '0' after clear, even though the fault condition persists. Any flag bit High will cause the interrupt to be asserted on the INT pin. The INT pin will be pulled Low until all the flags are clear again.

0x0E	FLAGS_1	[5]	R/W	0	I_LOAD_READY Flag Bit 1 = Buck load current measurement data ready 0 = Buck load current measurement data not ready
0x0E	FLAGS_1	[4]	R/W	0	UVLO Flag Bit 1= Input undervoltage lockout (UVLO): Input voltage sagged below UVLO threshold. 0 = No UVLO ⁽¹⁾
0x0E	FLAGS_1	[3]	R/W	0	T_WARNING Flag Bit 1= Thermal warning: The IC temperature exceeds 120°C, in advance of the thermal shutdown protection. 0 = No thermal warning ⁽¹⁾
0x0E	FLAGS_1	[2]	R/W	0	THSD Flag Bit 1 = Thermal shutdown event detected 0 = No thermal shutdown ⁽¹⁾
0x0E	FLAGS_1	[1]	R/W	0	OVP Flag Bit 1= Indicates over-voltage protection (OVP) circuit activation. 0 = No OVP event. The OVP circuitry monitors VDDA5V power input. ⁽¹⁾
0x0E	FLAGS_1	[0]	R/W	0	SCP Flag Bit 1= Indicates short-circuit protection (SCP) circuit activation. The bit is activated when a short-circuit condition is detected on output rail. 0 = No SCP event ⁽²⁾
0x0F	INT_MASK_0	[2]	R/W	0	MASK_nPG Interrupt mask for power good fault flag 1 = nPG does not set interrupt. 0 = nPG sets interrupt, when triggered.
0x0F	INT_MASK_0	[1]	R/W	0	MASK_OVP Interrupt mask for Over-Voltage Protection (OVP) fault flag 1 = OVP does not set interrupt. 0 = OVP sets interrupt, when triggered.
0x0F	INT_MASK_0	[0]	R/W	0	MASK_SCP Interrupt mask for short-circuit protection SCP fault flag 1 = SCP does not set interrupt. 0 = SCP sets interrupt, when triggered.
0x10	GENERAL	[5]	R/W	0	EN_SS Enable Spread Spectrum
0x10	GENERAL	[3]	R/W	0	DIS_DIF Disable Differential-to-single-ended amplifier
0x10	GENERAL	[2]	R/W	0	F_SLP 1 = Forcing Low-Power mode on the converter when bit LP_B0 (in address location 0x07) is set to = '1', that is, the converter is forced to Low-Power mode regardless of the load current level. 0 = Converter will exit Low-Power mode when operating conditions allow.
0x10	GENERAL	[1]	R/W	0	SLP_POL Sets the polarity of the NSLP pin 1 = NSLP is active high 0 = NSLP is active low
0x10	GENERAL	[0]	R/W	1	LP_EN 1 = enables Low-Power mode. In order to reduce power consumption under low load conditions, the unit will automatically switch off unused internal blocks. 0 = Low-Power mode not enabled

(2) The flag bit(s) can be cleared only by writing a zero to the associated register bit(s) or power cycling the device (V_{IOSYS} to LOW). Reading or RESET does not clear the flag bits. After clearing, the OVP, SCP, nPG fault flag(s) will be raised again '1' if the fault condition persists. The THSD flag will remain '0' after clear, even though the fault condition persists. Any flag bit High will cause the interrupt to be asserted on the INT pin. The INT pin will be pulled Low until all the flags are clear again.

0x11	RESET	[7:1]	R/W	0000000	RESERV Reserved
		[0]		0	SW_RESET Writing this bit with '1' and '0', in this order, will reset the registers to the default values. If NRST is still kept HIGH, the converter output(s) will be regulated to the programmed register values. If a full POR reset is required V _{IOSYS} must be pulled low. The fault flags are persistent over SW_reset.
0x12	DELAY_BUCK0	[7:0]	R/W	0000 0000	DELAY_B0 Master delay Sets the delay time from when NRST is asserted to when the V _{OUT} rail is enabled. Sets the delay time from when NRST is de-asserted to when the V _{OUT} rail is disabled. DELAY = DELAY_B0 * 100 μ s If DELAY_B0 = FFh, supply is never enabled. ⁽³⁾
0x18	CHIP_ID	[7:6]	R	00	VENDOR Contains Vendor ID
		[5:4]	R	00	ALL_LAYER Contains Revision ID
		[3:0]	R	0010	METAL_LAYER Contains Revision ID
0x19	PFM_LEV_B0	[6:4]	R/W	011	PFM_ENTRY_B0 ⁽⁴⁾ Sets the target PFM entry level for Buck 0. The final PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level. 000 = 50 mA 001 = 75 mA 010 = 100 mA 011 = 125 mA 100 = 175 mA 101 = 225 mA 110 = 275 mA 111 = 325 mA
0x19	PFM_LEV_B0	[2:0]	R/W	101	PFM_EXIT_B0 ⁽⁴⁾ Sets the target PFM exit level for Buck 0. The final PFM-to-PWM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level. 000 = 100 mA 001 = 125 mA 010 = 150 mA 011 = 175 mA 100 = 225 mA 101 = 275 mA 110 = 325 mA 111 = 375 mA
0x1F	PHASE_LEV_B0	[6:4]	R/W	100	ADD_PH_B0 ⁽⁵⁾ Sets the level on which a phase is added. 000 = 0.3A * No. of Active Phases 001 = 0.4A * No. of Active Phases 010 = 0.5A * No. of Active Phases 011 = 0.6A * No. of Active Phases 100 = 0.7A * No. of Active Phases 101 = 0.8A * No. of Active Phases 110 = 0.9A * No. of Active Phases 111 = 1.0A * No. of Active Phases

(3) If this register is set to FFh when the converter is already started, it will cause an immediate power down of the converter.

(4) For proper operation, the PFM exit current level should be at least 50 mA higher than the PFM entry current level.

(5) ADD_PH_B0 and SHED_PH_B0 values must be chosen so that the resulting hysteresis is a minimum of 100 mA and ADD_PH_B0 > SHED_PH_B0.

0x1F	PHASE_LEV_B0	[2:0]	R/W	010	SHED_PH_B0⁽⁵⁾ Sets the level of phase shedding. 000 = 0.3A * No. of Active Phases 001 = 0.4A * No. of Active Phases 010 = 0.5A * No. of Active Phases 011 = 0.6A * No. of Active Phases 100 = 0.7A * No. of Active Phases 101 = 0.8A * No. of Active Phases 110 = 0.9A * No. of Active Phases 111 = 1.0A * No. of Active Phases
0x21	SEL_I_LOAD	[6:4]	R/W	000	BUCK_LOAD_CURR This register reports 3 MSB bits of the magnitude of the average load current of the selected Buck Converter. The value is reported with a resolution of 10 mA per LSB and max 20A current.
0x21	SEL_I_LOAD	[2:0]	R/W	000	LOAD_CURRENT_SOURCE These bits are used for choosing the Buck Converter whose load current will be measured. 000 = Converter 0 load current will be measured. 001 = Converter 1 load current will be measured. 010 = Converter 2 load current will be measured. 011 = Converter 3 load current will be measured. 100 = Converter 4 load current will be measured. 101 = Converter 5 load current will be measured. 110 = Master total load current will be measured.
0x22	LOAD_CURR	[7:0]	R	0000 0000	BUCK_LOAD_CURR This register reports 8 LSB bits of the magnitude of the average load current of the selected Buck Converter. The value is reported with a resolution of 10 mA per LSB and 20A max current. The current reported is an average over the last 5 milliseconds. The host system has read-only access to this register. This register is cleared to 0 on all resets. 0000 0000 Load current lower than 10 mA 0000 0001 10 mA = Load current < 20 mA ... 1111 1110 2540 mA = Load current < 2550 mA 1111 1111 Load current 2550 mA or higher. Note: Not production tested. Typical values for reference only.
0x2E	INT_MASK_2	[3]	R/W	1	MASK_ILOAD_READY Interrupt mask for load current measurement flag 1 = Load current meas. completed does not set interrupt. 0 = Load current meas. completed sets interrupt.
0x2E	INT_MASK_2	[2]	R/W	0	MASK_UVLO Interrupt mask for under-voltage lock-out flag 1 = UVLO does not set interrupt. 0 = UVLO sets interrupt, when triggered.
0x2E	INT_MASK_2	[1]	R/W	1	MASK_TWARNING Interrupt mask for thermal warning flag 1 = T_WARNING does not set interrupt. 0 = T_WARNING sets interrupt, when triggered.
0x2E	INT_MASK_2	[0]	R/W	1	MASK_TEMP Interrupt mask for die temperature flag bits 1 = TEMP[1:0] value change does not set interrupt. 0 = TEMP[1:0] value change sets interrupt.
0xDD	LOCK_REG	[7:0]	R/W	N/A	LOCK_WORD As a safety precaution, the pre-programmed system configuration is locked until a lock word is applied on this register, to protect that configuration from accidental changes. If your application is going to run with a different configuration, please contact the Texas Instruments Sales Office/Distributors for further information and specifications.

APPLICATIONS INFORMATION

Application Description

The performance of the LP8755 device depends greatly on the care taken in designing the Printed Wiring Board (PWB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items. The separate power pins VINBxx are not connected together internally. The VINBxx power connections shall be connected together outside the package using power plane construction.

The DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. (Please request DC bias curves from the manufacturer as part of the inductor selection process.) Minimum effective value of inductance to ensure good performance is 0.25 μH at 3.2A (Default I_{LIMITP} typ.) bias current over the inductor's operating temperature range. The inductor's DC resistance should be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Table 10 below lists suggested inductors and suppliers. Shielded inductors radiate less noise and are preferable.

Application Components

Table 10. Inductor Selection

Item	Model	Vendor	Dimensions LxWxH (mm)	D.C.R (m Ω)MAX
L1 to L6; Step-down converter inductor 0.47 μH	XFL4015-471ME ⁽¹⁾ LQH32PNNR47NN0 ⁽²⁾ DFE252012 R47 ⁽³⁾ DFE201612C R47N ⁽⁴⁾ LQM2MPNNR47MGH ⁽⁴⁾	Coilcraft Murata TOKO TOKO Murata	4.0 x 4.0 x 1.5 3.2 x 2.5 x 1.55 2.5 x 2 x 1.2 2.0 x 1.6 x 1.2 2.0 x 1.6 x 1.0	8.4 30 $\pm$ 20 % 39 50 46
L1 to L6; Step-down converter inductor 0.68 μH	DFE322512 R68	TOKO	3.2 x 2.5 x 1.2	37
L1 to L6; Step-down converter inductor 1.0 μH	DFE322512 1R0	TOKO	3.2 x 2.5 x 1.2	45

(1) Best efficiency.

(2) Good balance between size and efficiency.

(3) Satisfactory compromise between size and efficiency.

(4) Applications for which solution size is critical, efficiency compromised on very high loads.

Input Capacitor Selection

A ceramic input capacitor of 10 μF , 10V is sufficient for most applications. Place the input capacitor as close as possible to the VINBxx pin and GND pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R or X5R types, do not use Y5V or F. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402. Minimum effective input capacitance to ensure good performance is 2.5 μF at maximum input voltage DC bias including tolerances and over ambient temp range, assuming that there is at least 22 μF of additional capacitance common for all the power input pins on the system power rail.

The input filter capacitor supplies current to the PFET (high-side) switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating.

Table 11. Recommended Input/Output Capacitors (X5R Dielectric)

Manufacturer	Part Number	Value	Case Size	Voltage Rating
Murata	GRM188R60J106ME84	10 μ F (20%)	0603	6.3V
TDK	C1608X5R1A106KT	10 μ F (10%)	0603	10V
Taiyo Yuden	LMK107BJ106MALTD	10 μ F (20%)	0603	10V
Samsung	CL10A226MP8NUNE	22 μ F (20%)	0603	10V

Output Capacitor Selection

Use ceramic capacitor, X7R or X5R types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. Minimum effective output capacitance to ensure good performance in 6-phase configuration is 30 μ F at the output voltage DC bias including tolerances and over ambient temp range. The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR} . The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR} . The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See recommended capacitors in [Table 11](#).

A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreasing the PFM switching frequency. For most 6-phase applications 4 x 22 μ F 0603 capacitors for C_{OUT} is suitable. Although the converter's loop compensation can be programmed to adapt to virtually several hundreds of microfarads C_{OUT}, an effective C_{OUT} less than 120 μ F is preferred -- there is not necessarily any benefit to having a C_{OUT} higher than 120 μ F. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (>100 μ F) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at startup, the time required to charge the output capacitor to target value might be longer. At shutdown, if the output capacitor is discharged by the internal discharge resistor, more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Layout and Routing Recommendations

The high frequency and large switching currents of the LP8755 make the choice of layout important. Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10A and over, good power-supply layout is more challenging than for most general PWB design. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range:

1. Place C_{IN} as close as possible to the VINBxx terminal and the GND terminal. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and LP8755's VINBxx pin(s) as well as the trace between the input capacitor's negative node and power GND pin or pins must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor - parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter, consisting of C_{OUT} and L, converts the switching signal at SW to the noiseless output voltage. For optimal EMI behavior, it should be placed as close as possible to the device, keeping the switch node small. Route the traces between the LP8755's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VDDA5V and GNDA) should be isolated from noisy signals. Connect VDDA5V directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. For additional noise immunity, adding a high-frequency decoupling capacitor of 100 nF to 1 μ F is recommended. Place the decoupling capacitor as close to the VDDA5V pin as possible. Current on VDDA5V trace is low, so the trace width is not an issue.
4. If the processor load supports voltage remote sensing, connect the LP8755's feedback pins FBBxx to the

respective sense pins on the processor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND, VIN, and SW, as well as high bandwidth signals such as the I²C. Avoid both capacitive as well as inductive coupling by keeping the sense lines short, direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended.

5. PGND, VIN, and SW should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND, VIN, and SW. They create a flux which is determined by the switching frequency. The flux generated affects neighboring layers due to capacitive coupling across layers.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PWB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PWB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PWB designs with vias to different planes. This results in reduced junction-to-ambient (θ_{JA}) and junction-to-board (θ_{JB}) thermal resistances, thereby reducing the device junction temperature, T_J . It's strongly recommended to perform a careful system-level 2D or full 3D dynamic thermal analysis at the beginning of the product design process, using a thermal modeling analysis software.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8755KME/NOPB	ACTIVE	DSBGA	YFQ	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85		Samples
LP8755KMX/NOPB	ACTIVE	DSBGA	YFQ	49	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

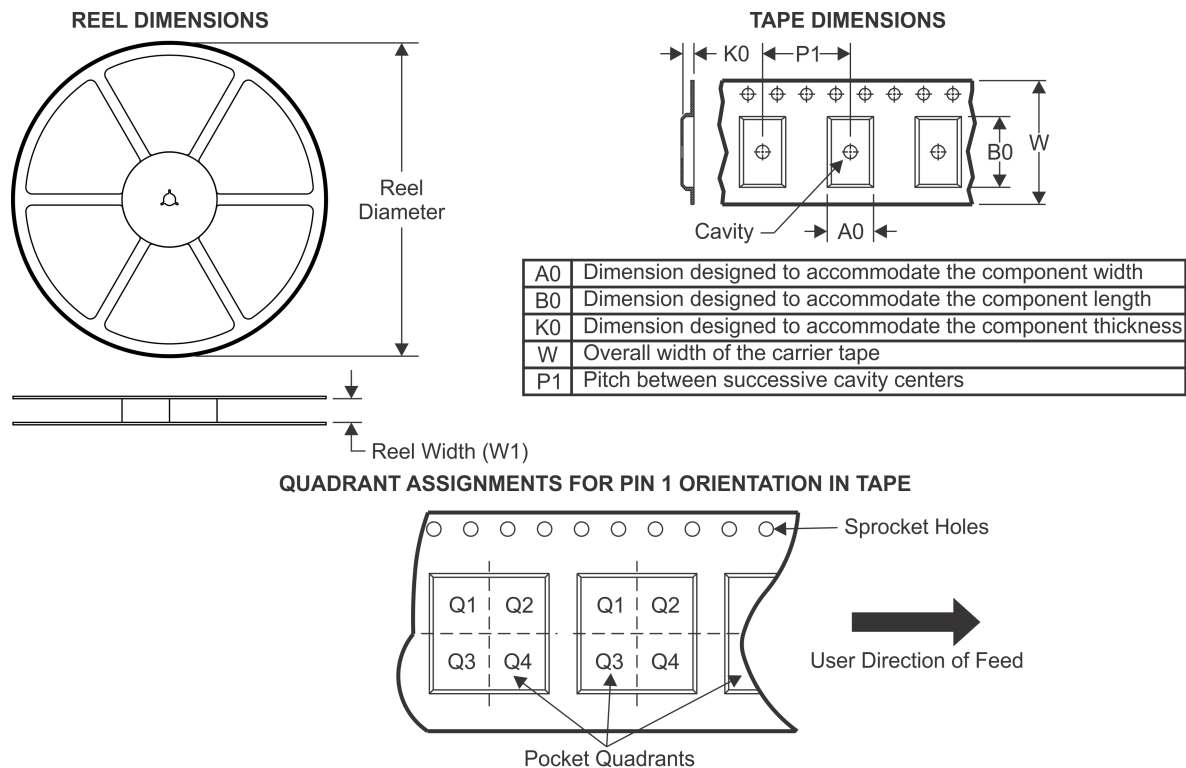
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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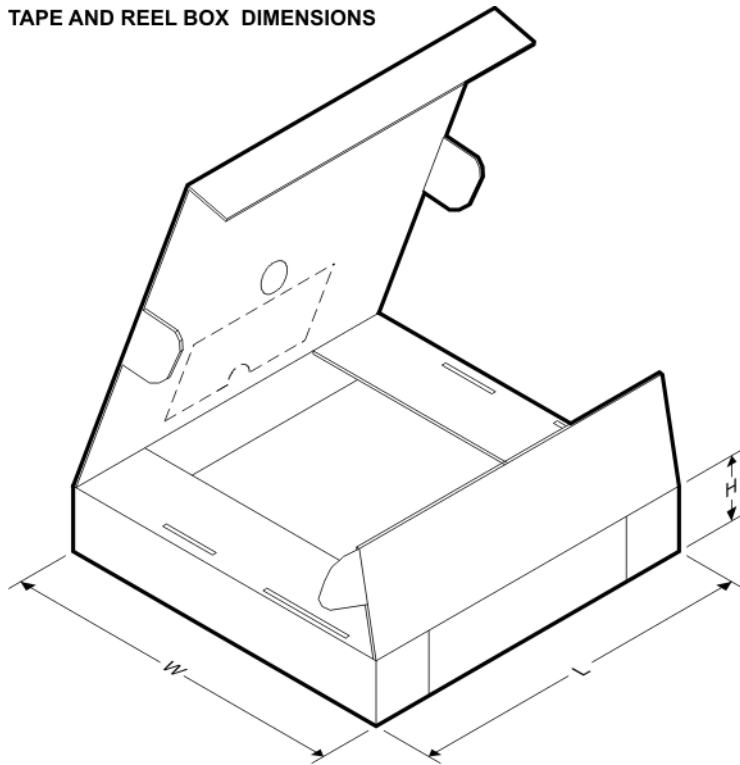
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8755KME/NOPB	DSBGA	YFQ	49	250	180.0	13.0	3.06	3.2	0.71	8.0	12.0	Q1
LP8755KMX/NOPB	DSBGA	YFQ	49	1000	180.0	13.0	3.06	3.2	0.71	8.0	12.0	Q1

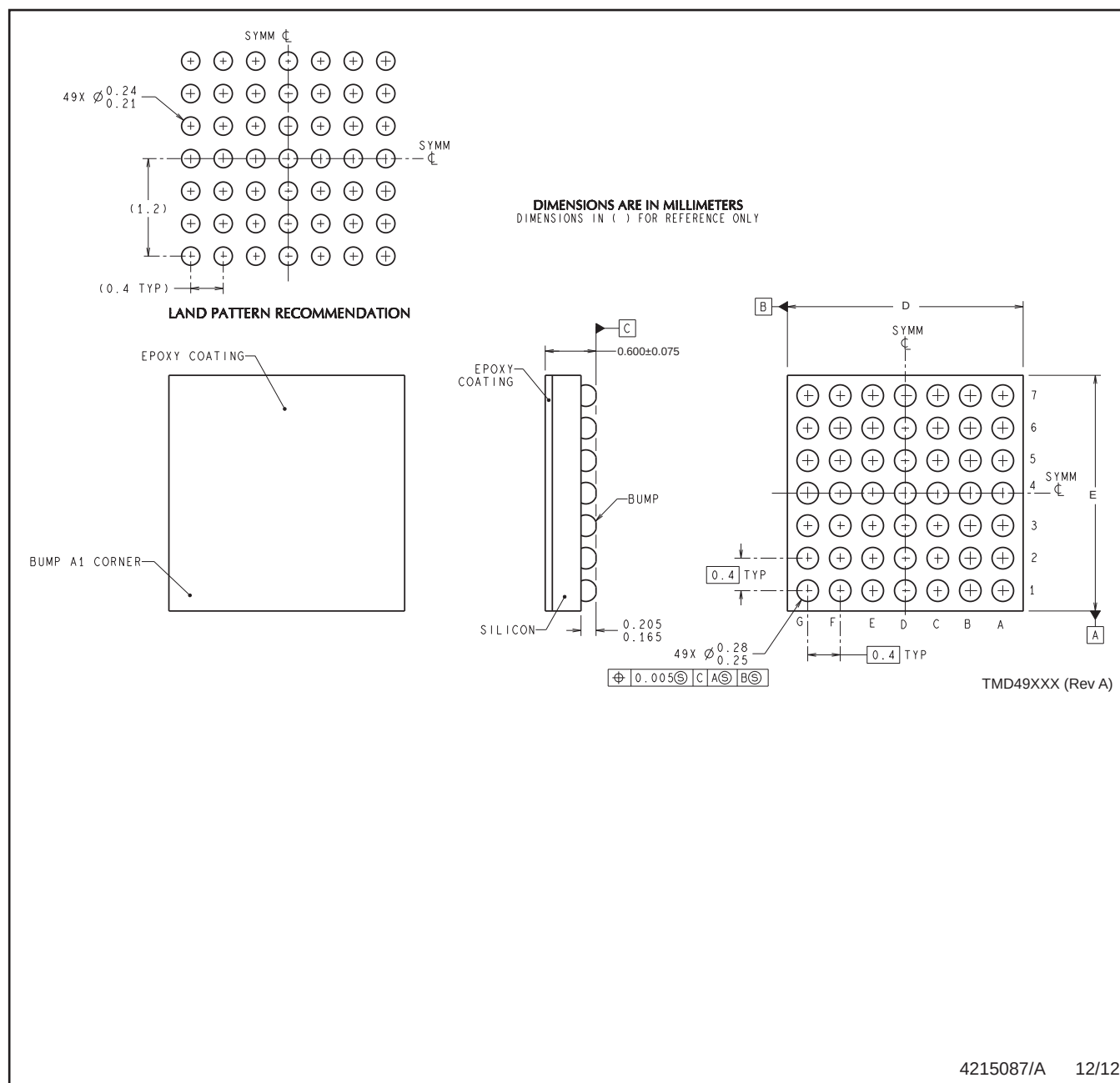
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8755KME/NOPB	DSBGA	YFQ	49	250	200.0	230.0	25.0
LP8755KMX/NOPB	DSBGA	YFQ	49	1000	200.0	230.0	25.0

YFQ0049



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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