NCP338

2A Ultra-Small Controlled Load Switch with Auto-discharge Path

The NCP338 is very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail.

Proposed in a wide input voltage range from 1.0 V to 3.6 V, in a small 0.8 x 1.2 mm WLCSP6, pitch 0.4 mm.

Features

- 1.0 V – 3.6 V Operating Range
- 16 mΩ P MOSFET at 3.6 V
- DC Current Up to 2 A
- Output Auto−discharge
- Active High EN Pin
- WLCSP6 0.8 x 1.2 mm
- ESD Ratings: 6 kV HBM, 250 V MM
- This is a Pb−Free Device

Typical Applications

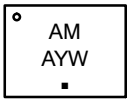
- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

ON Semiconductor®

http://onsemi.com

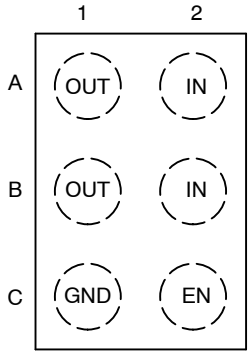
MARKING DIAGRAM

WLCSP6
CASE 567FY



AM = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

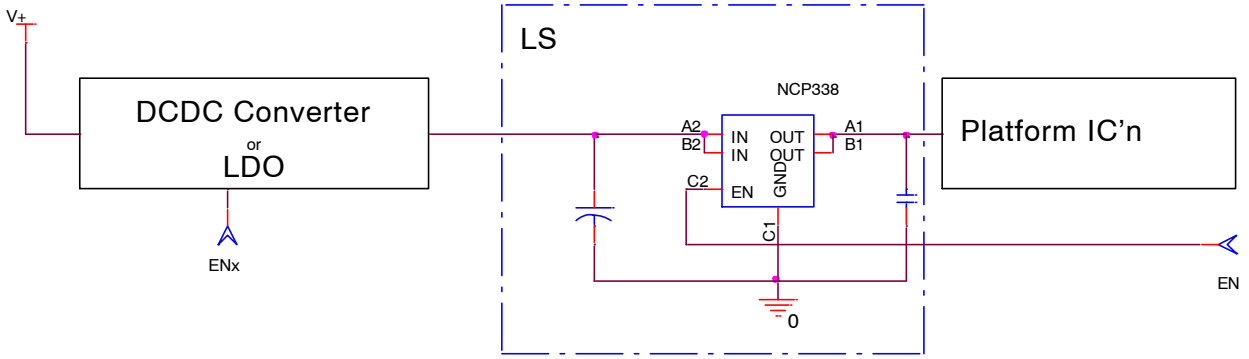


Figure 1. Typical Application Circuit

© Semiconductor Components Industries, LLC, 2013

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2, B2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	C1	POWER	Ground connection.
EN	C2	INPUT	Enable input, logic high turns on power switch.
OUT	A1, B1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

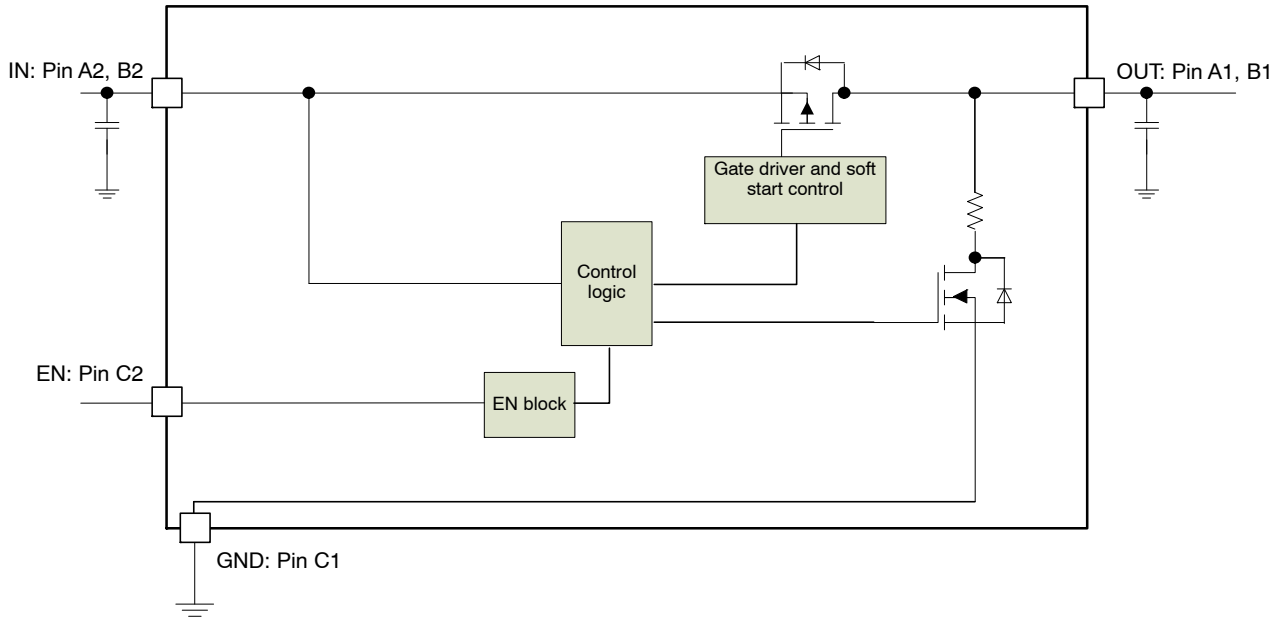


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins	V_{EN} , V_{IN} , V_{OUT}	−0.3 to + 4.0	V
From IN to OUT Pins: Input/Output	V_{IN} , V_{OUT}	0 to + 4.0	V
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Human Body Model (HBM) ESD Rating are (Note 1 and 2)	ESD HBM	6000	V
Machine Model (MM) ESD Rating are (Note 1 and 2)	ESD MM	250	V
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.0		3.6	V
V_{EN}	Enable Voltage			0		3.6	
T_A	Ambient Temperature Range			−40	25	+85	°C
T_J	Junction Temperature Range			−40	25	+125	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)			100		°C/W
I_{OUT}	Maximum DC current					2	A
P_D	Power Dissipation Rating (Note 6)	$T_A \le 25°C$	WLCSP package			1	W
		$T_A = 85°C$	WLCSP package			0.4	W

4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation ($_{PD}$) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for $_{TA}$ between −40°C to +85°C for $_{VIN}$ between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 3.6 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance at −200 mA	V_{IN} = 3.6 V	T_A = 25°C		16	27	mΩ
			−40°C < T_A < 85°C			30	
		V_{IN} = 2.5 V	T_A = 25°C		21	36	
			−40°C < T_A < 85°C			40	
		V_{IN} = 1.8 V	T_A = 25°C		27	40	
			−40°C < T_A < 85°C			45	
		V_{IN} = 1.2 V	T_A = 25 °C		52	87	
			−40°C < T_A < 85°C			99	
	Static drain−source on−state resistance at −100 mA	V_{IN} = 1.1 V	T_A = 25°C		67		
Rdis	Output discharge path	EN = low	Vin = 3.3 V		65	90	Ω
V_{IH}	High−level input voltage	Vin = 1.8 V		0.95			V
V_{IL}	Low−level input voltage					0.5	V
I_{EN}	EN leakage current				20		nA
CURRENT CONSUMPTION							
Istd	Standby current	V_{OUT} = open, EN = low, V_{IN} = 3.6 V			20	300	nA
		V_{OUT} = open, EN = low, V_{IN} = 1.8 V			4		
Iq	Quiescent current	V_{OUT} = open, EN = high, V_{IN} = 3.6 V			200	600	
		V_{OUT} = open, EN = high, V_{IN} = 1.8 V			80	300	

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.
8. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 3.6 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TIMINGS							
T_{ON}	Turn on time	V_{IN} = 1.2 V	C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		40		μs
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		40		
T_R	V_{OUT} rise time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		20		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		25		
T_{OFF}	Turn off time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		10		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		10		
T_{FALL}	V_{OUT} fall time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		20		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		200		
TIMINGS							
T_{ON}	Turn on time	V_{IN} = 1.8 V	C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		40		μs
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		40		
T_R	V_{OUT} rise time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		30		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		35		
T_{OFF}	Turn off time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		10		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		10		
T_{FALL}	V_{OUT} fall time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		15		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)		150		

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.
8. Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 3.6 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TIMINGS							
T_{ON}	Turn on time	V_{IN} = 3.6 V	C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		30		μs
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)	0	32	80	
T_R	V_{OUT} rise time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		20		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)	0	20	50	
T_{OFF}	Turn off time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		10		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)	0	10	40	
T_{FALL}	V_{OUT} fall time		C_{LOAD} = 0.1 μF, R_{LOAD} = 500 Ω (Note 7)		10		
			C_{LOAD} = 1 μF, R_{LOAD} = 500 Ω (Note 7)	0	100	300	

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.
8. Guaranteed by design and characterization.

TIMINGS

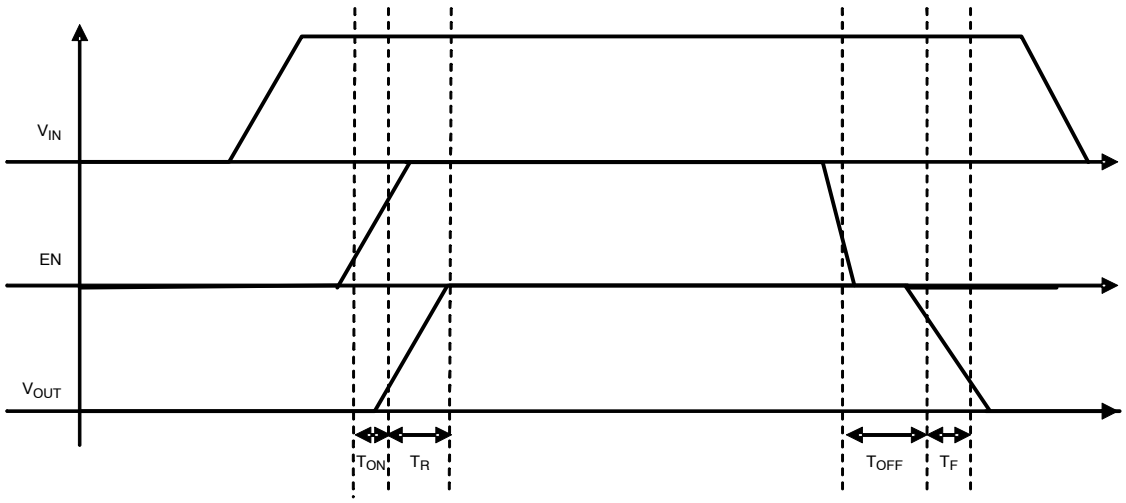


Figure 3. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

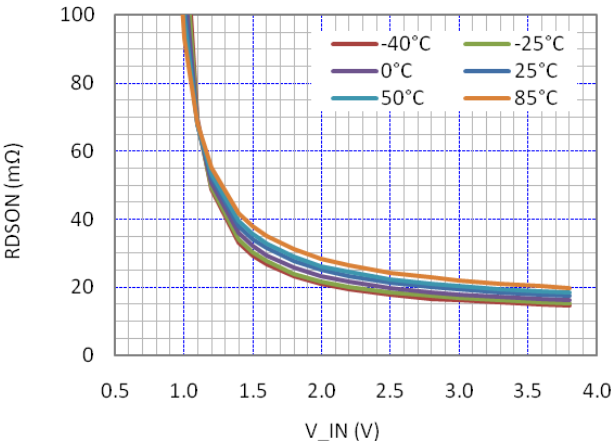


Figure 4. $R_{DS(on)}$ (mΩ) vs. Vin (V) in Temperature

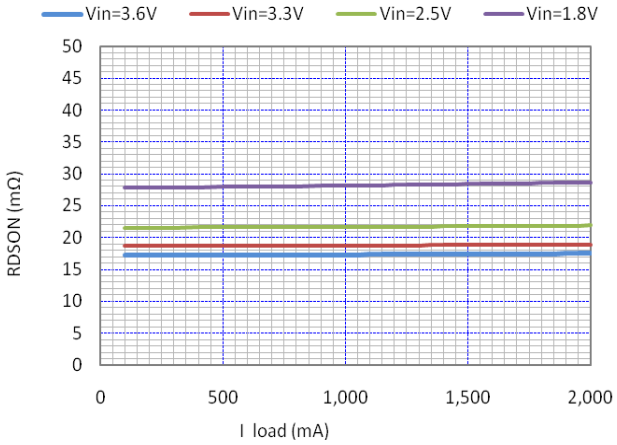


Figure 5. $R_{DS(on)}$ (mΩ) vs. I_{load} at Different Input Voltage

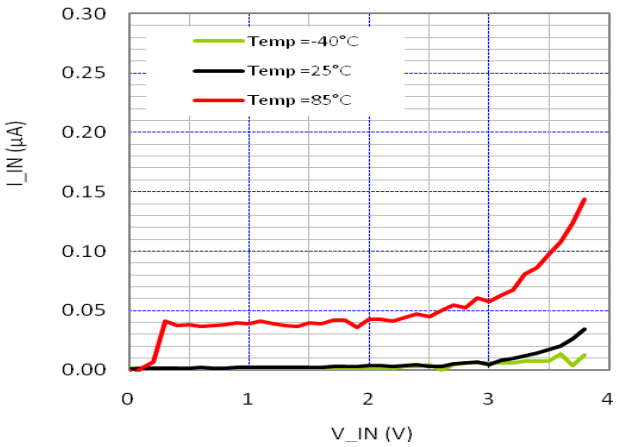


Figure 6. Standby Current (µA) vs. Vin (V)

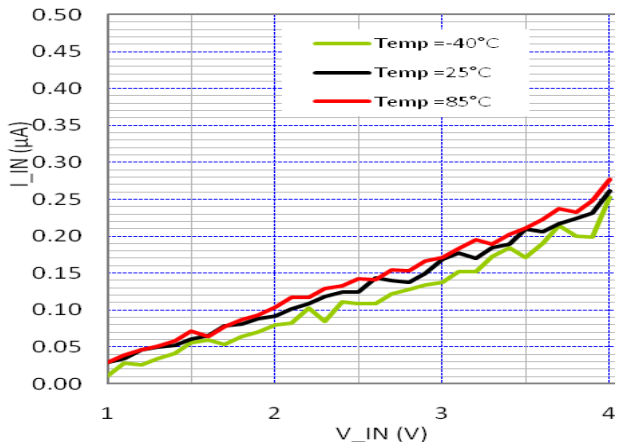


Figure 7. Quiescent Current (µA) vs. Vin (V)

FUNCTIONAL DESCRIPTION

Overview

The NCP338 is a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.0 V to 3.6 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P−MOS switch off.

The IN/OUT path is activated with a minimum of Vin of 1.2 V and EN forced to high level.

Auto Discharge

N−MOSFET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 1.0 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at 65 Ω.

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part to for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

PCB Recommendations

The NCP338 integrates an up to 2 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

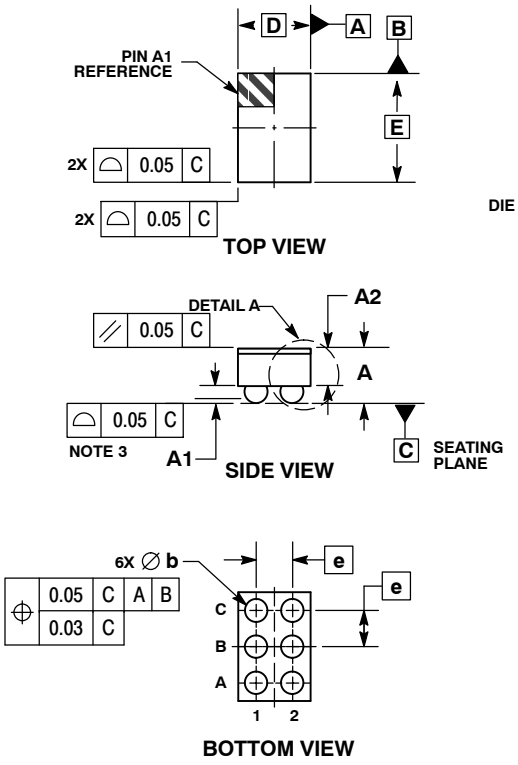
ORDERING INFORMATION

Device	Marking	Autodischarge	Package	Shipping†
NCP338FCCT2G	AM	Yes	WLCSP 0.8 x 1.2 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

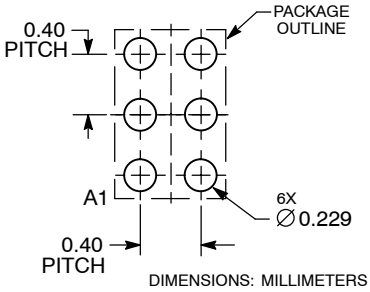
WLCSP6, 0.80x1.20
CASE 567FY
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.28 REF	
A3	0.04 REF	
b	0.21	0.25
D	0.80 BSC	
E	1.20 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NCP338/D