
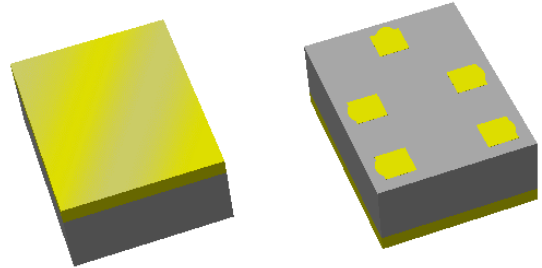


Data Sheet

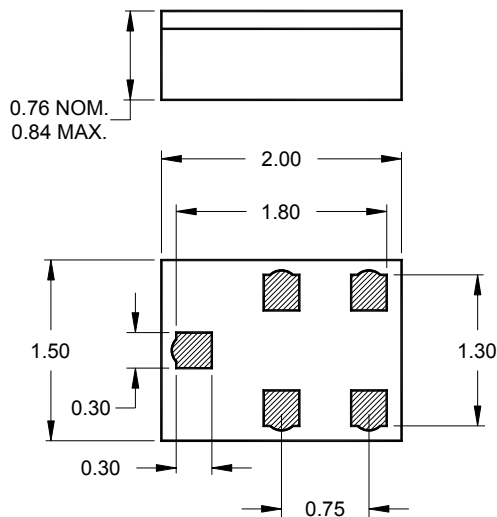
Features

- For CDMA-ZIF applications
- Usable bandwidth 25 MHz
- Low loss
- Single-ended input, 50 Ω
- Balanced output, 100 Ω
- No Impedance matching required
- Superior amplitude and phase balance
- Ceramic Chip Scale Package (CSP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



Package

Surface Mount 2.00 x 1.50 x 0.76 mm

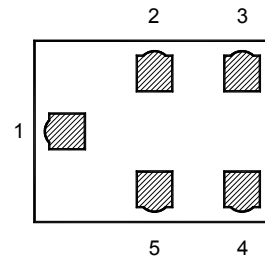


Dimensions shown are nominal in millimeters
 All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
 Lid: Kovar or Alloy 42, Au over Ni plated
 Terminations: Au plating 0.5 - 1.0 μ m,
 over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



Pin No.	Description
1	Input, Single-ended
3,4	Output, Balanced
2,5	Case ground

Data Sheet

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ -30 to +85 °C

Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency	-	881.5	-	MHz
Maximum Insertion Loss 869 - 894 MHz	-	2.0	2.5	dB dB
Amplitude Variation 869 - 894 MHz	-	0.6	1.2	dBp-p
Absolute Attenuation 10 - 824 MHz	50	70	-	dB
824 - 849 MHz	35	37	-	dB
914 - 960 MHz	24	27	-	dB
960 - 3000 MHz	50	56	-	dB
Input/Output Return Loss 869 - 894 MHz	9	12	-	dB
Output Amplitude Balance (S_{31} / S_{21}) 869 - 894 MHz	-0.5	0	0.5	dB
Output Phase Balance [$\phi(S_{31}) - \phi(S_{21}) + 180$] 869 - 894 MHz	-5	0	5	degree
Optimal Source Impedance ⁽⁴⁾	-	50	-	Ω
Optimal Load Impedance ⁽⁴⁾	-	188 251nH	-	Ω

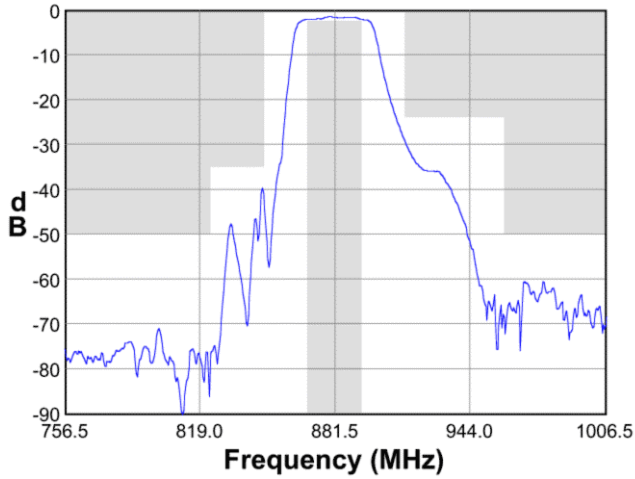
Notes:

1. All specifications are based on the Sawtek reference test system
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. This is the optimum impedance in order to achieve the performance shown

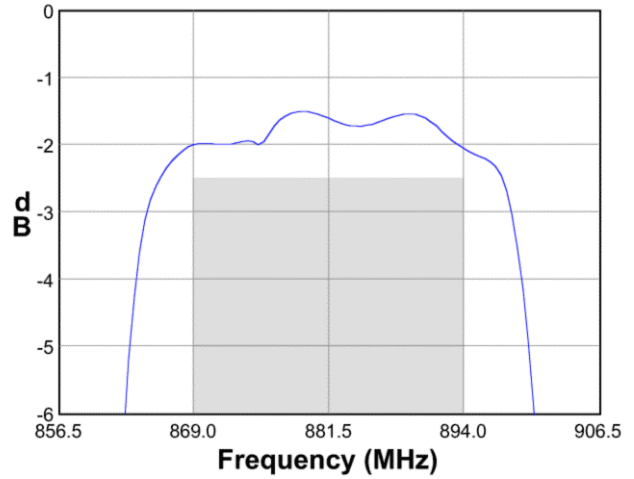
Data Sheet

Typical Performance (at +25°C)

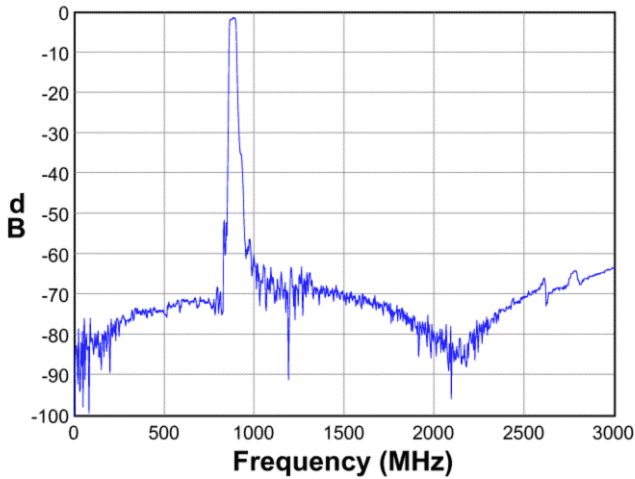
Frequency Response



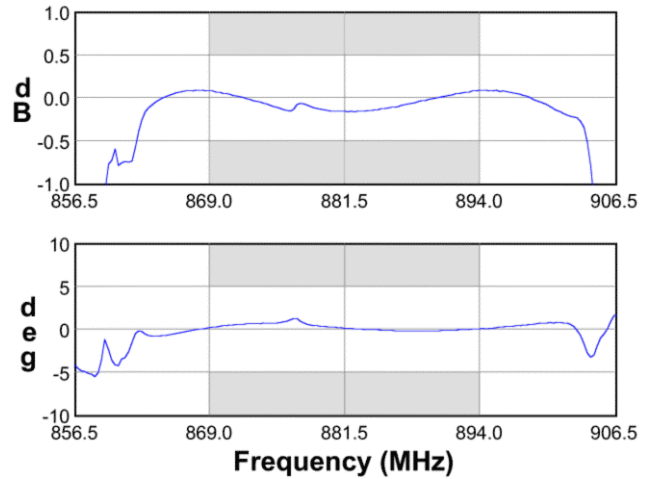
Passband Response



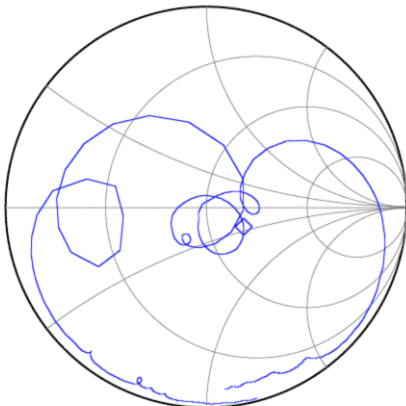
Wideband Response



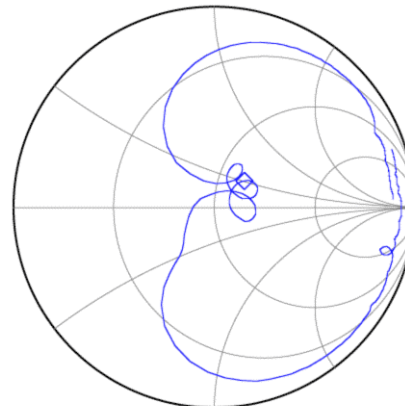
Amplitude/Phase Balance



Input Smith Chart



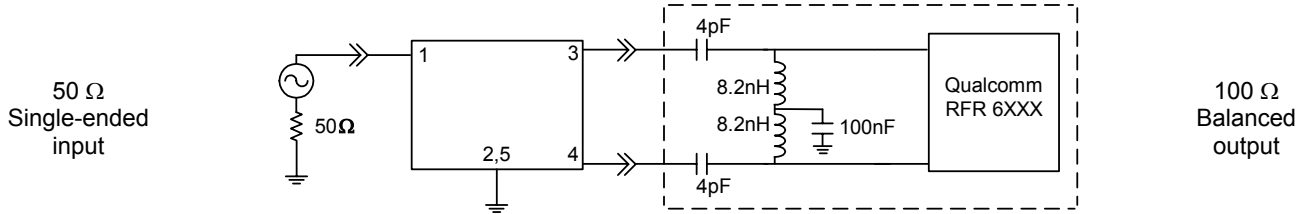
Output Smith Chart



Data Sheet

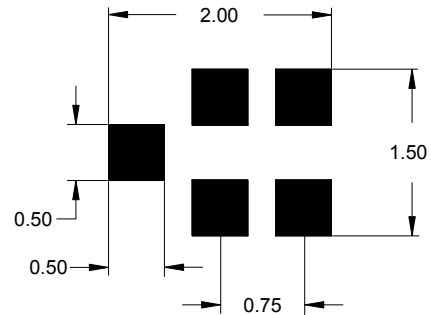
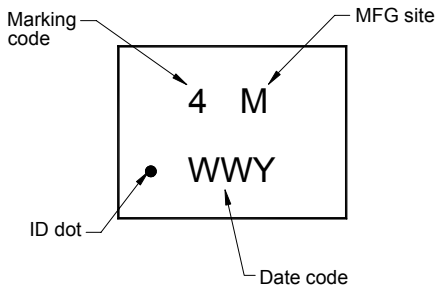
Matching Schematics

Actual matching values may vary due to PCB layout and parasitics



Marking

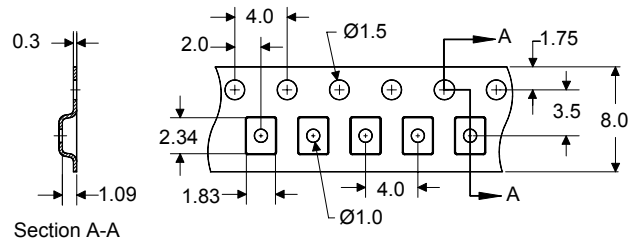
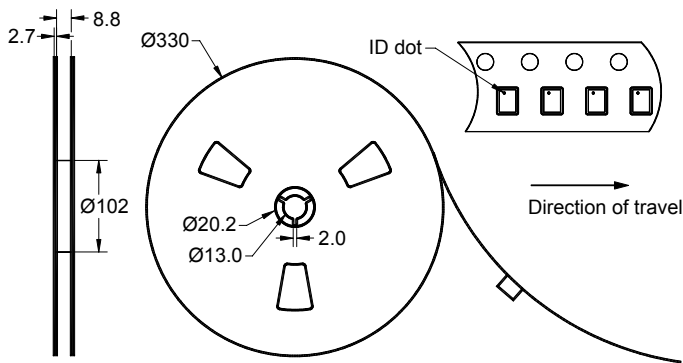
PCB Footprint



The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code

This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel



Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel


Data Sheet

Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-30	+85	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JEDEC J-STD-020C **Pb**-free process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS information](#)

[Other Technical Information](#)

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[representatives or distributors](#)