SONY

CXA3506R

3-channel 8-bit 120MSPS A/D Converter Amplifier PLL

Description

The CXA3506R is a 3-channel 8-bit 120MSPS A/D converter with built-in amplifier and PLL developed for LCD projectors and LCD monitors.

The CXA3506R inputs RGB graphics signals from personal computers or others. After the input levels are controlled, the A/D conversion is performed with a clock generated by PLL.

The digital output levels are compatible with TTL.

This IC operates at a maximum conversion rate of 120MHz, and can support up to XGA. Control register supports both I^2C and 3-wire bus.

Features

- Supply voltage: 5V, 3.3V
- Power consumption: 1.7W typ. (120MSPS)
- 144-pin LQFP
- 3-ch AMP and PLL eliminate design time for mutual connections.

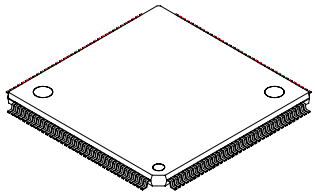
Structure

Bipolar silicon monolithic IC

Applications

- LCD monitors
- LCD projectors
- Digital TVs
- PDPs

144 pin LQFP (Plastic)



Functions and Performance

- Power save function
- Supports both I^2C and 3-wire bus

Amplifier block

- Clamp
- Main contrast: 8-bit
- Sub contrast: 8-bit × 3
- Main brightness: 8-bit × 3
- CbCr offset: 6-bit × 2
- Supports YCbCr input
- Two input systems
- AMP monitor output/SW monitor output
- SYNCSEP function

A/D converter block

- Maximum conversion rate: 120MSPS
- Supports XGA input
- Supports demultiplexed output
- Supports both in-phase and alternate phase during demultiplexing
- Supports YUV4:2:2 output
- Output high impedance mode
- Built-in reference voltage

PLL block

- Sync input frequency: 10kHz to 100kHz
- Clock delay: 1/32 to 64/32CLK
- VCO counter: 12-bit
- Low clock jitter
- CLK inversion
- CLK and 1/2CLK outputs
- Phase comparison hold
- Output high impedance mode

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E99Y22B1Z-PS

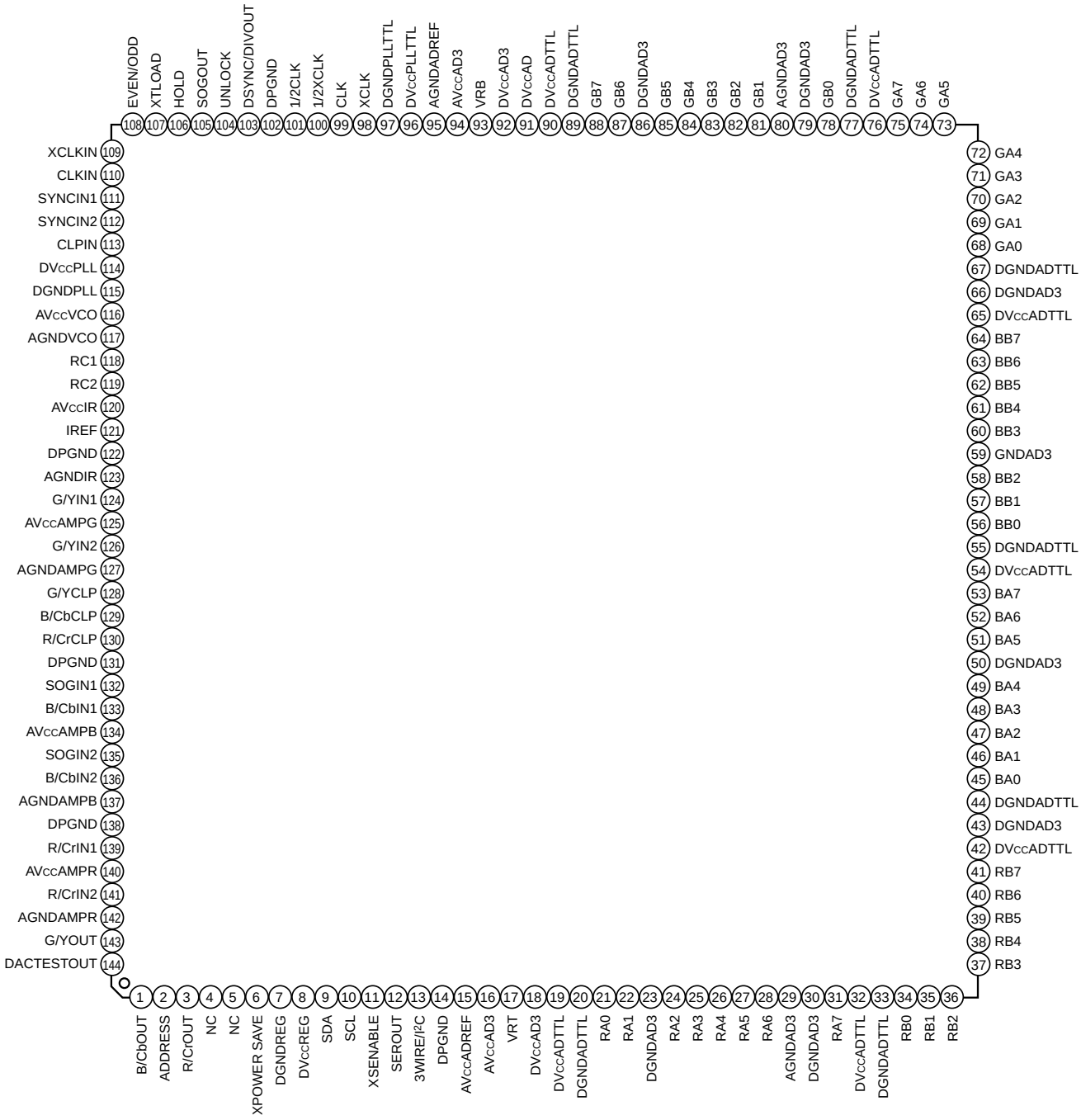
Absolute Maximum Ratings (Ta = 25°C)

Item		Maximum ratings	Unit
Supply voltage	DVccREG, AVccADREF, DVccADTTL, DVccAD, DVccPLLTTL, AVccVCO, DVccPLL, AVccIR, AVccAMPR, AVccAMPG, AVccAMPB	5.5	V
	AVccAD3, DVccAD3	5.5	V
Input voltage	ADDRESS, XPOWERSAVE, XSENABLE, 3WIRE/I²C, HOLD, XTLOAD, EVEN/ODD, XCLKIN, CLKIN, SYNCIN1, SYNCIN2, CLPIN, RC1, RC2, R/CrIN1, R/CrIN2, R/CrCLP, G/YCLP, B/CbCLP, SOGIN1, G/YIN1, SOGIN2, G/YIN2, B/CbIN1, B/CbIN2, RCrOUT, G/YOUT, B/CbOUT, DACTESTOUT	GND – 0.5 to 5V Vcc + 0.5 or 5.5	V
	SDA, SCL	GND – 0.5 to 5.5	V
Storage temperature	Tstg	–65 to +150	°C
Allowable power dissipation	P_D	5	W

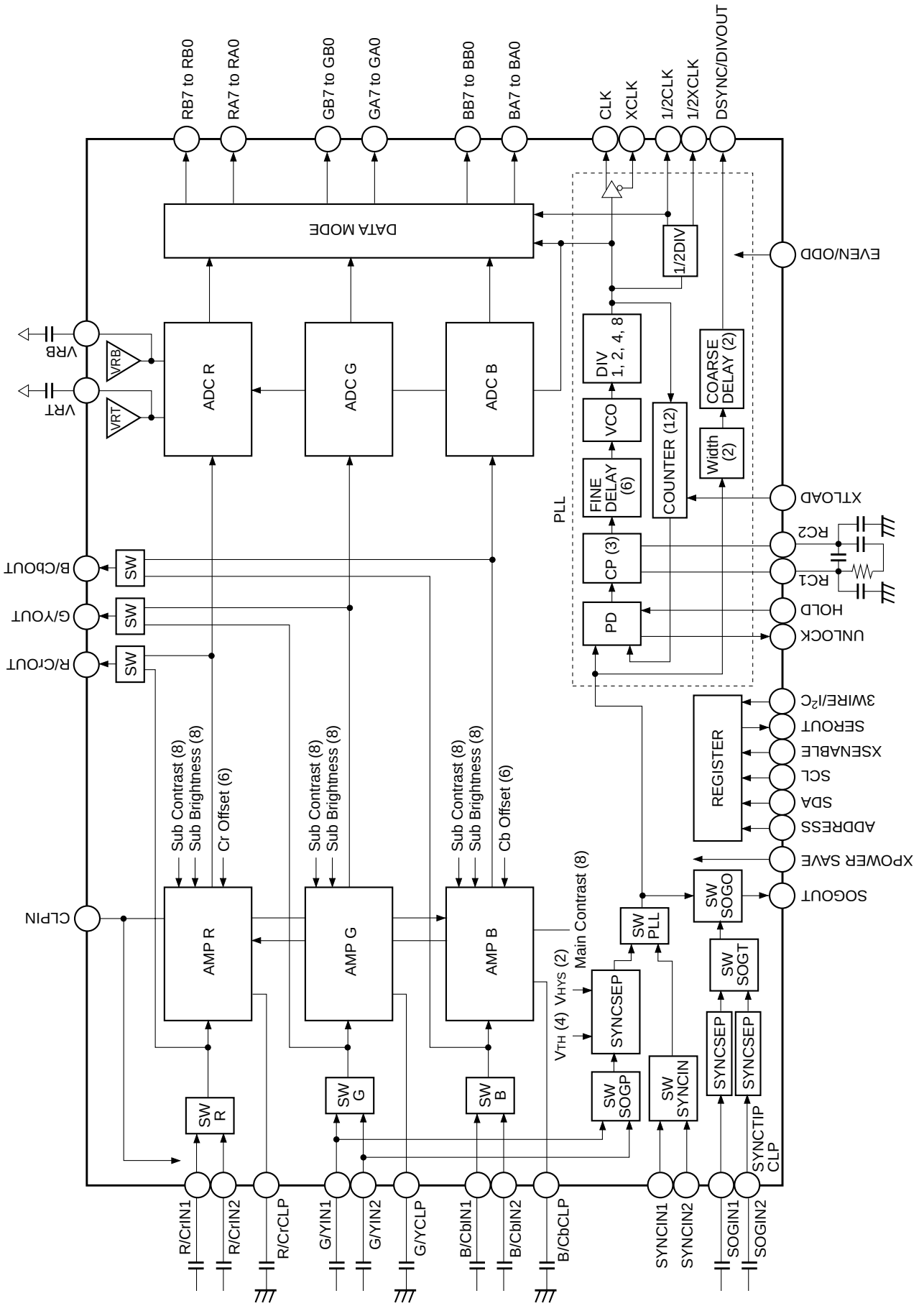
Recommended Operating Conditions

Item			Min.	Typ.	Max.	Unit
Supply voltage	DVccREG, AVccADREF, DVccADTTL, DVccAD, DVccPLLTTL, DVccPLL, AVccVCO, AVccIR, AVccAMPR, AVccAMPG, AVccAMPB		4.75	5	5.25	V
	AVccAD3, DVccAD3		3	3.3	3.6	V
TTL input pin	XPOWERSAVE, HOLD, XTLOAD, EVEN/ODD, SYNCIN1, SYNCIN2, CLPIN	High level	2	—	—	V
		Low level	—	—	0.8	V
PECL input pin	CLKIN, XCLKIN	High level	DVccPLL –0.8	—	—	V
		Low level	—	—	DVccPLL –1.6	V
Maximum conversion rate	Straight mode		100	—	—	MSPS
	DMUX mode		120	—	—	MSPS
	YUV4:2:2 D2 mode		100	—	—	MSPS
	YUV4:2:2 special mode		100	—	—	MSPS
Operating ambient temperature	Ta		–10	—	+75	°C

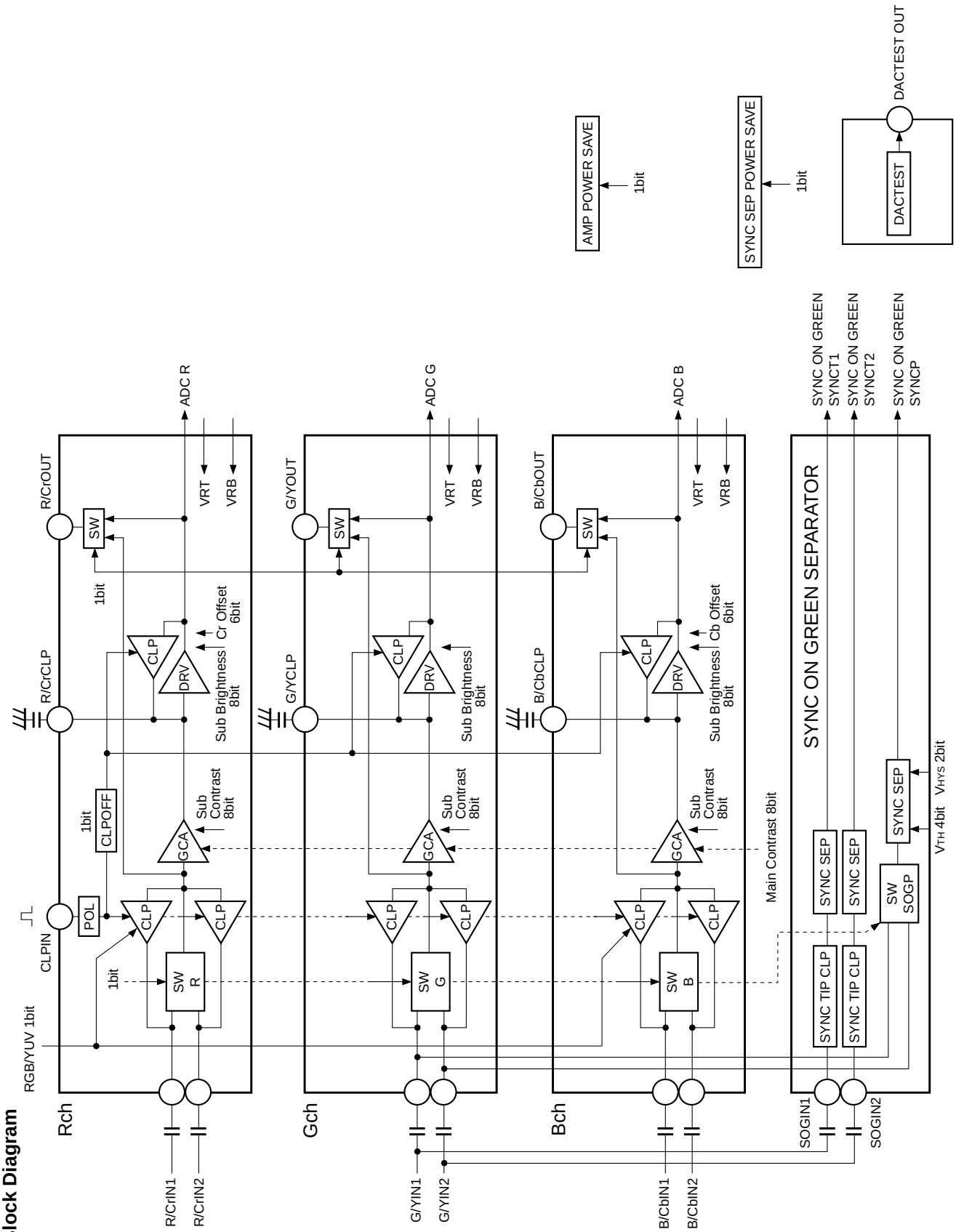
Pin Configuration (Top View)



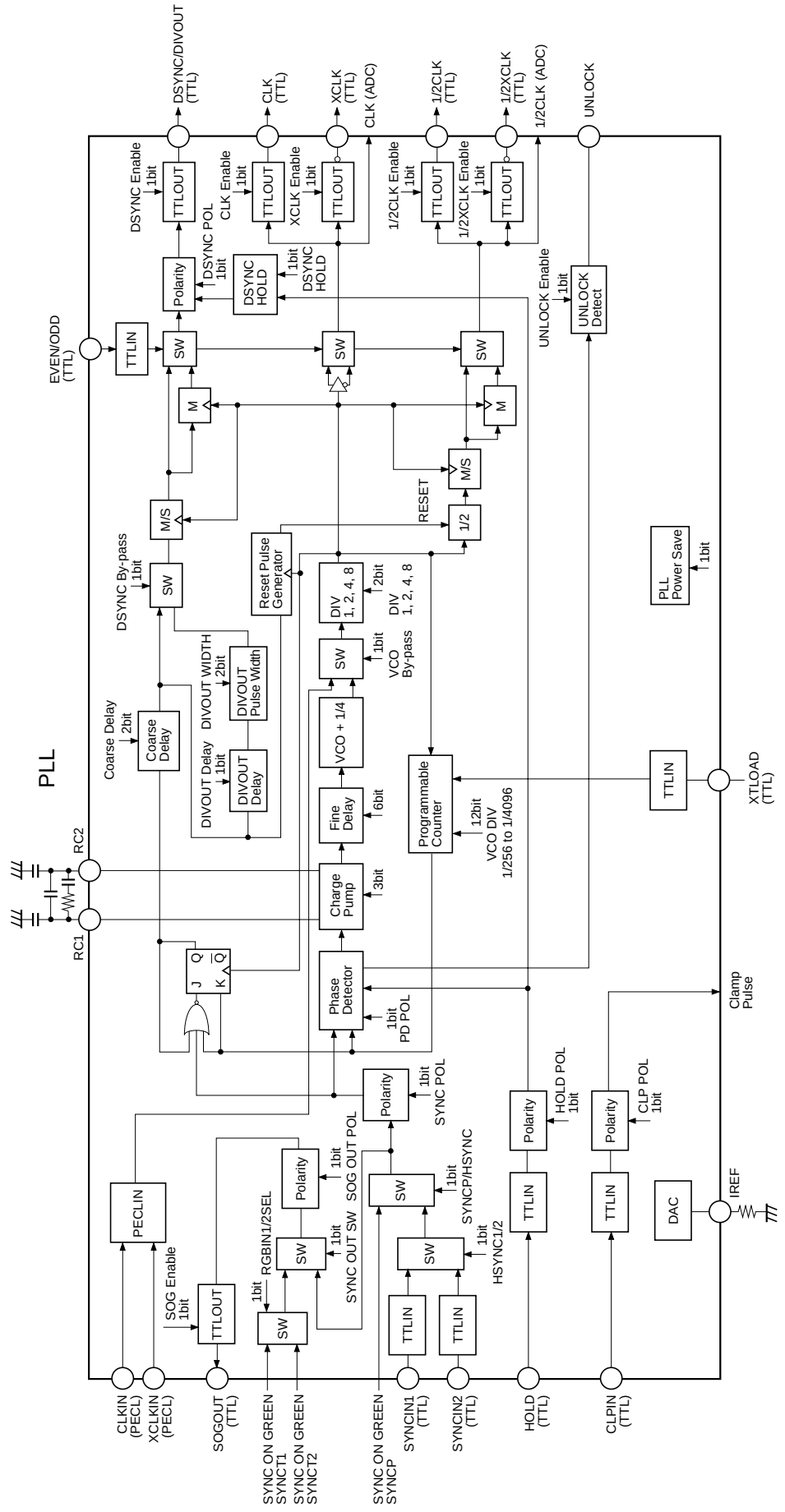
TOP Block Diagram



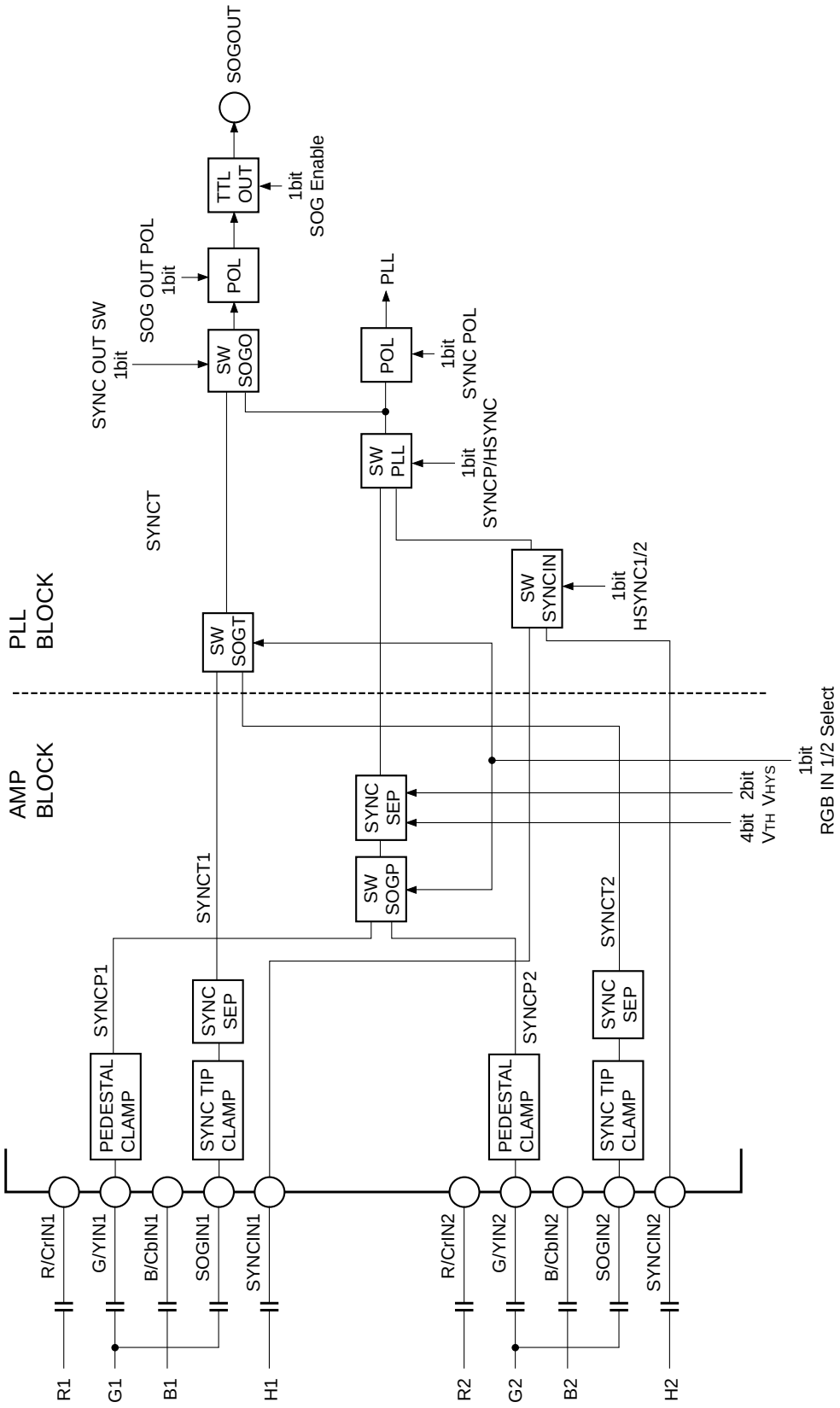
Amplifier Block Diagram



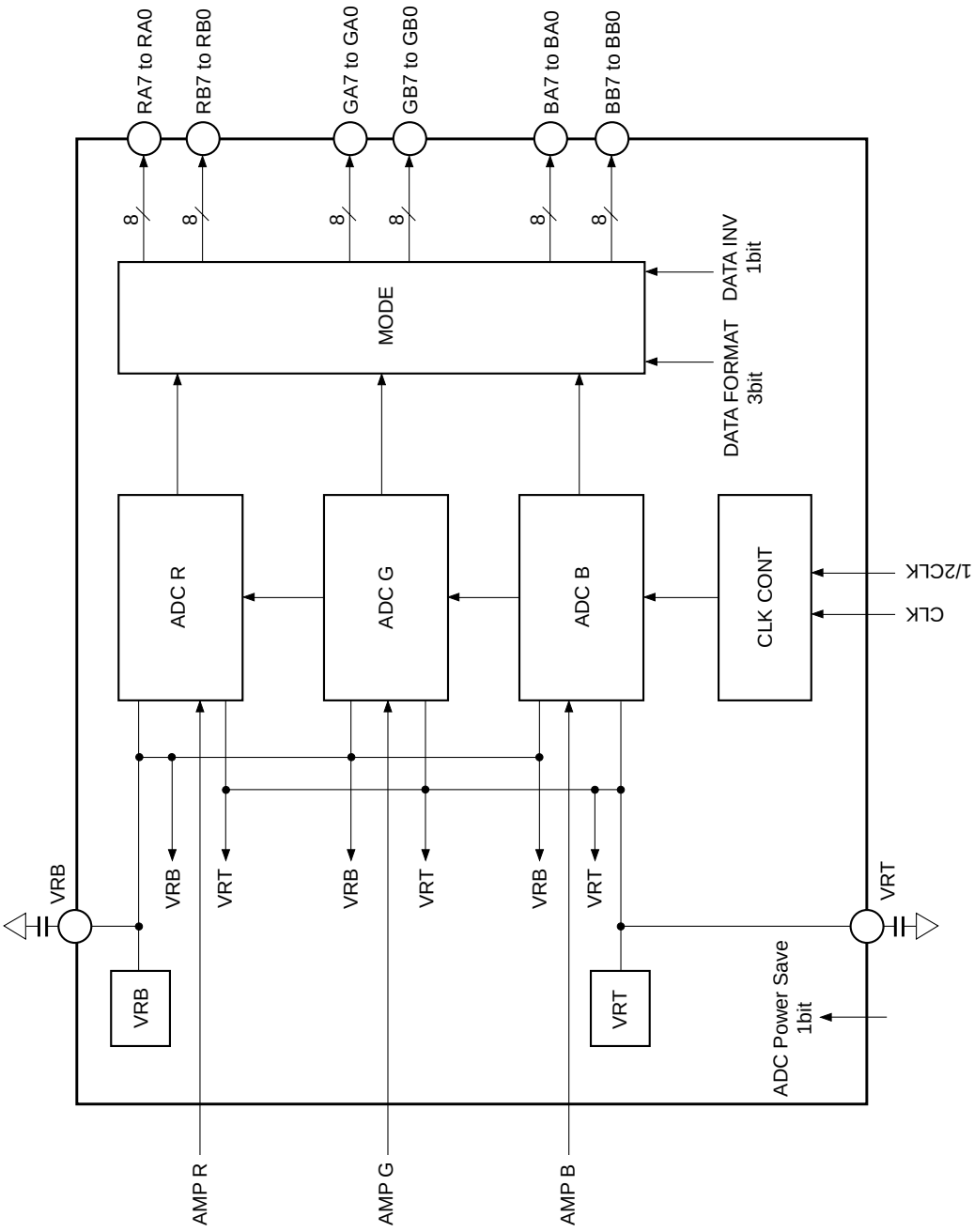
PLL Block Diagram



SYNC Block Diagram



ADC Block Diagram



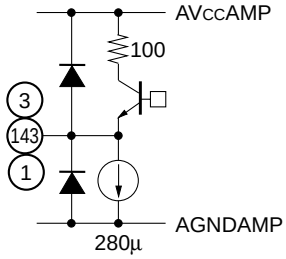
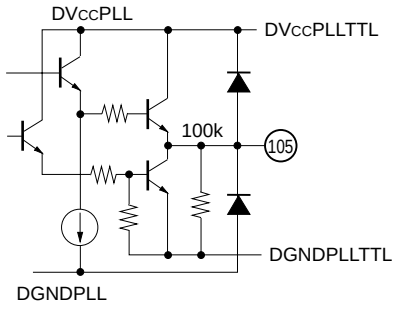
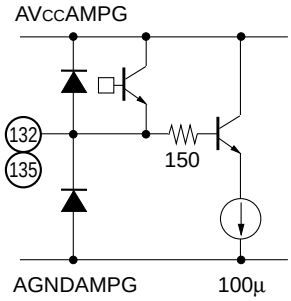
Pin Description

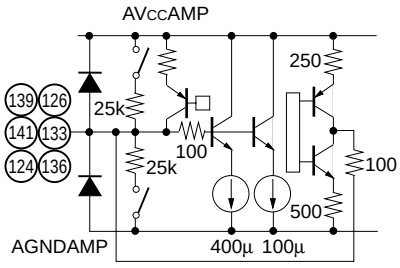
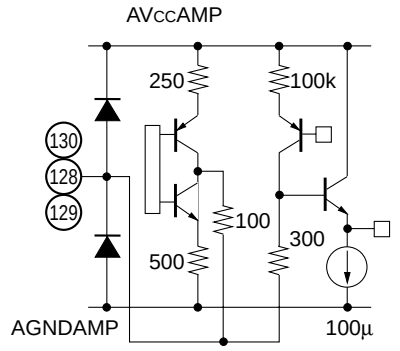
Pin No.	Symbol	I/O	Typical signal	Description
1	B/CbOUT	O	1.83V	Amplifier output signal monitor
2	ADDRESS	I	—	I^2C slave address setting
3	R/CrOUT	O	1.83V	Amplifier output signal monitor
4	NC	—	—	Not used
5	NC	—	—	Not used
6	XPOWER SAVE	I	TTL	Power save setting
7	DGNDREG	—	GND	Register GND
8	DVccREG	—	5V	Register power supply
9	SDA	I	—	Control register data input
10	SCL	I	—	Control register CLK input
11	XSENABLE	I	TTL	Enable signal input for 3-wire control register
12	SEROUT	O	TTL	3-wire control register data readout
13	3WIRE/I^2C	I	—	Selection of input between I^2C bus and 3-wire bus
15	AVccADREF	—	5V	Reference power supply for A/D converter
16, 94	AVccAD3	—	3.3V	Analog power supply for A/D converter
17	VRT	O	2.9V	Top reference voltage output for A/D converter
18, 92	DVccAD3	—	3.3V	Digital power supply for A/D converter
19, 32, 42, 54, 65, 76, 90	DVccADTTL	—	5V	TTL output power supply for A/D converter
20, 33, 44, 55, 67, 77, 89	DGNDADTTL	—	GND	TTL output GND for A/D converter
21, 22, 24 to 28, 31	RA0 to RA7	O	TTL	Data output for R-channel port A side
23, 30, 43, 50, 59, 66, 79, 86	DGNDAD3	—	GND	Digital GND for A/D converter
29, 80	AGNDAD3	—	GND	Analog GND for A/D converter
34 to 41	RB0 to RB7	O	TTL	Data output for R-channel port B side
45 to 49, 51 to 53	BA0 to BA7	O	TTL	Data output for B-channel port A side
56 to 58, 60 to 64	BB0 to BB7	O	TTL	Data output for B-channel port B side
68 to 75	GA0 to GA7	O	TTL	Data output for G-channel port A side
78, 81 to 85, 87, 88	GB0 to GB7	O	TTL	Data output for G-channel port B side
91	DVccAD	—	5V	Digital power supply for A/D converter
93	VRB	O	1.9V	Bottom reference voltage output for A/D converter
95	AGNDADREF	—	GND	Reference voltage GND for A/D converter

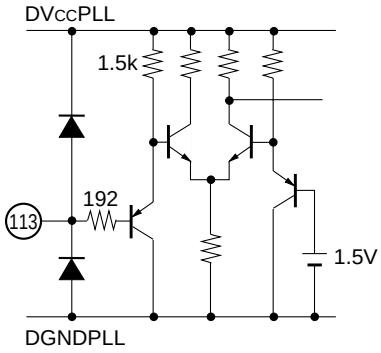
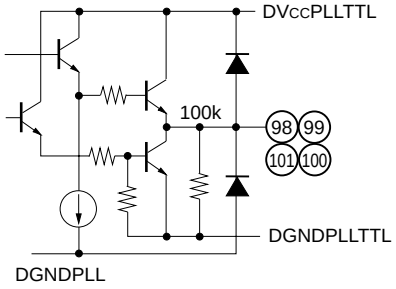
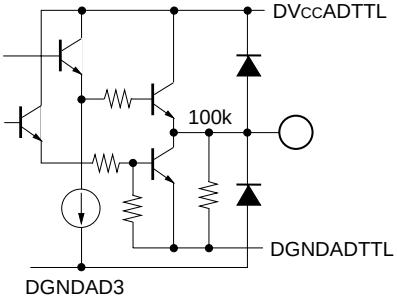
Pin No.	Symbol	I/O	Typical signal	Description
96	DVccPLLTTL	—	5V	TTL output power supply for PLL
97	DGNDPLLTTL	—	GND	TTL output GND for PLL
98	XCLK	O	TTL	Inverted CLK output
99	CLK	O	TTL	CLK output
100	1/2XCLK	O	TTL	Inverted 1/2CLK output
101	1/2CLK	O	TTL	1/2CLK output
103	DSYNC/ DIVOUT	O	TTL	DSYNC or DIVOUT signal output
104	UNLOCK	O	Open collector	Unlock signal output
105	SOGOUT	O	TTL	Output for SYNC ON GREEN
106	HOLD	I	TTL	Input for phase comparison disable signal
107	XTLOAD	I	TTL	Programmable counter reset setting
108	EVEN/ODD	I	TTL	Inverted pulse input of ADC sampling CLK
109	XCLKIN	I	PECL	Inverted CLK input for testing
110	CLKIN	I	PECL	CLK input for testing
111	SYNCIN1	I	TTL	Sync input 1
112	SYNCIN2	I	TTL	Sync input 2
113	CLPIN	I	TTL	Clamp pulse input
114	DVccPLL	—	5V	Digital power supply for PLL
115	DGNDPLL	—	GND	Digital GND for PLL
116	AVccVCO	—	5V	Analog power supply for PLL VCO
117	AGNDVCO	—	GND	Analog GND for PLL VCO
118	RC1	—	2.1V	External pin for PLL loop filter
119	RC2	—	2 to 4.5V	External pin for PLL loop filter
120	AVccIR	—	5V	Analog power supply for IREF
121	IREF	I	1.2V	Current setup
123	AGNDIR	—	GND	Analog GND for IREF
124	G/YIN1	I	—	G/Y signal input 1
125	AVccAMPG	—	5V	Power supply for G/Y amplifier block
126	G/YIN2	I	—	G/Y signal input 2
127	AGNDAMPG	—	GND	GND for G/Y amplifier block
128	G/YCLP	—	—	Clamp capacitor for brightness
129	B/CbCLP	—	—	Clamp capacitor for brightness
130	R/CrCLP	—	—	Clamp capacitor for brightness
132	SOGIN1	I	2.8V	SYNC ON GREEN signal input 1
133	B/CbIN1	I	—	B/Cb signal input 1

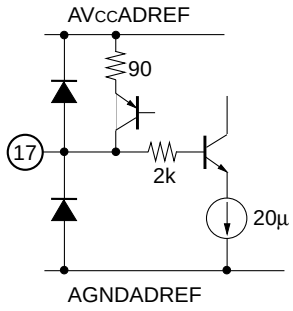
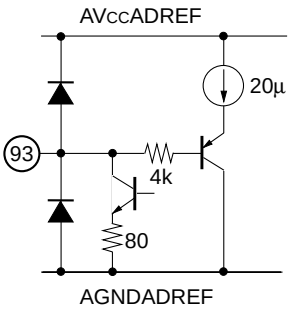
Pin No.	Symbol	I/O	Typical signal	Description
134	AV$_{CC}$AMPB	—	5V	Power supply for B/Cb amplifier block
135	SOGIN2	I	2.8V	SYNC ON GREEN signal input 2
136	B/CbIN2	I	—	B/Cb signal input 2
137	AGNDAMPB	—	GND	GND for B/Cb amplifier block
139	R/CrIN1	I	—	R/Cr signal input 1
140	AV$_{CC}$AMPR	—	5V	Power supply for R/Cr amplifier block
141	R/CrIN2	I	—	R/Cr signal input 2
142	AGNDAMPR	—	GND	GND for R/Cr amplifier block
143	G/YOUT	O	1.83V	Monitor pin for amplifier output signal
144	DAC TEST OUT	O	5V	DAC testing output for amplifier block control register
14, 102, 122, 131, 138	DPGND	—	GND	GND

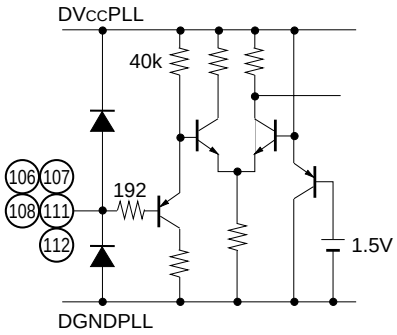
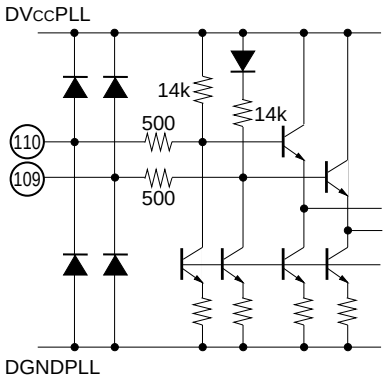
Pin Description and Pin Equivalent Circuit

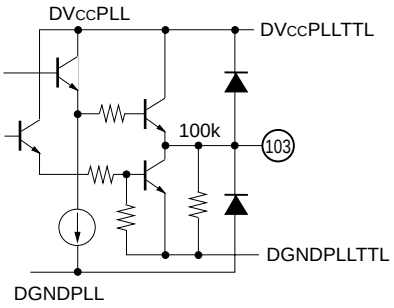
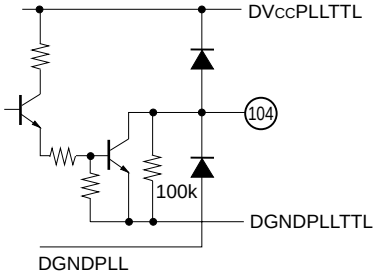
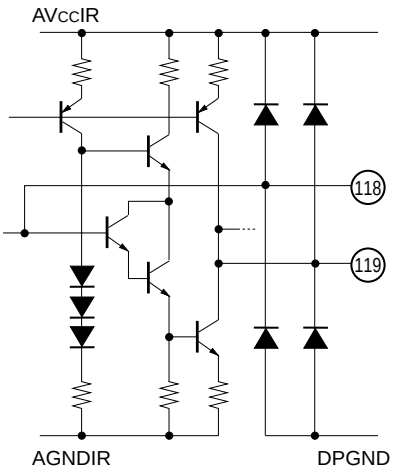
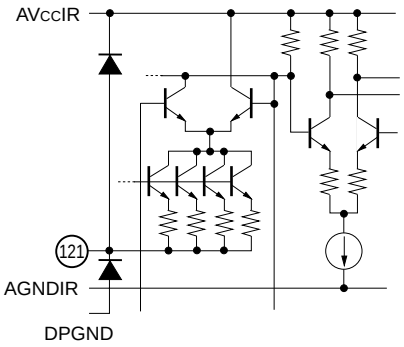
Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
3	R/CrOUT	O	1.83V		Amplifier output signal monitor. Each monitor can output either the entered signal immediately before A/D converter or the signal after switching between 2 types of input signals. The 2 types of input signals can be selected by the control register and output. These pins are emitter follower outputs, but the internal bias current is so small that a 820Ω resistor should be connected between these pins and GND to monitor high frequency signals. When not used, connect to AVCCAMP.
143	G/YOUT	O	1.83V		
1	B/CbOUT	O	1.83V		
140	AVCCAMPR	—	5V		Power supply for amplifier block.
125	AVCCAMPG	—	5V		
134	AVCCAMPB	—	5V		
142	AGNDAMPR	—	GND		GND for amplifier block.
127	AGNDAMPG	—	GND		
137	AGNDAMPB	—	GND		
105	SOGOUT	O	TTL		Sync separated SYNC signal output. Separates and outputs the SYNC signal from SYNC ON GREEN input signal. (SYNC signal input from SYNCIN1 and SYNCIN2 pins can be output.) Both positive and negative polarity outputs are supported. The polarity is selected by the control register.
132	SOGIN1	I	2.8V		SYNC ON GREEN signal inputs. Input via a 0.1µF capacitor. When not used, connect to AVCC. The SYNC TIP clamp level is approximately 2.0V + Vf (0.8V) = approximately 2.8V. At this time, if the pin voltage is lowered, these pins go to low impedance and current flows from the IC. When these pins are at the SYNC TIP level or higher, the clamp circuit is off and only an input base current of approximately 1.2µA flows.
135	SOGIN2	I	2.8V		

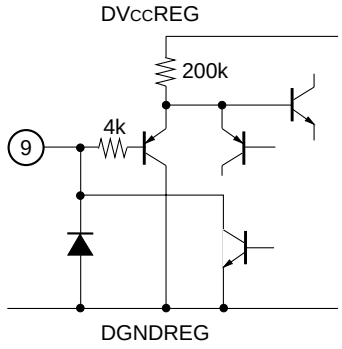
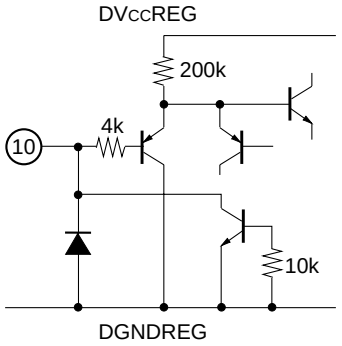
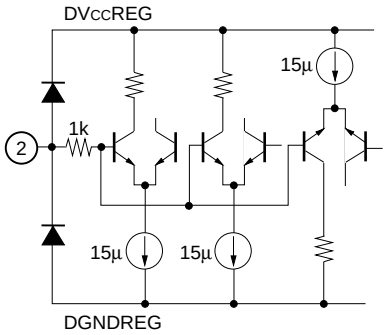
Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
Amplifier block					
139	R/CrIN1	I	*1		Analog input signal. Input via a 0.1µF ceramic capacitor. The typical signal level is 0.7V. Signals from 0.5V (min.) to 1.0V (max.) can be supported. IN1 and IN2 are selected by the control register. Leave these pins open when not used. RGB input and YCbCr input can be selected by the control register. *1 The clamp level typical values are as follows. In case RGB is input 2.2V + Vf (0.8V) = approximately 3V In case YCbCr is input G/YIN: 2.2V + Vf (0.8V) = approximately 3V R/CrIN, B/CbIN: 2.7V + Vf (0.8V) = approximately 3.5V Clamp period: A clamp current of ±1.2mA (max.) flows. Signal period: A base current of 0.5µA flows to the IC.
141	R/CrIN2	I	*1		
124	G/YIN1	I	*1		
126	G/YIN2	I	*1		
133	B/CbIN1	I	*1		
136	B/CbIN2	I	*1		
130	R/CrCLP	—	*2		Clamp capacitor connector for brightness. Connect 0.1µF ceramic capacitors between these pins and GND. *2 Typical levels of the clamp are as follows. In case RGB is input SUB BRIGHTNESS 00H: 2.68V 80H: 2.81V FFH: 2.94V In case YCbCr is input G/YCLP is the same as above. R/Cr, B/CbCLP are as follows. CbCr Offset 00H: 3.04V 20H: 3.07V 3FH: 3.102V Clamp period: A clamp current of ±1.2mA (max.) flows. Signal period: A base current of 0.5µA flows to the IC.
128	G/YCLP	—	*2		
129	B/CbCLP	—	*2		

Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
113	CLPIN	I	TTL		Clamp pulse input for the signal of analog input clamp and brightness clamp. Both positive and negative polarity inputs are supported. The polarity is selected by the control register. The input pulse width should be 200ns or more.
A/D converter block					
99	CLK	O	TTL		CLK output. Output the same frequency CLK as that of ADC sampling. These are complemental TTL levels. These pins can be independently controlled on and off (power save) by the control register.
98	XCLK	O	TTL		
101	1/2CLK	O	TTL		1/2CLK output. Output a half frequency CLK of that of ADC sampling. These are complemental TTL levels. These pins can be independently controlled on and off (power save) by the control register.
100	1/2XCLK	O	TTL		
21, 22, 24 to 28, 31	RA0 to RA7	O	TTL		Data output for R-channel port A side.
34 to 41	RB0 to RB7	O	TTL		Data output for R-channel port B side.
68 to 75	GA0 to GA7	O	TTL		Data output for G-channel port A side.
78, 81 to 85, 87, 88	GB0 to GB7	O	TTL		Data output for G-channel port B side.
45 to 49, 51 to 53	BA0 to BA7	O	TTL		Data output for B-channel port A side.
56 to 58, 60 to 64	BB0 to BB7	O	TTL		Data output for B-channel port B side.
15	AVccADREF	—	5V		Reference power supply for A/D converter.
95	AGNDADREF	—	GND		Reference GND for A/D converter.
16, 94	AVccAD3	—	3.3V		Analog power supply for A/D converter.
29, 80	AGNDAD3	—	GND		Analog GND for A/D converter.
18, 92	DVccAD3	—	3.3V		Digital power supply for A/D converter.
91	DVccAD	—	5V		Digital power supply for A/D converter.

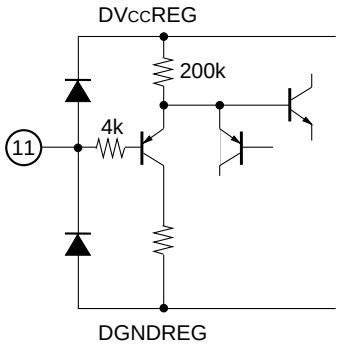
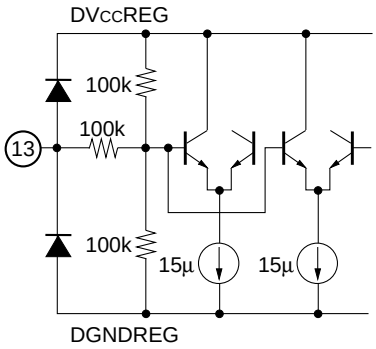
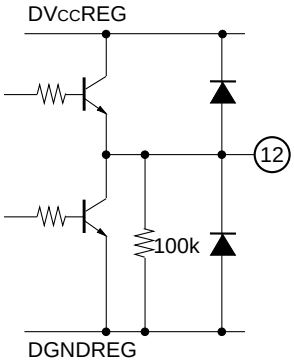
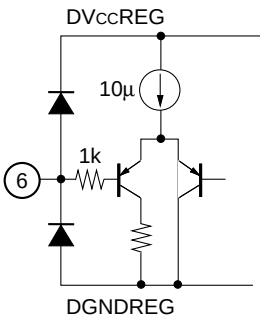
Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
23, 30, 43, 50, 59, 66, 79, 86	DGNDAD3	—	GND		Digital GND for A/D converter.
19, 32, 42, 54, 65, 76, 90	DVccADTTL	—	5V		TTL output power supply for A/D converter.
20, 33, 44, 55, 67, 77, 89	DGNDADTTL	—	GND		TTL output GND for A/D converter.
17	VRT	O	2.9V		Top reference voltage output for A/D converter input dynamic range. Connect to AVccAD3 via a 1µF ceramic capacitor.
93	VRB	O	1.9V		Bottom reference voltage output for A/D converter input dynamic range. Connect to AVccAD3 via a 1µF ceramic capacitor.

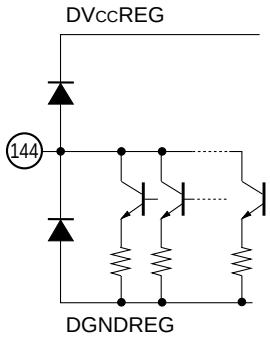
Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
PLL block					
111	SYNCIN1	I	TTL		Input SYNC signal at TTL level. The input polarity is switched by the control register. Leave this pin open when not used.
112	SYNCIN2	I	TTL		Input SYNC signal at TTL level. The input polarity is switched by the control register. Leave this pin open when not used.
106	HOLD	I	TTL		Input signal for phase comparison HOLD. Phase comparison is stopped, and VCO oscillation frequency is held. When not be hold, fix the pin as follows. When HOLDPOL register is "1", fix this pin to low level. When HOLDPOL register is "0", leave this pin open or fix to high level.
108	EVEN/ODD	I	TTL		Input the signal used to invert the A/D converter sampling CLK. Low: EVEN mode High: ODD mode Normally fix it to low level.
107	XTLOAD	I	TTL		Programmable counter reset. Normally fix it to high level or leave open. In programmable counter test mode, set it to low level to call up the register contents. When not used, leave this pin open or fix to high level.
110	CLKIN	I	PECL		CLK input for ADC operation check. Input PECL level signal complementally. When using this pin, set CLK to external input by the control register. Leave this pin open when not used.
109	XCLKIN	I	PECL		

Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
103	DSYNC/ DIVOUT	O	TTL		This pin can output either DSYNC signal or DIVOUT signal. It can be selected by the control register. In addition, the output polarity can be selected by the control register.
104	UNLOCK	—	—		UNLOCK signal output. Make a discrimination between lock and unlock in the analog manner by connecting the external circuit. Leave this pin open when not used. Do not connect this pin to neither power supply nor GND.
118	RC1	—	2.1V		External pin for PLL loop filter.
119	RC2	—	2 to 4.5V		External pin for PLL loop filter.
121	IREF	I	1.2V		Connect an external resistor (3kΩ) to supply a stabilized current to the inside of the IC. (charge pump current, etc.) Connect this pin to GND via 0.1µF ceramic capacitor connected as close to the pin as possible. The band gap voltage is output.
114	DVccPLL	—	5V		Digital power supply for PLL.
115	DGNDPLL	—	GND		Digital GND for PLL.
96	DVccPLLTTL	—	5V		TTL output power supply for PLL.

Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
97	DGNDPLLTTL	—	GND		TTL output GND for PLL.
120	AVccIR	—	5V		Analog power supply for IREF.
123	AGNDIR	—	GND		Analog GND for IREF.
116	AVccVCO	—	5V		Analog power supply for PLL VCO.
117	AGNDVCO	—	GND		Analog GND for PLL VCO.
Control register block					
9	SDA	I	—		Input control register data. Switching between the I^2C and 3-wire bus mode is performed by the 3WIRE/I^2C pin.
10	SCL	I	—		Input control register CLK. Switching between the I^2C and 3-wire bus mode is performed by the 3WIRE/I^2C pin.
2	ADD	I	—		Set slave address when using I^2C bus mode. Slave address: 1 0 0 1 1 S2 S1 0 Connect this pin to GND during 3-wire bus mode.

	S2	S1
Vcc to 3/4Vcc	0	1
3/4Vcc to 2/4Vcc	1	1
2/4Vcc to 1/4Vcc	1	0
1/4Vcc to GND	0	0

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Typical signal</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>11</td><td>XSENABLE</td><td>I</td><td>TTL</td><td> 
</td><td>Inputs enable signal for 3-wire bus.
High level: Control disabled
Low level: Control enabled
Connect this pin to GND when using I²C.</td></tr>
<tr><td>13</td><td>3WIRE/I²C</td><td>I</td><td>—</td><td> 
</td><td>Selection of input between I²C bus and 3-wire bus.
<table><tr><td>Vcc to 2/3Vcc</td><td>3-wire bus mode</td></tr><tr><td>2/3Vcc to 1/3Vcc</td><td>I²C 3V mode</td></tr><tr><td>1/3Vcc to GND</td><td>I²C 5V mode</td></tr></table></td></tr>
<tr><td>12</td><td>SEROUT</td><td>O</td><td>TTL</td><td> 
</td><td>When using the read mode of 3-wire bus mode, the register information written once is output in series order from the LSB of the setting sub address data.</td></tr>
<tr><td>7</td><td>DGNDREG</td><td>—</td><td>GND</td><td></td><td>GND for register.</td></tr>
<tr><td>8</td><td>DVccREG</td><td>—</td><td>5V</td><td></td><td>Power supply for register.</td></tr>
<tr><td>6</td><td>XPOWER SAVE</td><td>I</td><td>TTL</td><td> 
</td><td>Power save for all functions including the control register block.
High level: Normal operation
Low level: Power save</td></tr>
</table>

Pin No.	Symbol	I/O	Typical signal	Equivalent circuit	Description
144	DAC TEST OUT	O	5V		DAC test output for control register of amplifier block. Current is output by open collector. Normally connect to AVcc.
14, 102, 122, 131, 138	DPGND	—	GND		This pin is connected to the die pad. Connect to the specified GND in Application Circuit.
4	NC	—	—		Not used. Leave this pin open or connect to GND.
5	NC	—	—		Not used. Leave this pin open or connect to GND.

Electrical Characteristics (Ta = 25°C, AVcc, DVcc = 5V, AVcc3, DVcc3 = 3.3V)

Supply Current

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current during operating						
5V current consumption	$I_{CC}5$	CLK = DC	—	180	240	mA
3.3V current consumption	$I_{CC}3$	CLK = DC	—	180	226	mA
Register control power save current						
5V power save current consumption	$I_{CC}5PS$		—	26	42	mA
3.3V power save current consumption	$I_{CC}3PS$		—	3.0	7.2	mA
XPOWER SAVE pin control power save current						
5V power save current consumption	$I_{CC}5XPS$		—	9.0	22	mA
3.3V power save current consumption	$I_{CC}3XPS$		—	3.0	7.2	mA

Register

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
3-wire control bus (SDA, SCL, SENABLE)						
High level input voltage	V_{IH}		2.0	—	5.0	V
Low level input voltage	V_{IL}		0	—	0.8	V
High level input current	I_{IH}		–2.0	—	0	µA
Low level input current	I_{IL}		–5.0	—	0	µA
Threshold voltage High → Low	V_{THHL1}		—	1.3	—	V
Threshold voltage Low → High	V_{THLH1}		—	1.65	—	V
Input capacitance	C_I		—	—	10	pF
SCL clock frequency	F_{SCL1}	in WRITE/READ mode	—	—	10	MHz
XSENABLE setup time	T_{ENS}	in WRITE/READ mode	3	10	—	ns
XSENABLE hold time	T_{ENH}	in WRITE/READ mode	0	10	—	ns
XSENABLE high level pulse width	T_{ENPW}	in WRITE/READ mode	300	—	—	ns
SDA setup time	T_{DS}	in WRITE/READ mode	3	10	—	ns
SDA hold time	T_{DH}	in WRITE/READ mode	0	10	—	ns
SDA delay time	T_D	in READ mode	—	11	—	ns

Register (Cont.)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
I²C control bus (SDA, SCL)							
I²C (High) mode	High level input voltage	V_{IH}		2.3	—	5.0	V
	Low level input voltage	V_{IL}		0	—	1.0	V
	High level input current	I_{IH}		–2.0	—	0	µA
	Low level input current	I_{IL}		–5.0	—	0	µA
	Threshold voltage High → Low	V_{THHL2}		—	1.6	—	V
	Threshold voltage Low → High	V_{THLH2}		—	1.95	—	V
I²C (Low) mode	High level input voltage	V_{IH}		2.0	—	5.0	V
	Low level input voltage	V_{IL}		0	—	0.8	V
	High level input current	I_{IH}		–1.0	—	0	µA
	Low level input current	I_{IL}		–5.0	—	0	µA
	Threshold voltage High → Low	V_{THHL3}		—	1.3	—	V
	Threshold voltage Low → High	V_{THLH3}		—	1.65	—	V
SDA low level output voltage		V_{OL}	I_{OH} = 3mA	0	0.15	0.5	V
Input capacitance		C_I		—	—	10	pF
SCL clock frequency		F_{SCL2}		0	50	100	kHz
Bus free-time STOP → START		T_{BUF}		4.7	5.0	—	µs
Hold time (resend)		$T_{HD;STA}$	START condition: After this period, first clock is generated.	4.0	5.0	—	µs
Hold time in SCL clock at Low state		T_{LOW}		4.7	5.0	—	µs
Hold time in SCL clock at High state		T_{HIGH}		4.0	5.0	—	µs
Setup time under resend START condition		$T_{SU;STA}$		4.7	5.0	—	µs
Data hold time		$T_{HD;DAT}$		0	5.0	—	µs
Data setup time		$T_{SU;DAT}$		250	5000	—	ns
Rise time		T_R		—	—	1000	ns
Fall time		T_F		—	—	300	ns
Setup time under STOP condition		$T_{SU;STO}$		4.0	5.0	—	µs
Capacitive load of each bus line		Cb		—	—	400	pF

AMP

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Brightness characteristics						
Brightness level H (ADC OUT)	V_{BRHAD}	Sub Brightness G, B, R = 255 ADC output conversion level	53	61	69	LSB
Brightness level L	V_{BRL}	Sub Brightness G, B, R = 0 G, B, R OUT pin voltage	1.388	1.588	1.788	V
Brightness level M	V_{BRM}	Sub Brightness G, B, R = 128 G, B, R OUT pin voltage	1.63	1.83	2.03	V
Brightness level H	V_{BRH}	Sub Brightness G, B, R = 255 G, B, R OUT pin voltage	1.86	2.06	2.26	V
Brightness level Low side variable range		$V_{BRL} – V_{BRM}$	—	–242	—	mV
Brightness level High side variable range		$V_{BRH} – V_{BRM}$	—	230	—	mV
Clamp characteristics						
Cb, Cr clamp level M (ADC OUT)	V_{CLMAD}	Cb, Cr offset = 32 ADC output conversion level	120	128	136	LSB
Cb, Cr clamp level L	V_{CLL}	Cb, Cr offset = 0 B, R OUT pin voltage	1.94	2.23	2.46	V
Cb, Cr clamp level M	V_{CLM}	Cb, Cr offset = 32 B, R OUT pin voltage	1.99	2.28	2.51	V
Cb, Cr clamp level H	V_{CLH}	Cb, Cr offset = 63 B, R OUT pin voltage	2.03	2.34	2.58	V
Cb, Cr clamp level Low side variable range		$V_{CLL} – V_{CLM}$	—	–60	—	mV
Cb, Cr clamp level High side variable range		$V_{CLH} – V_{CLM}$	—	60	—	mV
Clamp pulse minimum width	T_{WCLP}		200	—	—	ns
Contrast characteristics						
Main contrast control L	V_{MCL}	Main Contrast = 0 Sub Contrast = 128 Vin = 1.2Vp-p RGB/YUV mode, G, B, R OUT	0.62	0.78	0.94	times
Main contrast control M	V_{MCM}	Main Contrast = 128 Sub Contrast = 128 Vin = 0.6Vp-p RGB/YUV mode, G, B, R OUT	1.23	1.53	1.84	times
Main contrast control H	V_{MCH}	Main Contrast = 255 Sub Contrast = 128 Vin = 0.45Vp-p RGB/YUV mode, G, B, R OUT	1.79	2.24	2.69	times
Sub contrast control L	V_{SCL}	Main Contrast = 128 Sub Contrast = 0 Vin = 0.85Vp-p RGB/YUV mode, G, B, R OUT	0.96	1.2	1.44	times

AMP (Cont.)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Sub contrast control H	V_{SCH}	Main Contrast = 128 Sub Contrast = 255 Vin = 0.55Vp-p RGB/YUV mode, G, B, R OUT	1.48	1.85	2.22	times
Gain difference among RGB	ΔGain	Main Contrast = 128 Sub Contrast = 128 Vin = 0.6Vp-p RGB/YUV mode, G, B, R OUT	–8	0	8	%
Frequency response	FC – 3dB	Main Contrast = 128 Sub Contrast = 128 Vin = 0.6Vp-p RGB/YUV mode, G, B, R OUT	—	220	—	MHz
Cross talk characteristics						
Cross talk between channels	CTC	Main Contrast = 128 Sub Contrast = 128 fin = 100MHz, Vin = 0.6Vp-p	—	–35	—	dB
Cross talk among RGB	CTB	Main Contrast = 128 Sub Contrast = 128 fin = 100MHz, Vin = 0.6Vp-p	—	–30	—	dB

SYNCSEP

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
SYNC SEP input characteristics						
SYNC TIP input minimum amplitude	V_{SYN}		0.2	—	—	Vp-p
SYNC TIP input minimum duty	D_{SYN}		5	—	—	%
SYNC SEP threshold voltage	V_{TH}	SYNC SEP V_{TH} = 1000 SYNC SEP V_{HYS} = 10	116	145	174	mV
SYNC SEP hysteresis voltage	V_{HYS}	SYNC SEP V_{TH} = 1000 SYNC SEP V_{HYS} = 10	36	45	54	mV

PLL

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Hold characteristics						
RC1 pin leak current	Ileak		—	—	1.0	nA
SYNC signal input characteristics						
SYNC signal input frequency range	F_{SYNC}		10	—	100	kHz
VCO characteristics						
Clock frequency	FCLK1	VCO frequency divider DIV = 1/1	80	—	120	MHz
Clock frequency	FCLK2	VCO frequency divider DIV = 1/2	40	—	80	MHz
Clock frequency	FCLK3	VCO frequency divider DIV = 1/4	14	—	40	MHz
Clock frequency	FCLK4	VCO frequency divider DIV = 1/8	5	—	14	MHz
VCO lock range	Vlock		2.0	—	4.5	V
VCO gain 1	KVCO1	VCO frequency divider DIV = 1/1	300	—	500	Mrad/sv
VCO gain 2	KVCO2	VCO frequency divider DIV = 1/2	150	—	250	Mrad/sv
VCO gain 3	KVCO3	VCO frequency divider DIV = 1/4	75	—	125	Mrad/sv
VCO gain 4	KVCO4	VCO frequency divider DIV = 1/8	37.5	—	62.5	Mrad/sv
Jitter characteristics						
SYNC input signal – Clock output jitter (NTSC)	Tj1p-p	Triggered at SYNC Fsync = 15.73kHz Fclk = 12.27MHz N = 780	2.4	2.7	3	ns
SYNC input signal – Clock output jitter (VGA)	Tj2p-p	Triggered at SYNC Fsync = 31.47kHz Fclk = 25.18MHz N = 800	1.6	1.8	2.0	ns
SYNC input signal – Clock output jitter (SVGA)	Tj3p-p	Triggered at SYNC Fsync = 48.08kHz Fclk = 50.00MHz N = 1040	1.3	1.4	1.5	ns
SYNC input signal – Clock output jitter (XGA)	Tj4p-p	Triggered at SYNC Fsync = 56.48kHz Fclk = 75.00MHz N = 1328	0.9	1.0	1.1	ns
Delay sync – Clock output jitter	Tj7p-p	Triggered at DSYNC	—	—	0.1	ns

ADC

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution			—	8	—	bit
DC characteristics						
Integral linearity error	ILE		—	1.0	—	LSB
Differential linearity error	DLE		—	0.4	0.7	LSB
Reference voltage						
Top reference voltage	VRT	AVccAD3 as a reference	–0.3	–0.4	–0.6	V
Bottom reference voltage	VRB	AVccAD3 as a reference	–1.3	–1.4	–1.6	V
Input dynamic range	VTB	VRT – VRB	0.9	1.0	1.1	V
AC characteristics						
Maximum conversion frequency of Straight Data out Mode	Fc		100	—	—	MSPS
Maximum conversion frequency of DMUX Parallel Data out Mode	Fc		120	—	—	MSPS
Maximum conversion frequency of DMUX Interleaved Data out Mode	Fc		120	—	—	MSPS
Maximum conversion frequency of 4:2:2 Data out D2 Mode	Fc		100	—	—	MSPS
Maximum conversion frequency of 4:2:2 Data out Special Mode	Fc		100	—	—	MSPS

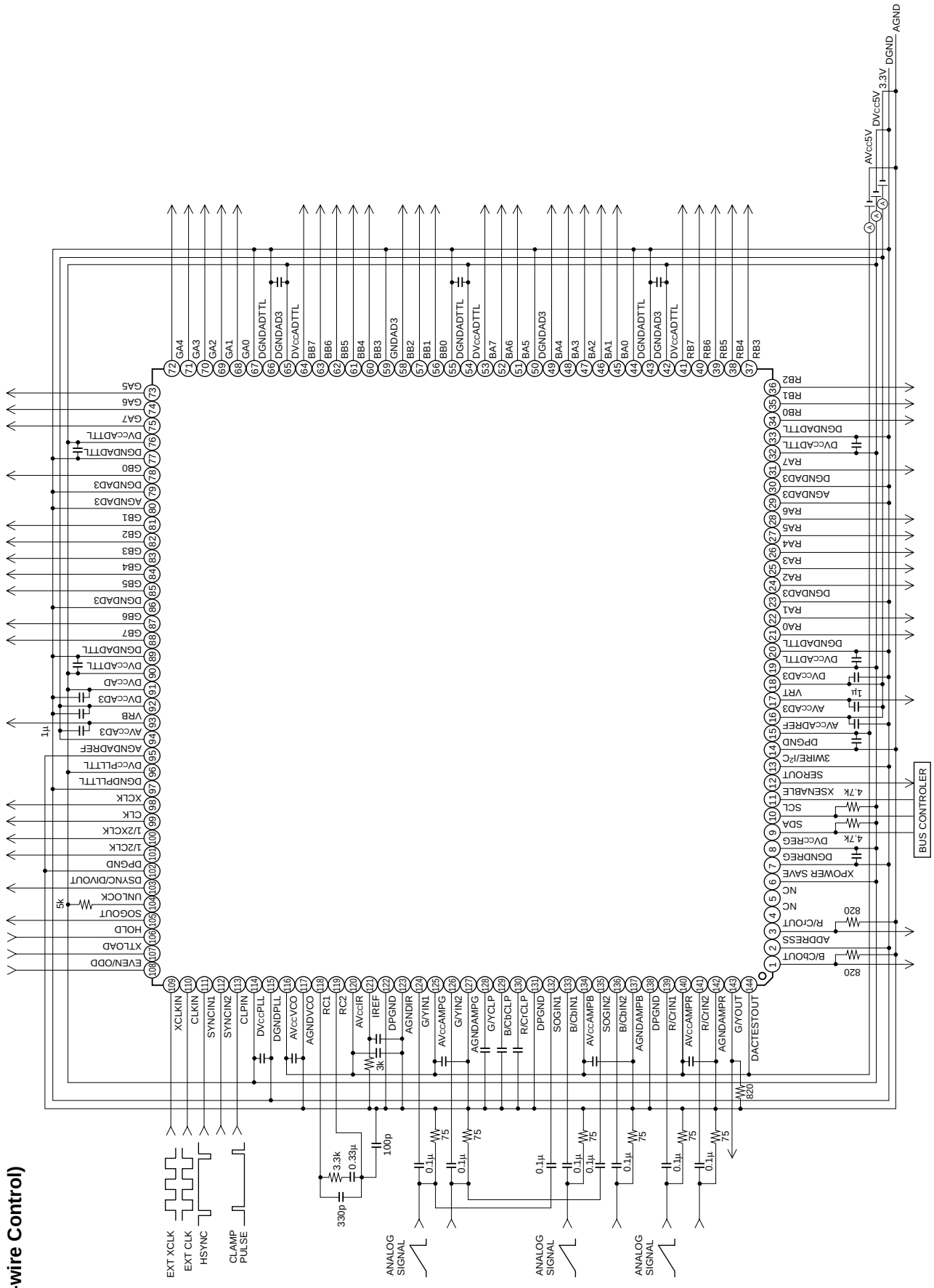
I/O

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Digital input (PECL)						
Digital input voltage: H	V_{IH1}	DVccPLL as a reference	–1.15	—	—	V
Digital input voltage: L	V_{IL1}	DVccPLL as a reference	—	—	–1.5	V
Digital input current: H	I_{IH1}	V_{IH1} = DV$_{CC}$PLL – 0.8V	–100	—	100	µA
Digital input current: L	I_{IL1}	V_{IL1} = DV$_{CC}$PLL – 1.6V	–200	—	0	µA
Digital input (TTL)						
Digital input voltage: H	V_{IH2}		2.0	—	—	V
Digital input voltage: L	V_{IL2}		—	—	0.8	V
Threshold voltage	V_{TH}		—	1.5	—	V
Digital input current: H	I_{IH2}	V_{IH} = 3.5V	–10	—	–5	µA
Digital input current: L	I_{IL2}	V_{IL} = 0.2V	–20	—	0	µA
Digital output (TTL)						
Digital output voltage: H	V_{OH1}	I_{OH} = –2mA	2.4	2.95	3.3	V
	V_{OH2}	I_{OH} = –2mA	2.3	2.7	3.0	V
	V_{OH3}	I_{OH} = –2mA	2.05	2.45	2.75	V
	V_{OH4}	I_{OH} = –2mA	1.85	2.2	2.5	V
Digital output voltage: L	V_{OL}	I_{OL} = 1mA	—	0.2	0.5	V

Timing Characteristics

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Clock output rise time	T_{R_CLK}	0.8 to 2.0V (CLK, 1/2CLK)	0.8	1.4	2.3	ns
Clock output fall time	T_{F_CLK}	2.0 to 0.8V (CLK, 1/2CLK)	1.0	1.5	2.8	ns
Delay sync output rise time	T_{R_DSYNC}	0.8 to 2.0V (DSYNC, DIVOUT, SOGOUT)	0.8	1.4	2.3	ns
Delay sync output fall time	T_{F_DSYNC}	2.0 to 0.8V (DSYNC, DIVOUT, SOGOUT)	1.0	1.5	2.8	ns
Data output rise time	T_{R_DATA}	0.8 to 2.0V	0.9	1.2	2.0	ns
Data output fall time	T_{F_DATA}	2.0 to 0.8V	0.9	1.2	2.0	ns
HOLD signal setup time	Ths		20	—	—	ns
HOLD signal hold time	Thh		20	—	—	ns
Delay sync delay time coarse delay	Td_1		3	—	6	CLK
Delay sync delay time fine delay	Td_2		1/32	—	64/32	CLK
Clock output delay from SYNC input signal	Td_3	CL = 9pF	6.0	7.0	8.0	ns
Delay time between clock output and DSYNC/DIVOUT signal	Td_4	CL = 9pF	0.8	1.0	1.3	ns
DIVOUT signal output delay time	Td_5	Difference between delay sync signal and DIVOUT signal	4	—	5	CLK
Clock – 1/2 clock	Td_6		0.9	1.2	1.6	ns
1/2 clock – Data	Td_7		2.3	2.6	3.2	ns
Clock – Data	Td_8		2.2	2.8	3.8	ns

Electrical Characteristics Measurement Circuit
(3-wire Control)



Control Register Functions Table

Block	Function	bit	Register Name	Control Range (typ.)	Register No.	Data							
						D7	D6	D5	D4	D3	D2	D1	D0
PLL	Feedback programmable counter control	12	VCO DIV	Frequency division ratio = (m + 1) × 8 + n	0	m4	m3	m2	m1	m0	n2	n1	n0
					1					m8	m7	m6	m5
PLL	VCO frequency divider control	2	DIV1, 2, 4, 8	00: 1/1 01: 1/2 10: 1/4 11: 1/8	1			O	O				
PLL	Delay control (lower order)	6	FINE DELAY	000000: 1/32CLK 111111: 64/32CLK	2			O	O	O	O	O	O
PLL	Delay control (higher order)	2	COARSE DELAY	00: 3CLK 01: 4CLK 10: 5CLK 11: 6CLK	2	O	O						
PLL	Charge pump current control	3	Charge.Pump	000: 100µA 001: 200µA 010: 300µA 011: 400µA 100: 500µA 101: 600µA 110: 700µA 111: 800µA	3						O	O	O
PLL	DIVOUT signal pulse width control	2	DIVOUT WIDTH	00: 1CLK 01: 2CLK 10: 4CLK 11: 8CLK	3				O	O			
PLL	DIVOUT signal delay control	1	DIVOUT DELAY	0: 4CLK 1: 5CLK	3			O					
PLL	Delay sync output polarity control	1	DSYNC POL	0: NEGATIVE 1: POSITIVE	4								O
PLL	Hold input polarity control	1	HOLD POL	0: NEGATIVE 1: POSITIVE	4							O	

Block	Function	bit	Register Name	Control Range (typ.)	Register No.	Data							
						D7	D6	D5	D4	D3	D2	D1	D0
PLL	Phase comparison input positive/negative control	1	PD POL	0: NEGATIVE 1: POSITIVE	4						O		
PLL	Sync input polarity control	1	SYNC POL	0: NEGATIVE 1: POSITIVE	4					O			
PLL	SOG OUT polarity control	1	SOG OUT POL	0: NEGATIVE 1: POSITIVE	4				O				
PLL	Clamp pulse input polarity control	1	CLP POL	0: NEGATIVE 1: POSITIVE	4			O					
PLL	External clock/internal VCO switching	1	VCO By-pass	0: EXT CLK 1: INT VCO	5								O
PLL	Delay sync output/DIVOUT switching	1	DSYNC By-pass	0: DIVOUT 1: DSYNC	5							O	
PLL	Delay sync hold function	1	DSYNC Hold	0: NORMAL 1: HOLD	5						O		
PLL	Output SOG/HSYNC switching	1	SYNC OUT SW	0: SYNCT 1: SYNCP/HSYNC	5					O			
PLL	HSYNC1, 2 input/SOGA switching	1	SYNCP/ HSYNC	0: SYNCP 1: HSYNC1, 2	5				O				
PLL	HSYNC1 input/HSYNC2 input switching	1	HSYNC 1/2	0: EXT SYNC1 1: EXT SYNC2	5			O					
PLL	TTL output off function (clock)	1	CLK Enable	0: TTL out OFF 1: TTL out ON	6								O
PLL	TTL output off function (inverse clock)	1	XCLK Enable	0: TTL out OFF 1: TTL out ON	6							O	
PLL	TTL output off function (1/2 clock)	1	1/2CLK Enable	0: TTL out OFF 1: TTL out ON	6						O		
PLL	TTL output off function (inverse 1/2 clock)	1	1/2XCLK Enable	0: TTL out OFF 1: TTL out ON	6					O			
PLL	TTL output off function (delay sync)	1	DSYNC Enable	0: TTL out OFF 1: TTL out ON	6				O				

Block	Function	bit	Register Name	Control Range (typ.)	Register No.	Data							
						D7	D6	D5	D4	D3	D2	D1	D0
PLL	TTL output off function (UNLOCK)	1	UNLOCK Enable	0: TTL out OFF 1: TTL out ON	6			O					
PLL	TTL output off function (SOG OUT)	1	SOG Enable	0: TTL out OFF 1: TTL out ON	6		O						
REGISTER	TTL output off function (SER OUT)	1	SEROUT Enable	0: TTL out OFF 1: TTL out ON	6	O							
AMP	Main contrast	8	MAIN CONTRAST	00000000: Mgain = × 0.78 11111111: Mgain = × 2.24	7	O	O	O	O	O	O	O	O
AMP	Sub contrast Gch	8	SUB CONTRAST G	00000000: Mgain = × 0.79 11111111: Mgain = 1.21	8	O	O	O	O	O	O	O	O
AMP	Sub contrast Bch	8	SUB CONTRAST B	00000000: Mgain = × 0.79 11111111: Mgain = 1.21	9	O	O	O	O	O	O	O	O
AMP	Sub contrast Rch	8	SUB CONTRAST R	00000000: Mgain = × 0.79 11111111: Mgain = 1.21	10	O	O	O	O	O	O	O	O
AMP	Sub brightness Gch	8	SUB BRIGHTNESS G	00000000: VRB – 61LSB 11111111: VRB + 61LSB	11	O	O	O	O	O	O	O	O
AMP	Sub brightness Bch	8	SUB BRIGHTNESS B	00000000: VRB – 61LSB 11111111: VRB + 61LSB	12	O	O	O	O	O	O	O	O
AMP	Sub brightness Rch	8	SUB BRIGHTNESS R	00000000: VRB – 61LSB 11111111: VRB + 61LSB	13	O	O	O	O	O	O	O	O
AMP	Cb input clamp level adjustment in YUV mode	6	Cb Offset	00000000: 128LSB – 16LSB 11111111: 128LSB + 16LSB	14			O	O	O	O	O	O
AMP	Cr input clamp level adjustment in YUV mode	6	Cr Offset	00000000: 128LSB – 16LSB 11111111: 128LSB + 16LSB	15			O	O	O	O	O	O
AMP	YCbCr input mode clamp level switching	1	YCbCr mode	0: RGB IN 1: YCbCr IN	16								O
AMP	RGB OUT output signal selection SW output and AMP output	1	RGB Out Select	0: AMP OUT 1: SW OUT	16							O	
AMP	RGB2 input selection	1	RGB In Select	0: IN1 1: IN2	16						O		

Block	Function	bit	Register Name	Control Range (typ.)	Register No.	Data							
						D7	D6	D5	D4	D3	D2	D1	D0
AMP	Brightness clamp off	1	Brightness CLP	0: ON 1: OFF	16					O			
SYNC SEP	SYNC SEP hysteresis level setting during SYNC ON GREEN	2	SYNC SEP V_{HYS}	00: 2mV 01: 20mV 10: 45mV 11: 70mV	17							O	O
SYNC SEP	SYNC SEP threshold level setting during SYNC ON GREEN	4	SYNC SEP V_{TH}	0000: 75mV 10mV step 1111: 215mV	17			O	O	O	O		
ADC	ADC DATA output polarity control	1	DATA OUT POL	0: all 1 → all 0(NEGATIVE) 1: all 0 → all 1(POSITIVE)	18								O
ADC	DATA output mode switching	3	DATA OUT MODE	000: Straight 001: DMUX Parallel 010: DMUX Interleaved 011: YUV4:2:2 D2 111: YUV4:2:2 Special	18					O	O	O	
ADC	ADC power save	1	ADC Power Save	0: active 1: power save	19								O
AMP	AMP power save	1	AMP Power Save	0: active 1: power save	19							O	
PLL	PLL power save	1	PLL Power Save	0: active 1: power save	19						O		
SYNC SEP	SYNC SEP power save	1	SYNC SEP Power Save	0: active 1: power save	19					O			
TTLOUT	TTLOUT CLP LEVEL	2	TTLOUT CLP	00: 2.20V 01: 2.45V 10: 2.70V 11: 2.95V	19			O	O				

Register Assignment

	Register No.	Register Name	Data								Sub Address					
			D7	D6	D5	D4	D3	D2	D1	D0	HEX code	A4	A3	A2	A1	A0	HEX code
PLL	Register 0	VCODIV1	VCODIV Bit7	VCODIV Bit6	VCODIV Bit5	VCODIV Bit4	VCODIV Bit3	VCODIV Bit2	VCODIV Bit1	VCODIV Bit0	38 (H)	0	0	0	0	0	00 (H)
		Reference	0	0	1	1	1	0	0	0							
	Register 1	VCODIV2			DIV1, 2, 4, 8 Bit1	DIV1, 2, 4, 8 Bit0	VCODIV Bit11	VCODIV Bit10	VCODIV Bit9	VCODIV Bit8	15 (H)	0	0	0	0	1	01 (H)
		Reference			0	1	0	1	0	1							
	Register 2	DELAY	Coarse Delay Bit1	Coarse Delay Bit0	Fine Delay Bit5	Fine Delay Bit4	Fine Delay Bit3	Fine Delay Bit2	Fine Delay Bit1	Fine Delay Bit0	20 (H)	0	0	0	1	0	02 (H)
		Reference	0	0	1	0	0	0	0	0							
	Register 3	CP			DIVOUT DELAY	DIVOUT Width Bit1	DIVOUT Width Bit0	Charge Pump Bit2	Charge Pump Bit1	Charge Pump Bit0	23 (H)	0	0	0	1	1	03 (H)
		Reference			1	0	0	0	1	1							
	Register 4	POLARITY			CLP POL	SOGOUT POL	SYNC IN POL	PD POL	HOLD POL	DSYNC POL	3F (H)	0	0	1	0	0	04 (H)
		Reference			1	1	1	1	1	1							
	Register 5	SYNC			HSYNC1/2	SYNCP/ HSYNC IN	SYNC OUT SW	DSYNC Hold	DSYNC By-pass	VCO By-pass	1B (H)	0	0	1	0	1	05 (H)
		Reference			0	1	1	0	1	1							
	Register 6	TTLOUT ENABLE	SEROUT Enable	SOG Enable	UNLOCK Enable	DSYNC Enable	1/2XCLK Enable	1/2CLK Enable	XCLK Enable	CLK Enable	FF (H)	0	0	1	1	0	06 (H)
		Reference	1	1	1	1	1	1	1	1							
AMP	Register 7	MAIN CONTRAST	Main Contrast Bit7	Main Contrast Bit6	Main Contrast Bit5	Main Contrast Bit4	Main Contrast Bit3	Main Contrast Bit2	Main Contrast Bit1	Main Contrast Bit0	80 (H)	0	0	1	1	1	07 (H)
		Reference	1	0	0	0	0	0	0	0							
	Register 8	SUB CONTRAST G	Sub Contrast G Bit7	Sub Contrast G Bit6	Sub Contrast G Bit5	Sub Contrast G Bit4	Sub Contrast G Bit3	Sub Contrast G Bit2	Sub Contrast G Bit1	Sub Contrast G Bit0	80 (H)	0	1	0	0	0	08 (H)
		Reference	1	0	0	0	0	0	0	0							
	Register 9	SUB CONTRAST B	Sub Contrast B Bit7	Sub Contrast B Bit6	Sub Contrast B Bit5	Sub Contrast B Bit4	Sub Contrast B Bit3	Sub Contrast B Bit2	Sub Contrast B Bit1	Sub Contrast B Bit0	80 (H)	0	1	0	0	1	09 (H)
		Reference	1	0	0	0	0	0	0	0							
	Register 10	SUB CONTRAST R	Sub Contrast R Bit7	Sub Contrast R Bit6	Sub Contrast R Bit5	Sub Contrast R Bit4	Sub Contrast R Bit3	Sub Contrast R Bit2	Sub Contrast R Bit1	Sub Contrast R Bit0	80 (H)	0	1	0	1	0	0A (H)
		Reference	1	0	0	0	0	0	0	0							

	Register No.	Register Name	Data											Sub Address					
			D7	D6	D5	D4	D3	D2	D1	D0	HEX code	A4	A3	A2	A1	A0	HEX code
AMP	Register 11	SUB BRIGHTNESS G	Sub Brightness G Bit7	Sub Brightness G Bit6	Sub Brightness G Bit5	Sub Brightness G Bit4	Sub Brightness G Bit3	Sub Brightness G Bit2	Sub Brightness G Bit1	Sub Brightness G Bit0	80 (H)	0	1	0	1	1	0B (H)
		Reference	1	0	0	0	0	0	0	0							
	Register 12	SUB BRIGHTNESS B	Sub Brightness B Bit7	Sub Brightness B Bit6	Sub Brightness B Bit5	Sub Brightness B Bit4	Sub Brightness B Bit3	Sub Brightness B Bit2	Sub Brightness B Bit1	Sub Brightness B Bit0	80 (H)	0	1	1	0	0	0C (H)
		Reference	1	0	0	0	0	0	0	0							
	Register 13	SUB BRIGHTNESS R	Sub Brightness R Bit7	Sub Brightness R Bit6	Sub Brightness R Bit5	Sub Brightness R Bit4	Sub Brightness R Bit3	Sub Brightness R Bit2	Sub Brightness R Bit1	Sub Brightness R Bit0	80 (H)	0	1	1	0	1	0D (H)
		Reference	1	0	0	0	0	0	0	0							
	Register 14	CbOFFSET			Cb Offset Bit5	Cb Offset Bit4	Cb Offset Bit3	Cb Offset Bit2	Cb Offset Bit1	Cb Offset Bit0	20 (H)	0	1	1	1	0	0E (H)
		Reference			1	0	0	0	0	0							
	Register 15	CrOFFSET			Cr Offset Bit5	Cr Offset Bit4	Cr Offset Bit3	Cr Offset Bit2	Cr Offset Bit1	Cr Offset Bit0	20 (H)	0	1	1	1	1	0F (H)
		Reference			1	0	0	0	0	0							
	Register 16	AMP MODE					Brightness CLP	RGB In1/2 Select	RGB Out Select	YCbCr mode	00 (H)	1	0	0	0	0	10 (H)
		Reference					0	0	0	0							
SYNC SEP	Register 17	SYNCSEP			Sync Sep V_{TH} Bit3	Sync Sep V_{TH} Bit2	Sync Sep V_{TH} Bit1	Sync Sep V_{TH} Bit0	Sync Sep V_{HYS} Bit1	Sync Sep V_{HYS} Bit0	22 (H)	1	0	0	0	1	11 (H)
		Reference			1	0	0	0	1	0							
ADC	Register 18	OUTPUT MODE					DATA OUT MODE Bit2	DATA OUT MODE Bit1	DATA OUT MODE Bit0	DATA OUT POL	03 (H)	1	0	0	1	0	12 (H)
		Reference					0	0	1	1							
POWER SAVE	Register 19	POWER SAVE			TTLOUT CLP Bit1	TTLOUT CLP Bit0	Sync Sep Power Save	PLL Power Save	AMP Power Save	ADC Power Save	30 (H)	1	0	0	1	1	13 (H)
		Reference			1	1	0	0	0	0							

Description of Operation

Control Register

Programmable control can be performed for many functions of this IC.

1) Mode selection

Both I^2C bus and 3-wire bus mode can be supported, and either of these modes can be selected by the 3WIRE/I^2C (Pin 13).

3WIRE/I^2C pin voltage	0V	1/2V_{CC}	V_{CC} (5V)
Setting mode	I^2C (High)	I^2C (Low)	3-wire bus

The pin threshold voltages are set at 1/3V_{CC} and 2/3V_{CC}.

2) Threshold voltage

In I^2C bus mode, both SDA (Pin 9) and SCL (Pin 10) are input. These input logic signals can have two threshold voltages by the 3-wire/I^2C.
These threshold voltages have the following hysteresis.

SDA, SCL pin threshold voltages

	Threshold voltage (Low → High)	Threshold voltage (High → Low)
I^2C (High) mode	1.95V	1.6V

	Threshold voltage (Low → High)	Threshold voltage (High → Low)
I^2C (Low) mode	1.65V	1.3V

In 3-wire bus mode, the threshold voltages of the logic signal input to the SDA, SCL and XSENABLE pins have the following hysteresis.

SDA, SCL and XSENABLE pin threshold voltages

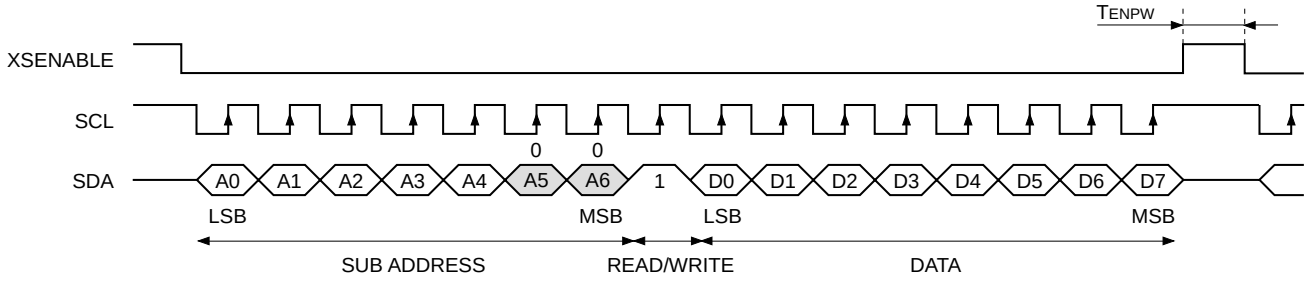
	Threshold voltage (Low → High)	Threshold voltage (High → Low)
3-wire bus mode	1.65V	1.3V

3-wire Bus Mode

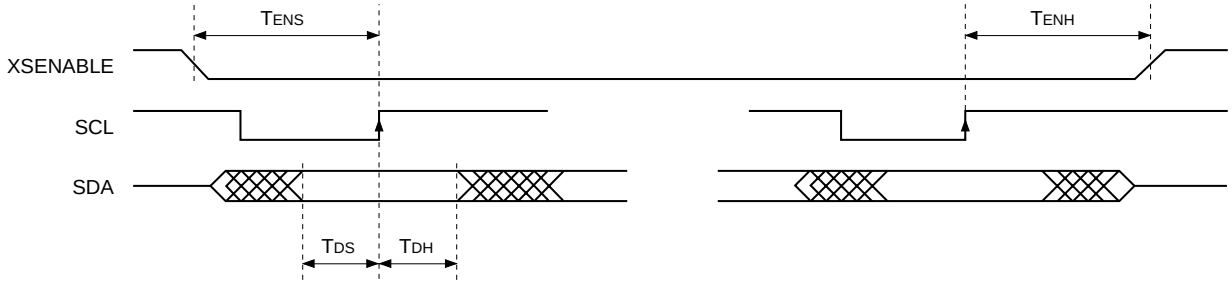
Various control can be performed by setting the internal control register values via the serial interface comprised of the three pins SDA (Pin 9), SCL (Pin 10) and XSENABLE (Pin 11).
Data can be accepted when XSENABLE is low level. When XSENABLE is high level, data cannot be accepted. The SDA pins of multiple IC can also be connected to the same bus line and each IC can be controlled independently by XSENABLE.
XSENABLE may change the state when SCL is high level.

1) Write mode

8-bit control data consisting of a 7-bit sub address and 1-bit READ/WRITE setting is input in series from the LSB to the SDA pin. When READ/WRITE setting is "1", data can be written to register. When this IC is used in 3-wire bus mode, the sub address is 5 bits, so always set the 2 MSB bits to "0".
Input the clock to the SCL pin. Data is loaded to the SDA pin at the rising edge of this clock. The data is set in the register at the rising edge of XSENABLE.
The SDA and SCL pins are also used in I^2C bus control mode.



READ/WRITE
0: READ Mode
1: WRITE Mode



Set the VCO post-stage frequency divider (DIV1, 2, 4, 8) and programmable counter (VCODIV) in the following order. The data is set when Register1 is sent.

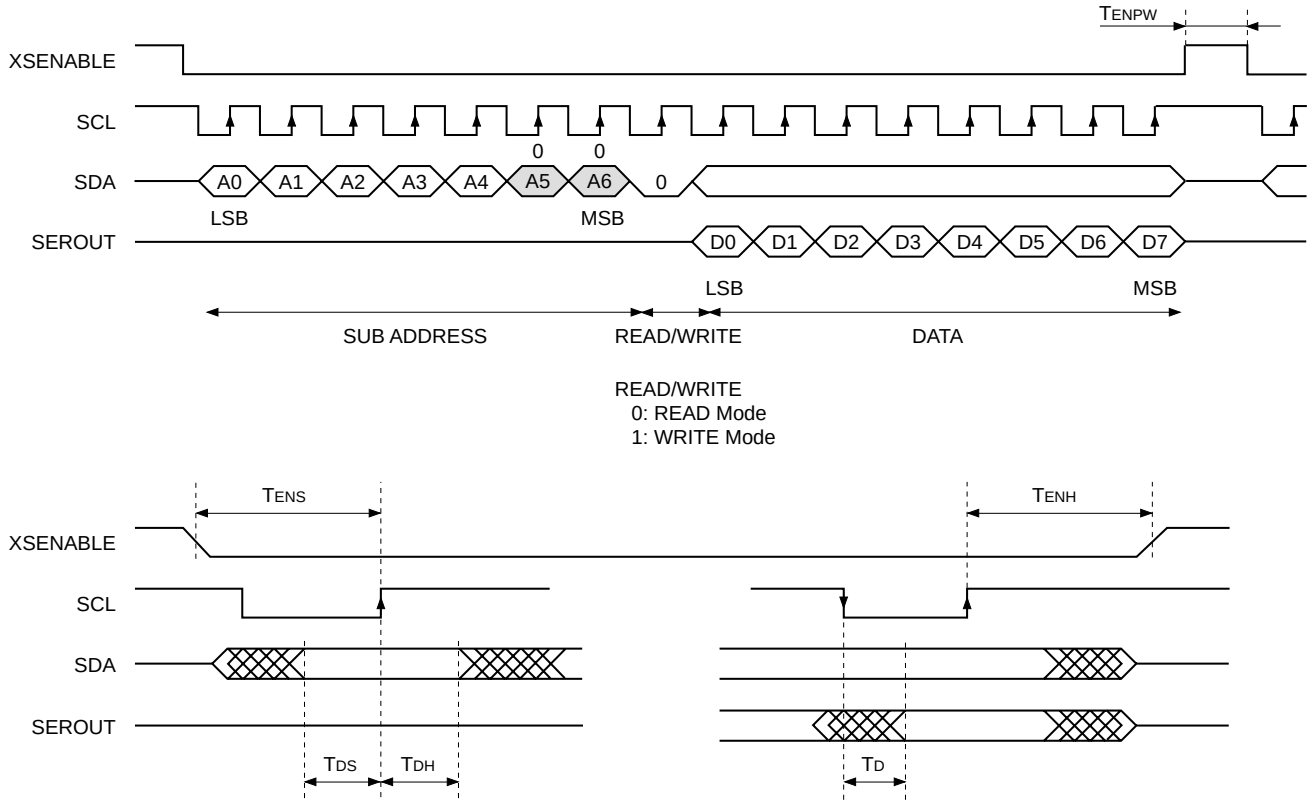
Register0 (SUB ADDRESS (H): 00)
↓
Register1 (SUB ADDRESS (H): 01)

2) Read mode

Input the 7-bit sub address and 1-bit READ/WRITE setting to the SDA pin.

When READ/WRITE setting is "0", the 8-bit internally set data is output in series from the LSB by the SEROUT (Pin 12). While data is being output from the SEROUT pin, don't care what data is input to the SDA pin.

Use the read function to check whether the data is set correctly inside the IC.



The SEROUT pin is TTL output.

When not using the READOUT function, the TTL output circuit can be turned off by control register.

Register: SEROUT ENABLE	0	1
SEROUT output status	Function off	Function on

Power-on Reset

When the power supply rises, the power-on reset circuit operates and all the control register data is set to "1". AMP, ADC, PLL and SYNCSEP are all set to power save mode, and all the TTL output pins are set to high impedance mode. Therefore, it is possible to share the same bus interface with other digital outputs having high impedance modes.

I²C BUS Mode

Various control can be performed by setting the internal control register values via the serial interface comprised of the SDA (Pin 9) and SCL (Pin 10). This mode has only a write mode for setting data, and there is no read mode. Therefore, address "S0" set READ/WRITE is always "0".

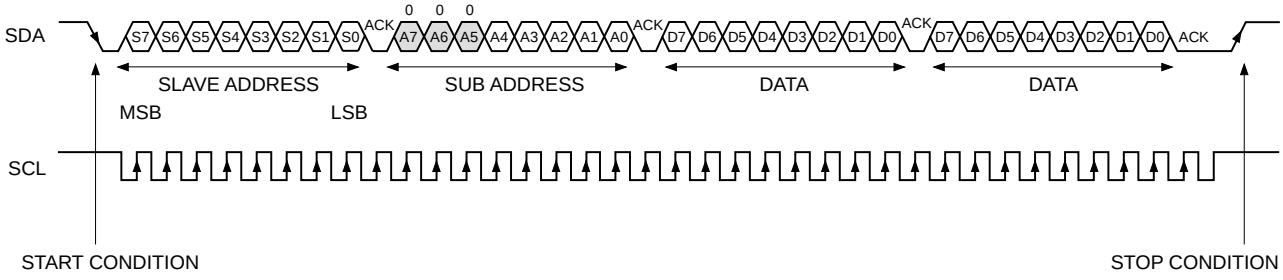
	S7	S6	S5	S4	S3	S2	S1	S0
SLAVE ADDRESS	1	0	0	1	1	x	x	0

Four different kinds of slave address (IC address) can be set by externally setting the ADDRESS (Pin 2) to a specific voltage.

ADDRESS pin voltage	0V	1/3Vcc	2/3Vcc	Vcc (5V)
SLAVE ADDRESS	1001 1000	1001 1100	1001 1110	1001 1010

The pin threshold voltages are set to 1/4Vcc, 1/2Vcc and 3/4Vcc.

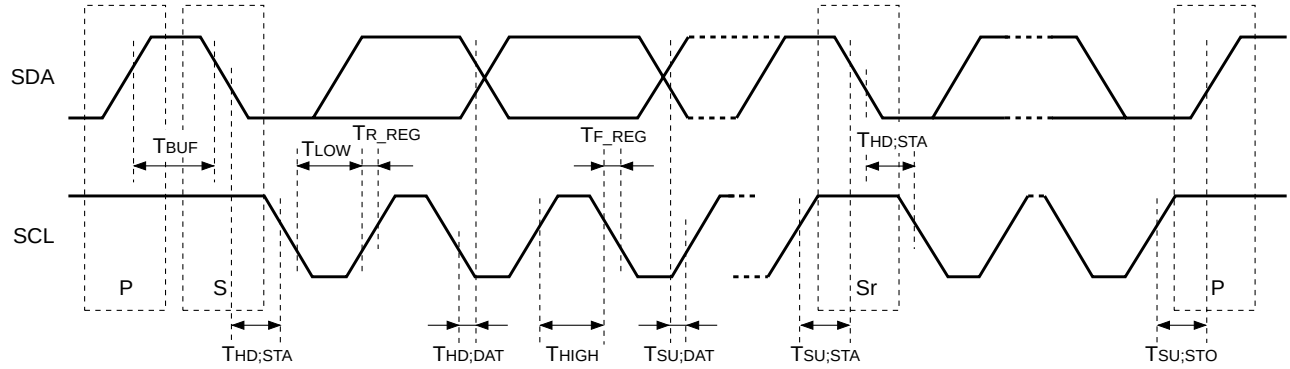
An 8-bit slave address (IC address), 8-bit sub address, and a number of 8-bit data strings are input in series from the MSB to the SDA pin. When this IC is used in I²C bus mode, sub address is 5 bits, and 3 bits of MSB side are set to always "0". ACK signal is returned from the IC to confirm that the data has been received for each 8-bit data.
The sub address can be designated optionally. The sub address is auto-incremented in order from the designated sub address, and the data strings are loaded in succession.
To set the data at a specific separated sub address, either send the stop condition and then reset the sub address, or also send the data of unchanged portions so that the data is continuous. Only auto-increment mode is supported, and the sub address + data + sub address + data mode where only specific sub addresses are designated is not supported.



• START CONDITION
When SCL pin is high level, the signal input to SDA pin has a falling edge, there is START CONDITION.

• STOP CONDITION
When SCL pin is high level, the signal input to SDA pin has a rising edge, there is STOP CONDITION.

I²C BUS Control Signals



Power-on Reset

When the power supply rises, the power-on reset circuit operates and all the control register data are set to "1". AMP, ADC, PLL and SYNCSEP are all set to power save mode, and all the TTL output pins are set to high impedance mode. Therefore, it is possible to share the same bus interface with other digital outputs having high impedance modes.

Amplifier

This is a 3-channel AMP that optimizes the AC coupled RGB analog input signals and YCbCr analog input signals for ADC input. Switch input mode between RGB input or YCbCr input with the control register. The AC coupled analog input signals are synchronously clamped by the externally input clamp pulse at a pedestal level. An input capacitor of 0.1µF is recommended.

Allowing two lines of input to be selected for the analog input signal, the AMP includes a high frequency, low cross talk video switch circuit for input switching. Switching is performed using a control register. When using only one line, leave the unused line open.
The input band of the analog input signal is 220MHz in the –3dB bandwidth range.

There are main contrast and sub-contrast of the gain used to adjust the analog input signal to full scale (1V typ.) of the ADC. Each can be adjusted to one of 256 levels using control registers. Main contrast is controlled by moving the gain of the 3 RGB channels. The each gain of the 3 RGB channels can be controlled independently.
In RGB input mode, the clamp level used for the black level adjustment can be adjusted independently for the 3 channels to any of 256 levels by using sub-brightness.

The ∗CLP pin*1 is connected to the hold capacitor of the clamp circuit for the sub-brightness. A hold capacitor of 0.1µF is recommended.
The ∗OUT pins*2 can output signal immediately before input to the ADC or the signal after switching between the two lines of input select switch. Either of them can be selected by control register. As for emitter follower output, since the internal bias current is small, be sure to connect an 820Ω resistor between the ∗OUT pins*2 and AGND in order to view the signal with a high frequency. A 75Ω driver cannot be supported. In addition, load capacitance should be 5pF or less.
When the SYNC ON GREEN signal is monitored at the ∗OUT pins*2 after the two lines of select switch, the sync amplitude is a maximum of 0.3V, for a limiter is applied at the amplifier input stage.

In YCbCr signal input mode, Y can be adjusted to any of 256 levels using the sub-brightness while Cb and Cr can be adjusted to any of 64 levels using the Cb or Cr offset.
A detailed description of the above registers is given below.

*1 ∗CLP pins: Overall naming for R/Cr CLP (Pin 130), G/Y CLP (Pin 128), B/Cb CLP (Pin 129)
*2 ∗OUT pins: Overall naming for R/Cr OUT (Pin 3), G/Y OUT (Pin 143), and B/Cb OUT (Pin 1)

- **Analog input signal mode switching**

  Analog input signal supports both RGB analog input signal and YCbCr analog input signal.
  This register switches the clamp level of the input clamp block and the amplifier output block in each mode. However, the G/Ych perform the same processing in both RGB input mode and YCbCr input mode.

Register: YCbCr mode	0	1
Analog input signal mode	RGB input	YCbCr input

- **Input channel switching**

  Input supports 2-channel input, and the input can be selected by an internal switch.

Register: RGB In Select	0	1
Analog input signal channel switching	IN1	IN2

- **Clamp pulse input polarity**

  The clamp pulse input polarity can be selected by an internal switch.

Register: CLP POL	0	1
Clamp pulse polarity	NEGATIVE	POSITIVE

• **Brightness clamp off function**

Clamp operation can be set to a mode where only the post-stage brightness clamp does not operate even if a clamp pulse is input to the CLPIN (Pin 113). At this time, all three channels of the ∗CLP pins[*1] are set to high impedance simultaneously, and the signal black level can be varied in an analog manner by setting the voltages externally. However, the voltage value set here is not related to the VRT (Pin 17) and VRB (Pin 93) voltages or the ∗OUT[*2] monitor signal output DC levels. Therefore the value should be set while monitoring the ADC data output or the data after that.

Register: Brightness CLP	0	1
Clamp operation	Clamp operation	Clamp off

• **Monitor signal output selection**

The two monitor signal outputs (∗OUT pins[*2]) of the amplifier can be selected by an internal switch. One is amplifier output signal immediately before input to the ADC, and other is after switching between the two lines of select switch.

Register: RGB Out select	0	1
Monitor output switching	Amplifier output	Switch output

• **Main contrast**

The RGB channel gains can be set collectively by an 8-bit DAC setting.

Register: MAIN CONTRAST	0	· · ·	128	· · ·	255
Amplifier gain (typ.) SUB CONTRAST = 128	0.78	· · ·	1.53	· · ·	2.24

• **Rch sub contrast**

The Rch contrast (R amplifier gain) can be adjusted independently within the range of ±21% relative to the main contrast by an 8-bit DAC setting.

Register: SUB CONTRAST R	0	· · ·	128	· · ·	255
Rch gain adjustment (typ.)	–21%	· · ·	0%	· · ·	+21%

• **Gch sub contrast**

The Gch contrast (G amplifier gain) can be adjusted independently within the range of ±21% relative to the main contrast by an 8-bit DAC setting.

Register: SUB CONTRAST G	0	· · ·	128	· · ·	255
Gch gain adjustment (typ.)	–21%	· · ·	0%	· · ·	+21%

• **Bch sub contrast**

The Bch contrast (B amplifier gain) can be adjusted independently within the range of ±21% relative to the main contrast by an 8-bit DAC setting.

Register: SUB CONTRAST B	0	· · ·	128	· · ·	255
Bch gain adjustment (typ.)	–21%	· · ·	0%	· · ·	+21%

• **Rch sub brightness in RGB mode**

The Rch sub brightness (black level voltage) can be set by an 8-bit DAC during RGB signal input.
The Rch sub brightness can be varied within the range of ±25% of the ADC input dynamic range (approximately 1V) centering on VRB (Pin 93) (approximately 1.9V).

Register: SUB BRIGHTNESS R	0	· · ·	128	· · ·	255
Level shift amount (typ.)	–61LSB	· · ·	0LSB	· · ·	+61LSB

Register: YCbCr mode	0
Input signal mode	RGB

• **Gch sub brightness in RGB mode**

The Gch sub brightness (black level voltage) can be set by an 8-bit DAC during RGB signal input.
The Gch sub brightness can be varied within the range of ±25% of the ADC input dynamic range (approximately 1V) centering on VRB (Pin 93) (approximately 1.9V).

Register: SUB BRIGHTNESS G	0	· · ·	128	· · ·	255
Level shift amount (typ.)	–61LSB	· · ·	0LSB	· · ·	+61LSB

Register: YCbCr mode	0
Input signal mode	RGB

• **Bch sub brightness in RGB mode**

The Bch sub brightness (black level voltage) can be set by an 8-bit DAC during RGB signal input.
The Bch sub brightness can be varied within the range of ±25% of the ADC input dynamic range (approximately 1V) centering on VRB (Pin 93) (approximately 1.9V).

Register: SUB BRIGHTNESS B	0	· · ·	128	· · ·	255
Level shift amount (typ.)	–61LSB	· · ·	0LSB	· · ·	+61LSB

Register: YCbCr mode	0
Input signal mode	RGB

• **Cbch black level shift in YCbCr mode**

The Cbch black level voltage can be set by a 6-bit DAC during YCbCr signal input.
The Cbch black level voltage can be varied within the range of ±16LSB centering on the ADC input dynamic range center ((VRT + VRB)/2).

Register: Cb Offset	0	· · ·	32	· · ·	63
Level shift amount (typ.)	112LSB	· · ·	128LSB	· · ·	144LSB

Register: YCbCr mode	1
Input signal mode	YCbCr

• **Crch black level shift in YCbCr mode**

The Crch black level voltage can be set by a 6-bit DAC during YCbCr signal input.
The Crch black level voltage can be varied within the range of ±16LSB centering on the ADC input dynamic range center ((VRT + VRB)/2).

Register: Cr Offset	0	· · ·	32	· · ·	63
Level shift amount (typ.)	112LSB	· · ·	128LSB	· · ·	144LSB

Register: YCbCr mode	1
Input signal mode	YCbCr

• **Input signal connection method**

Input		Output	
Pin No.	Symbol	Pin No.	Symbol
Pin 124 Pin 126	G/YIN1 G/YIN2	68 to 75 78, 81 to 85, 87, 88	GA0 to GA7 GB0 to GB7
Pin 133 Pin 136	B/CbIN1 B/CbIN2	45 to 49, 51 to 53 56 to 58, 60 to 64	BA0 to BA7 BB0 to BB7
Pin 139 Pin 141	R/CrIN1 R/CrIN2	21, 22, 24 to 28, 31 34 to 41	RA0 to RA7 RB0 to RB7

1. When inputting both RGB and YCbCr, input according to the table above.
2. SYNCSEP is connected to G/YIN.
3. When inputting RGB and not using SYNCSEP, there is no difference between the three channels so the input order may be optional.
4. When inputting Y, Cb and Cr, be sure to input according to the table above. It is possible for only the R/Cr IN and B/Cb IN pins to be clamped to the center of the ADC input dynamic range.

SYNCSEP

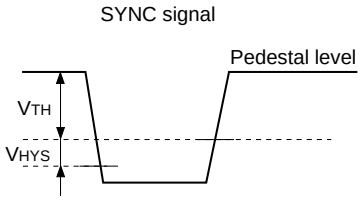
The SYNCSEP function can be used to separate and output the SYNC signal that is superimposed on the SYNC ON GREEN signal (including the SYNC ON Y signal).
There are two major SYNCSEP circuits. One is the circuit for creating a SYNC signal to be input to the PLL, and the other is a circuit for outputting a SYNC signal from the SOGOUT (Pin 105) so that a clamp pulse can be created externally. These SYNCSEP circuits perform processing on entirely different channels.
(See the block diagram for the SYNCSEP operational description.)

- **SYNCSEP circuit for the PLL SYNC signal**

  In the case of the SYNC ON GREEN signal, the SYNC ON GREEN signal is AC coupled to the G/YIN1 (Pin 124) or the G/YIN2 (Pin 126) and the sync component is separated and used as a reference. An input capacitor of 0.1µF is recommended.
  When a signal is input to this pin, the pedestal level is clamped by a clamp pulse input to the CLPIN (Pin 113). After this, the signal is split into a signal to the amplifier circuit and the signal to the SYNCSEP circuits, and the SYNC signal is sent through a two lines of input select switch (SW SOGP) and the SYNC signal is separated by the SYNCSEP circuits. At this time, it is possible to minimize the jitter of the SYNC signal sent to the PLL by using a control register to select the threshold level (V_{TH}) and hysteresis level (V_{HYS}) of the SYNCSEP circuit according to the type of noise on the superimposed SYNC signal.

SOG SYNC SEP threshold (Versus pedestal level)

Register: SYNC SEP V_{TH}	0000	· · ·	1111
Threshold	75mV	9.3mV step	215mV



SOG SYNC SEP hysteresis

Register: SYNC SEP V_{HYS}	00	01	10	11
Hysteresis	2mV	20mV	45mV	70mV

The SYNC signal separated by the SYNCSEP circuits can be switched at the SW PLL circuit with an externally input SYNC signal (the SYNC signal input from the SYNCIN1 or SYNCIN2 pin) by using control registers (SYNCP/HSYNC). The selected signal is input to the PLL block.

Selecting between the sync separated SYNC signal and the externally input SYNC signal

Register: SYNCP/HSYNC IN	0	1
SYNC signal type	Sync separated signal	Externally input SYNC signal
SYNC signal input pin	G/YIN1 pin G/YIN2 pin	SYNCIN1 pin SYNCIN2 pin

• **SYNCSEP circuits for the SYNC signal for the clamp pulse**

A SYNC ON GREEN signal is input to the SOGIN1 (Pin 132) or SOGIN2 (Pin 135). The AC coupled signal is internally sync tip clamped and the minimum level (bottom of sync) is turned into the internally-set DC level (approximately 2.8V).

The sync tip clamped input signal is separated from the threshold of 165mV (at SYNC DUTY 5%) above from the bottom of the sync by the SYNCSEP circuit. After this, the signal is output at TTL level from the SOGOUT pin and used as a reference signal for generating a clamp pulse.

Since no clamp pulse is required for the sync tip clamp, it is possible to output a SYNC signal from the SOGOUT pin even when there is no external clamp pulse present such as when power supply is turned on.

An input capacitor of 0.1µF is recommended.

A control register can be used to select output either the SYNC signal separated out from the signal input from the SOGIN1 pin or the SOGIN2 pin by SW SOG O or the previously described PLL SYNC signal output from the SW PLL circuit.

Output from the SOGOUT pin

SYNCT1, SYNCT2/SYNCP1, SYNCP2/SYNCIN1, SYNCIN2 output selection

SYNCT1, SYNCT2: The SYNC signal sync tip clamped and separated from the SOGIN1 and SOGIN2 pins

SYNCP1, SYNCP2: The SYNC signal pedestal clamped and separated from the G/YIN1 and G/YIN2 pins

SYNCIN1, SYNCIN2: The SYNC signal input from the SYNCIN1 and SYNCIN2 pins

Register: SYNC OUT SW	0	1
Output from the SOGOUT pin	SYNCT1, SYNCT2	SYNCP1, SYNCP2 or SYNCIN1, SYNCIN2

The SOGIN1, SOGIN2 and the previously described G/YIN1, G/YIN2 are interlocked as for the 2-ch selection (Register: RGB In Select).

Input channel selection

Register: RGB In Select	0	1
G/YIN pin selection	IN1	IN2
SOGIN pin selection	IN1	IN2

The polarity of signals output from the SOGOUT pin can be set by using registers.

Register: SOGOUT POL	0	1
SOGOUT output polarity	Negative	Positive

• **SYNC ON GREEN output enable**

When the SOGOUT pin is not used, it is possible to turn off the TTL output using a control register. But it cannot be set to high impedance.

Register: SOG Enable	0	1
SOGOUT output status	Off	On

PLL

- **SYNC signal input**

The SYNC (HSYNC) used by the PLL is input from the SYNC signal input pins. There are two sets of input pins, SYNCIN1 (Pin 111) and SYNCIN2 (Pin 112), which are switched by the control register.

SYNCIN1 input, SYNCIN2 input switching

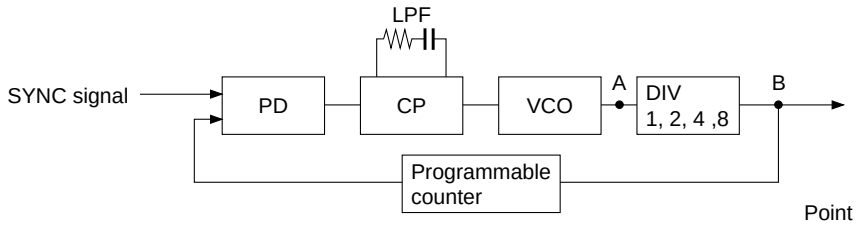
Register: HSYNC1/2	0	1
SYNC signal input pin	SYNCIN1	SYNCIN2

SYNC signals within the range from 10kHz to 100kHz can be input. The input supports both positive and negative polarity.

SYNC signal input polarity

Register: SYNC POL	0	1
SYNC signal input polarity	Negative	Positive

Set the register in accordance with the polarity of the externally input SYNC.
When SYNC is positive polarity, set SYNC POL to "1". (Clock is generated in sync with the rising edge of SYNC.)
When SYNC is negative polarity, set SYNC POL to "0". (Clock is generated in sync with the falling edge of SYNC.)
When there is no SYNC input, the VCO oscillates at random and a random pulse is output from the CLK output.



Point A: VCO oscillation frequency
Point B: Clock frequency

- **Phase detector (PD)**

The phase detector compares the phase of the SYNC signal with that of the programmable counter output signal. The phase comparison is performed at the edge, and a phase difference between the compared signals is output as a pulse.
There is no hysteresis function for the input pins of the SYNC signal (SYNCIN1 and SYNCIN2) input to the phase detector. If necessary external waveform shaping should be done as jitter results when a noisy signal is input. Set the control register, PD POL, to "1" as for the input polarity of the phase detector.

- **Hold function**

The hold function holds the VCO input voltage and generates oscillation itself without performing phase comparison. The VCO oscillation frequency is held during this period without performing phase comparison, by inputting the HOLD signal from the HOLD (Pin 106).
HOLD signal polarity can be set by using the control register: HOLD POL.

Register: HOLD POL	0	1
HOLD signal input polarity	Held while HOLD signal is Low	Held while HOLD signal is High

For details, see the hold timing diagram.

• **Charge pump (CP)**

The charge pump sets charge pump current to flow for the amount of time corresponding to the pulse width output from the phase detector. The phase detector gain is determined by the charge pump current.
The amount of current can be varied by using a control register.
This IC is used to set the charge pump current value according to the VCO oscillation frequency as given below.

[CP Setting Matrix]

VCO oscillation frequency: CP setting values
40MHz to 85MHz: 200µA
85MHz to 110MHz: 300µA
110MHz to 140MHz: 400µA
140MHz to 155MHz: 500µA
155MHz to 165MHz: 600µA

The VCO oscillation frequency is that at the Point A in the diagram.

Register: Charge Pump Bit2	0	0	0	0	1	1	1	1
Register: Charge Pump Bit1	0	0	1	1	0	0	1	1
Register: Charge Pump Bit0	0	1	0	1	0	1	0	1
Charge pump current	100µA	200µA	300µA	400µA	500µA	600µA	700µA	800µA

• **Loop filter (LPF)**

The control voltage input to the VCO is the pulse current output from the charge pump circuit that is smoothed by an integrating circuit (loop filter). The resistor and capacitor values of the integrating circuit are as follows. (For the circuit configuration, see the application circuit.)

C1 = 0.33µF
C2 = 330pF
R1 = 3.3kΩ

For the resistor and capacitors, use a metal film chip resistor with little temperature variation and ceramic chip capacitors. In particular, the 0.33µF capacitor should be equivalent to high dielectric constant series capacitor type B or better.
(Electrostatic capacitance change ratio ±10%: T = –25 to +85°C)
In case of using any resistors or capacitors except those given above, it is not guaranteed.

• **VCO**

The VCO oscillation frequency range covers from 40MHz to 165MHz.

• **VCO frequency dividers (DIV 1, 2, 4, 8)**

The oscillation frequency of the VCO can be divided to 1/1, 1/2, 1/4, or 1/8 according to a control register setting. Depending on the combination of the VCO oscillation frequency and VCO frequency divider, the Point B clock frequency covers an operating range of 5MHz to 120MHz. The matrix of the VCO frequency divider setting is as follows.

[VCO Frequency Divider Setting Matrix]

Clock frequency: DIV setting value

5MHz to 14MHz: 1/8
14MHz to 40MHz: 1/4
40MHz to 80MHz: 1/2
80MHz to 120MHz: 1/1

Register: DIV 1, 2, 4, 8 Bit1	0	0	1	1
Register: DIV 1, 2, 4, 8 Bit0	0	1	0	1
Counter frequency	1/1	1/2	1/4	1/8

• **Programmable counter**

The clock frequency at Point B is divided and a programmable counter output signal is generated.
The frequency division ratio can be set optionally by using a 12-bit control register. This is determined by using lower order 3 bits and upper order 9 bits in the following formula.

Frequency division ratio = $(m + 1) \times 8 + n$

m: 9 bits (VCO DIV Bit 3 to 11)
n: 3 bits (VCO DIV Bit 0 to 2)

Register No.	Register Name	Data7 MSB	Data6	Data5	Data4	Data3	Data2	Data1	Data0 LSB
Register 0	VCODIV1	m4	m3	m2	m1	m0	n2	n1	n0
Register 1	VCODIV2					m8	m7	m6	m5

After the set value for the frequency division ratio is changed, that set value is loaded into the programmable counter when the output value of the programmable counter becomes "all 0".

• **Clock output**

When the input polarity of the SYNC signal is positive, the clock output is synchronized to the rising edge of the SYNC signal and is available as complementary signals CLK (Pin 99) and XCLK (Pin 98). The delay time of the clock output can be varied in the range of 1/32CLK to 64/32CLK by using a control register (see PLL timing diagram). Although the clock output can be turned off independently by using a control register, it cannot be set to high impedance. The operational frequency of the clock is up to 100MHz.

Register: CLK Enable, XCLK Enable	0	1
Clock output status	Off	On

• **1/2 clock output**

1/2 clock signal is a signal that resets the clock by using a reset pulse created from an internal delay sync signal and divides the clock in half. The complementary signal is output from the 1/2CLK (Pin 101) and 1/2XCLK (Pin 100). (See the PLL timing diagram). Although the 1/2 clock output can also be independently turned off by the control register, it cannot be set to high impedance.

Register: 1/2CLK Enable, 1/2XCLK Enable	0	1
1/2 Clock Output Status	Off	On

• **Delay sync output**

Two types of delay sync signal (DSYNC and DIVOUT) can be output from the DSYNC/DIVOUT (Pin 103). This is selected by switching a control register. The DSYNC signal is output as the input SYNC signal undergone timing control. The DIVOUT signal is output as the programmable counter output undergone timing control.

Both can be used as reset signals for any connected IC such as a scaling IC.

Delay sync output signal (DSYNC/DIVOUT (Pin 103))

Register: DSYNC By-pass	0	1
Signal output from the DSYNC/DIVOUT pin	DIVOUT signal	DSYNC signal

• **DSYNC signal**

A SYNC signal input that has been timing controlled by a clock generated by a PLL is output.

Although only the forward edge is completely managed at this time with delay settings, etc., the back edge has an undefined width for one clock cycle because it latches and outputs the input SYNC signal.

• **DIVOUT signal**

A timing controlled programmable counter output signal is output. In addition to the COARSE DELAY that has been set by using the DSYNC signal, the delay time setting is output with a delay of 4 or 5 clocks. The pulse width is also managed by a clock.

[Function Correspondence Table for the DSYNC Signal/DIVOUT Signal]

Function	DSYNC signal	DIVOUT signal	Register
COARSE DELAY	3CLK to 6CLK	3CLK to 6CLK	COARSE DELAY
FINE DELAY	1/32CLK to 64/32CLK	1/32CLK to 64/32CLK	FINE DELAY
Pulse width	Fixed (depends on input SYNC signal width)	1, 2, 4, 8CLK	DIVOUT WIDTH
DIVOUT DELAY	—	4, 5CLK	DIVOUT DELAY
Output polarity	On/Off	On/Off	DSYNC POL
Output enable	On/Off	On/Off	DSYNC Enable
Output during HOLD	On/Off	On/Off	DSYNC Hold

• **Delay time setting (Fine Delay/Coarse Delay)**

The delay sync output, clock output, and 1/2 clock output can make delay time setting (Fine Delay/Coarse Delay) for the input signal. The amount of delay time is from 3CLK Delay to 6CLK Delay for Coarse Delay and from 1/32CLK to 64/32CLK for Fine Delay.

The delay time (Fine Delay/Coarse Delay) can be set by using the control registers shown below.

Register: FINE DELAY	000000	000001	· · · · · · · · · · · ·	111111
Delay time	1/32CLK	2/32CLK	· · · · · · · · · · · ·	64/32CLK

Register: COARSE DELAY	00	01	10	11
Delay time	3CLK	4CLK	5CLK	6CLK

• **DIVOUT signal output pulse width**

The pulse width of the DIVOUT signal output can be set to 1, 2, 4, 8 clock pulse widths by using a control register.

Register: DIVOUT WIDTH	00	01	10	11
DSYNC signal width	1CLK	2CLK	4CLK	8CLK

• **DIVOUT signal output delay time setting**

The DIVOUT signal is output with 4 or 5 clock delay based on the delay time (Fine Delay/ Coarse Delay) set as described above.

The clock delay time can be set by using a control register.

Register: DIVOUT DELAY	0	1
Delay time	4CLK	5CLK

• **Delay sync output polarity**

The polarity of the delay sync signal output from the DSYNC/DIVOUT pin can be selected either negative or positive by using a control register.

Register: DSYNC POL	0	1
Delay sync output polarity	Negative	Positive

• **Delay sync output status**

Although it is possible to turn off the signal output from the DSYNC/DIVOUT pin by using a control register, it cannot be set to high impedance.

Register: DSYNC Enable	0	1
Delay sync output status	Off	On

• **Delay sync output status during hold**

Register: The delay sync output during the hold period can be controlled with the DSYNC Hold register and the HOLD signal.

Register: DSYNC Hold	0	1
Delay sync output status	Using HOLD signal logic	DSYNC signal/DIVOUT signal

The output status resulting from this setting differs based on status of the DSYNC By-pass register.

Register: DSYNC Hold	Register: DSYNC By-pass	HOLD signal logic (When HOLD POL register = 1)	Delay sync output
0	0	H	L
0	0	L	DIVOUT signal
0	1	H	L
0	1	L	DSYNC signal
1	0	H	DIVOUT signal
1	0	L	DIVOUT signal
1	1	H	DSYNC signal
1	1	L	DSYNC signal

The values given in the above table are for when the DSYNC POL register is set to "1". The delay sync output status is reversed when DSYNC POL is set to "0".

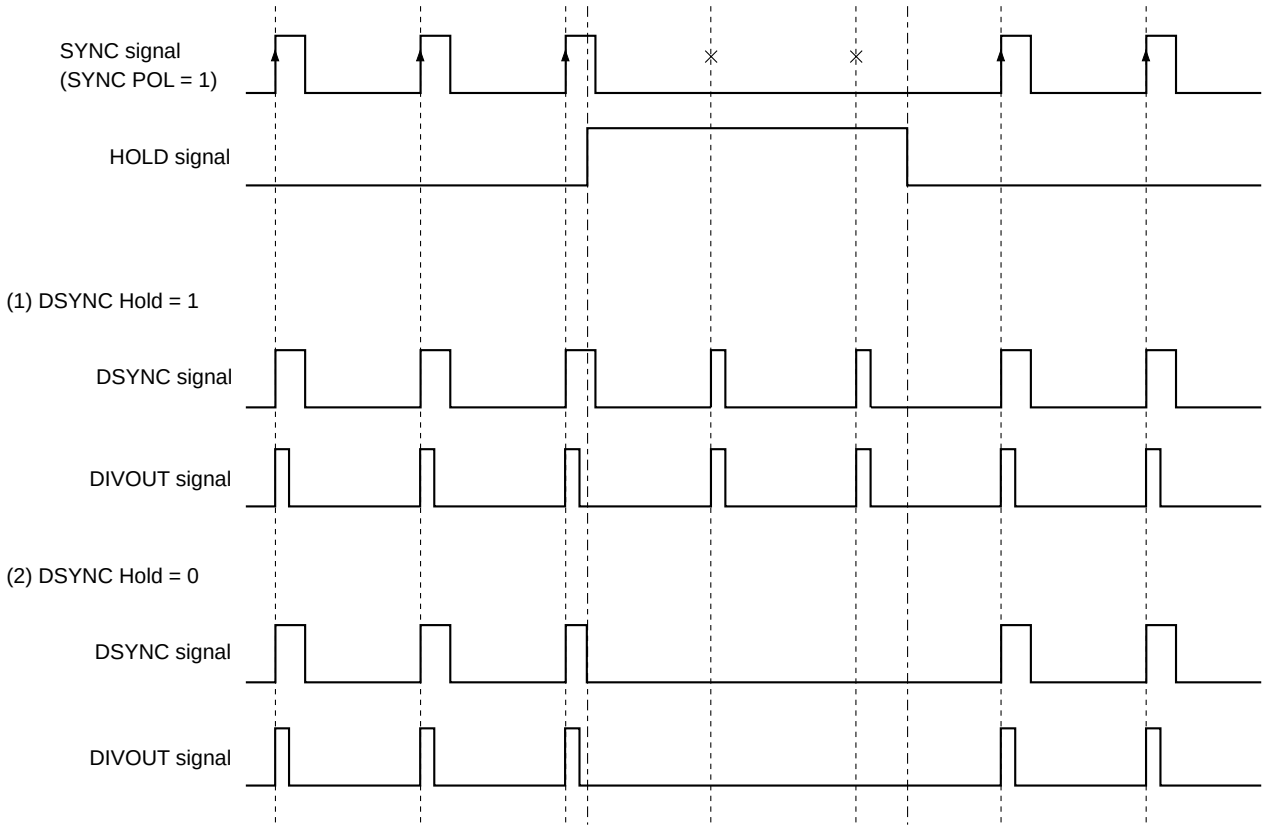
• **XTLOAD signal (reset signal)**

This input pin forces to reset the divider function of the programmable counter.
Since this signal is not normally used, leave it open or fix to high level.
When it is used, this signal is in conjunction with the HOLD signal. See the note given later regarding the combined use of these signals.

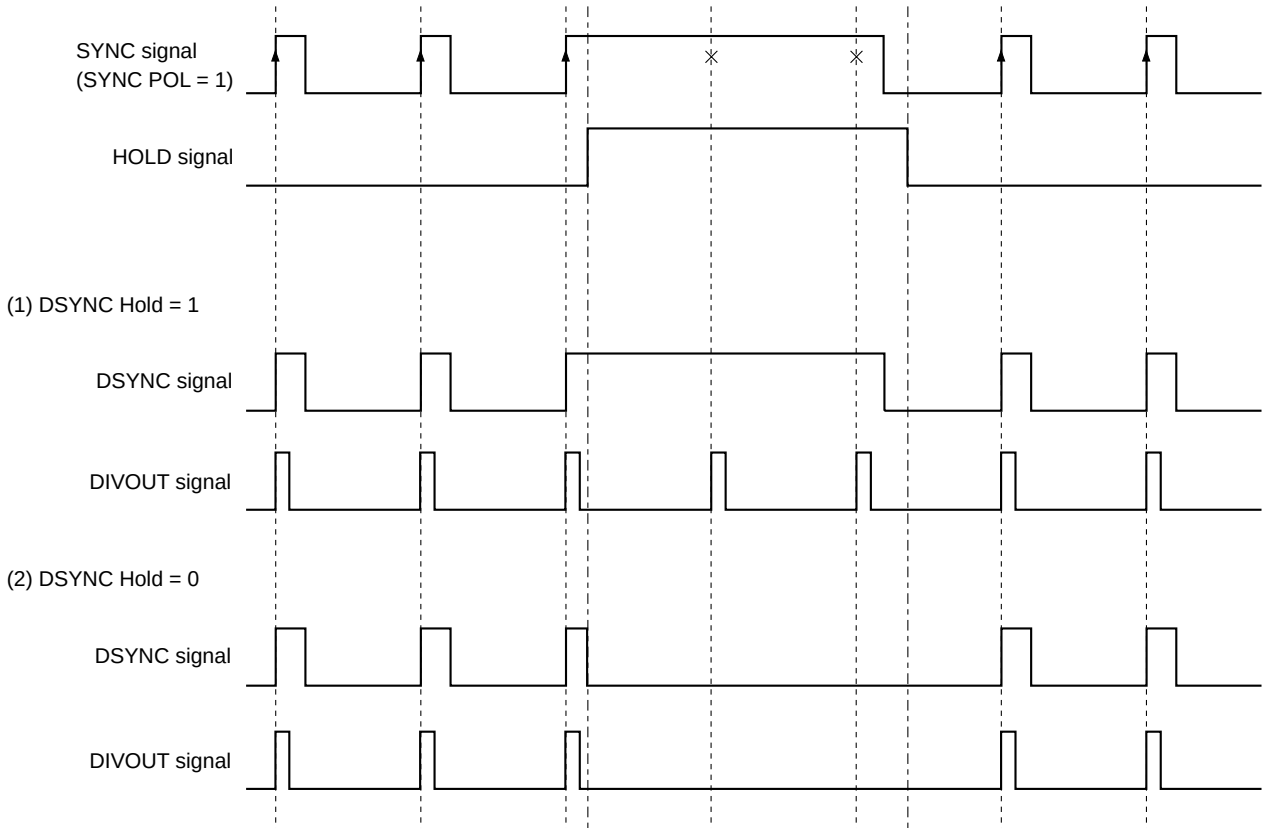
XTLOAD pin	L	H
Programmable counter status	Forcible reset	Count

Register: The DSYNC Hold register and HOLD signal can be used to control the delay sync output during the hold period. The relationship between the delay sync output and the SYNC signal is shown below.
(For each of CASE 1 to 3, the DSYNC POL register is "1". In addition, the DSYNC signal output and DIVOUT signal output can be switched by using the DSYNC By-pass register.)

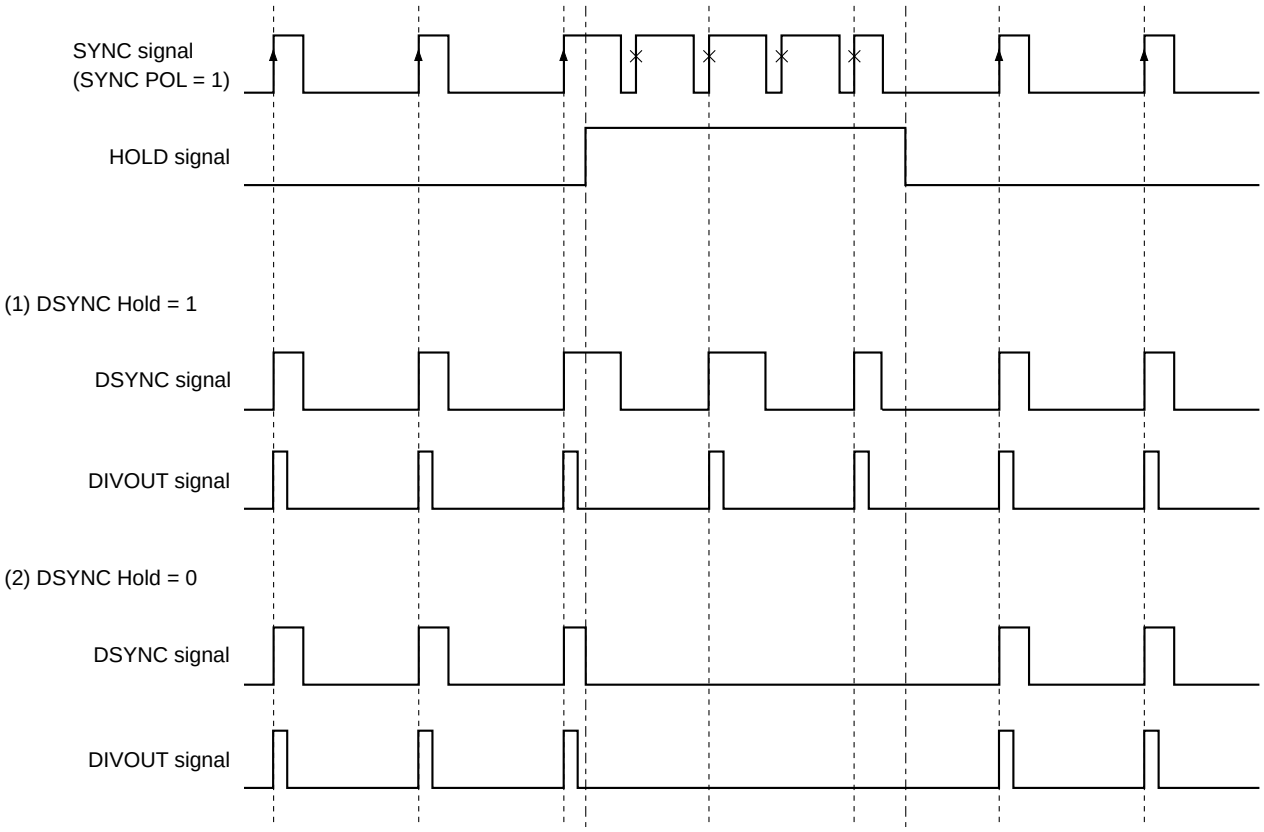
CASE 1



CASE 2

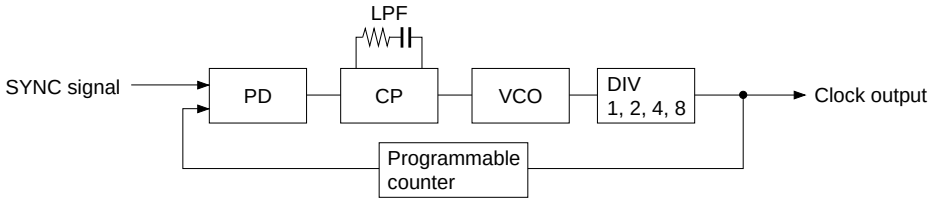

SYNC signal
(SYNC POL = 1)
HOLD signal
(1) DSYNC Hold = 1
DSYNC signal
DIVOUT signal
(2) DSYNC Hold = 0
DSYNC signal
DIVOUT signal

CASE 3

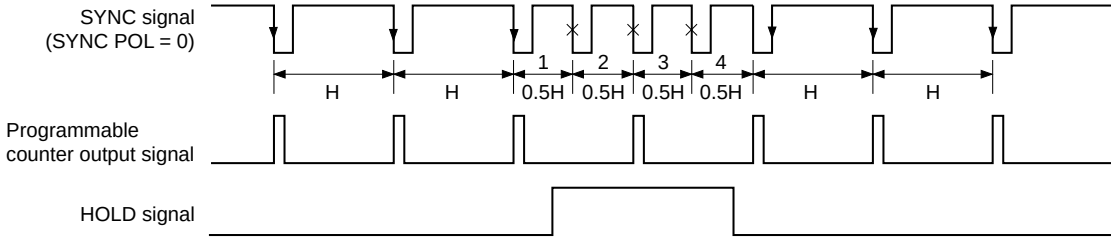

SYNC signal
(SYNC POL = 1)
HOLD signal
(1) DSYNC Hold = 1
DSYNC signal
DIVOUT signal
(2) DSYNC Hold = 0
DSYNC signal
DIVOUT signal

Notes on Using the HOLD Signal and XTLOAD Signal (Reset Signal)

If the cycle of the SYNC signal is lost, the phase difference between the SYNC signal and the programmable counter output in the phase detector will increase, and it will cause PLL unlock. At this time, the HOLD signal is input to the HOLD (Pin 106), phase comparison is stopped while the signal is high level (when the HOLD POL register is set to "1"), and the clock can be stably oscillated by holding the VCO oscillation frequency. Note, however, the correspondence differs depending on whether the number of locations where the SYNC signal period changes (the 0.5H region in the diagram) is odd or even.

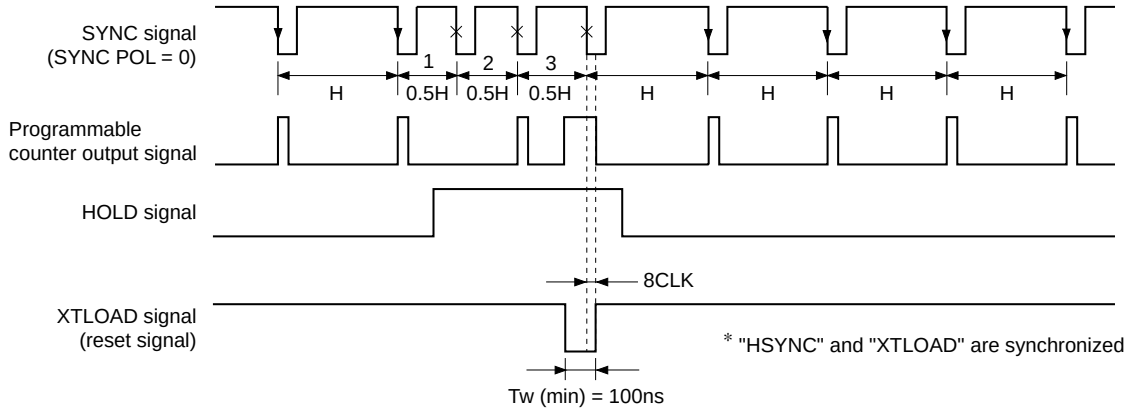


Case 1: When the 0.5H region is even (correspondence with HOLD signal only)



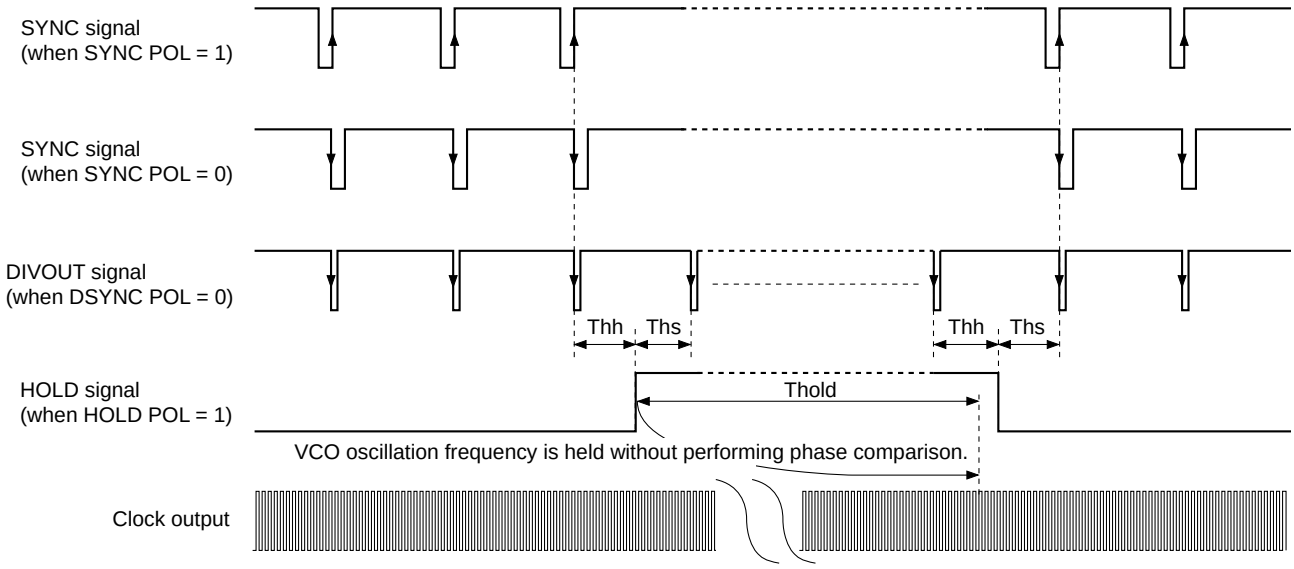
When the number of the 0.5H period is even, it is possible to hold the period of the programmable counter output stable by applying the HOLD signal before the frequency changes.
This corresponds to the vertical blanking period of the composite sync (computer signal).

Case 2: When the 0.5H region is odd (correspondence with HOLD signal + XTLOAD signal (reset signal))



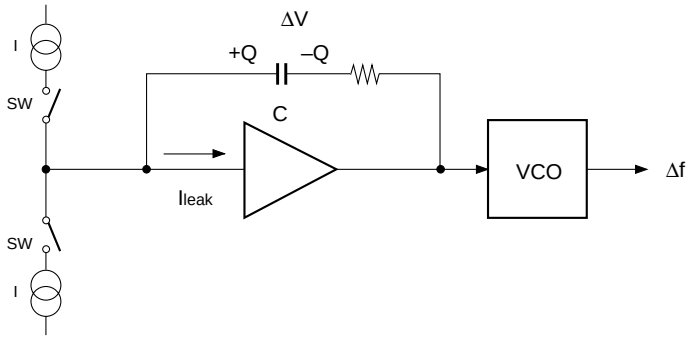
When the number of the 0.5H period is odd, if only the HOLD signal is used, the phase difference between the SYNC signal and the programmable counter output signal will increase in the extra 0.5H region and the lock will be lost momentarily.
In this case, the 0.5H region is held by the HOLD signal, and it is possible to use the XTLOAD signal (reset signal) at 1H backward to the official counter period by resetting/setting the counter value.
Although there are no particular restrictions on the setup time and hold time of the XTLOAD signal (reset signal), the pulse width of the XTLOAD signal (reset signal) is restricted while the HOLD signal is high. (When the HOLD POL register is set to "1".)
If the rising edge of the XTLOAD signal (reset signal) is delayed by 8CLK from the falling edge of the SYNC signal, counter output will be obtained by synchronizing with the falling edge of the next SYNC signal. See the diagram for details on timing.

• **HOLD signal timing**



The HOLD signal setup time (Ths) is the time from the rising edge of the HOLD signal to the falling edge of the DIVOUT signal. The HOLD signal hold time (Thh) is the time from the falling edge of the DIVOUT signal to the rising edge of the HOLD signal. See the above timing diagram for details on the relationship with SYNC POL.

The frequency variation of CLK while held can be calculated as given below.



$C \cdot \Delta V = Q = I_{leak} \cdot Thold$

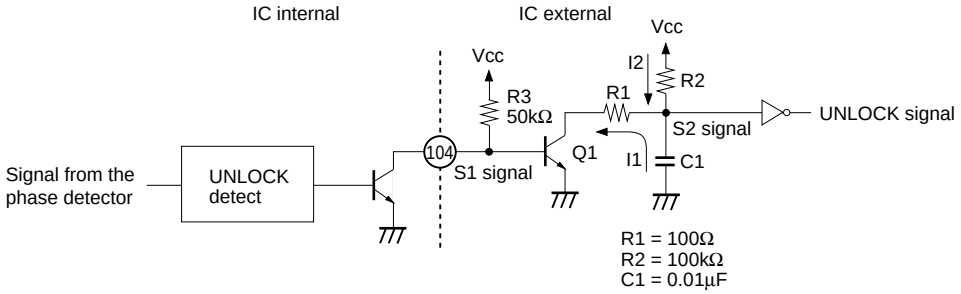
C: Loop filter capacitance
ΔV: Varying voltage due to leak current
I_{leak}: Leak current of the internal amplifier
Thold: Hold time

$\Delta V = Ileak \cdot Thold/C$
$\Delta f = \Delta V \cdot KVCO = I_{leak} \cdot Thold/C \cdot KVCO$

For example,
Assuming f = 100MHz, I_{leak} = 1nA, Thold = 1ms, C = 0.33µF, KVCO = 2π · 55 [MHz/V],
$\Delta V = 1 \cdot 10^{-9} \cdot 1 \cdot 10^{-3}/(0.1 \cdot 10^{-6}) = 3 \cdot 10^{-6}$ [V]
$\Delta f = 1 \cdot 10^{-9} \cdot 1 \cdot 10^{-3}/(0.1 \cdot 10^{-6}) \cdot 2\pi \cdot 70 \cdot 10^{6} = 1050$ [Hz]

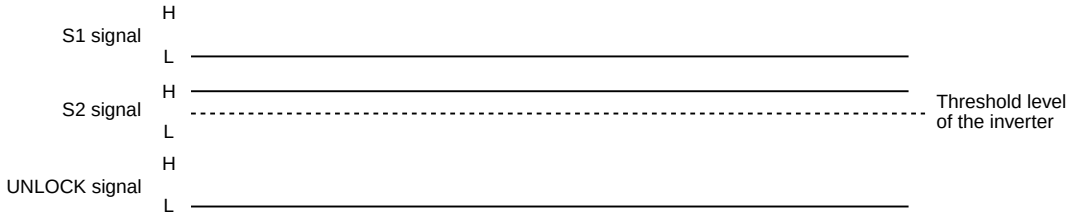
• UNLOCK timing

If the phase difference between the SYNC signal input and the programmable counter output signal to the phase detector (PD) increases, it becomes impossible for the VCO to maintain stable oscillation. This status is converted into the UNLOCK signal and output. It is possible to perform analog lock/unlock by connecting an external circuit to this pin.

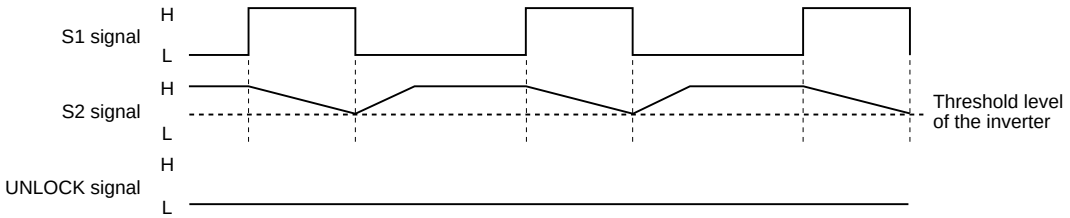


The UNLOCK output is an open collector. By connecting the external circuit shown above to this output pin, it is possible to adjust the sensitivity of the S2 signal by varying the constants R1, R2 and C1. (The constants R1, R2 and C1 above are reference values. The resistor R3 should be 50kΩ and Q1 should be 2SC series. The operations of the three cases are described below.

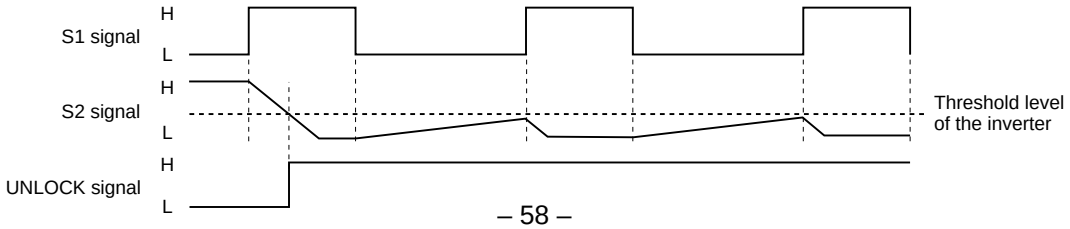
Case 1: When there is no phase difference (PLL locked status)
The S1 signal is low and the S2 signal is high. The UNLOCK signal is low.



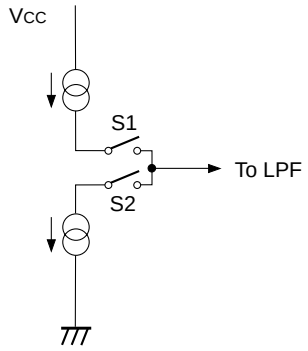
Case 2: When there is a phase difference, the S1 signal will goes low and high as shown in the figure below. At this time, the falling edge slew rate of the S2 signal is determined by the current I1 flowing into this open collector. The falling edge slew rate of the S2 signal will therefore be delayed as resistor R1 increases. In addition, since the rising edge slew rate of the S2 signal is determined by the current I2, the rising edge slew rate of the S2 signal will become faster as the resistor R2 decreases. If the integrated S2 signal does not fall below the threshold level of the next inverter, the UNLOCK signal will remain low. This will therefore be judged as locked even if there is a phase difference.



Case 3: However, even if the same phase difference as described above is assumed, the decreasing resistor R1 will increase the current I1 flowing into the open collector. The falling edge slew rate of the S2 signal will therefore become faster. In addition, if resistor R2 is increased, the rising edge slew rate of the S2 signal will become slower. If the integrated S2 signal is under the threshold level of the next inverter, the UNLOCK signal will go from low to high and the PLL will be judged as unlocked.

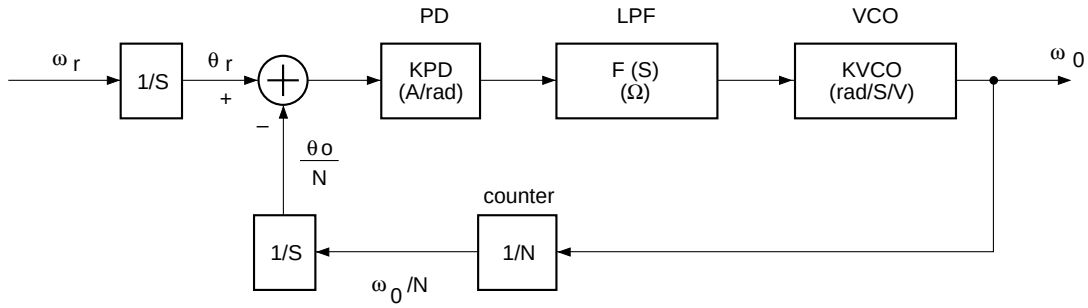


The CXA3506R's charge pump is a constant-current output type as shown below.



When a constant-current output charge pump circuit is used inside the PLL, the phase detector (PD) output acts as a current source, and the dimension of its transmittance KPD is A/rad. Also, when considering the VCO input as a voltage, the LPF transmittance dimension must be expressed in ohms (Ω = V/A).

Therefore, the PLL transmittance when a constant-current output charge pump circuit is used is as follows.



The PLL closed loop transmittance is obtained by the following formula.

$$\frac{\theta o/N}{\theta r} = \frac{KPD \cdot F(S) \cdot KVCO \cdot 1/N \cdot 1/S}{1 + KPD \cdot F(S) \cdot KVCO \cdot 1/N \cdot 1/S} \quad \cdots(1)$$

Here, KPD, F(S) and KVCO are:

KPD: Phase comparator gain (A/rad)
F(S): Loop filter transmittance (Ω)
KVCO: VCO gain (rad/s/V)

*1 The reason for the 1/S inside the phase detector is as follows.

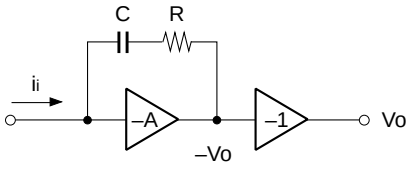
$\theta o\,(t)/N = \int_0^t \omega 0\,(t)/N dt + \theta o\,(t = 0)/N$: (a)
$\theta o\,(t = 0) = 0$
$\theta o\,(t)/N = \int_0^t \omega 0\,(t)/N dt$: (b)

Performing Laplace conversion:

$\theta o\,(S)/N = \frac{1}{S} W_0\,(S)/N$: (c)

The loop filter F(S) is described below.
The loop filter smoothes the output pulse from the phase detector (PD) and inputs it as the DC component to the VCO. In addition to this, however, the loop filter also functions as an important element in determining the PLL response characteristics.
Typical examples of loop filters include lag filters, lag-lead filters, active filters, etc. However, the CXA3506R's LPF is a current input type active filter as shown below, so the following calculations show an actual example of deriving the PLL closed loop transmittance when using this type of filter and then using this transmittance to create a formula for setting the filter constants.

Current input type active filter



The filter transmittance is as follows.

$$\frac{Vo}{A} + Vo = (R + \frac{1}{SC}) \cdot i_i$$

$$F(S) = \frac{1 + SRC}{SC} \cdot \frac{A}{1 + A}$$

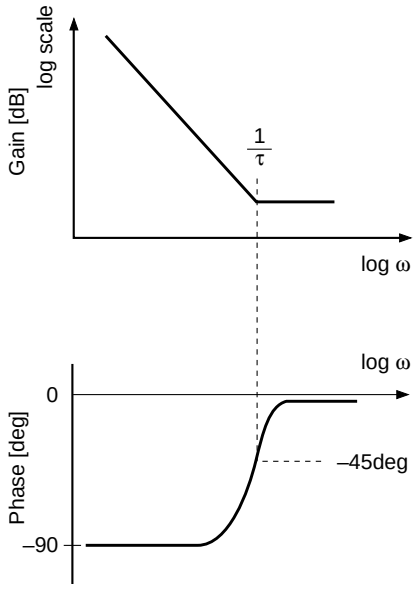
$$= \frac{1 + S\tau}{SC} \cdot \frac{A}{1 + A}$$

$$\therefore \tau = RC$$

Here, assuming A > 1, then:

$$F(S) = \frac{1 + S\tau}{SC} \quad \cdots\cdots\cdots\cdots\cdots\cdots(2)$$

The Bode diagram for formula (2) is as follows.



Next, substituting (2) into (1) and obtaining the overall closed loop transmittance for the PLL:

$$\frac{\theta o/N}{\theta r} = \frac{\frac{KPD \cdot KVCO \cdot \tau}{NC} \cdot S + \frac{KPD \cdot KVCO}{NC}}{S^2 + \frac{KPD \cdot KVCO \cdot \tau}{NC} \cdot S + \frac{KPD \cdot KVCO}{NC}} \quad \cdots(3)$$

$$= \frac{2\zeta\omega nS + \omega n^2}{S^2 + 2\zeta\omega nS + \omega n^2} \quad \cdots\cdots\cdots\cdots\cdots\cdots(4)$$

$$\omega n = \sqrt{\frac{KPD \cdot KVCO}{NC}} \quad \cdots\cdots\cdots\cdots\cdots\cdots(5)$$

$$\zeta = \frac{1}{2} \omega n\tau \cdots\cdots\cdots\cdots\cdots\cdots(6)$$

Here, ωn and ζ are as follows.

ωn characteristic angular frequency:

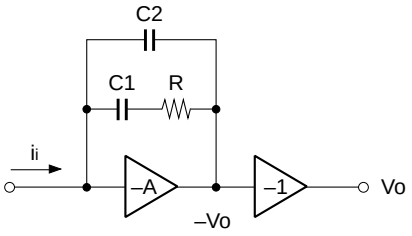
The oscillatory angular frequency when PLL oscillation is assumed to have been maintained by the loop filter and individual loop gains is called the characteristic angular frequency: ωn.

ζ damping factor:

This is the PLL transient response characteristic, and serves as a measure of the PLL stability. It is determined by the loop gain and the loop filter.

A capacitor C2 is added to the actual loop filter.
This added capacitor C2 is used to reduce the R noise, and a value of around 1/10 to 1/1000 of C1 should be selected as necessary.

Current input type active filter with added capacitor C2



The filter transmittance is as follows.

$$F(S) = \frac{1 + C1 \cdot R \cdot S}{S((C1 + C2) + C1 \cdot C2 \cdot R \cdot S)}$$

$$= \frac{1 + \tau 1 \cdot S}{S(C1 + C2)(1 + \tau 2 \cdot S)} \quad \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

$$\tau 1 = C1 \cdot R$$

$$\tau 2 = \frac{C1 \cdot C2 \cdot R}{C1 + C2}$$

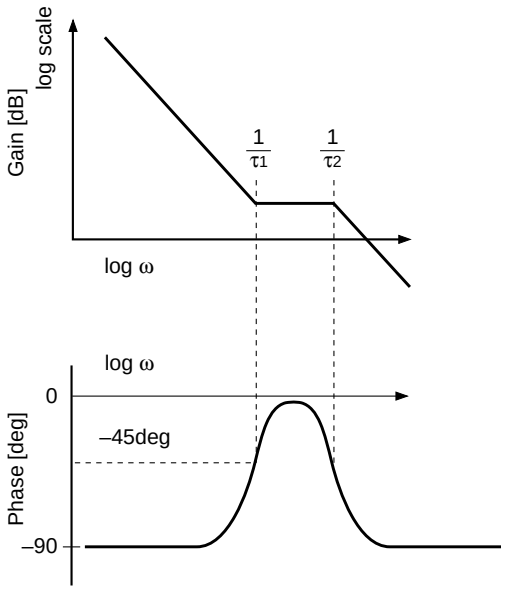
Here, assuming C2 = C1/100, then:

$$\tau 2 = \frac{C1 \cdot C1/100 \cdot R}{C1 + C1/100}$$

$$= \frac{1}{101} \; C1 \cdot R$$

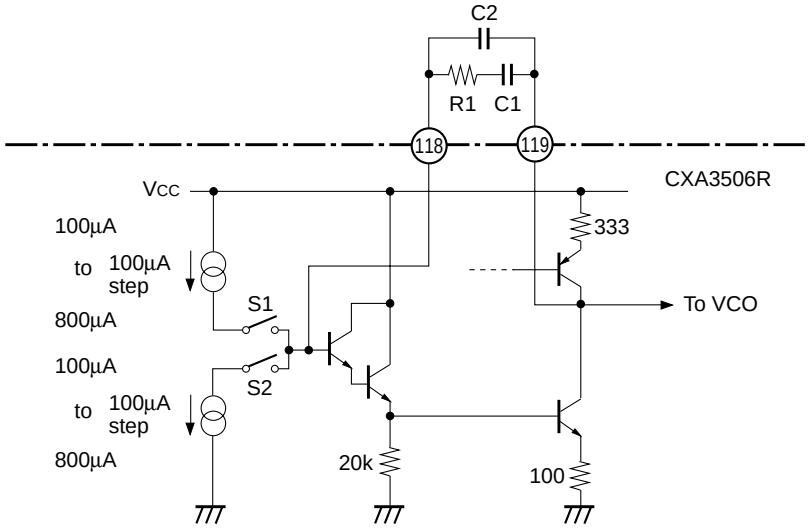
$$= \frac{1}{101} \; \tau 1$$

The Bode diagram for formula (3) is as follows.



Next, the various parameters inside an actual CXA3506R are obtained.

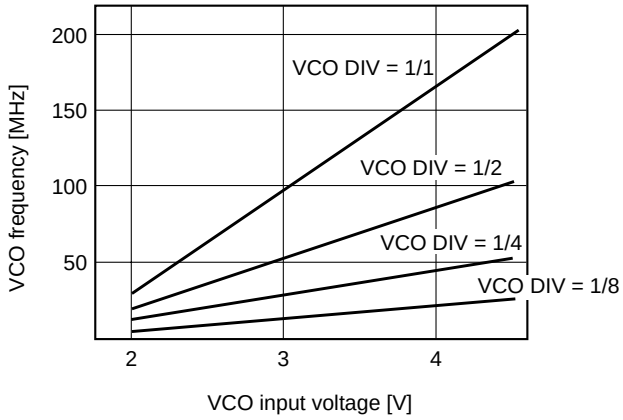
The CXA3506R's charge pump output block and the LPF circuit are as follows.



First, KPD is as follows.

KPD = 100µ/2π or 200µ/2π or 300µ/2π or 400µ/2π or
500µ/2π or 600µ/2π or 700µ/2π or 800µ/2π (A/rad)

Typical KVCO characteristics curves for the CXA3506R's internal VCO are as follows.



Therefore, KVCO is as follows.

KVCO = 2π · 55 or 2π · 27.5 or 2π · 13.75 or 2π · 6.875 (rad/s/V)

ωn and ζ calculated for various types of computer signals are shown below.

Here, the various parameters are as follows.

FSYNC: Input sync frequency, FCLK: Output clock frequency

KPD × 2π: Phase comparator gain × 2π (KPD × 2π = 100 or 200 or 300 or 400 or 500 or 600 or 700 or 800)

KVCO/2π: VCO gain (when VCO DIV = 1/1, KVCO/2π = 55)
(when VCO DIV = 1/2, KVCO/2π = 55/2)
(when VCO DIV = 1/4, KVCO/2π = 55/4)
(when VCO DIV = 1/8, KVCO/2π = 55/8)

N: Counter value, C1: Loop filter capacitance value, R1: Loop filter resistance value

MODE	Resolution	FSYNC	FCLK	KPD × 2π	C.Pump setting			KVCO /2π	DIV 1, 2, 4, 8 setting		N setting	C1	R1	ωn	fn	ζ	VCO oscillation frequency
		kHz	MHz	µA	bit2	bit1	bit0	M/(S*V)	bit1	bit0		µF	kΩ	kHzrad	kHz		MHz
NTSC		15.73	12.27	300	0	1	0	55/8	1	1	780	0.33	3.3	2.83	0.45	1.54	98.18
NTSC		15.73	18.41	200	0	0	1	55/4	1	0	1170	0.33	3.3	2.67	0.42	1.45	73.64
NTSC		15.73	24.55	300	0	1	0	55/4	1	0	1560	0.33	3.3	2.83	0.45	1.54	98.18
NTSC		15.73	27.00	300	0	1	0	55/4	1	0	1716	0.33	3.3	2.70	0.43	1.47	108.00
PAL		15.63	14.69	200	0	0	1	55/4	1	0	940	0.33	3.3	2.98	0.47	1.62	58.75
PAL		15.63	22.03	300	0	1	0	55/4	1	0	1410	0.33	3.3	2.98	0.47	1.62	88.13
PAL		15.63	29.38	400	0	1	1	55/4	1	0	1880	0.33	3.3	2.98	0.47	1.62	117.50
PAL		15.63	27.00	300	0	1	0	55/4	0	1	1728	0.33	3.3	2.69	0.43	1.46	108.00
480p		31.47	72.00	500	1	0	0	55/2	0	1	2288	0.33	3.3	4.27	0.68	2.32	144.01
1080i		33.75	74.25	500	1	0	0	55/2	0	1	2200	0.33	3.3	4.35	0.69	2.37	148.50
720p		45.00	74.25	500	1	0	0	55/2	0	1	1650	0.33	3.3	5.03	0.80	2.74	148.50
PC-98	640 × 400	24.82	21.05	200	0	0	1	55/4	1	0	848	0.33	3.3	3.13	0.50	1.71	84.19
VGA	640 × 480	31.47	25.18	300	0	1	0	55/4	1	0	800	0.33	3.3	3.95	0.63	2.15	100.70
MAC	640 × 480	35.00	30.24	400	0	1	1	55/4	1	0	864	0.33	3.3	4.39	0.70	2.39	120.96
VESA	640 × 480	37.86	31.50	400	0	1	1	55/4	1	0	832	0.33	3.3	4.48	0.71	2.44	126.00
SVGA	800 × 600	35.16	36.00	500	1	0	0	55/4	1	0	1024	0.33	3.3	4.51	0.72	2.46	144.02
SVGA	800 × 600	37.88	40.00	600	1	0	1	55/4	1	0	1056	0.33	3.3	4.87	0.77	2.65	160.01
SVGA	800 × 600	46.88	49.51	300	0	1	0	55/2	0	1	1056	0.33	3.3	4.87	0.77	2.65	99.01
SVGA	800 × 600	48.08	50.00	300	0	1	0	55/2	0	1	1040	0.33	3.3	4.90	0.78	2.67	100.01
SVGA	800 × 600	53.67	56.25	400	0	1	1	55/2	0	1	1048	0.33	3.3	5.64	0.90	3.07	112.49
MAC	832 × 624	49.72	57.28	400	0	1	1	55/2	0	1	1152	0.33	3.3	5.38	0.86	2.93	114.55
XGA	1024 × 768	48.36	65.00	400	0	1	1	55/2	0	1	1344	0.33	3.3	4.98	0.79	2.71	129.99
XGA	1024 × 768	56.48	75.01	500	1	0	0	55/2	0	1	1328	0.33	3.3	5.60	0.89	3.05	150.01
XGA	1024 × 768	60.02	78.75	600	1	0	1	55/2	0	1	1312	0.33	3.3	6.17	0.98	3.36	157.49
MAC	1024 × 768	60.24	80.00	600	1	0	1	55/2	0	1	1328	0.33	3.3	6.14	0.98	3.34	160.00
XGA	1024 × 768	68.68	94.50	300	0	1	0	55/1	0	0	1376	0.33	3.3	6.03	0.96	3.28	94.50

• CP setting matrix

Internal VCO oscillation frequency: CP setting value

40MHz to 85MHz: 200µA
85MHz to 110MHz: 300µA
110MHz to 140MHz: 400µA
140MHz to 155MHz: 500µA
155MHz to 165MHz: 600µA

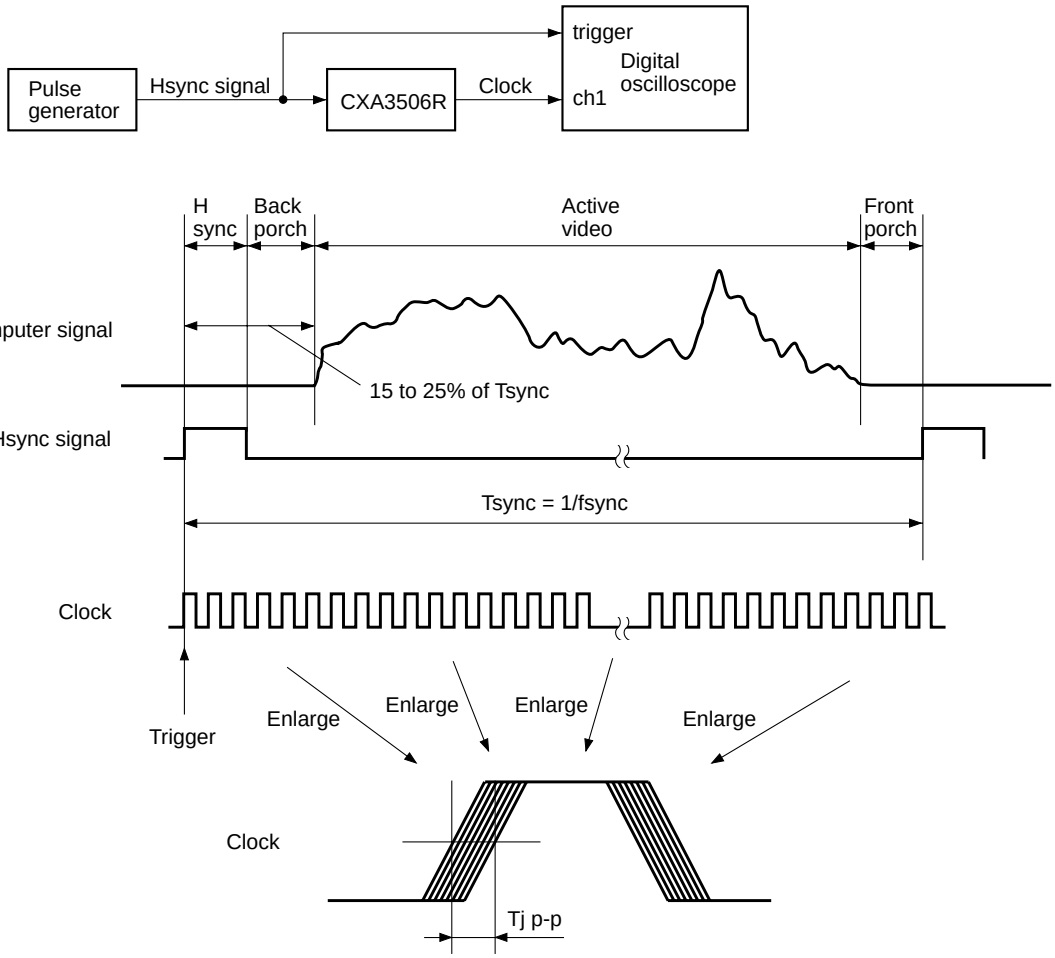
• DIV setting matrix

Output oscillation frequency: DIV setting value

5MHz to 14MHz: 1/8
14MHz to 40MHz: 1/4
40MHz to 80MHz: 1/2
80MHz to 120MHz: 1/1

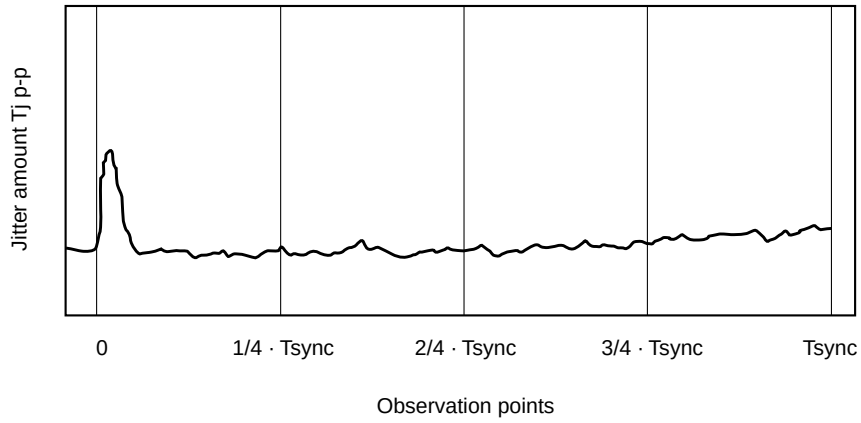
CLK Jitter Evaluation Method

The generated CLK is obtained by inputting Hsync to the CXA3506R. Apply this CLK to a digital oscilloscope and observe the CLK waveform using Hsync as the trigger.



The CLK jitter is measured at peak to peak in the long-term write mode of the digital oscilloscope as shown in the figure. The CLK jitter size varies according to the difference in the relative position with respect to Hsync. Therefore, when the observation point is changed, the CLK jitter at that point is observed.

The figure below shows a typical example of the CLK jitter for the CXA3506R.
The CLK jitter increases slightly at the rising edge of Hsync (in the case of positive polarity), and then settles down thereafter. However, this is not a problem as the active pixels start after about 20% of the H cycle has passed from the rising edge of Hsync.



A/D Converter

- **Analog input signal**

The RGB analog input signal and YCbCr analog input signal are converted to digital signals and output. Be sure to adjust the input dynamic range of the ADC in the pre-stage amplifier block by performing contrast and brightness settings for the analog signal input to the ADC. (See the item on the amplifier for details on the setting procedure.)

- **Sampling clock**

Although the sampling clock is created by a PLL (internal CLK), it is also possible to externally input a clock to the ADC (external CLK) directly for checking ADC operations. In this case, be sure to make the register settings below in order to input a PECL level clock from the CLKIN (Pin 110) and the XCLKIN (Pin 109).

Register: VCO By-pass	0	1
ADC clock	External CLK	Internal CLK

Note, however, that even if an external CLK is input under the above settings, it is impossible to run the ADC at the input clock frequency unless the PLL's VCO frequency divider is set to 1/1. Running the ADC on an external CLK is done in order to check the operations of the ADC. Normally, it should be run on the internal CLK generated by the PLL.

- **Reference voltage**

The input dynamic range of the ADC is determined based on the reference voltage from the VRT (Pin 17) and the VRB (Pin 93). Since this reference voltage is created using an internal band gap voltage, there is no need for an external reference voltage circuit. The voltage at the VRT pin is set to a voltage approximately 0.4V lower than the voltage coming from the AV$_{CC}$AD3 power pin. Also, the VRB pin is set to a voltage approximately 1.0V lower than that at the VRT pin.

Capacitors of 1µF or more should be connected between the AV$_{CC}$AD3 power supply pins for these reference voltage pins (VRT pin and VRB pin).

If the value of the capacitor is too low or no capacitor is attached, the reference voltage circuit will cause an oscillation that results in noise or malfunction because the ADC faithfully samples this oscillation.

It is impossible to apply an external voltage to a reference voltage pin. Note that it is also impossible to use the voltage generated by a reference voltage pin as an external voltage source.

- **Operational mode**

The ADC output data of this IC supports five types of operational mode. Each operational mode is set by using a control register.

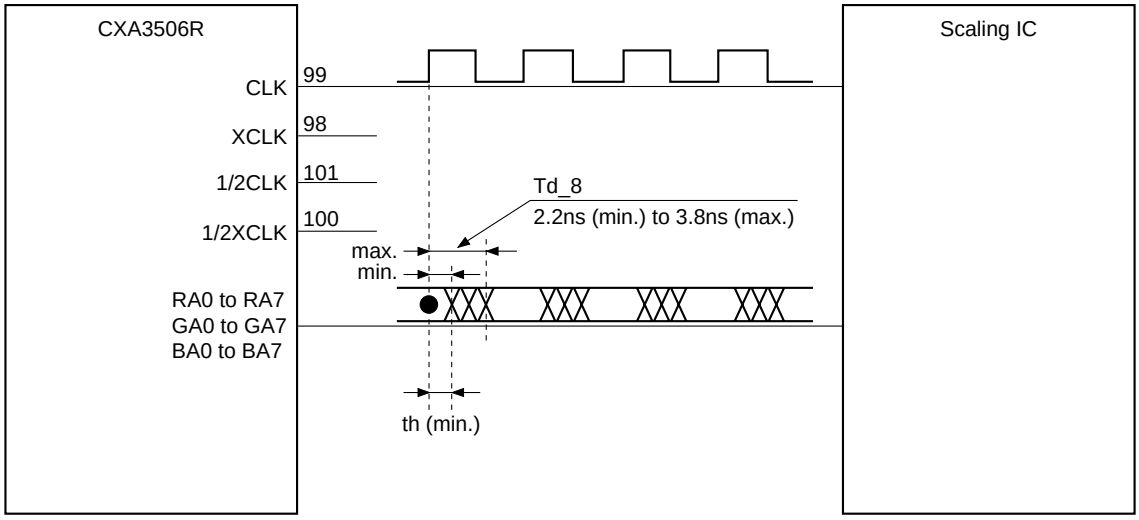
	Register: DATA OUT MODE		
	D3	D2	D1
Straight Data out Mode	0	0	0
DMUX Parallel Data out Mode	0	0	1
DMUX Interleaved Data out Mode	0	1	0
4:2:2 Data out D2 Mode	0	1	1
4:2:2 Data out special Mode	1	1	1

For a description of each operational mode, see the next page.

• **Description of the operational modes**

(Straight Data out Mode)

An RGB analog input signal AC coupled is optimized by using a 3-ch AMP and the signal is input to the ADC.
The analog input signal input to the ADC is sampled by using a clock generated by the PLL.
The identical signal with the sampling clock for analog input signal is output from the CLK (Pin 99).
The sampled analog input signal is output from the port A side of the data output with a 3-clock pipeline delay. Note that output for port B side is turned off at this time and cannot be set to high impedance.
The ADC data output is output with a propagation delay (Td_8) ranges from 2.2ns (min.) to 3.8ns (max.) versus the clock output from the CLK pin.
The operational frequency in Straight Data out Mode is 100MHz at the sampling clock frequency.
Also, note, when operating in Straight Data out Mode, that the output on the port B side (RB0 to RB7, GB0 to GB7, and BB0 to BB7) is turned off and cannot be set to high impedance.
All TTL output are set to high impedance only when this IC is put into power save mode.
The following type of interface is possible when this IC is operated in Straight Data out Mode.

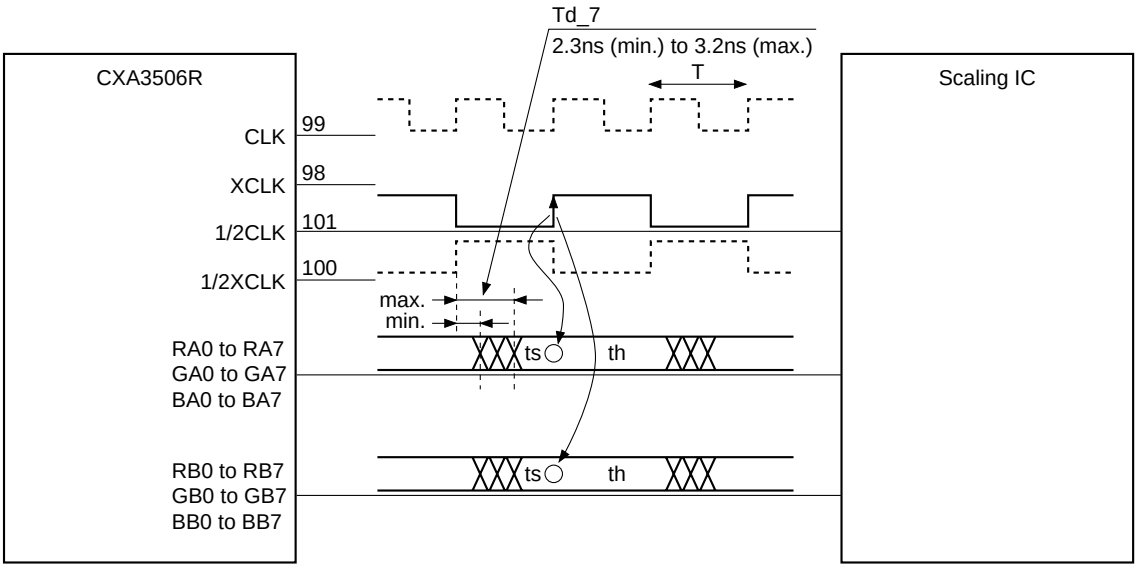


The hold time of the post-stage scaling IC using the interface shown above is,

th (min.) = 2.2ns

(DMUX Parallel Data out Mode)

The RGB analog input signal AC coupled is optimized by using a 3-ch AMP and the signal is input to the ADC.
The analog signal input to the ADC is sampled by using a clock generated by the PLL.
The identical signal with the sampling clock for analog input signal is output from the CLK (Pin 99). At each clock cycle, sampled data is divided into pins in port A side and port B side.
The data output on the port A side possesses a 3-clock pipeline delay versus the sampling clock, while the data output on the port B side possesses a 2-clock pipeline delay.
The output timing is the same for data output from both ports. Data is maintained for two cycles (2T) of the sampling clock.
ADC data is output with a propagation delay (Td_7) ranges from 2.3ns (min.) to 3.2ns (max.) versus the clock output from the 1/2XCLK (Pin 100).
An interface of the following type is possible when this IC is run in DMUX Parallel Data out Mode.



With the interface shown above, the post-stage scaling IC acquire data by using the clock signal output from the 1/2CLK pin of the ADC.
In case of this interface, the setup time of the post-stage scaling IC is,

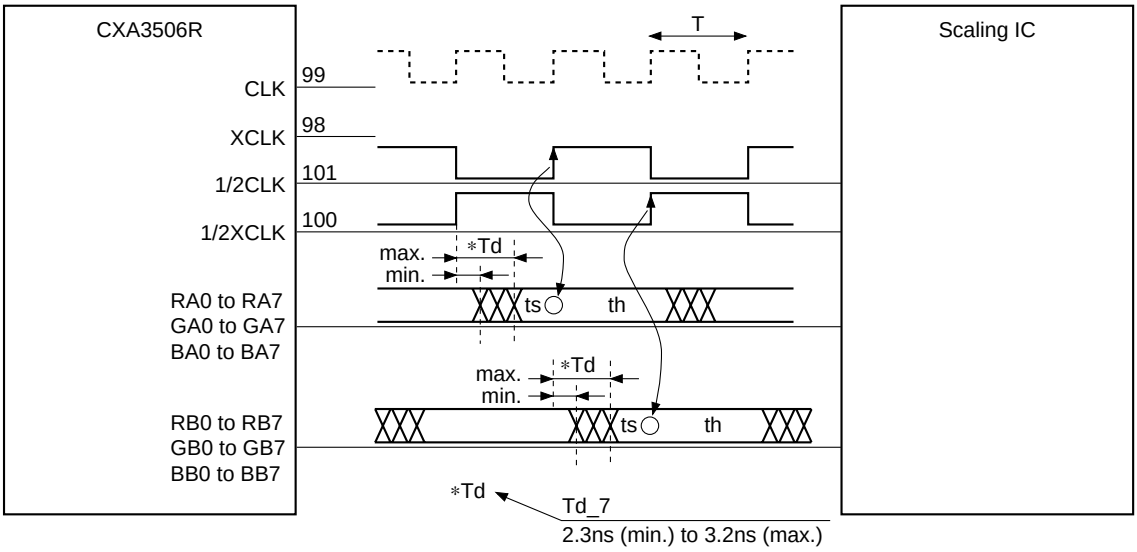
ts (min.) = T – 3.2ns

While the hold time is,

th (min.) = T + 2.3ns

(DMUX Interleaved Data out Mode)

The RGB analog input signal AC coupled is optimized by using a 3-ch AMP and the signal is input to the ADC.
The analog signal input to the ADC is sampled by using a clock generated by the PLL.
The identical signal with the sampling clock for analog input signal is output from the CLK (Pin 99). At each clock cycle, sampled data is divided into pins in port A and port B.
The data output on the port A side possesses a 2-clock pipeline delay versus the sampling clock, while the data output on the port B side also possesses a 2-clock pipeline delay.
Although the data output from both ports is maintained for two cycles (2T) of the sampling clock, there is one cycle (T) difference between the output timing for port A side and port B side.
Data output on port A side possesses a propagation delay (Td_7) ranges from 1.3ns (min.) to 2.2ns (max.) versus the clock output from the 1/2XCLK (Pin 100), while data output on port B side possesses a propagation delay (Td_1/2clk to data) ranges from 2.3ns (min.) to 3.2ns (max.) versus the clock output from the 1/2CLK (Pin 101).
An interface of the following type is possible when this IC is run in DMUX Interleaved Data out Mode.



With the interface shown above, port A data is acquired into the post-stage scaling IC by using the clock signal output from the 1/2CLK pin of the ADC, while port B data is acquired by using the clock signal output from the 1/2XCLK pin.
In case of this interface, the setup time of the post-stage scaling IC is,

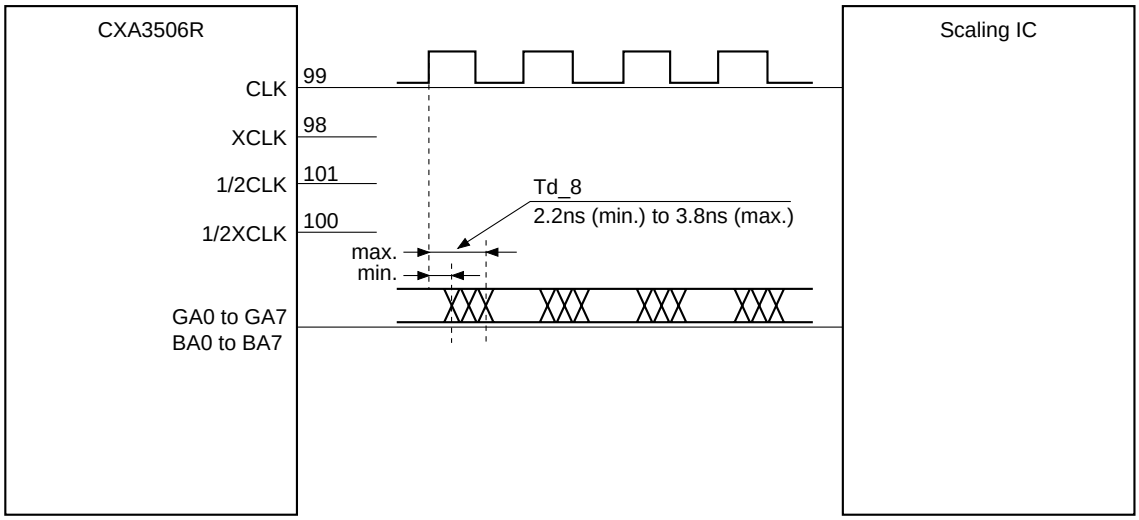
ts (min.) = T – 3.2ns

While the hold time is,

th (min.) = T + 2.3ns

(4:2:2 Data out D2 Mode)

The YCbCr analog input signal AC coupled is optimized by using a 3-ch AMP and the signal is input to the ADC.
The analog signal input to the ADC is sampled by using a clock generated by the PLL.
The identical signal with the sampling clock for analog input signal is output from the CLK (Pin 99).
In 4:2:2 Data out D2 Mode, the only Y signal is A/D converted just as in Straight Data out Mode and output to the data output ports GA0 to GA7. The Cb and Cr signals are all simultaneously A/D converted at a half sampling rate compared with the Y signal, then multiplexed within the IC, and output to the data output ports BA0 to BA7 in the order U (Cb) and V (Cr).
When the SYNC ON Y signal is input, it is necessary to separate out the SYNC signal superimposed on the signal. See the operational description of SYNCSEP for details.
Data output of ADC possesses a propagation delay (Td_8) ranges from 2.2ns (min.) to 3.8ns (max.) versus the clock output from the CLK pin.
The operating frequency in 4:2:2 Data out D2 Mode is 100MHz as the sampling clock frequency.
Although RA0 to RA7, RB0 to RB7, GB0 to GB7, and BB0 to BB7 are all put into output off mode when the IC operates in 4:2:2 Data out D2 Mode, they cannot be set to high impedance.
All TTL output is set to high impedance when this IC is put into power save mode.
An interface of the following type is possible when this IC is run in 4:2:2 Data out D2 Mode.

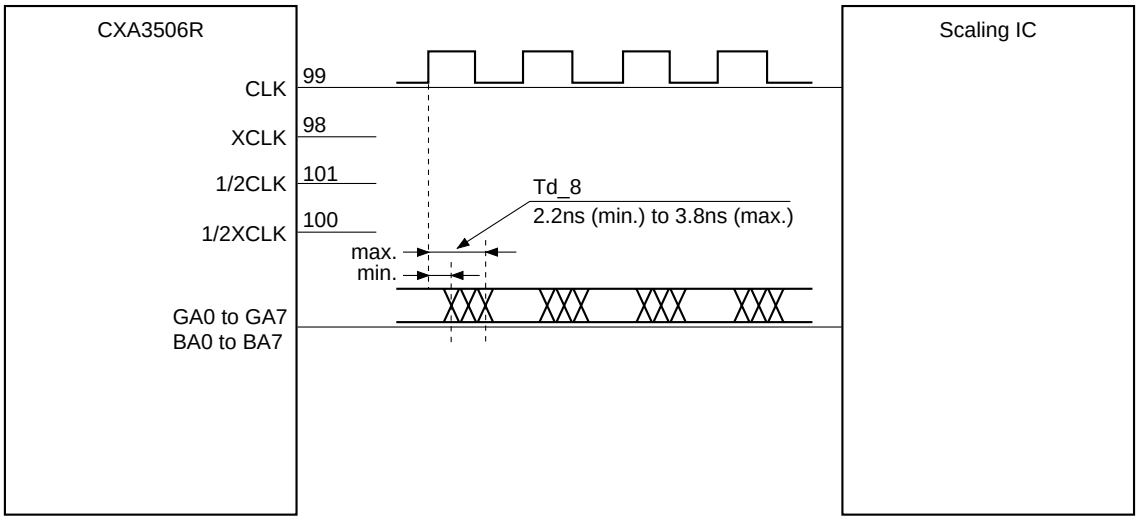


The hold time of the post-stage scaling IC using the interface shown above is,

th (min.) = 2.2ns

(4:2:2 Data out special Mode)

The YCbCr analog input signal AC coupled is optimized by using a 3-ch AMP and the signal is input to the ADC.
The analog input signal to the ADC is sampled by using a clock generated by the PLL.
The identical signal with the sampling clock for analog input signal is output from the CLK (Pin 99).
In 4:2:2 Data out special Mode, the only Y signal is A/D converted just as in Straight Data out Mode and output to the data output ports GA0 to GA7. The Cb and Cr signals are A/D converted at every other sampling at a half sampling rate of the Y signal, then multiplexed within the IC, and output to the data output ports BA0 to BA7 in the order U (Cb) and V (Cr).
When the SYNC ON Y signal is input, it is necessary to separate out the SYNC signal superimposed on the signal. See the operational description of SYNCSEP for details.
ADC data output possesses a propagation delay (Td_8) ranges from 2.2ns (min.) to 3.8ns (max.) versus the clock output from the CLK pin.
The operating frequency in 4:2:2 Data out special Mode is 100MHz as the sampling clock frequency.
In addition, although RA0 to RA7, RB0 to RB7, GB0 to GB7, and BB0 to BB7 are all put into output off mode when the IC operates in 4:2:2 Data out Special Mode, they cannot be set to high impedance.
All TTL output is set to high impedance when this IC is put into power save mode.
An interface of the following type is possible when this IC is run in 4:2:2 Data out D2 Mode.



The hold time of the post-stage scaling IC using the interface shown above is,

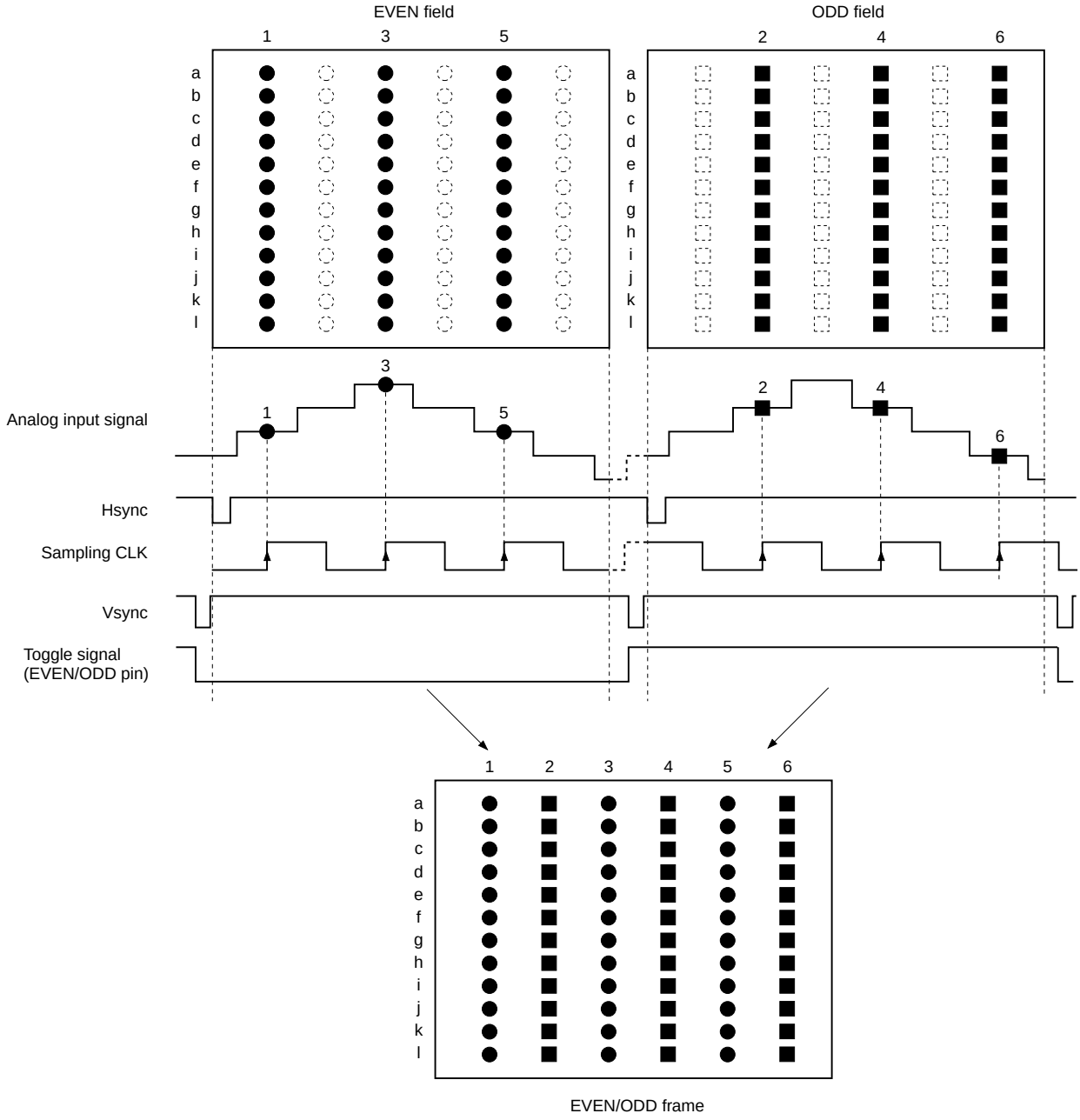
th (min.) = 2.2ns

• **EVEN/ODD function**

When a toggle signal created by dividing the Vsync signal in half is input to the EVEN/ODD (Pin 108), the ADC sampling clock is inverted every Vsync signal.
This function can be used to configure a single frame screen from two fields by AD converting an RGB analog input signal that requires high speed and high resolution, such as a UXGA 60Hz (162MHz) or more signal, at half the frequency of the original ADC sampling rate.
There are no particular control register settings when using the EVEN/ODD function. The sampling clock is inverted based on the polarity of the signal input to the EVEN/ODD pin. Be sure to input signal to the EVEN/ODD pin at TTL level.

EVEN/ODD pin	L	H
Operational mode	EVEN	ODD

Example of Using the EVEN/ODD Function



TTL Output High Level Setting

All the TTL output pins can be set to high level by the control register.
All the TTL output pins are set simultaneously.
The TTL output pins are as follows.
RA7 to RA0, RB7 to RB0, GA7 to GA0, GB7 to GB0, BA7 to BA0, BB7 to BB0,
SEROUT, SOGOUT, Delay Sync Output, 1/2CLK, 1/2XCLK, CLK and XCLK

Register: TTLOUT CLP	00	01	10	11
High level (typ.)	2.2V	2.45V	2.7V	2.95V

The TTL output can be input directly to a 3V power supply IC without level conversion.
Set high level in accordance with the supply voltage.

Power Save

1) Power save for all functions

All functions of the chip can be stopped to save power by the XPOWER SAVE (Pin 6). The control register is also set to power save mode at this time.

XPOWER SAVE pin	L	H
Operating status	Power save	Power on

The pin input level is TTL level.

2) Power save every block by using the control register

The blocks except the registers can also be set to power save mode by the control register.
Selects according to using state.

Register	0	1
ADC Power Save	Power on	Power save
AMP Power Save	Power on	Power save
PLL Power Save	Power on	Power save
SYNC SEP Power Save	Power on	Power save

TTL Output Mode during Power Save Mode

All TTL output pins are set to high impedance when the IC is put into power save mode.
Since this IC supports power on reset, AMP, ADC, PLL, and SYNCSEP are set to power save mode when power is turned on and all TTL output pins are set to high impedance.
However, note that the TTL output pins don't change into high impedance, when control register are used to set each TTL output disable mode separately. Even though there are also modes in which data output ports are set to output off mode based on the ADC operational mode, it cannot be set to high impedance.

ADC Data Output Modes

	XPOWER SAVE mode	ADC Power Save mode	Straight mode	DMUX Parallel mode	DMUX Interleaved mode	YUV 4:2:2 D2 mode	YUV 4:2:2 Special mode
RA7 to 0	Hi-Z	Hi-Z	DATA	DATA	DATA	—*	—*
RB7 to 0	Hi-Z	Hi-Z	—*	DATA	DATA	—*	—*
GA7 to 0	Hi-Z	Hi-Z	DATA	DATA	DATA	DATA	DATA
GB7 to 0	Hi-Z	Hi-Z	—*	DATA	DATA	—*	—*
BA7 to 0	Hi-Z	Hi-Z	DATA	DATA	DATA	DATA	DATA
BB7 to 0	Hi-Z	Hi-Z	—*	DATA	DATA	—*	—*

Other TTL Output Pin Modes

	XPOWER SAVE mode	PLL Power Save mode	CLK Disable	XCLK Disable	1/2CLK Disable	1/2XCLK Disable	DSYNC Disable	SOGOUT Disable	SEROUT Disable	UNLOCK Disable
CLK	Hi-Z	Hi-Z	—*	Signal	Signal	Signal	Signal	Signal	Signal	Signal
XCLK	Hi-Z	Hi-Z	Signal	—*	Signal	Signal	Signal	Signal	Signal	Signal
1/2CLK	Hi-Z	Hi-Z	Signal	Signal	—*	Signal	Signal	Signal	Signal	Signal
1/2XCLK	Hi-Z	Hi-Z	Signal	Signal	Signal	—*	Signal	Signal	Signal	Signal
DSYNC/ DIVOUT	Hi-Z	Hi-Z	Signal	Signal	Signal	Signal	—*	Signal	Signal	Signal
SOGOUT	Hi-Z	Hi-Z	Signal	Signal	Signal	Signal	Signal	—*	Signal	Signal
SEROUT	Hi-Z	Hi-Z	Signal	Signal	Signal	Signal	Signal	Signal	—*	Signal
UNLOCK	Hi-Z	Hi-Z	Signal	Signal	Signal	Signal	Signal	Signal	Signal	—*

* A dash (–) indicates output off status that cannot be set to high impedance.

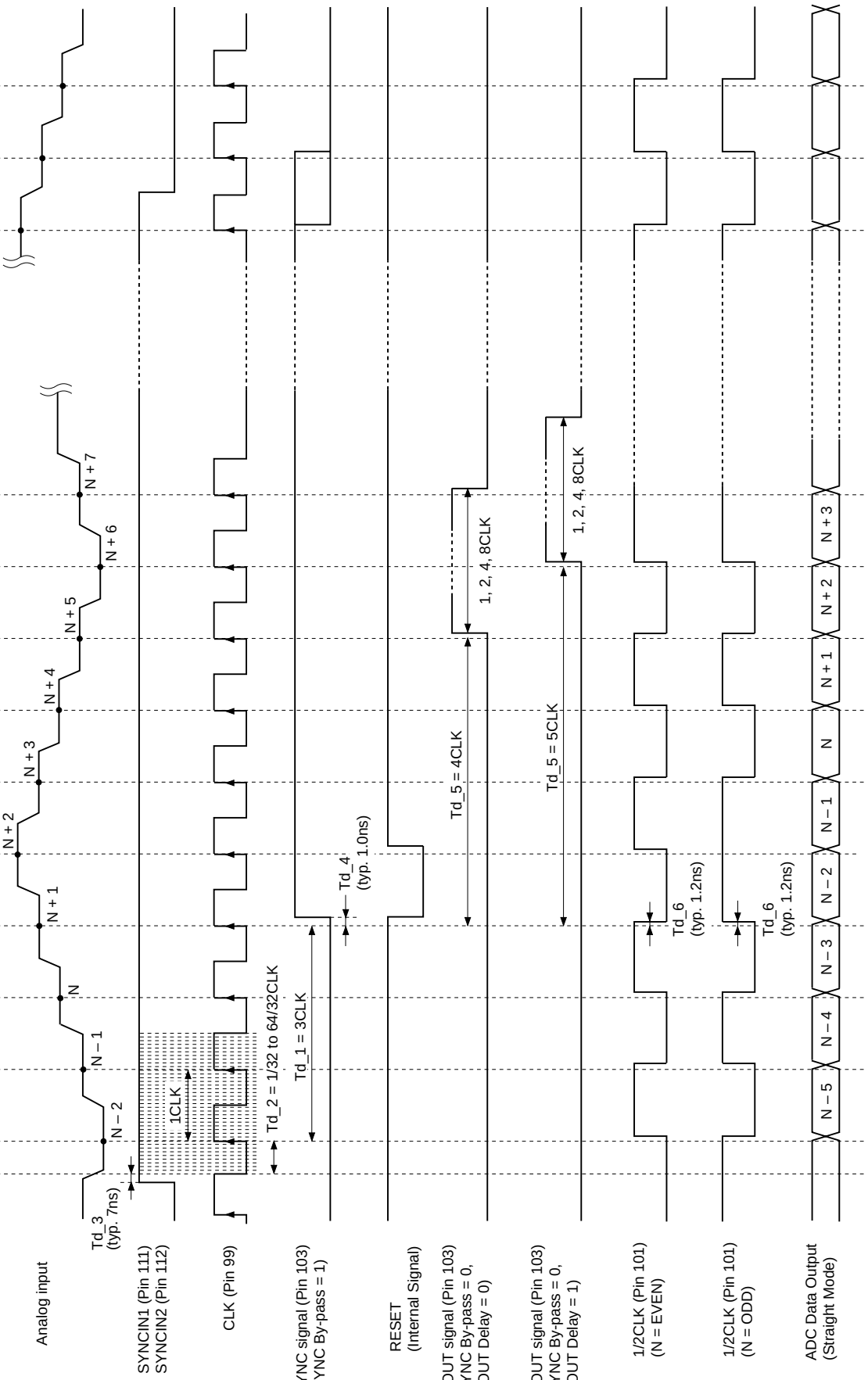
Supply Current

The default value for the current consumption and the control register-based power save current (I_{CC5PS}, I_{CC3PS}), and power save current (I_{CC5XPS}, I_{CC3XPS}) when the XPOWER SAVE function is used, are indicated to each block as follows.
(The current consumption values given here are the typical values for when the IC is run at a clock frequency of 80MSPS.)

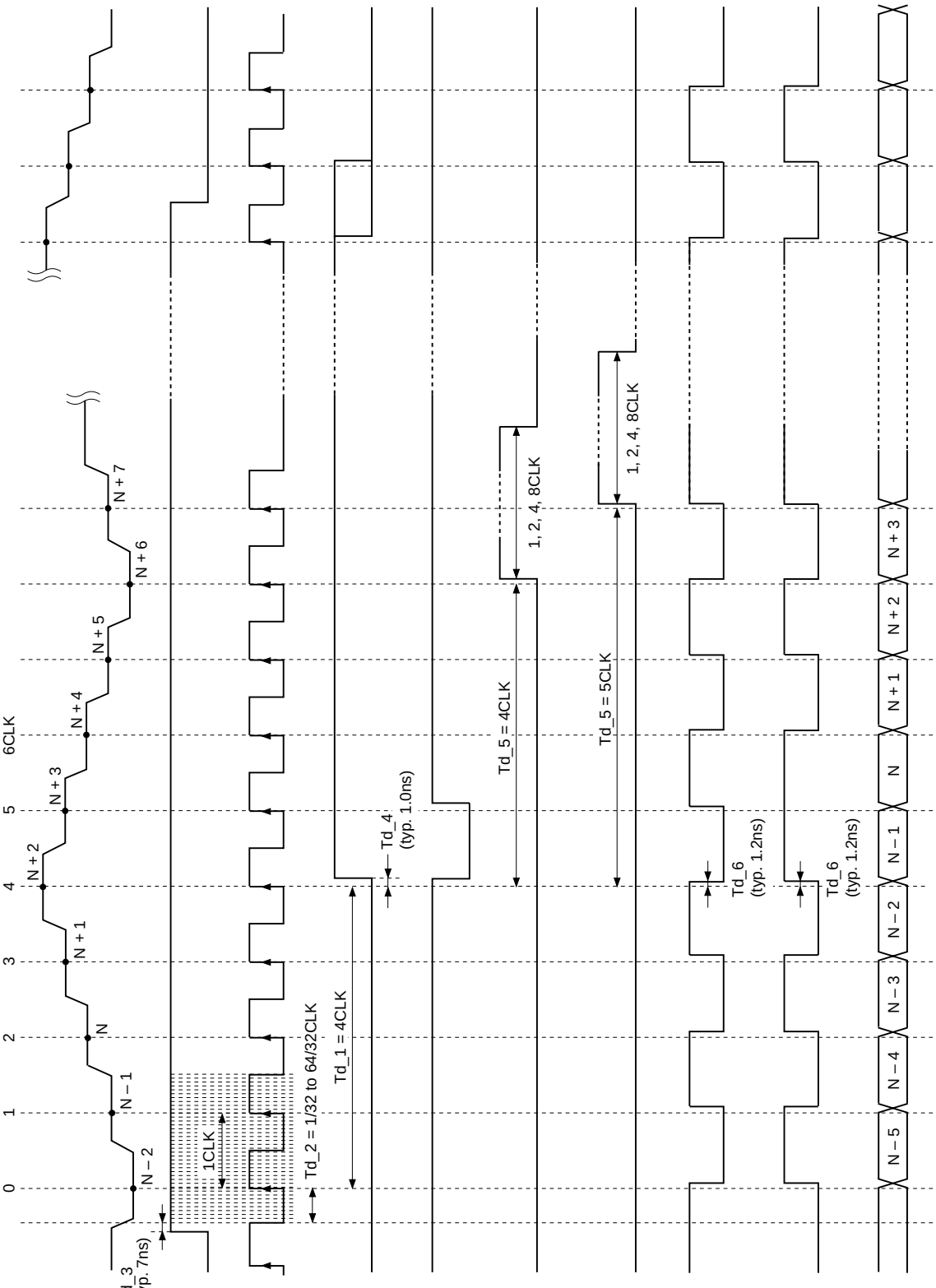
Block	Supply pin names	Supply voltage	Current consumption (typ.)	Register PS current consumption	XPS current consumption
Register	$DV_{CC}REG$	5V (D)	17.2mA	17.2mA	1.2mA
AMP (SYNCSEP)	$AV_{CC}AMP^*$	5V (A)	80.0mA	0.7mA	0.7mA
PLL	$AV_{CC}VCO$ + $AV_{CC}IR$	5V (A)	16.0mA	0mA	0mA
	$DV_{CC}PLL$ + $DV_{CC}PLLTTL$	5V (D)	41.4mA	2.0mA	1.0mA
ADC	$AV_{CC}ADREF$	5V (A)	6.8mA	0.4mA	0.4mA
	$DV_{CC}AD$ + $DV_{CC}ADTTL$	5V (D)	73.2mA	6.0mA	6.0mA
	$AV_{CC}AD3$ + $DV_{CC}AD3$	3.3V (A)	180mA	3.0mA	3.0mA

$AV_{CC}AMP^*$ = $AV_{CC}AMPR$ + $AV_{CC}AMPG$ + $AV_{CC}AMPB$

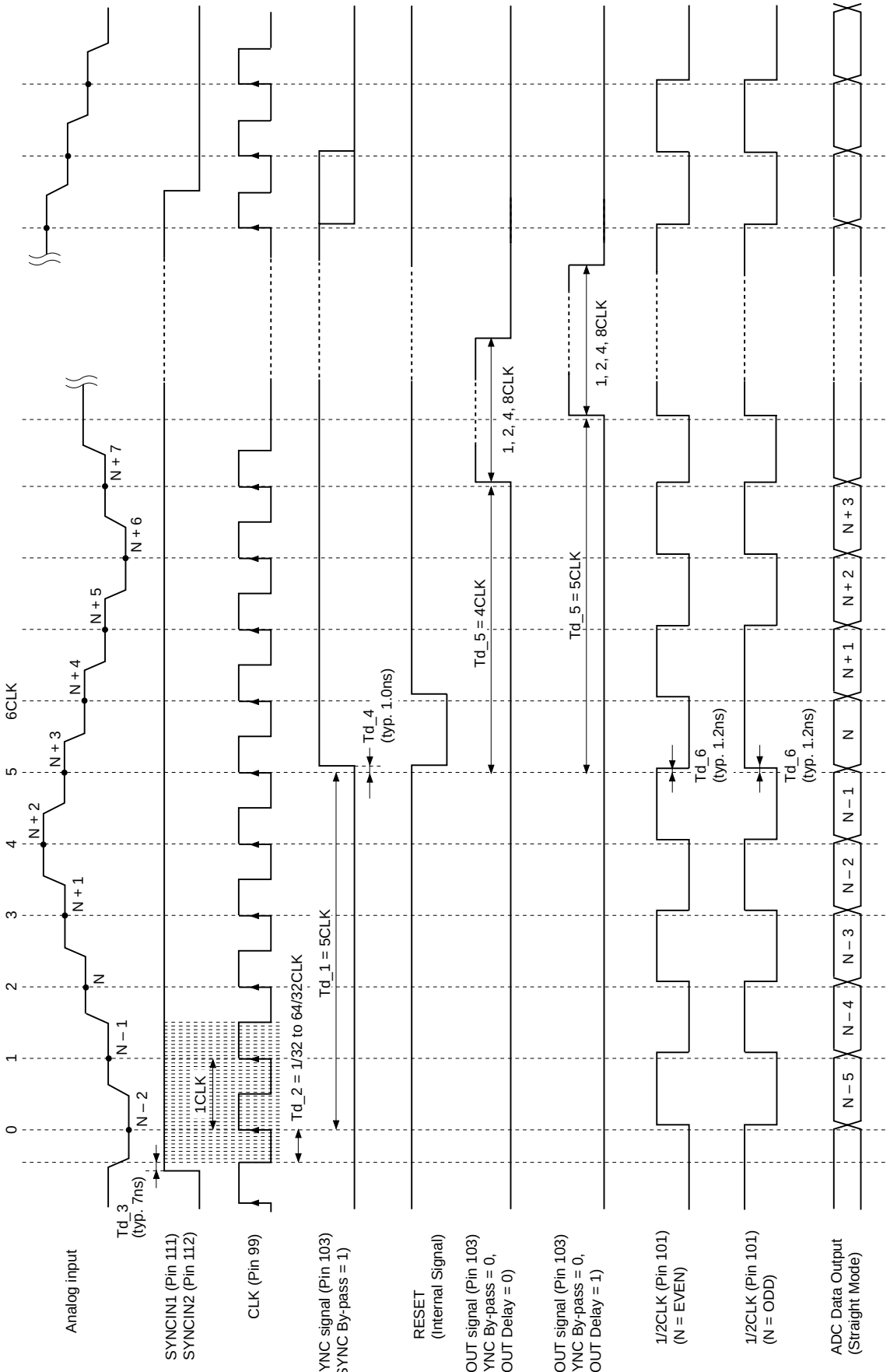
PLL Timing Chart (Td1 = 3CLK)



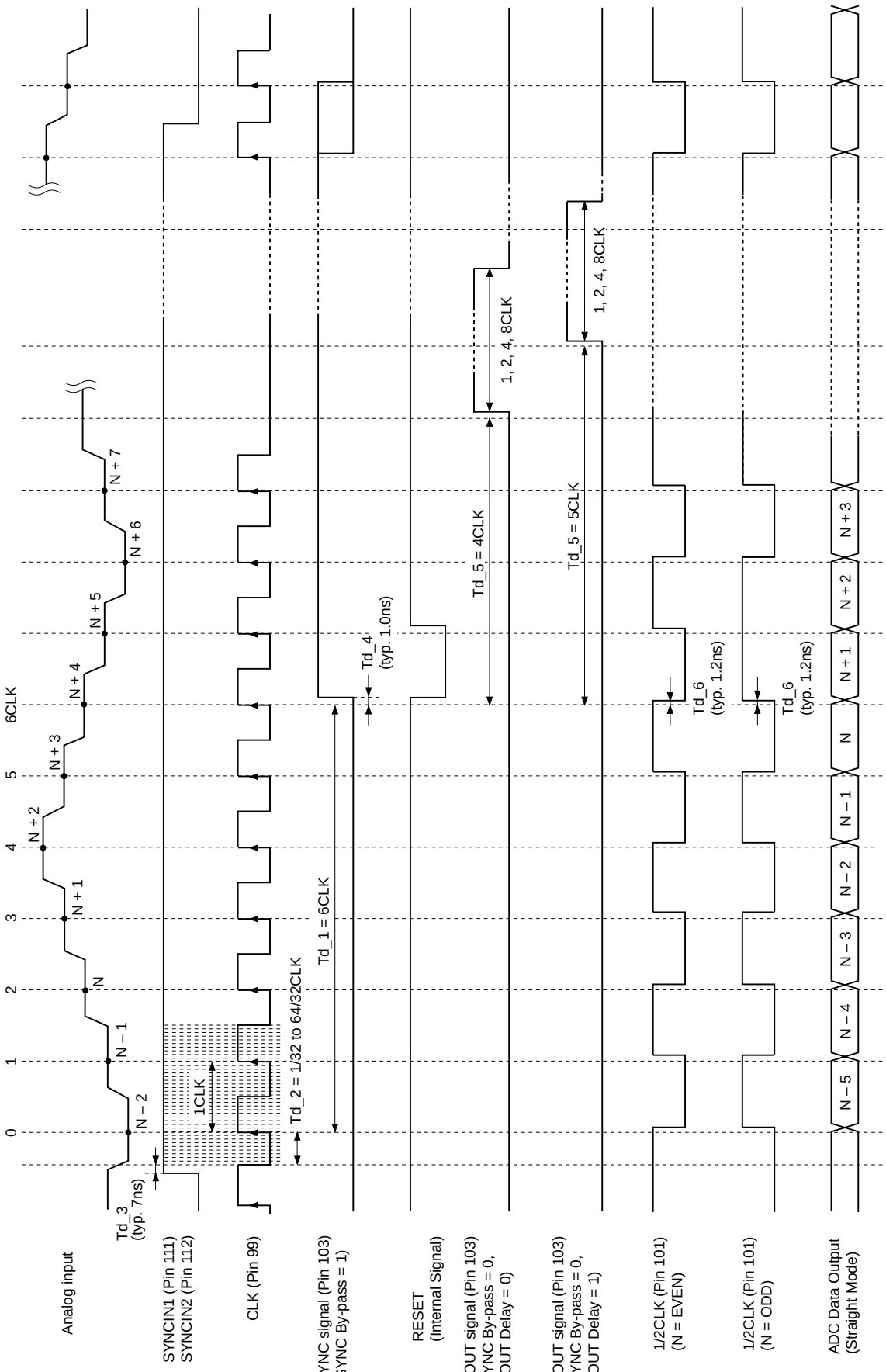
PLL Timing Chart (Td1 = 4CLK)



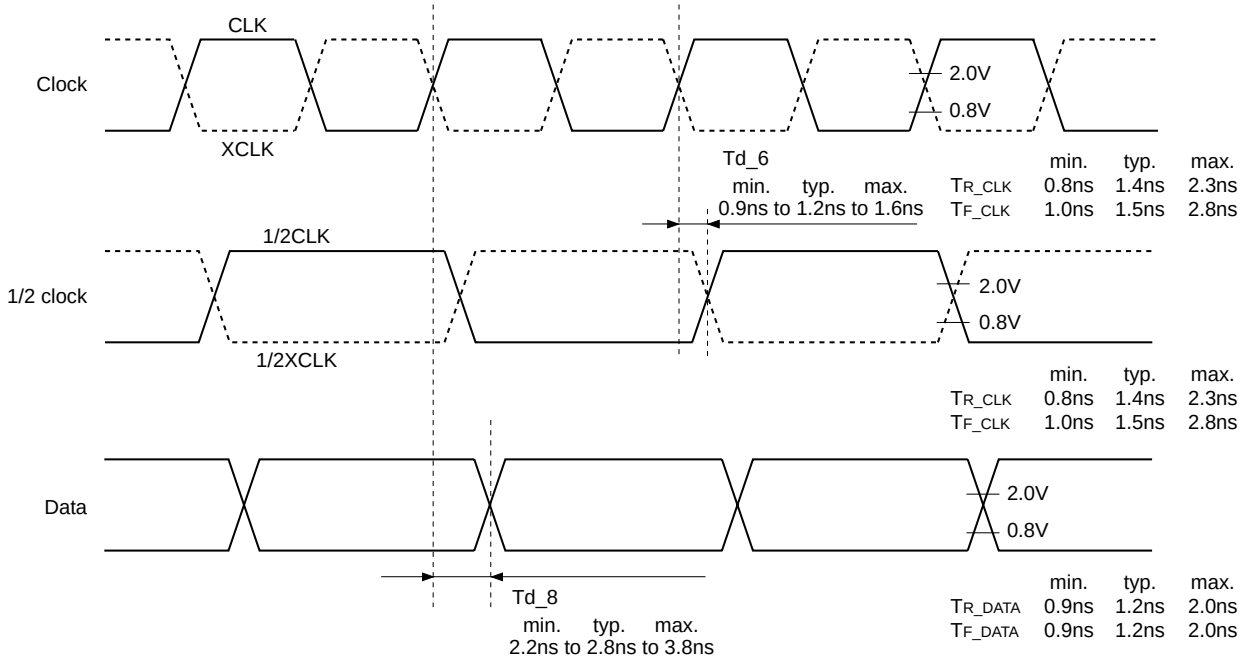
PLL Timing Chart (Td1 = 5CLK)



PLL Timing Chart (Td1 = 6CLK)

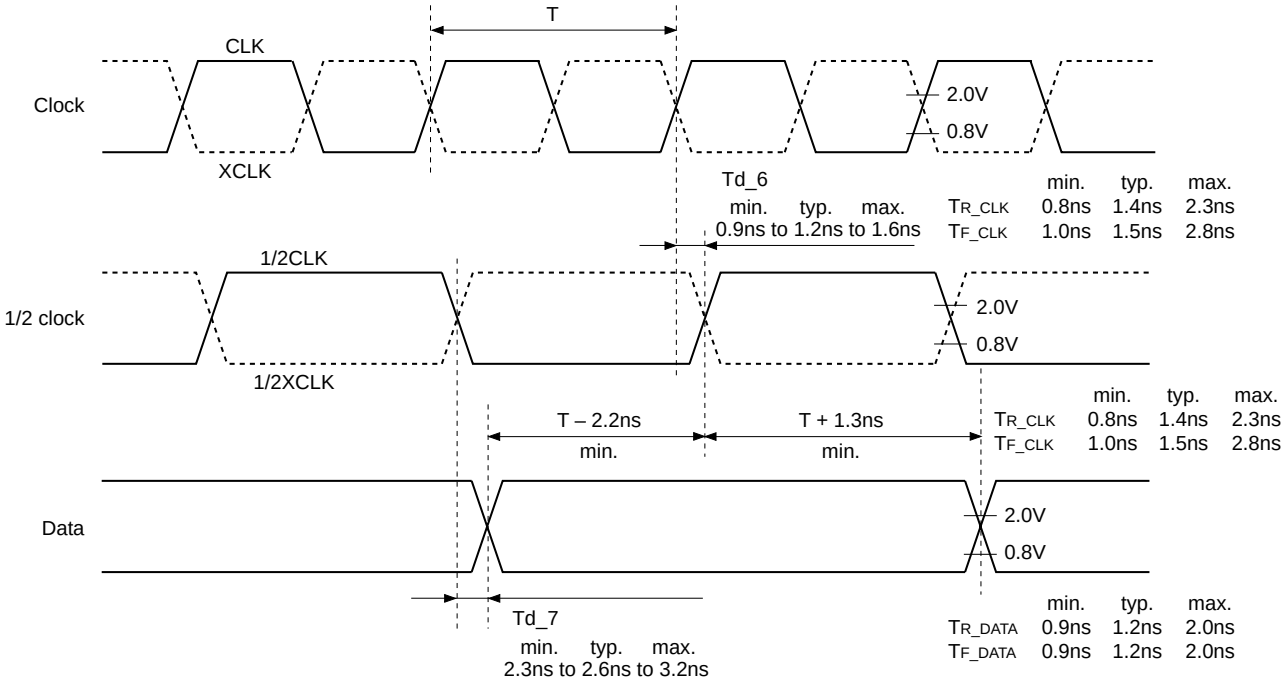


ADC Timing Diagram



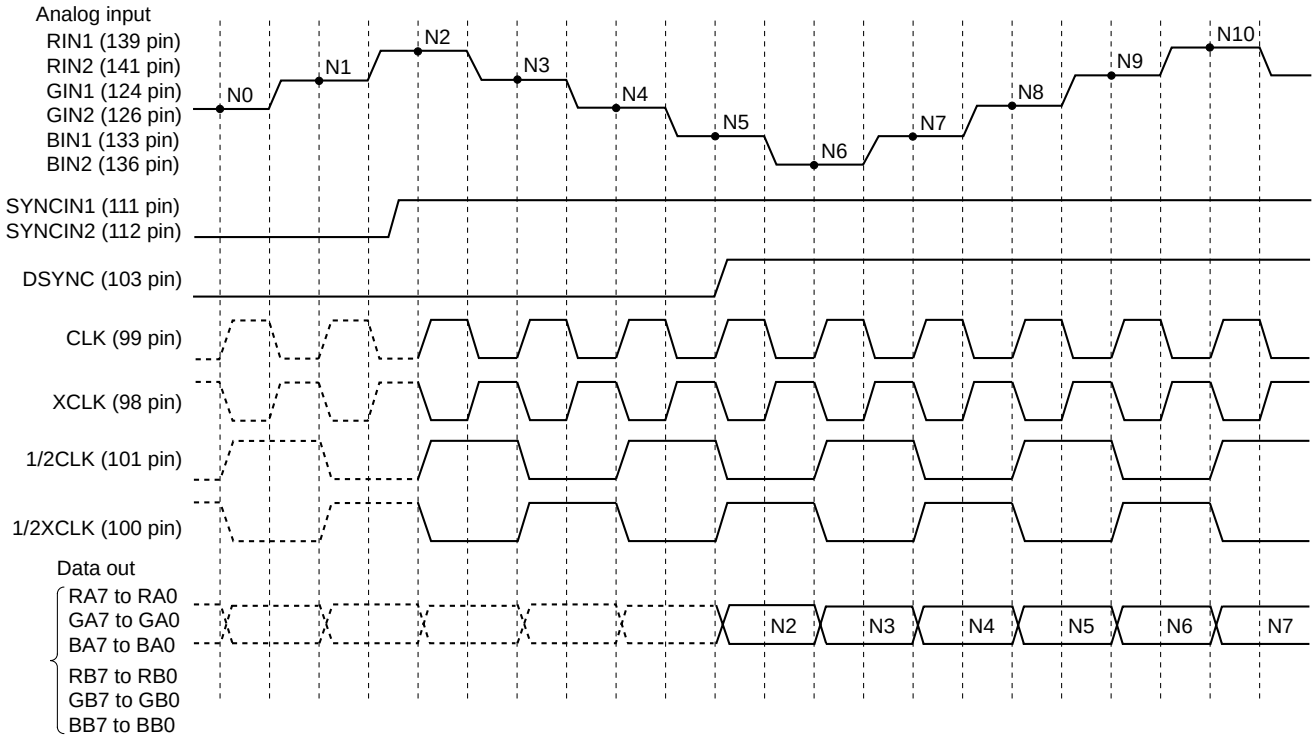
The timing diagram above supposes that one data cycle represents the same amount of time as one clock cycle concerning the three modes as follows:
Straight Data out Mode, 4:2:2 Data out D2 Mode, and 4:2:2 Data out special Mode.

ADC Timing Diagram

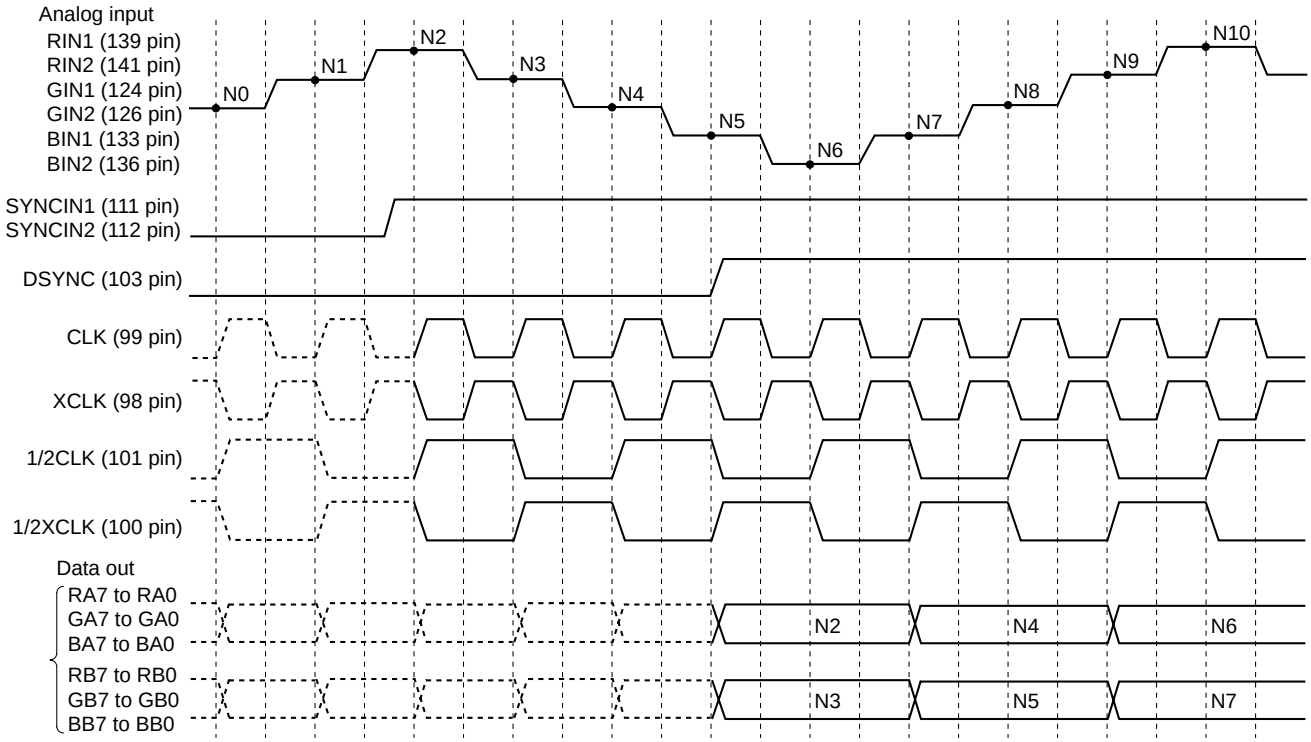


The timing diagram above supposes DMUX Parallel Data out Mode. It is possible for the post-stage scaling IC to acquire data by using a 1/2 clock. The output delay time in this mode is the same as that in DMUX Interleaved Data out Mode.

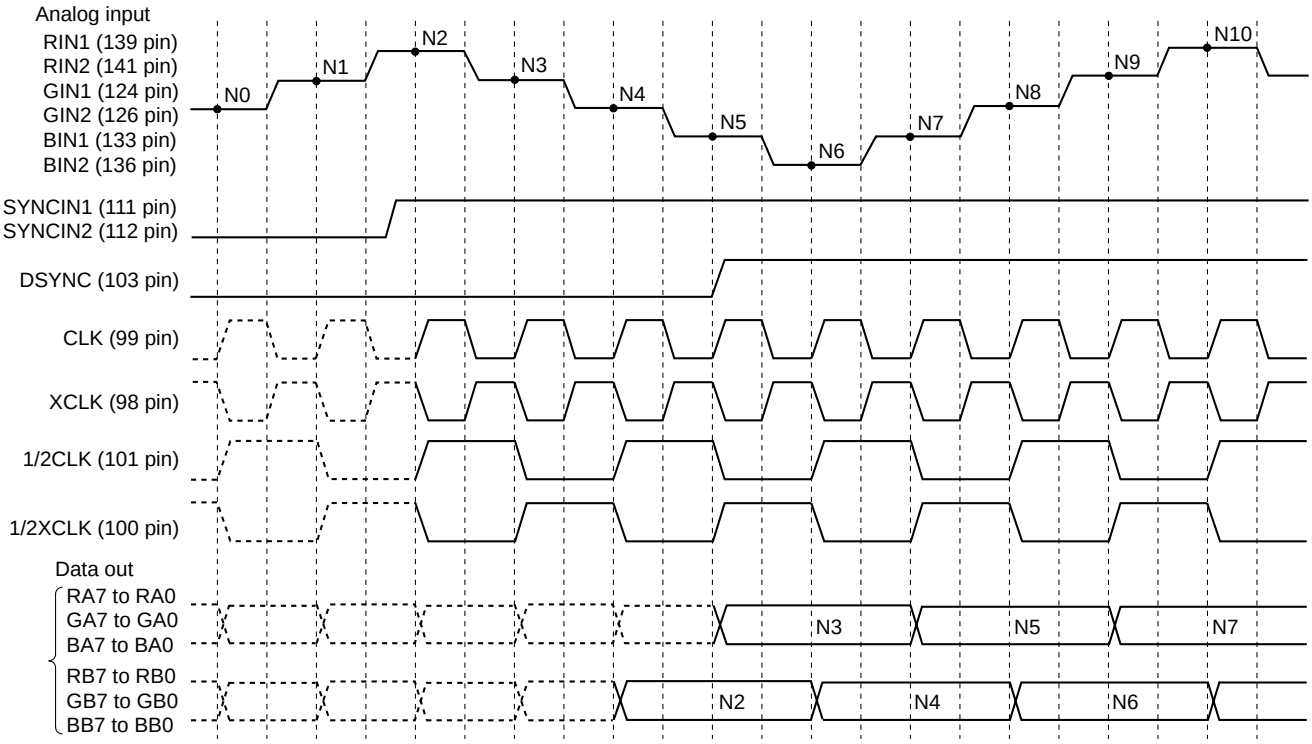
ADC Timing Diagram (Straight Data out Mode)



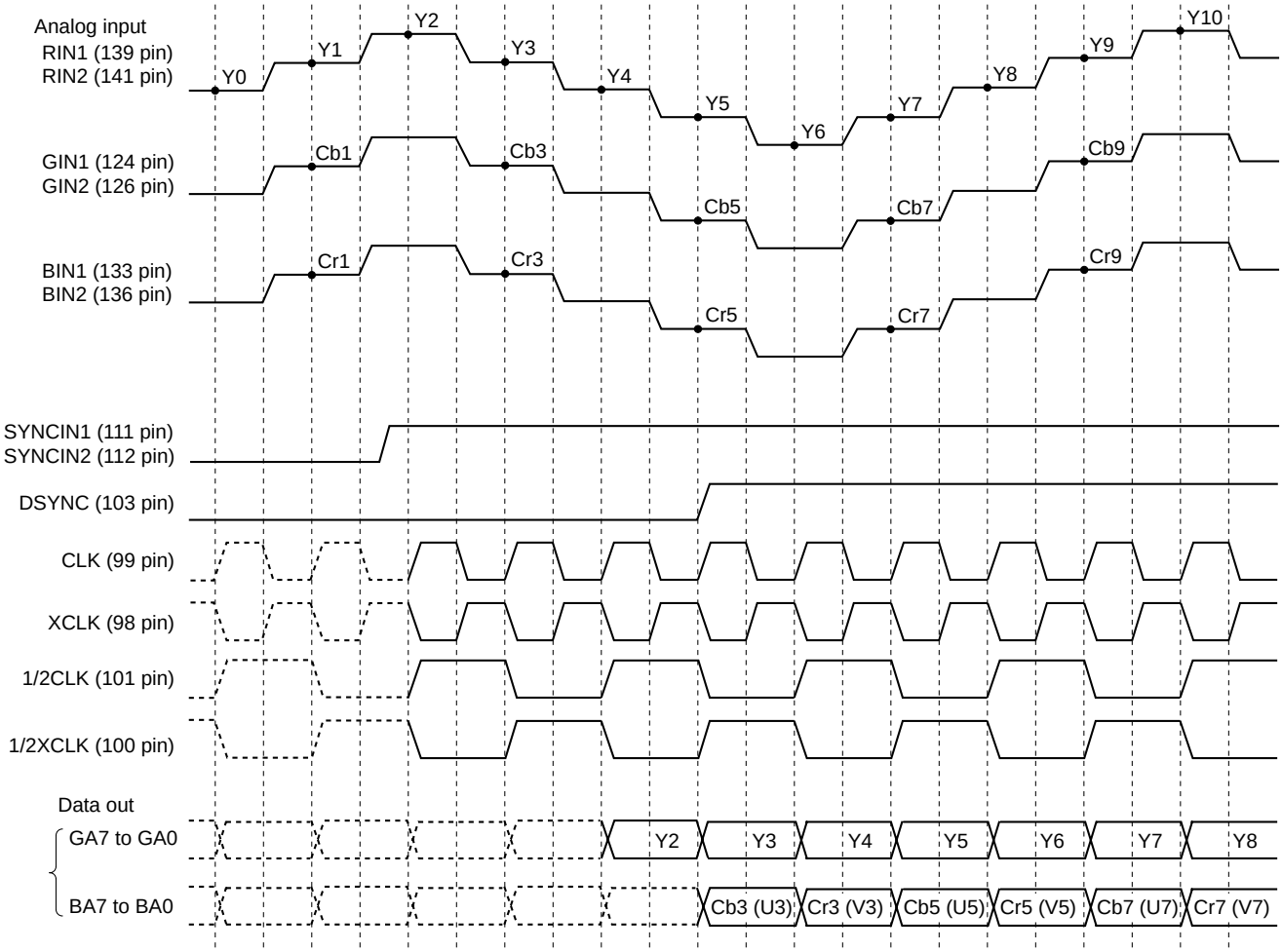
ADC Timing Diagram (DMUX Parallel Data out Mode)



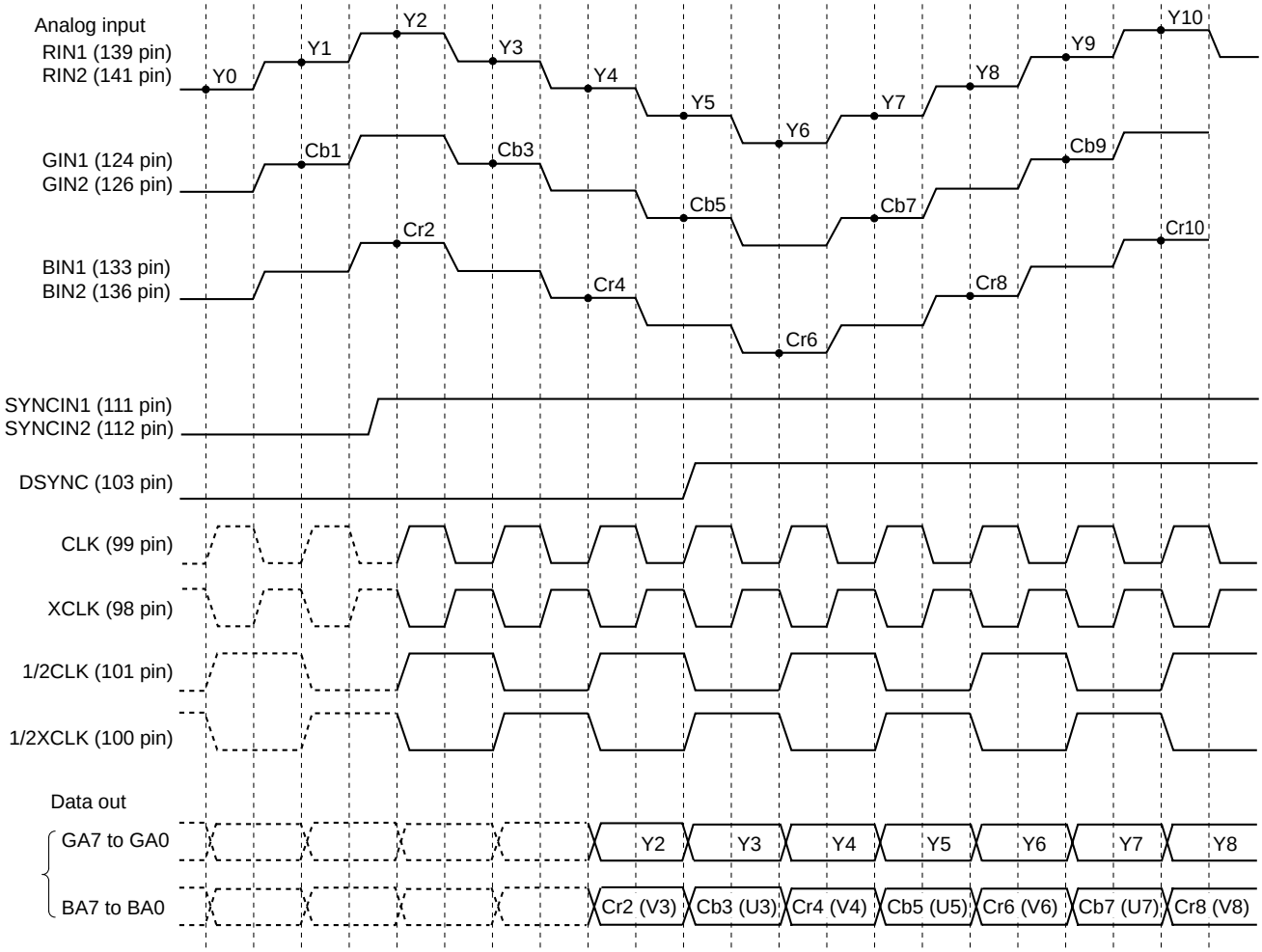
ADC Timing Diagram (DMUX Interleaved Data out Mode)



ADC Timing Diagram (4:2:2 Data out D2 Mode)

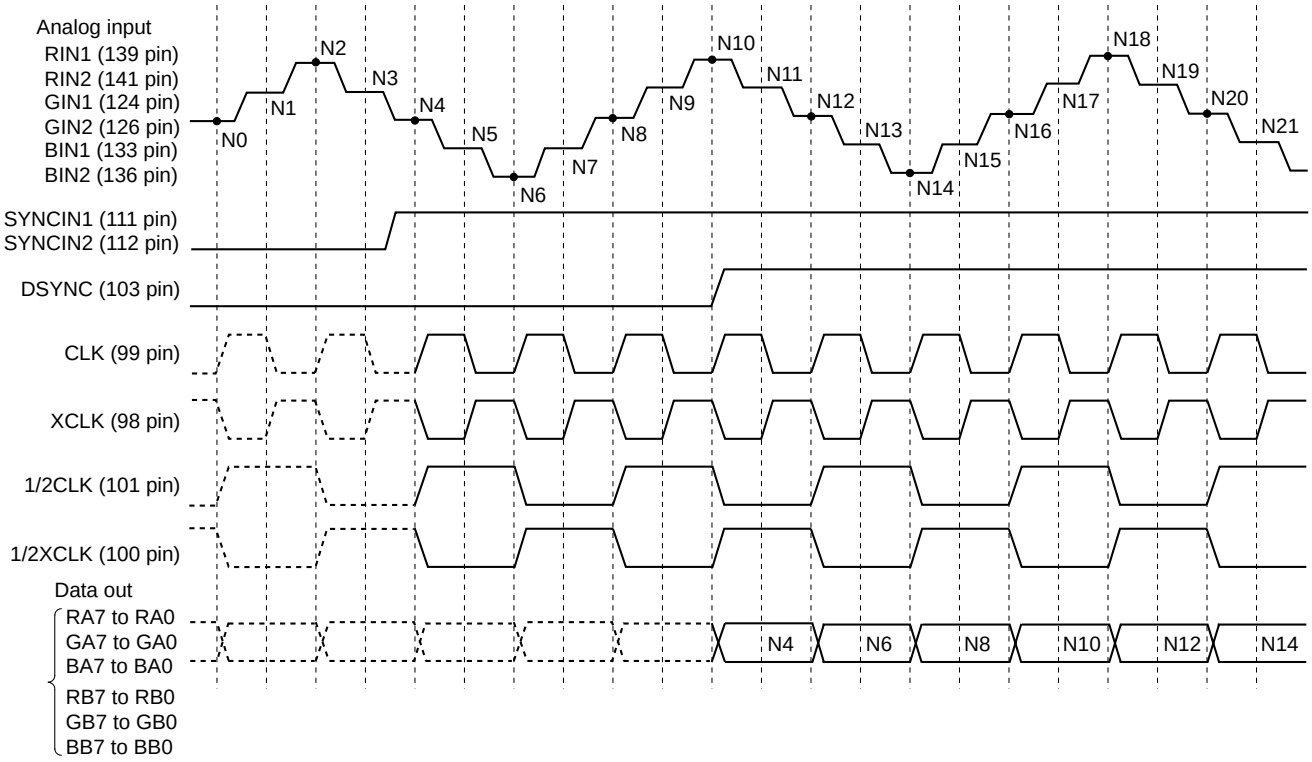


ADC Timing Diagram (4:2:2 Data out special Mode)

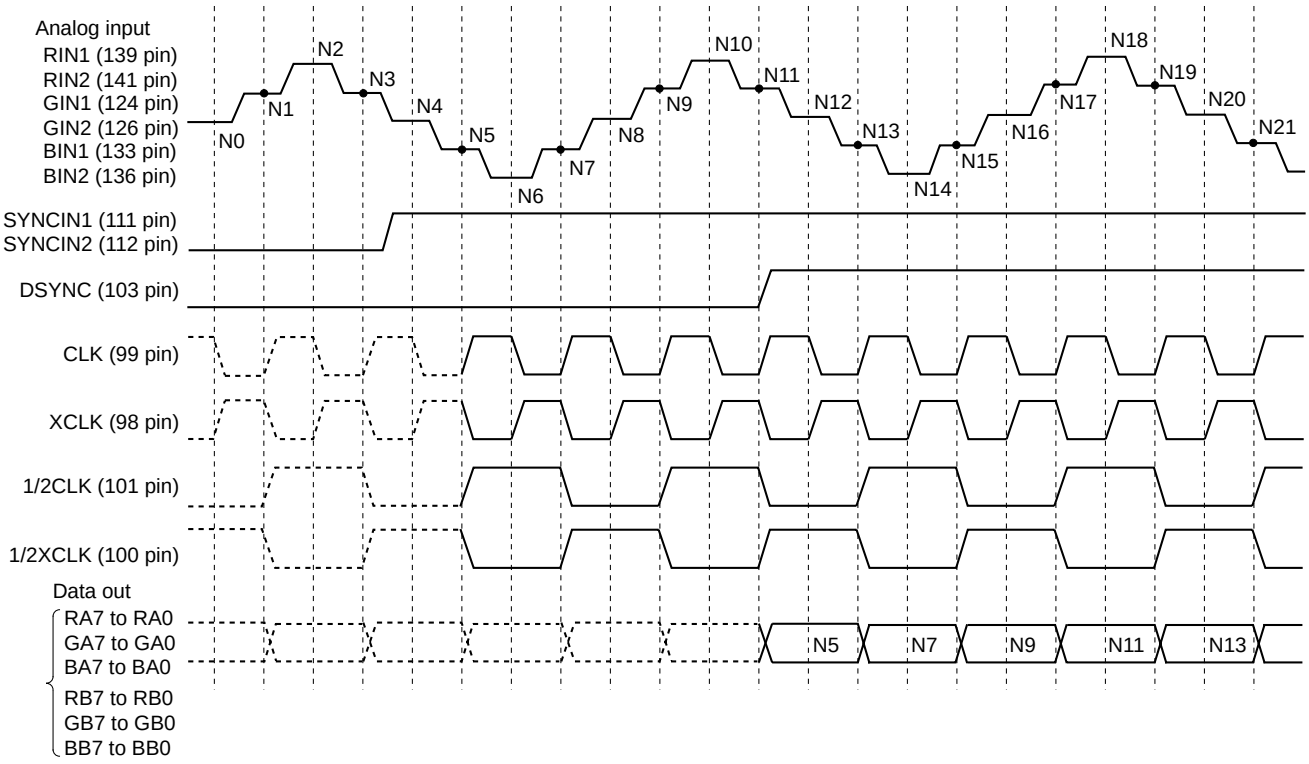


ADC Timing Diagram (Straight Data out Mode, EVEN/ODD)

EVEN

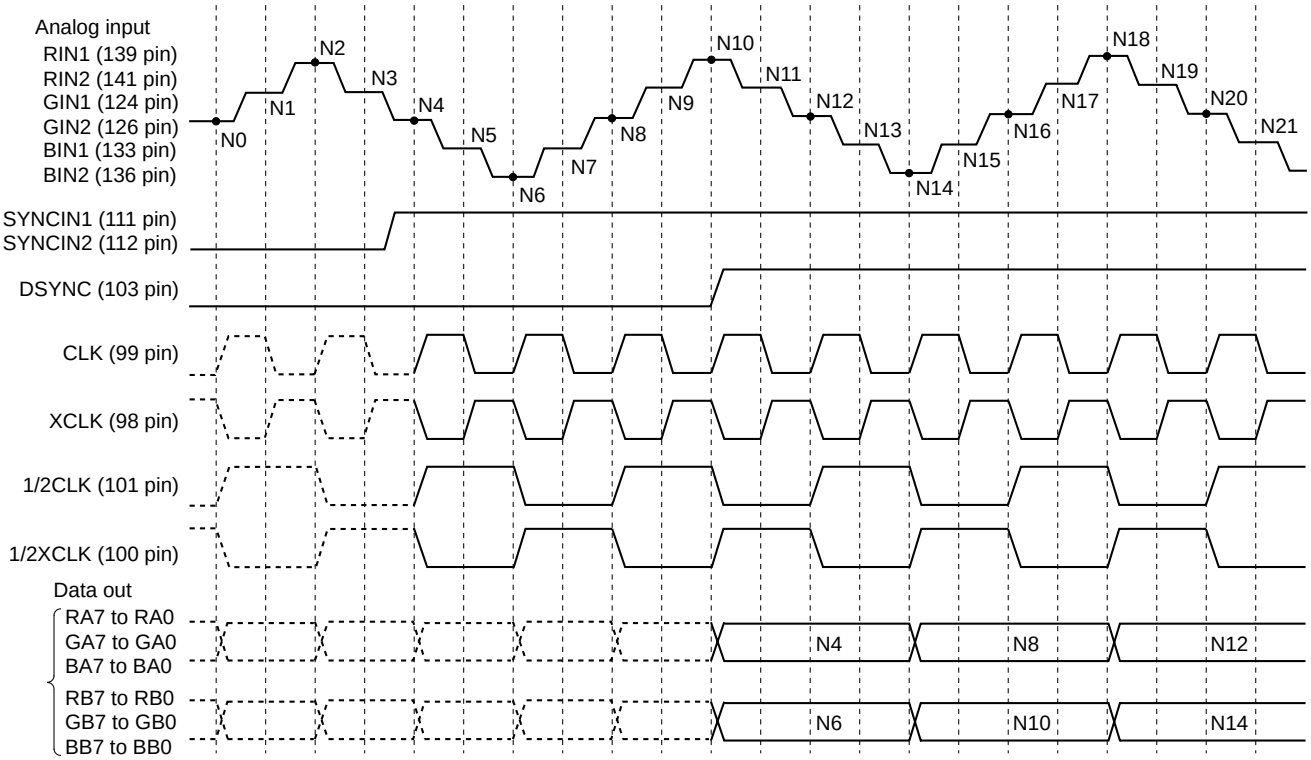


ODD

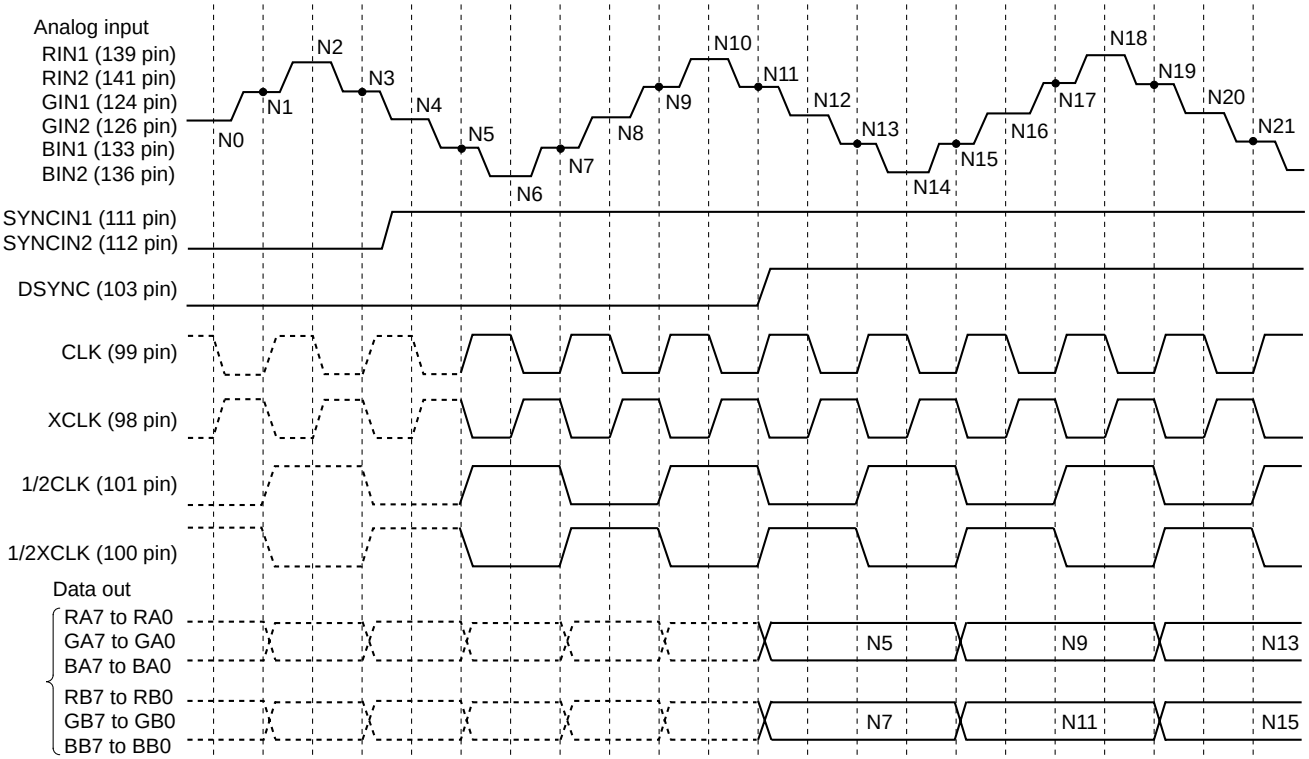


ADC Timing Diagram (DMUX Parallel Data out Mode, EVEN/ODD)

EVEN

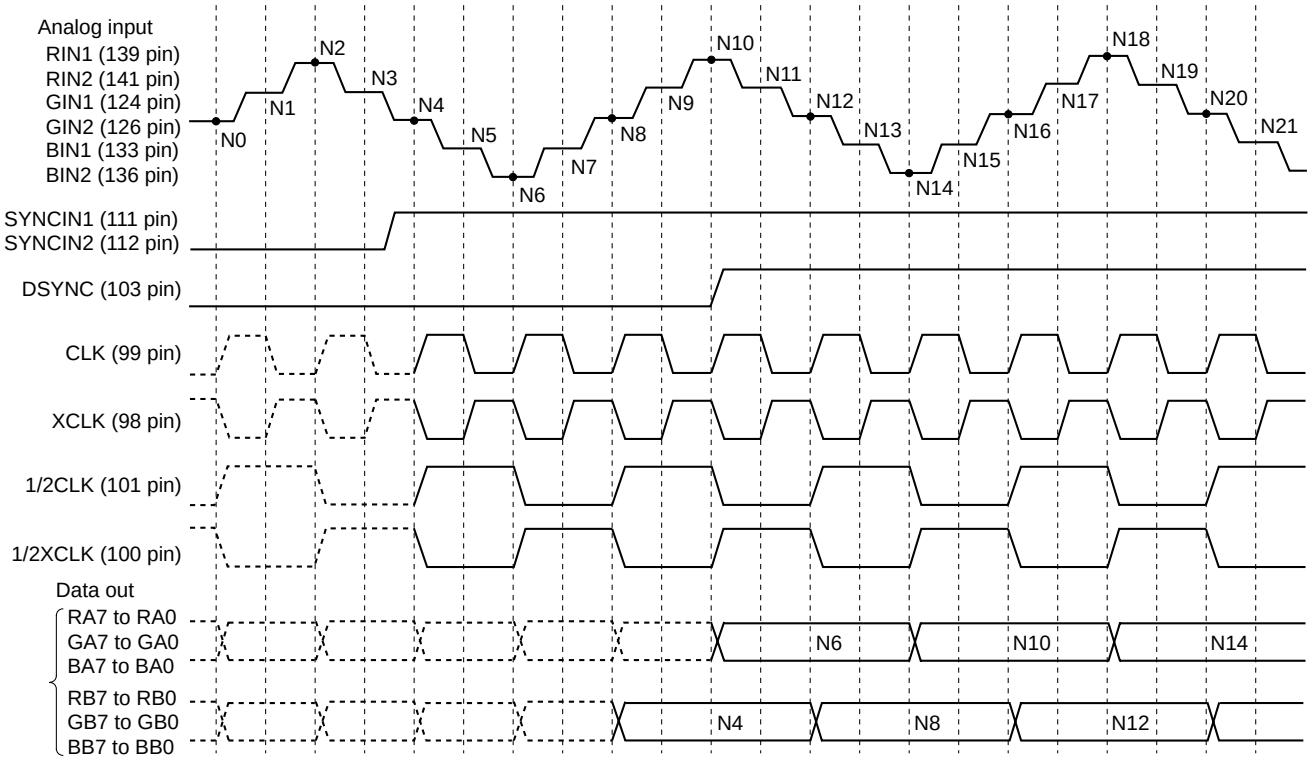


ODD

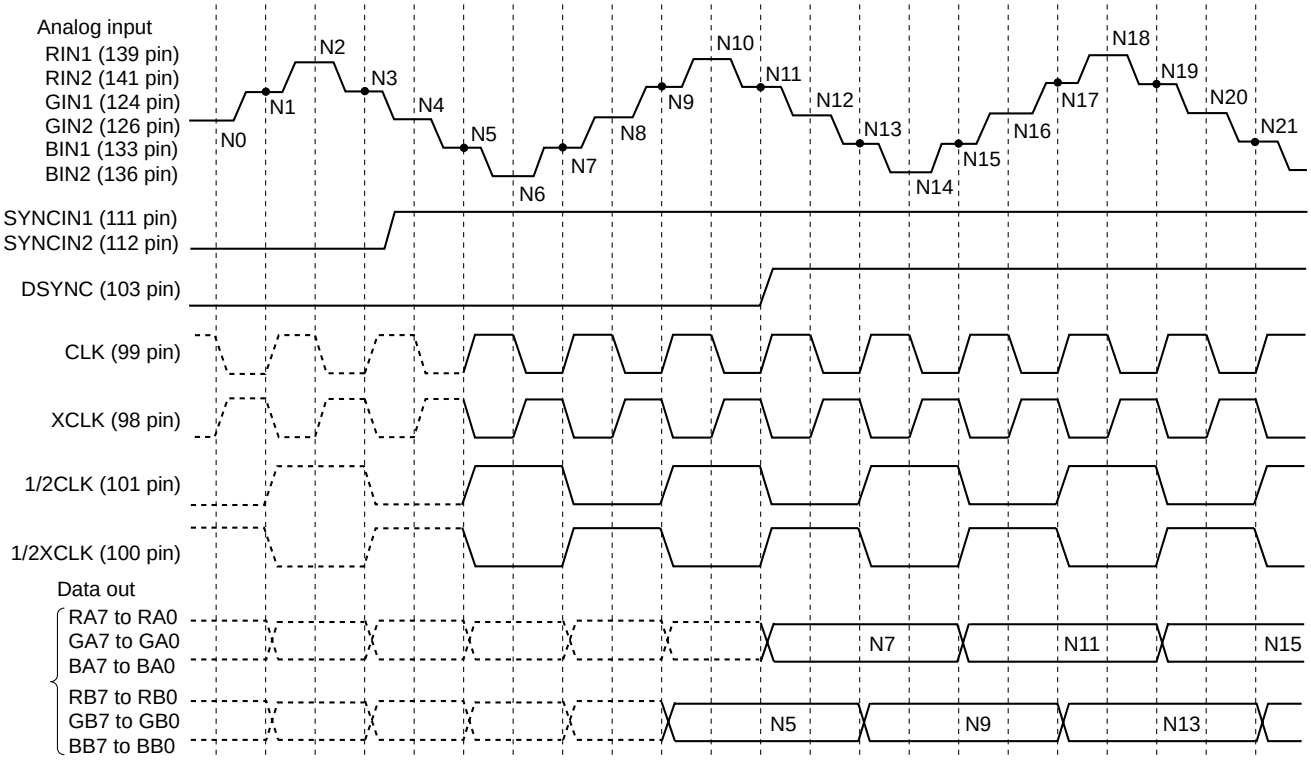


ADC Timing Diagram (DMUX Interleaved Data out Mode, EVEN/ODD)

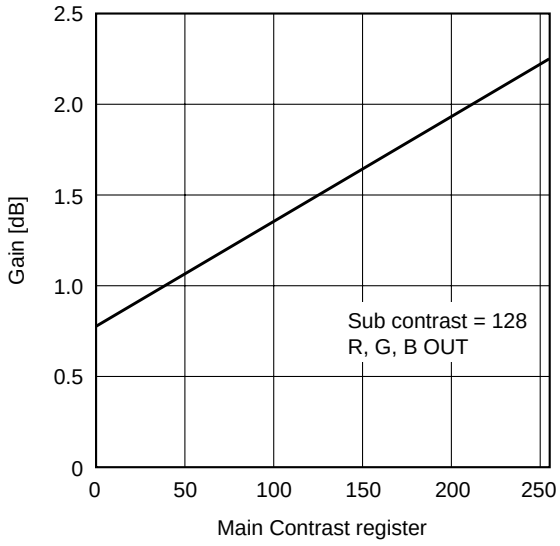
EVEN



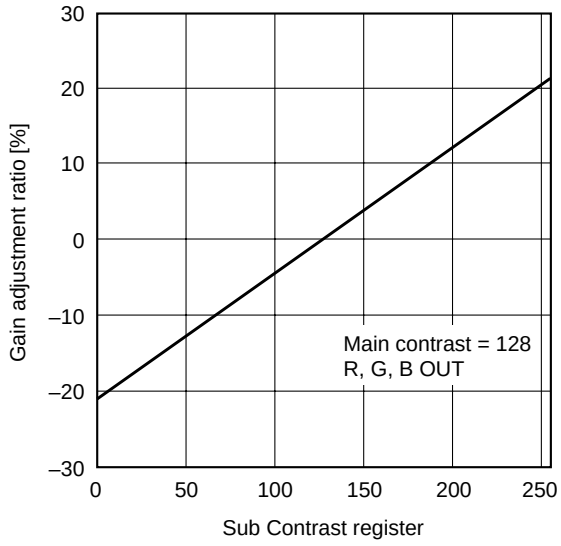
ODD



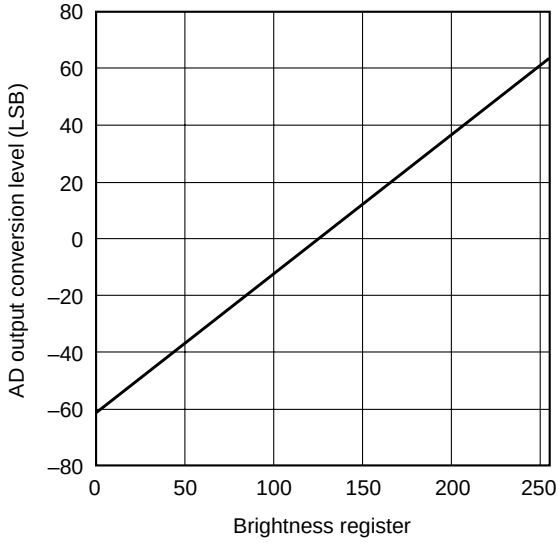
Main Contrast Control Characteristics



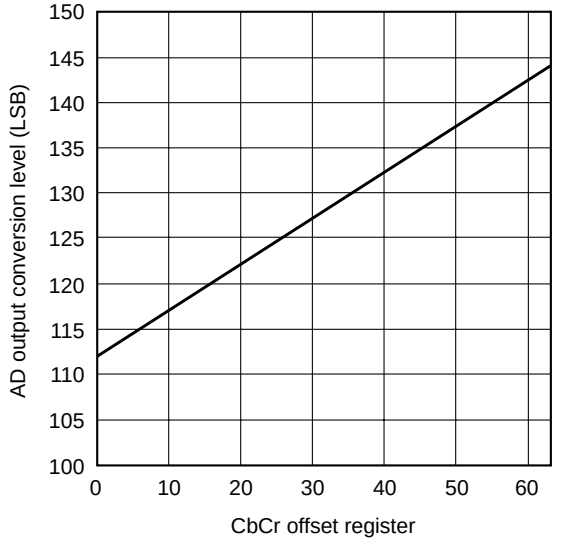
Sub Contrast Control Characteristics



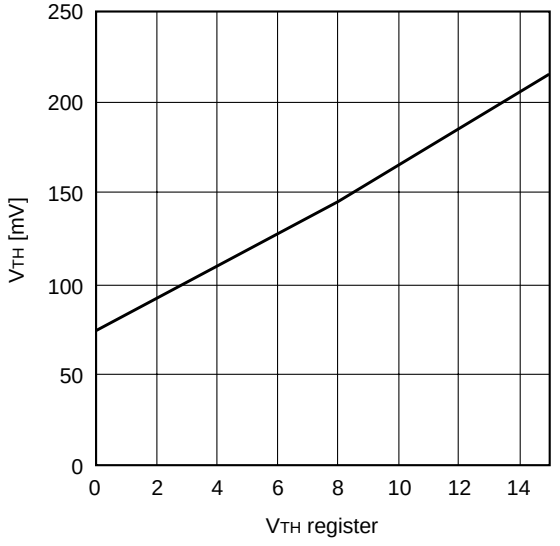
Brightness Level Control Characteristics



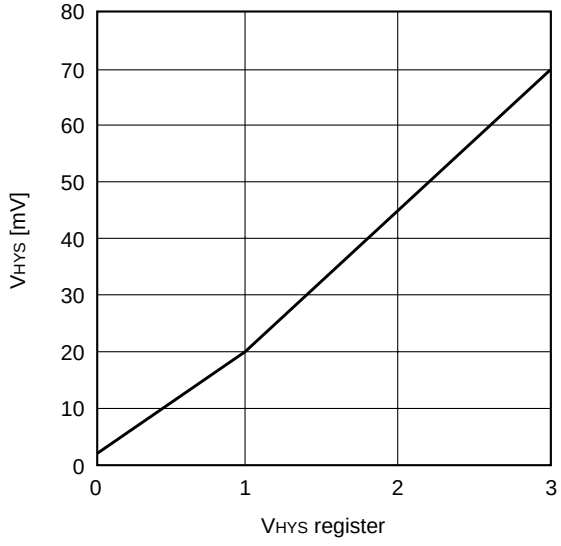
CbCr Clamp Level Control Characteristics



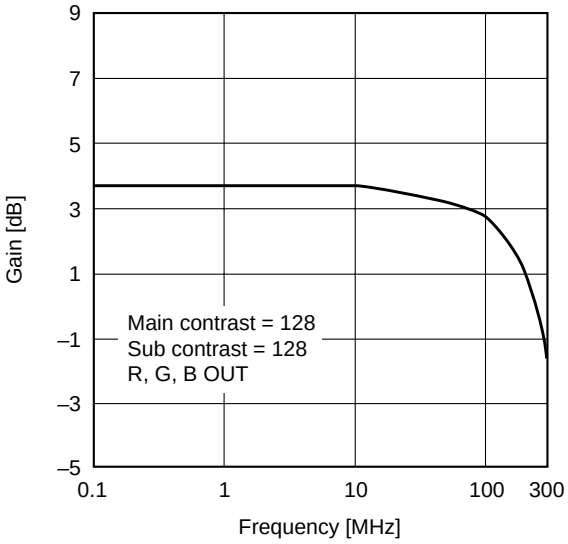
SYNC SEP V_{TH} Control Characteristics



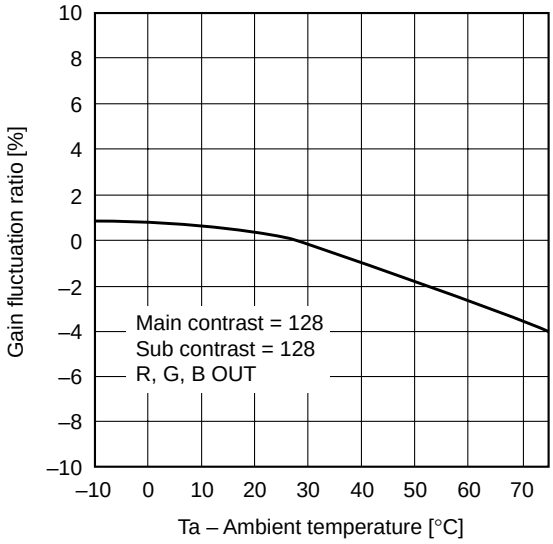
SYNC SEP V_{HYS} Control Characteristics



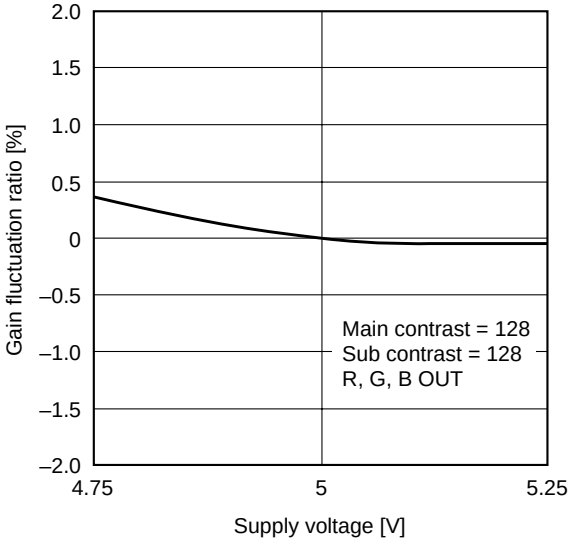
Frequency Response



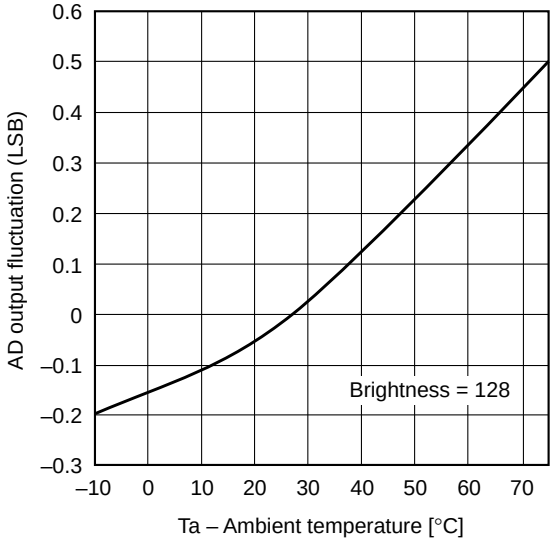
Gain Temperature Characteristics



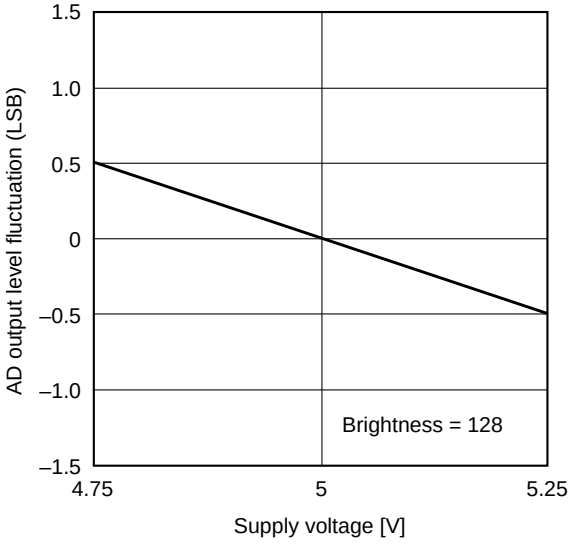
Gain Supply Voltage Characteristics



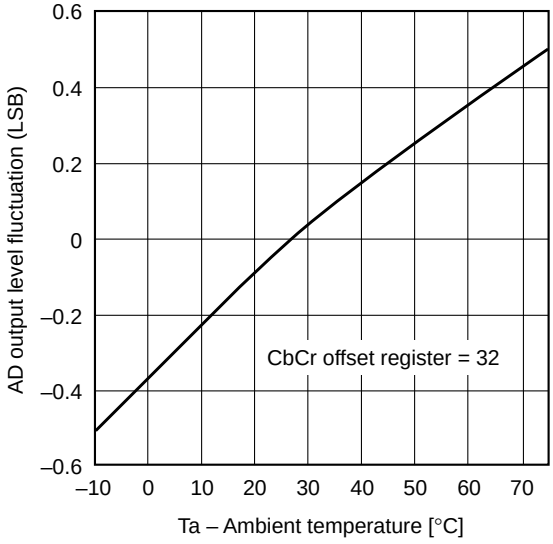
Brightness Level Temperature Characteristics



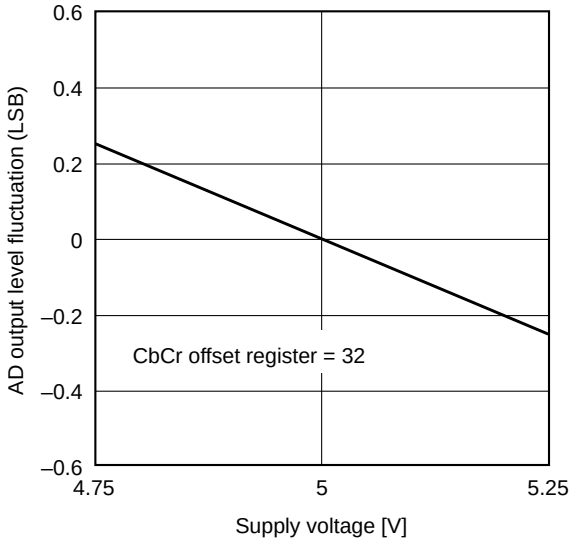
Brightness Supply Voltage Characteristics



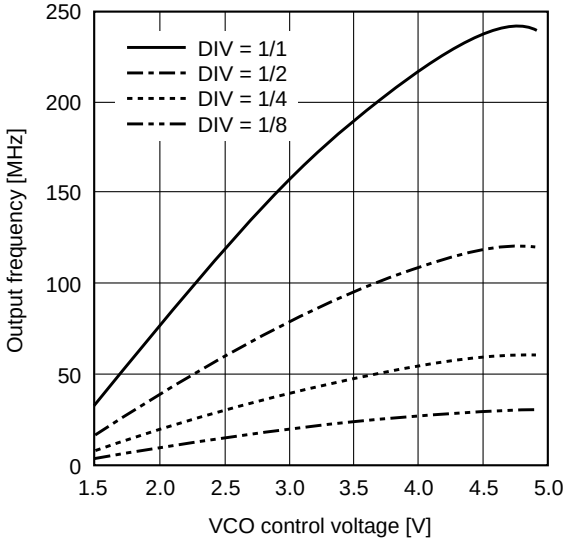
CbCr Clamp Level Temperature Characteristics



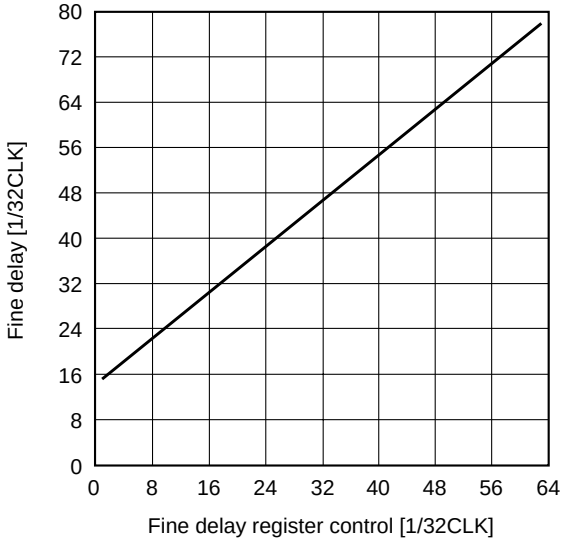
CbCr Clamp Level Supply Voltage Characteristics



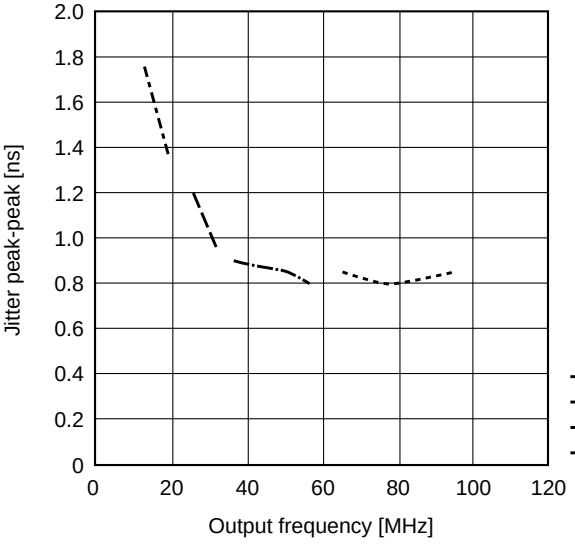
KVCO Characteristics



Fine Delay vs. Control

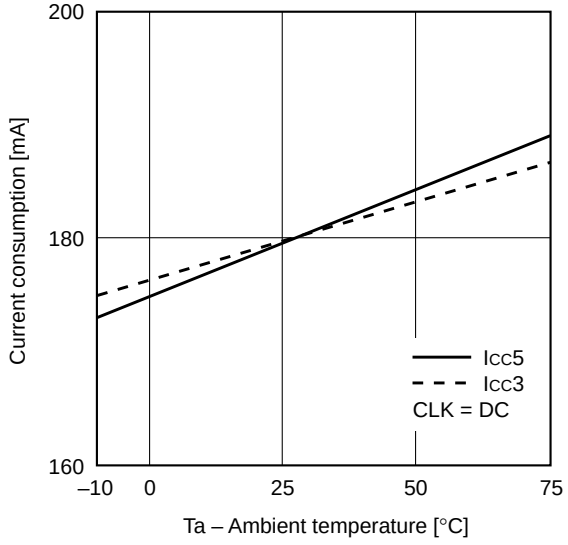


Jitter Peak-Peak vs. Output Frequency

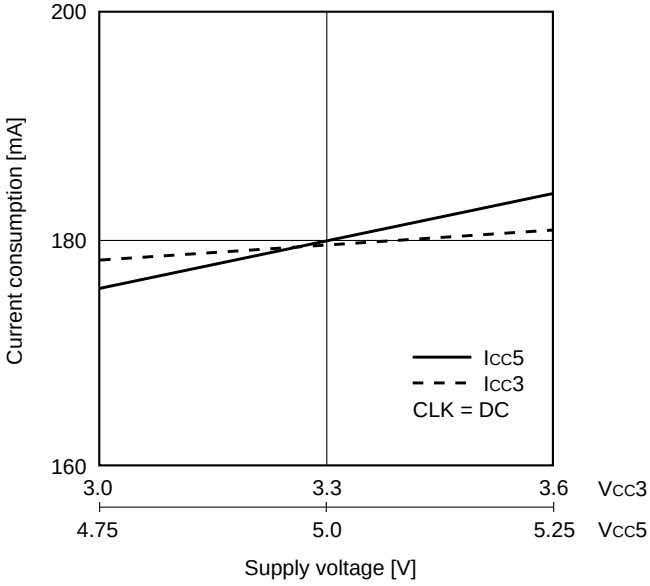


NTSC, DIV = 1/8, CP = 010, 100
VGA, DIV = 1/4, CP = 010, 011
SVGA, DIV = 1/4, 1/2, CP = 010, 100, 101
XGA, DIV = 1/2, CP = 011, 100

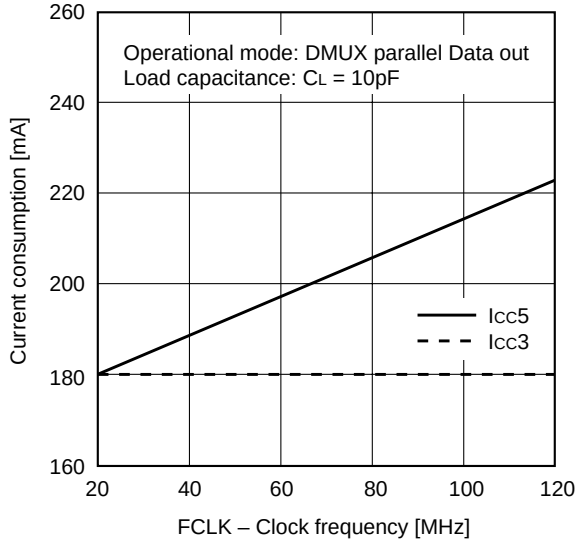
Current Consumption vs. Temperature Characteristics



Current Consumption vs. Supply Voltage Fluctuation



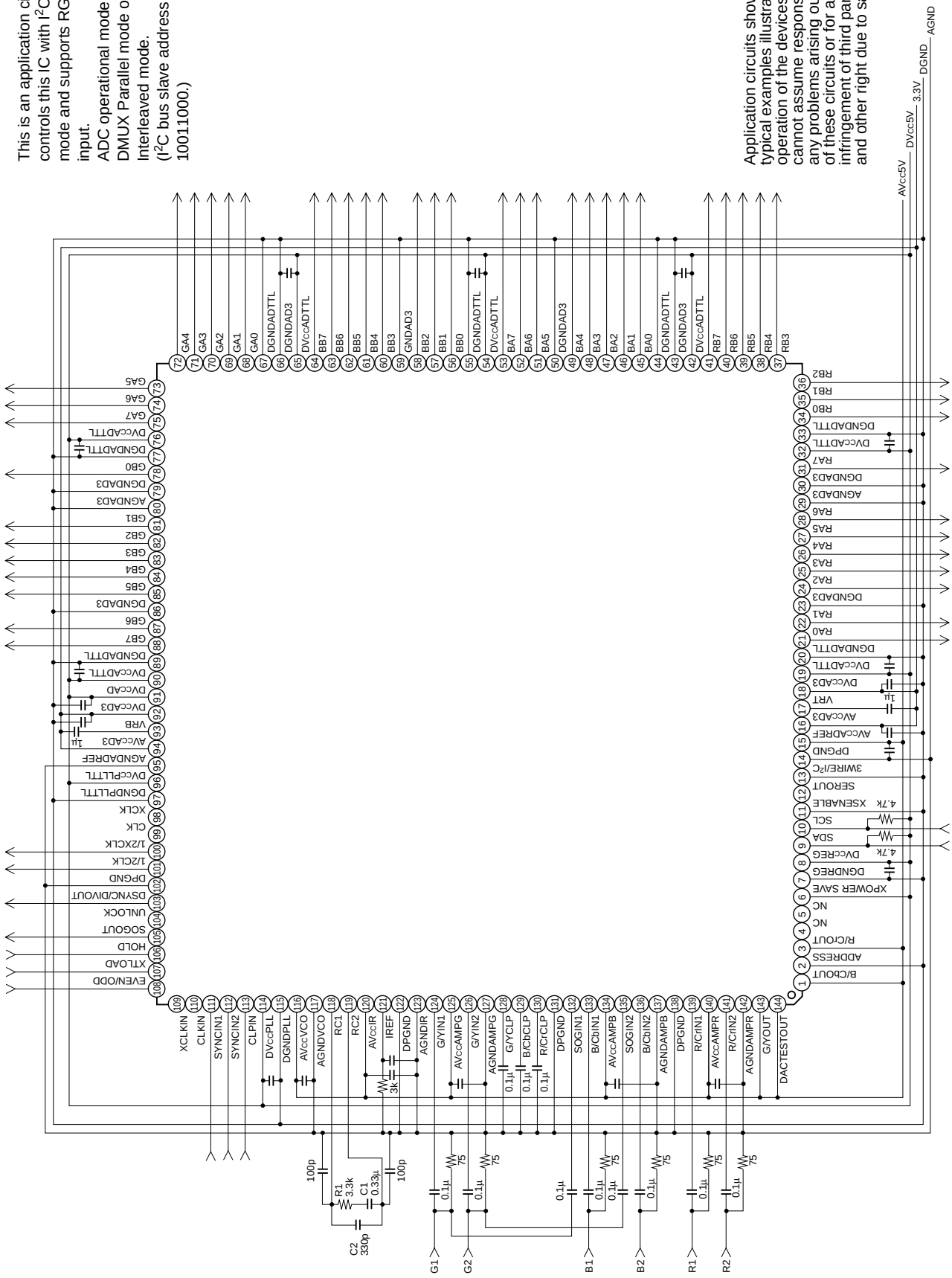
Current Consumption vs. Frequency Response



Application Circuit (I²C (High) mode)

This is an application circuit which controls this IC with I²C (High) mode and supports RGB2 channel input.
ADC operational mode supports DMUX Parallel mode or DMUX Interleaved mode.
(I²C bus slave address is 10011000.)

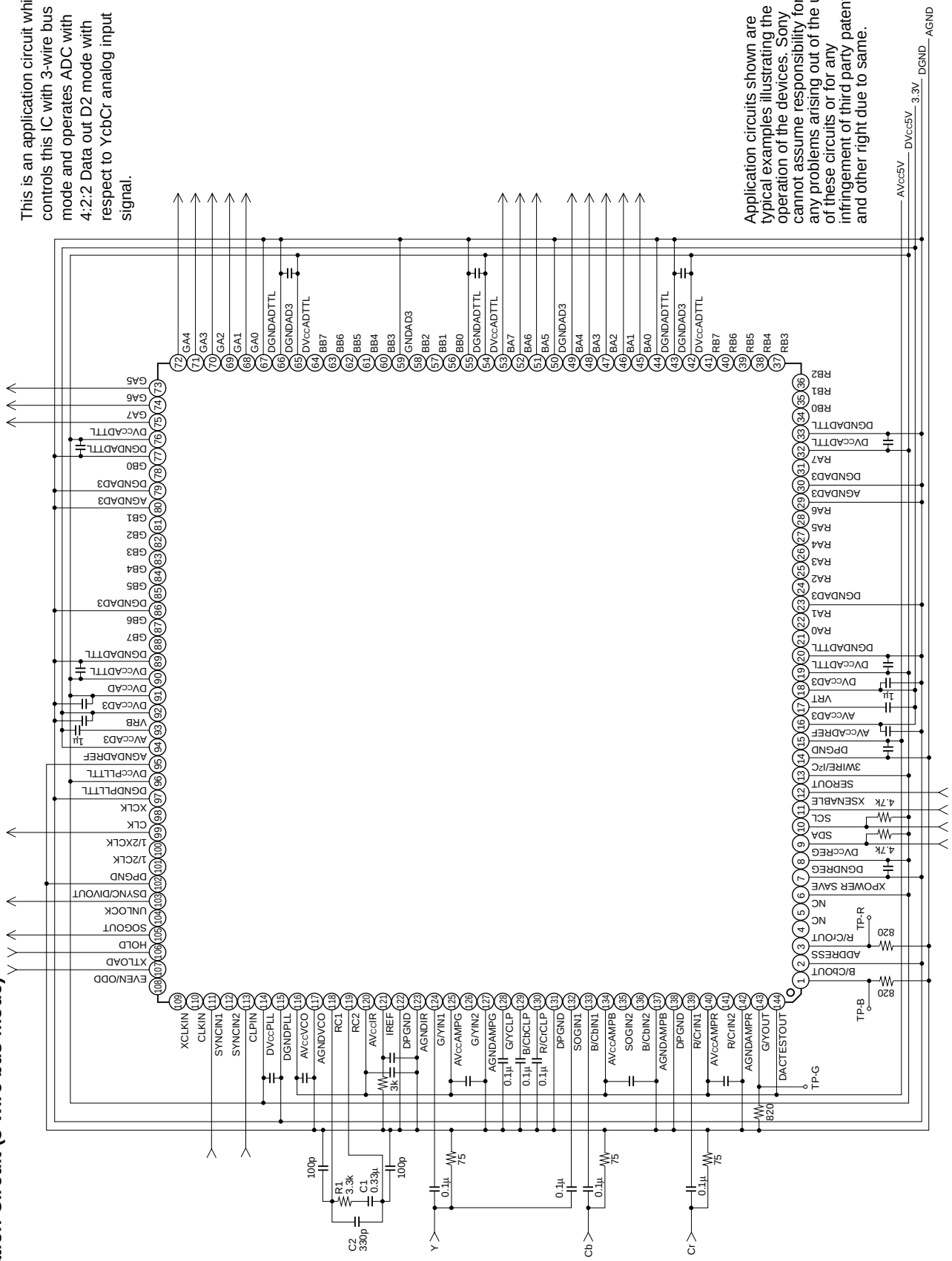
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.



Application Circuit (3-wire bus mode)

This is an application circuit which controls this IC with 3-wire bus mode and operates ADC with 4:2:2 Data out D2 mode with respect to YcbCr analog input signal.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.



Notes on Operation

- On the PC board, prepare a solid ground pattern having as large an area as possible, and placing the IC in the center, divide this area into an analog region and digital region.

- The loop filter area of the PLL block plays an important role in terms of performance. It is therefore located as close as possible to the IC pins and the periphery is guarded with AGND. Also, be sure to use capacitors and resistors for the loop filter that should be temperature compensated and do not change the values.

- Be sure to use a metal film resistor for the resistor connected to IREF (Pin 121).

- The wiring for SYNCIN1 (Pin 111) and SYNCIN2 (Pin 112) should be as short as possible and each needs to be shielded by ground.

- Use a 0.1µF ceramic chip capacitor for the bypass capacitor attached between the power supply and ground. The capacitor should be attached to the pin as close as possible.

- Use a 1µF ceramic chip capacitor for the capacitor attached to the VRT (Pin 17) and the VRB (Pin 93) and connect to the AV$_{CC}$AD3 (Pin 16 and Pin 94) as close as possible.

- Equalize and shorten the lines of RGB analog input signals, if possible. Each line needs to be shielded by ground. (This is the same for the R/CrCLP, G/YCLP, and B/CbCLP pins.)

- A 0.1µF capacitor is recommended for attachment to the RGB analog input pins. The less the capacitance becomes, the more the sag by leak current becomes. The more the capacitance becomes, the more start up time takes in case of putting power source into the IC. (This is the same for the R/CrCLP, G/YCLP, and B/CbCLP pins.)

- Design boards so that the wiring for the R/CrIN, G/YIN, and B/CbIN and R/CrOUT, G/YOUT, B/CbOUT pins is as separated as possible.

- Use a pattern width that takes characteristic impedance into account for signal wires terminated at 75Ω.

- There are no particular restrictions on the power-on sequence.

- Although there are AV$_{CC}$AD3 and DV$_{CC}$AD3 as 3.3V power supply, use the same 3.3V analog power supply to each on the board.

- AGNDAD3 and DGNDAD3 are the ground for AV$_{CC}$AD3 and DV$_{CC}$AD3, respectively. Use the same ground for AGNDAD3 and DGNDAD3. Although AGND is the ground recommended for AGNDAD3 and DGNDAD3, there are no problems in terms of operation even if connected to DGND. (The special evaluation board in the Application Circuit is connected to DGND.)

- Although 5V power supply is divided into both analog and digital power supply lines, be sure to wire boards so that no potential difference arises between these power supplies.

- Load capacitance of the data output wires causes the change for the worse of slew rate and noise. Be sure to use short layouts with the finest wires possible.

- Put this IC into power save mode when making a connection between data output and another IC. (High impedance cannot be set when pins are disabled separately.)

CXA3506R Evaluation Board

Overview

The CXA3506R Evaluation Board is a special board designed for the easy evaluation of the CXA3506R developed for the LCD projector and monitor so that performance can be maximized. The DSUB 15-pin connector is used as the input connector that allows the direct input of a video signal from a PC. The input video signal is A/D converted by the CXA3506R and a pin for monitoring is designed onto the board so that output data can be checked directly.

The 10-bit high speed D/A converters are built onto the board so that the performance of the IC can be easily checked. Picture quality can be easily evaluated by using a CRT monitor since the D/A-converted video signal is output from the DSUB 15-pin connector for output in addition to the DSYNC output of the CXA3506R.

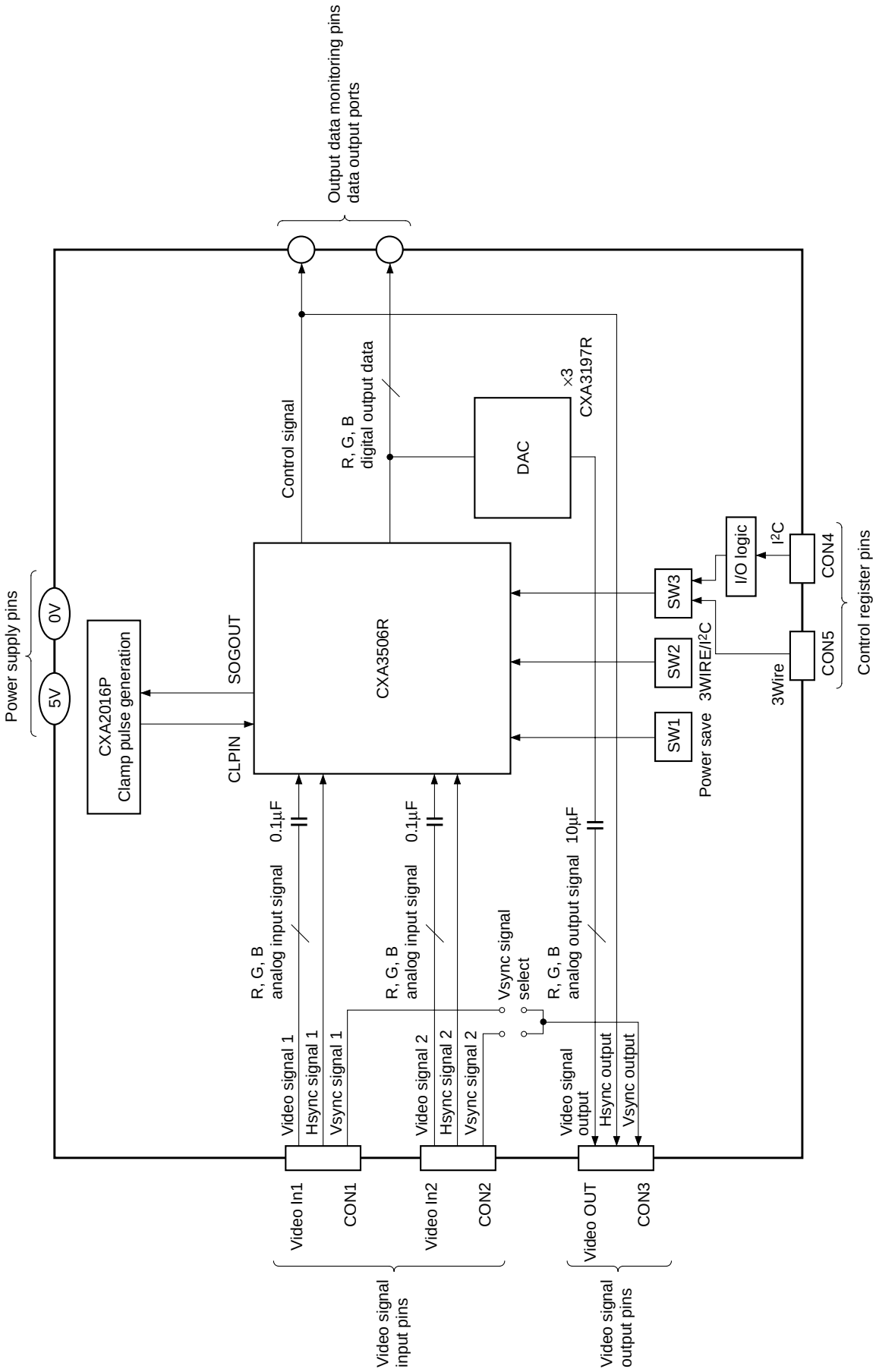
Features

- Single +5V power supply (with built-in 3.3V regulator)
- Allows two-line video signal input
- Data output port is also used as output data monitoring pin
- CXA3506R output is D/A converted and is easily monitored by a CRT
- Supports 2 types of control registers (3-wire and I^2C)

Operating Conditions

- Supply voltage: +5V (typ.)
- Current consumption: 830mA (typ.)
- Input signal: Separated sync video signal

CXA3506R EVB Block Diagram



Using the CXA3506R Evaluation Board

The CXA3506R Evaluation Board can be used to easily evaluate just by connecting a power supply, video signals, and control register signals.
The procedure is described below.

1. Connect the power supply to the power connection pin. (GND/+5V)
   Do not apply power supply in this state.

2. Check the direction of SW1.
   SW1 is the power save control switch. The CXA3506R is put into power save mode when SW1 is set to the rear position (↑). Set SW1 to the forward (↓) position when using the CXA3506R.
   SW1 is connected to the XPOWER SAVE pin.

3. Connect the special control register signal cable.
   Connect the cable to CON4 when using I^2C control. Set SW2 and SW3 to the forward (↓) position. While, connect the cable to CON5 when using 3-wire control. Set SW2 and SW3 to the rear (↑) position.
   In addition, check that the short pin (I^2C) is in the "00" position in case of using I^2C control.

4. Input the RGB analog signals from the CON1 pin (Video In 1).
   XGA60 is recommended as the initial signal because the control program default value is set for the XGA60.
   XGA60: Vsync 60Hz
   Hsync: Video signal for 48kHz
   N = 1344

5. The RGB analog signal for simple picture quality evaluations is output from the CON3 pin (Video Out).
   Be sure to connect the CON3 pin to a CRT monitor that can process a signal of XGA60 or more.

6. Turn on the power.
   Check a current to be about 360mA flows through the 5V power supply.
   If there is much more current than this, immediately turn off the power and check that there are no misconnections.

7. Run the control program.
   Click on "re-load" at the bottom right of the control program screen, and check a current to be about 830mA flows through the 5V power supply.
   If everything works normally, an processed image for picture quality evaluation appears on the CRT monitor.
   Reconfirm the above items from the beginning if the processed image does not appear.

3-wire Control Program Installation and Startup Method

[Operating Environment]

Windows95 or Windows98

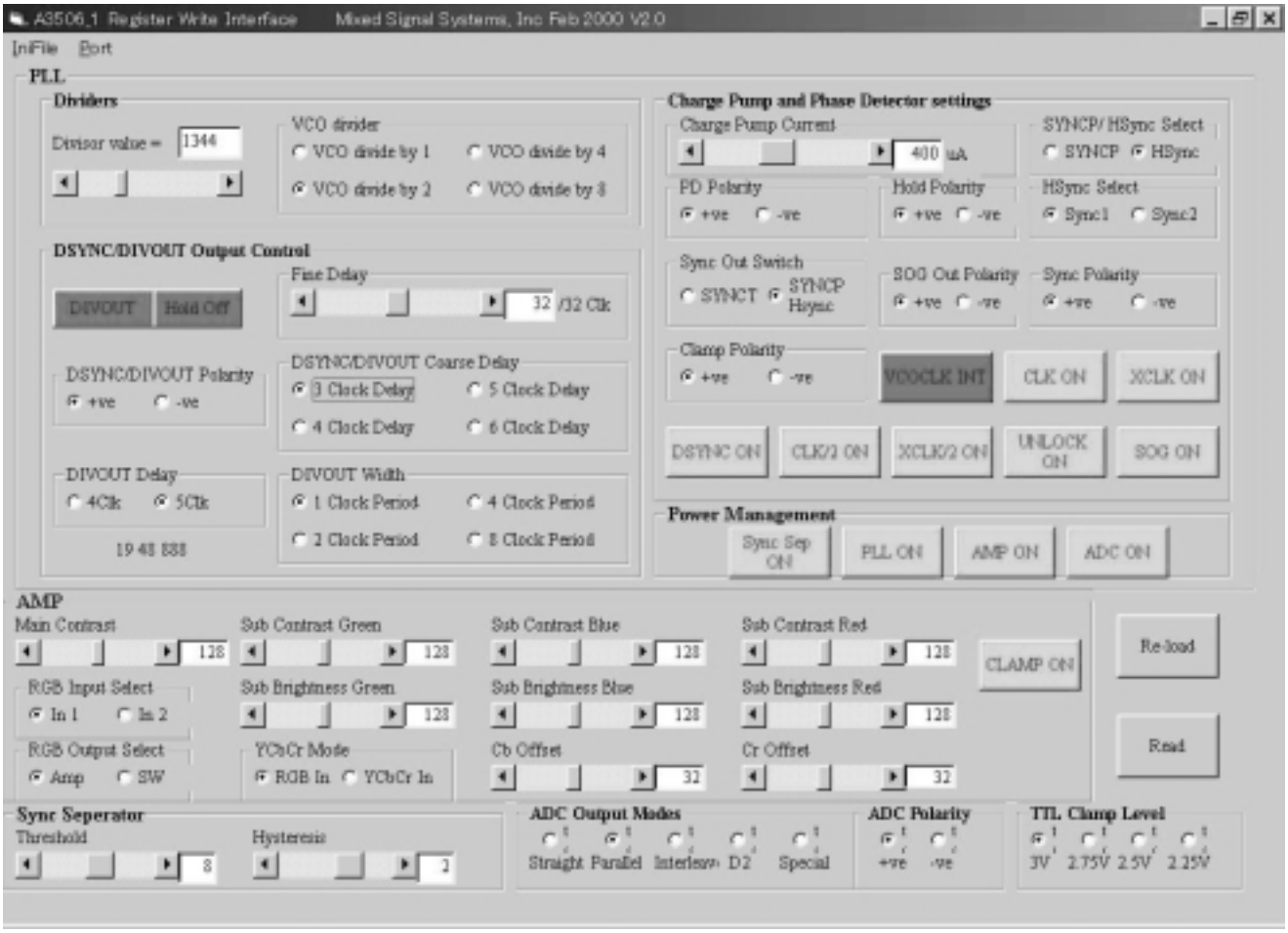
[Program Installation and Startup]

The installation program is configured from the following four files and stored in two floppy disks.

setup.exe, A3506_1.cab, A3506_2.cab, and Setup.lst

1. Copy the four files from the floppy disk onto the PC.
2. Click setup.exe.
   The installer will start. Follow all on-screen instructions.
3. Once installation complete, a folder titled "Project1" will be created in the Program files folder.
4. The following control window will open when the A3506.exe file starts.

Use this window to make board settings in response to the printer port address of the PC. Be sure to set the address for the PC from the pull-down menu port at the top-left of the control screen. There are two types of addresses: 378 and 3BC.



I²C Control Program Installation and Startup Method

[Operating Environment]

Windows95 or Windows98

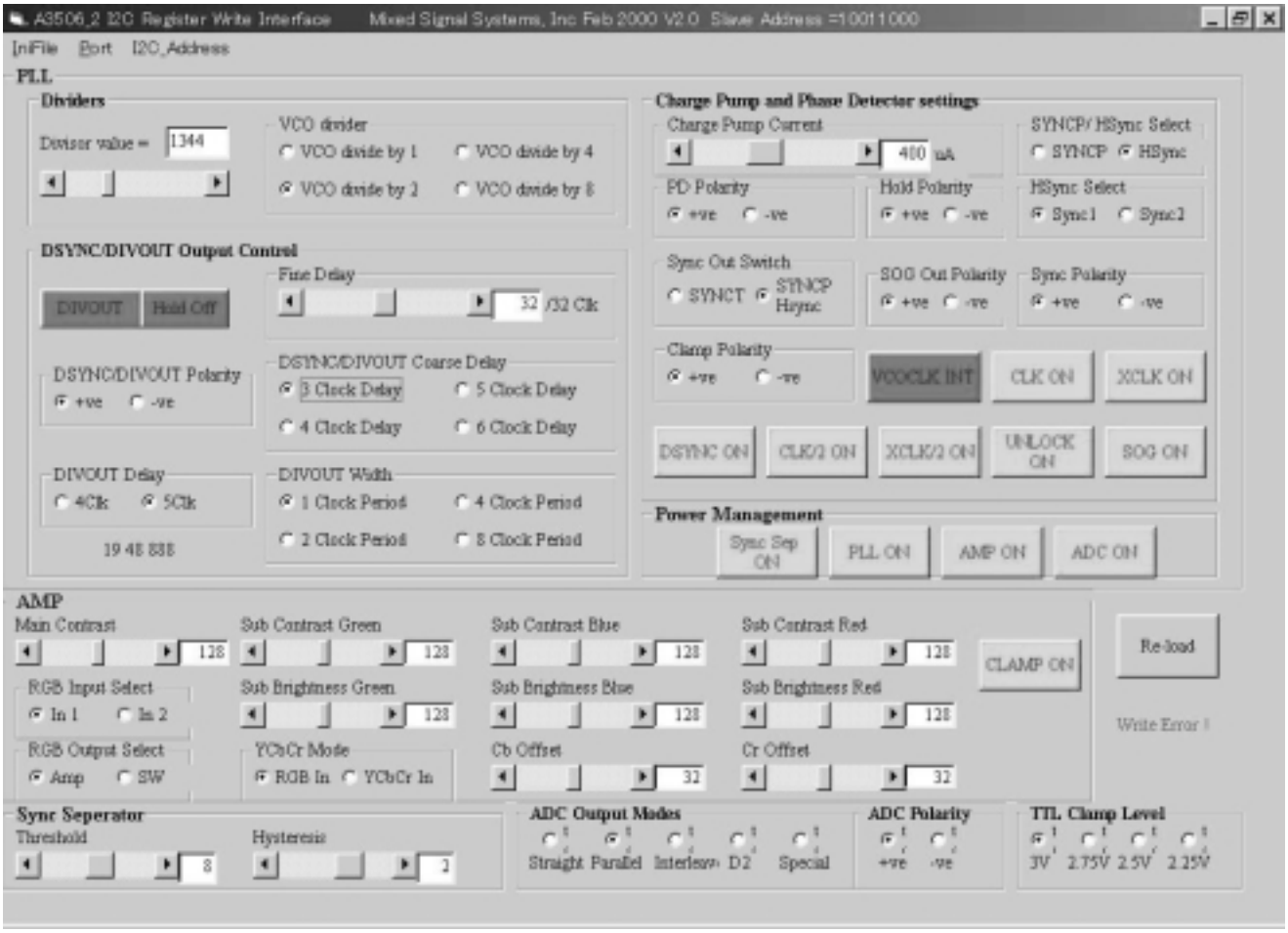
[Program Installation and Startup]

The installation program consists of the following four files and is stored in two floppy disks.

setup.exe, A3506_1.cab, A3506_2.cab, Setup.lst

1. Copy these four files from the floppy disk onto the PC.
2. Click setup.exe.
   The installer will start. Follow all on-screen instructions.
3. Once installation complete, a folder titled "Project1" will be created in the Program files folder.
4. The following control window will open when the A3506.exe file starts.

Use this window to make board settings in response to the printer port address of the PC. Be sure to set the address for the PC from the pull-down menu port at the top-left of the control screen. There are two types of addresses: 378 and 3BC.



Notes on Using CXA3506R EVB

1. RGB analog signals input from CON1 or CON2 are A/D converted.
   The digital signals are D/A converted.
   In addition, the analog signals are output in AC coupling.
   Therefore, the output are the RGB analog signals output from CON3.
   In this reason, when the RGB analog signals output from CON3 undergo picture quality evaluation by using a CRT monitor, note that on-screen evaluation cannot be confirmed about the functions of SUB BRIGHTNESS and Cb/Cr OFFSET. This is due to the fact that the DC component disappears because the RGB analog signals are output in AC coupled after output by the D/A converter, even if the DC offset is changed.

2. The current consumption for this board immediately after turning on the board's power is approximately 360mA. Board current is 830mA when the CXA3506R control register is started after this.
   When turning on power to the board, be sure to check the board current and make sure that connections are correct.

3. Although this board is equipped with a –5V power supply pin, it can operate by using a single 0/+5V power supply.
   Be sure to leave the –5V power supply pin open.

Notes Regarding the Control Program

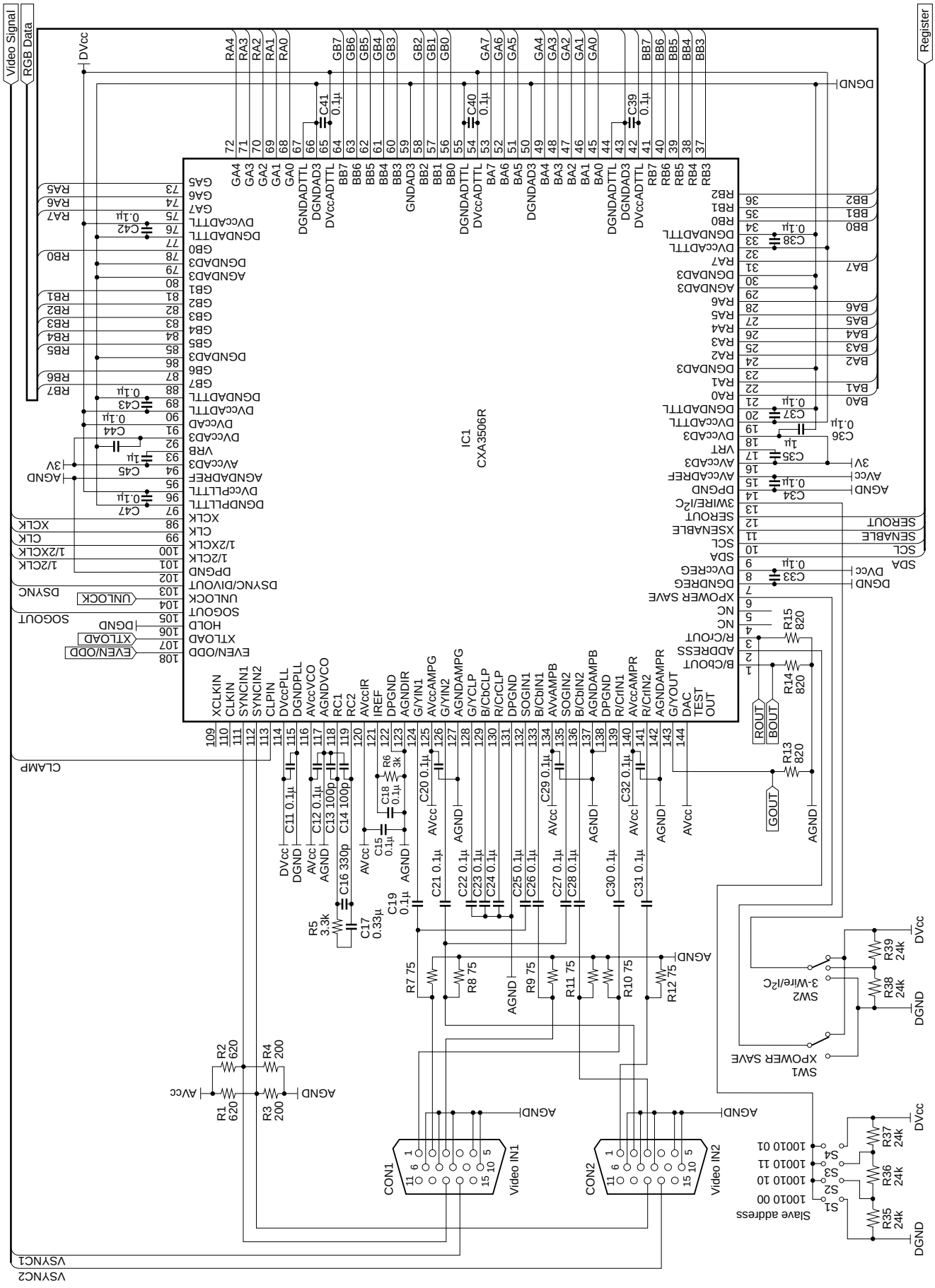
1. When the program is accurately installed on the PC, be sure to re-check items 2 and 3 of the operational procedures above when the IC does not move.

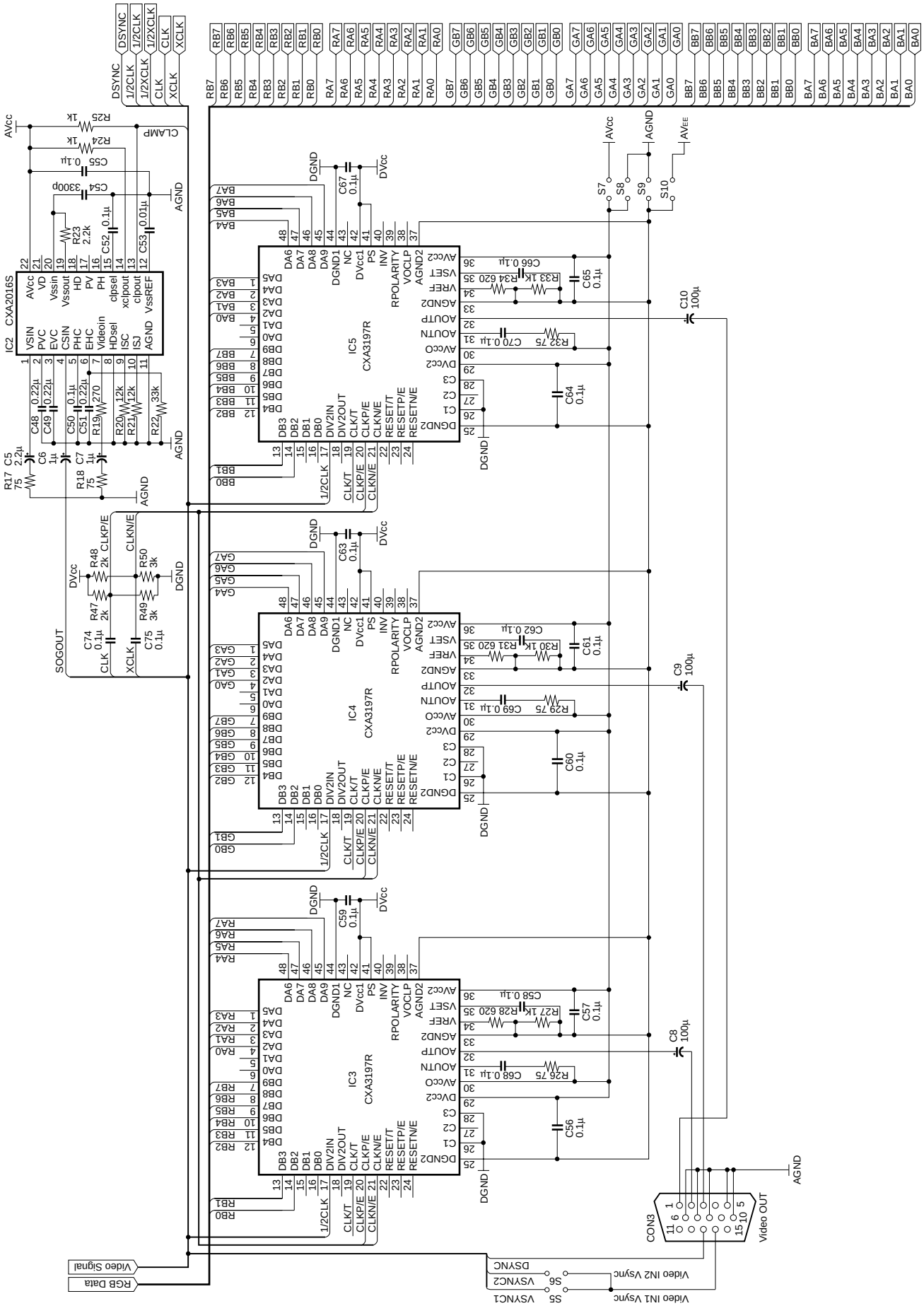
2. If the CXA3506R does not move even after item 1 above is checked, it is possible that the control signals of the control register are not output from the PC printer board. In this case, be sure to re-check the board settings listed for item 4 under "Program Installation and Startup".

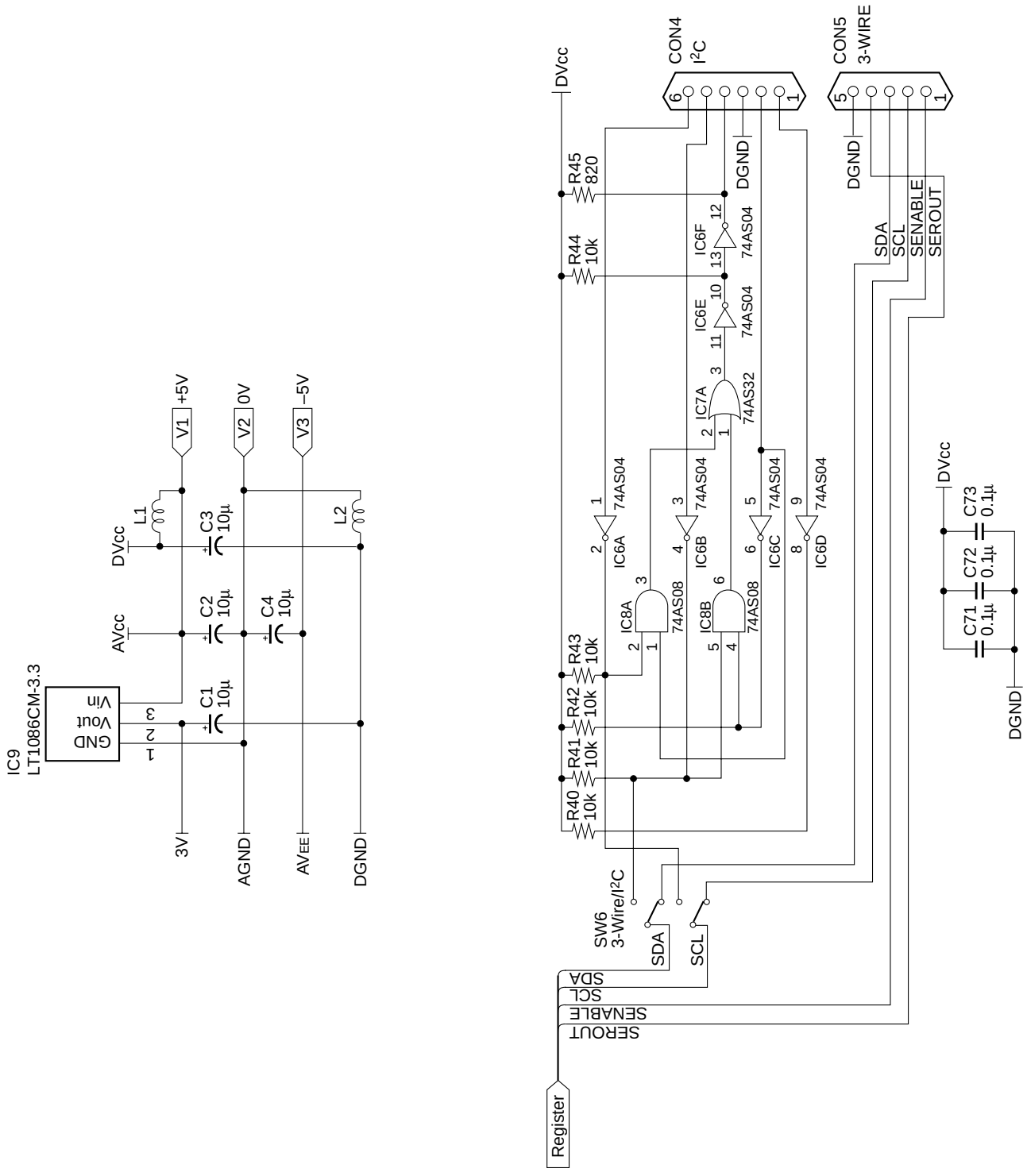
CXA3506R Evaluation Board Parts List

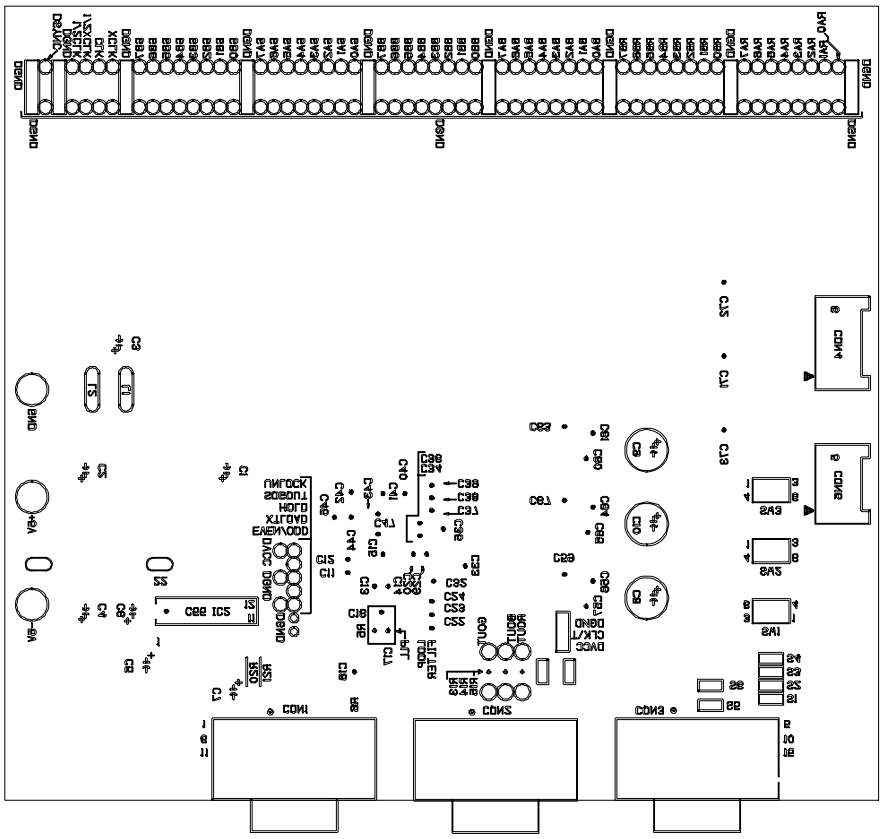
Parts No.	Product name	Manufacturer
IC1	CXA3506R	SONY
IC2	CXA2016S	SONY
IC3, 4, 5	CXA3197R	SONY
IC6	SN74LS04N	Texas Instruments
IC7	SN74LS32N	Texas Instruments
IC8	SN74LS08N	Texas Instruments
IC9	LT1086CM-3.3	Linear Technology
CON1, 2, 3	D02-N15SAG-13L9	SANSHIN ELECTRONICS
CON4	53053-0510	Molex
CON5	53053-0610	Molex
SW1	G-12AP	NIHON KAIHEIKI IND.
SW2	G-13AP	NIHON KAIHEIKI IND.
SW3	G-22AP	NIHON KAIHEIKI IND.
L1, 2	ZBF503D-00	TDK

R1, 2	620	Chip resistor	C1 to 4	10µ	Tantalum capacitor
R3, 4	200	Chip resistor	C5	2.2µ	Tantalum capacitor
R5	3.3k	Chip metal film resistor	C6, 7	1µ	Tantalum capacitor
R6	3k	Lead metal film resistor	C8 to 10	100µ	Electrolytic capacitor
R7 to 12	75	Chip resistor	C11, 12	0.1µ	Chip capacitor
R13 to 15	820	Chip resistor	C13, 14	100p	Chip capacitor
R17, 18	75	Chip resistor	C15	0.1µ	Chip capacitor
R19	270	Chip resistor	C16	330p	Chip capacitor
R20, 21	12k	Lead metal film resistor	C17	0.33µ	Chip capacitor
R22	33k	Chip resistor	C18 to 34	0.1µ	Chip capacitor
R23	2.2k	Chip resistor	C35	1µ	Chip capacitor
R24, 25, 27	1k	Chip resistor	C36 to 44	0.1µ	Chip capacitor
R26, 29, 32	75	Chip resistor	C45	1µ	Chip capacitor
R28, 31, 34	620	Chip resistor	C47	0.1µ	Chip capacitor
R30, 33	1k	Chip resistor	C48, 49	0.22µ	Chip capacitor
R35 to 37	24k	Chip resistor	C50	0.1µ	Chip capacitor
R38, 39	24k	Chip resistor	C51	0.22µ	Chip capacitor
R40 to 44	10k	Chip resistor	C52	0.1µ	Chip capacitor
R45	820	Chip resistor	C53	0.01µ	Chip capacitor
R47, 48	2k	Chip resistor	C54	3300p	Chip capacitor
R49, 50	3k	Chip resistor	C55 to 70	0.1µ	Chip capacitor
			C71 to 75	0.1µ	Chip capacitor

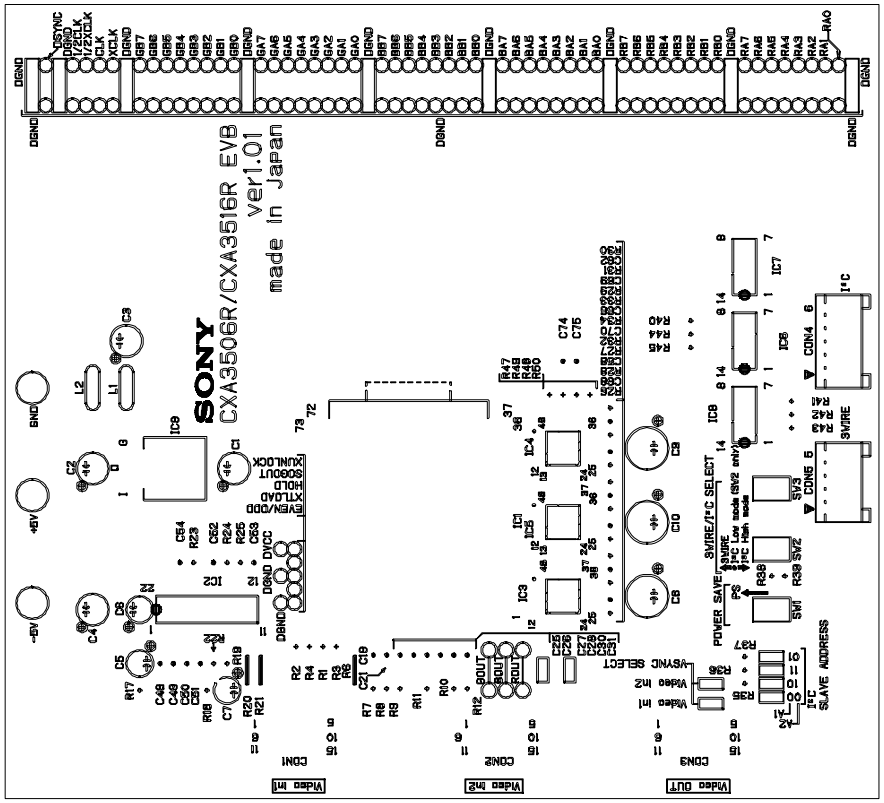

Video Signal
RGB Data
Register
IC1
CXA3506R
CON1
CON2
Video IN1
Video IN2
SW1
XPOWER SAVE
SW2
3-Wire/I2C
Slave address
100100 00
100100 10
100100 11
100100 01
DVcc
AVcc
AGND
DGND
CLAMP
VSYNC1
VSYNC2


IC2 CXA2016S
IC3 CXA3197R
IC4 CXA3197R
IC5 CXA3197R
CON3
Video OUT
Video Signal
RGB Data
Video IN1 Vsync
Video IN2 Vsync
SOGOUT
CLAMP
AGND
DGND
DVcc
AVcc
AVEE
DSYNC
1/2CLK
1/2XCLK
CLK
XCLK
S5
S6
S7
S8
S9
S10
VSYNC1
VSYNC2

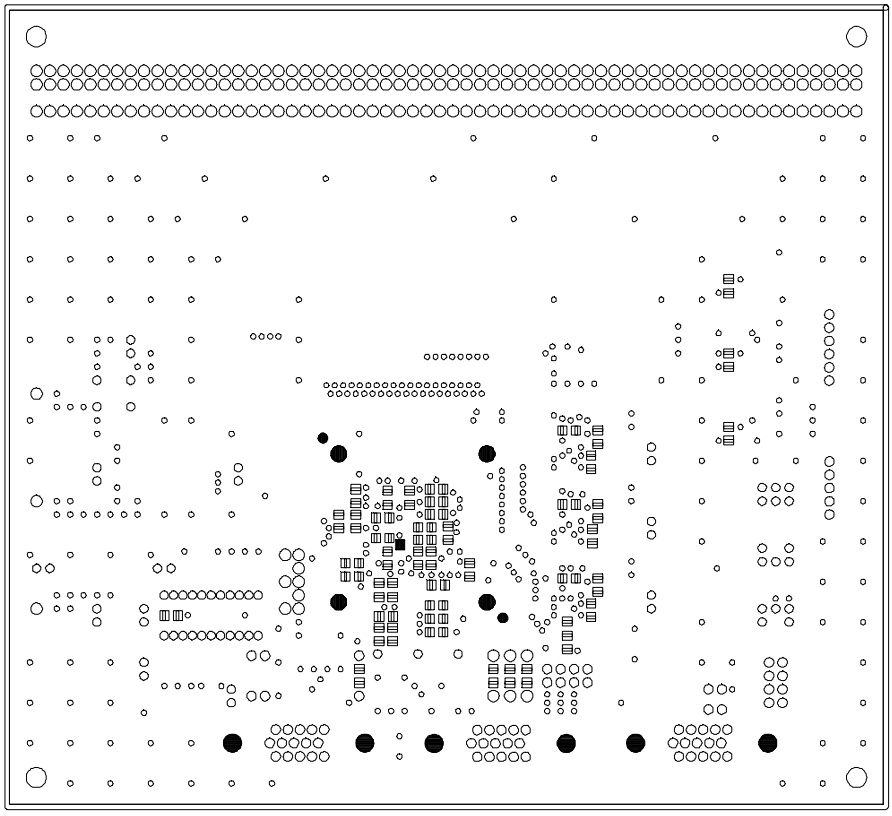

IC9
LT1086CM-3.3
GND
Vout
Vin
3
2
1
C1 10µ
C2 10µ
C3 10µ
C4 10µ
L1
L2
DVcc
AVcc
V1 +5V
V2 0V
V3 −5V
3V
AGND
AVEE
DGND
CON4
I²C
CON5
3-WIRE
R45 820
R44 10k
R43 10k
R42 10k
R41 10k
R40 10k
IC6A 74AS04
IC6B 74AS04
IC6C 74AS04
IC6D 74AS04
IC6E 74AS04
IC6F 74AS04
IC7A 74AS32
IC8A 74AS08
IC8B 74AS08
C71 0.1µ
C72 0.1µ
C73 0.1µ
SW6
3-Wire/I²C
SDA
SCL
SENABLE
SEROUT
Register



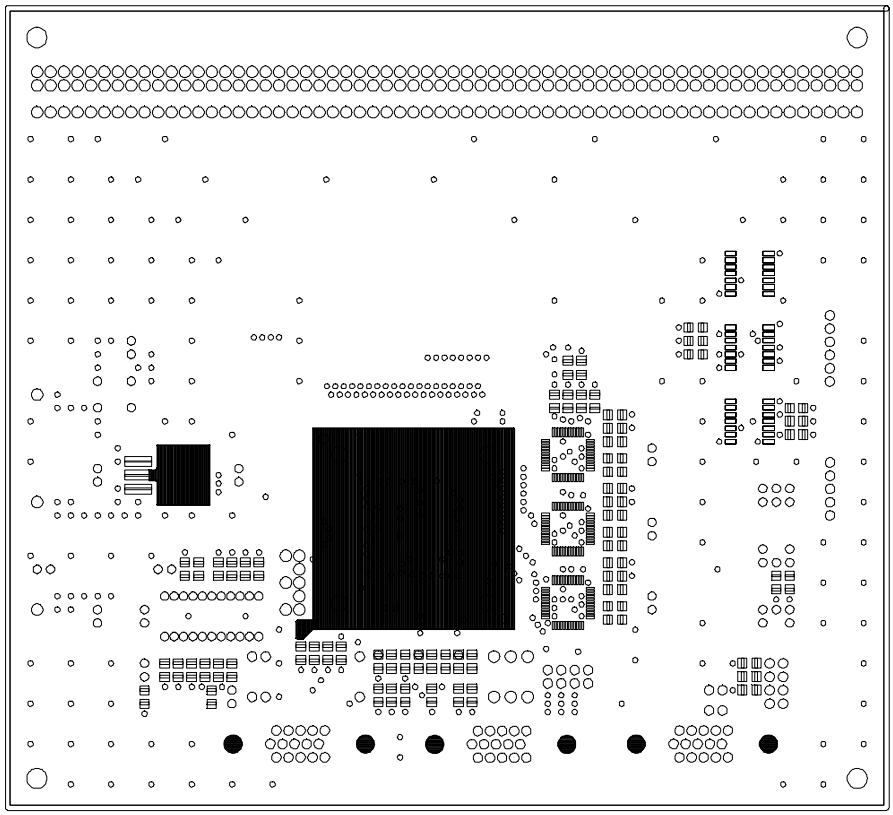
3506RVIF G5



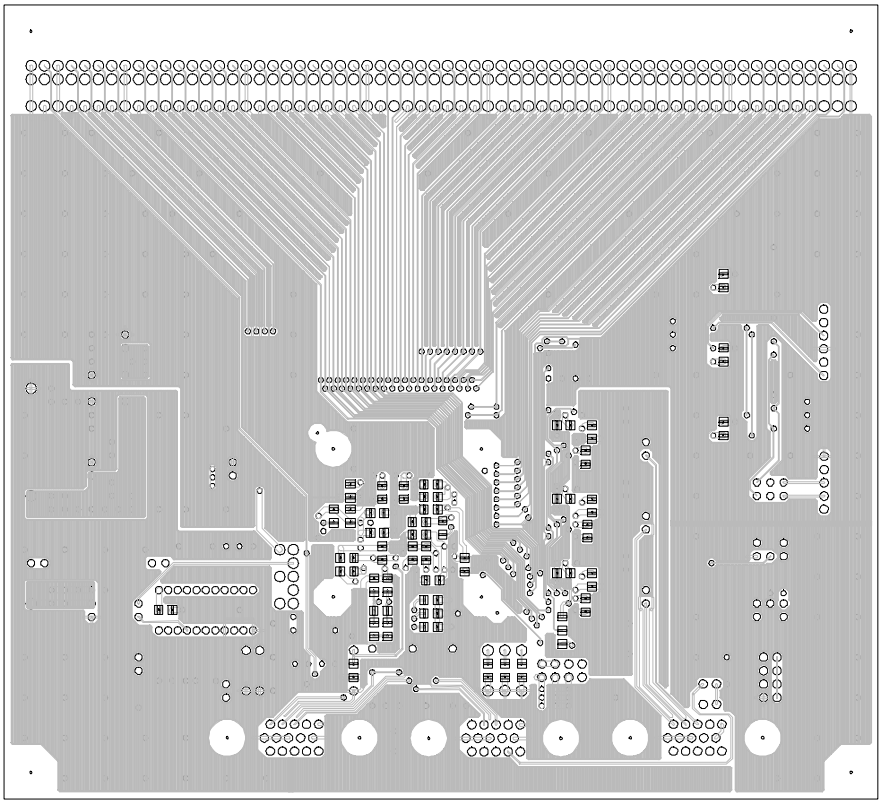
3506RVIF G4

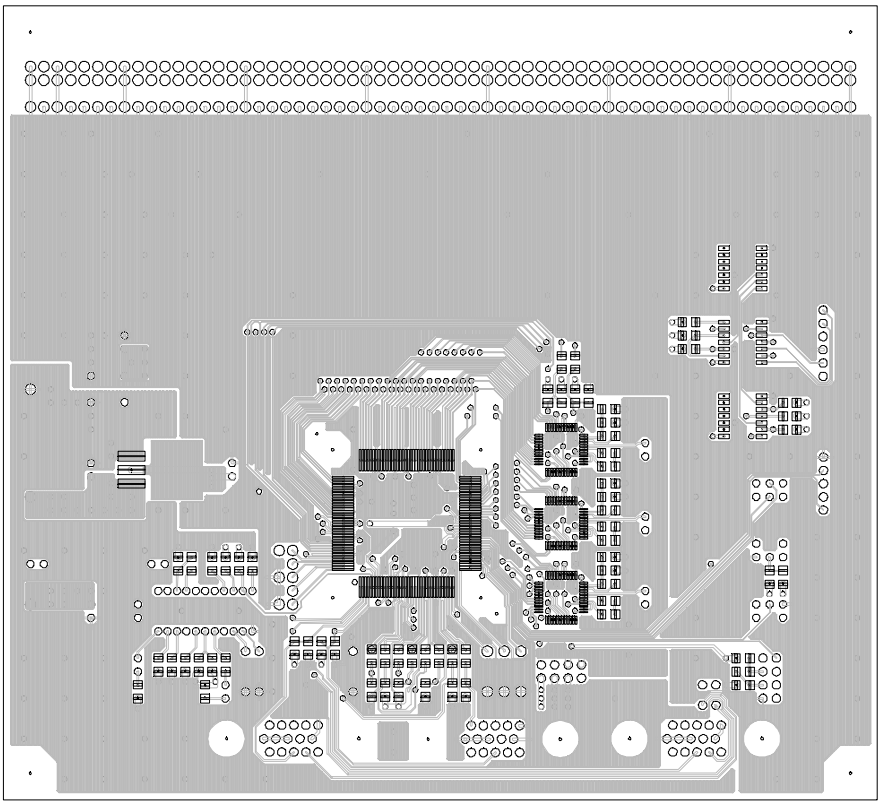


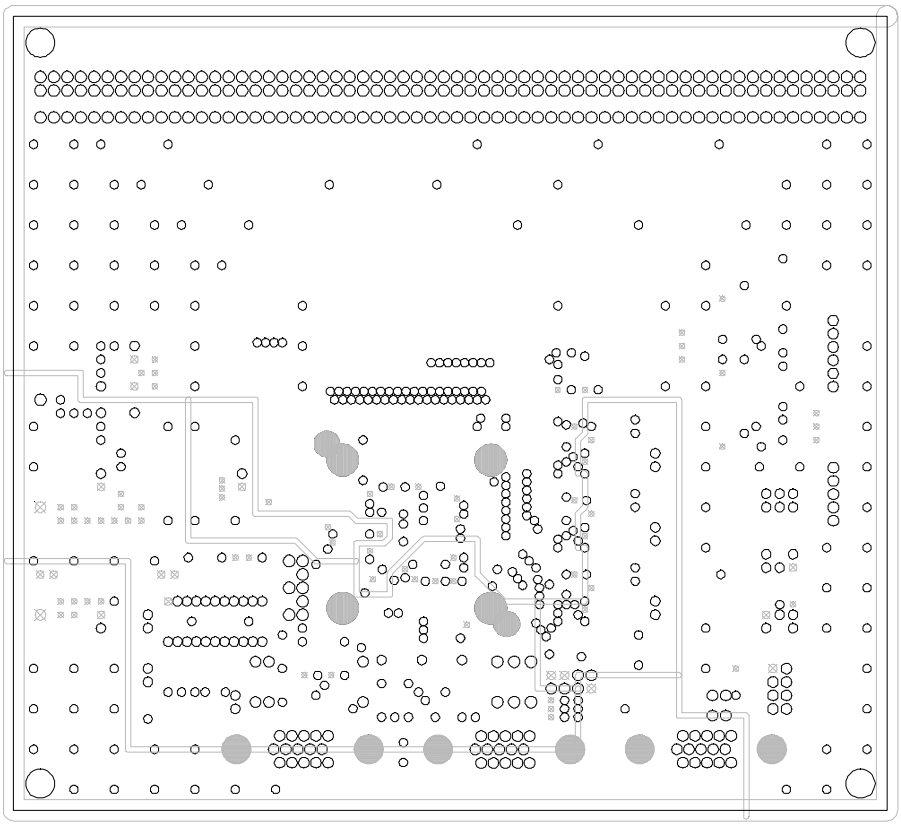
3506RVIF G7

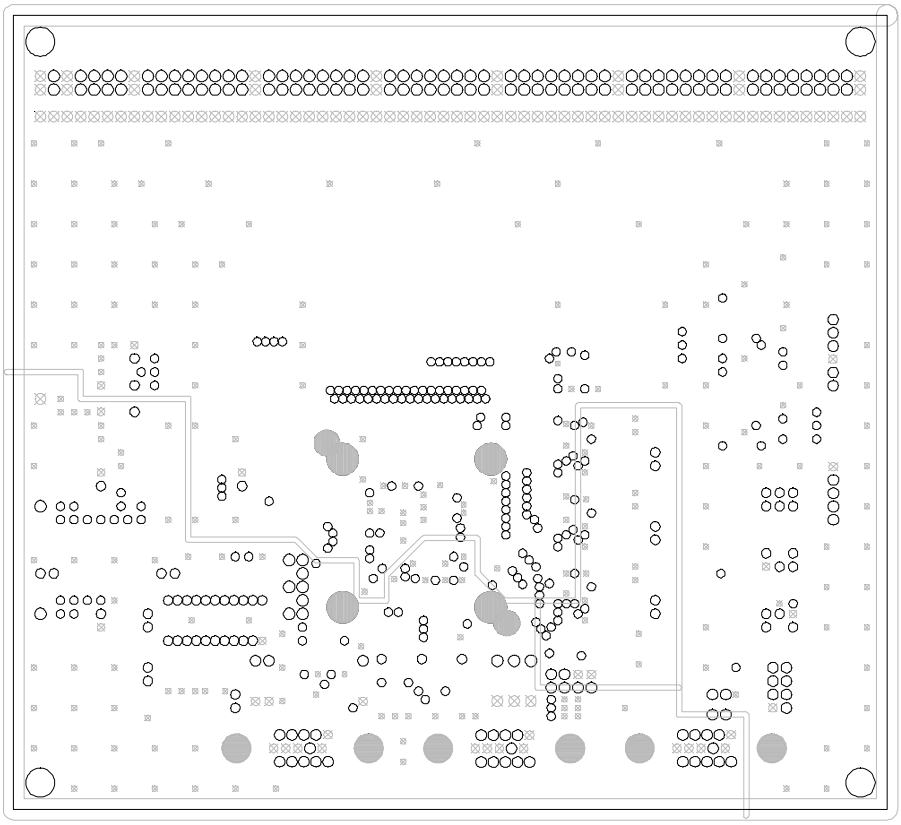


3506RVIF G6


3506RVIF G3

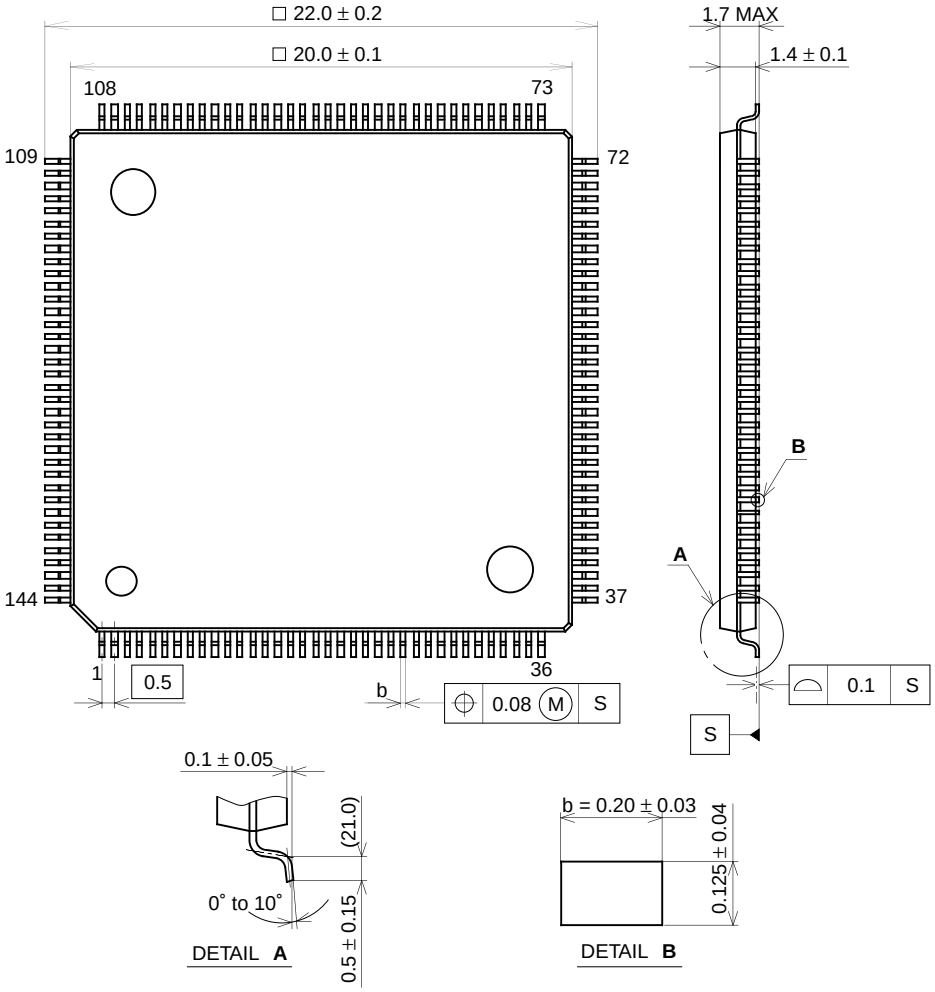

3506RVIF G2


350GRVIF GB
. VCC(L2)


350GRVIF GB
. GND(L3)

Package Outline Unit: mm

144PIN LQFP (PLASTIC)



SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.3 g