12-BIT, OCTAL, ULTRALOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **2.7-V to 5.5-V Single Supply**
- **12-Bit Linearity and Monotonicity**
- **Rail-to-Rail Voltage Output**
- **Settling Time: 5 µs (Max)**
- **Ultralow Glitch Energy: 0.1 nVs**
- **Ultralow Crosstalk: –100 dB**
- **Low Power: 1.8 mA (Max)**
- **Per-Channel Power Down: 2 µA (Max)**
- **Power-On Reset to Zero Scale and Mid Scale**
- **SPI-Compatible Serial Interface: Up to 50 MHz**
- **Simultaneous or Sequential Update**
- **Asynchronous Clear**
- **Binary and Twos-Complement Capability**
- **Daisy-Chain Operation**
- **1.8-V to 5.5-V Logic Compatibility**
- **Specified Temperature Range: –40°C to 105°C**
- **Small, 5-mm x 5-mm, 32-Lead QFN Package**

APPLICATIONS

- **Portable Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**
- **Programmable Attenuators**
- **Industrial Process Control**

DESCRIPTION

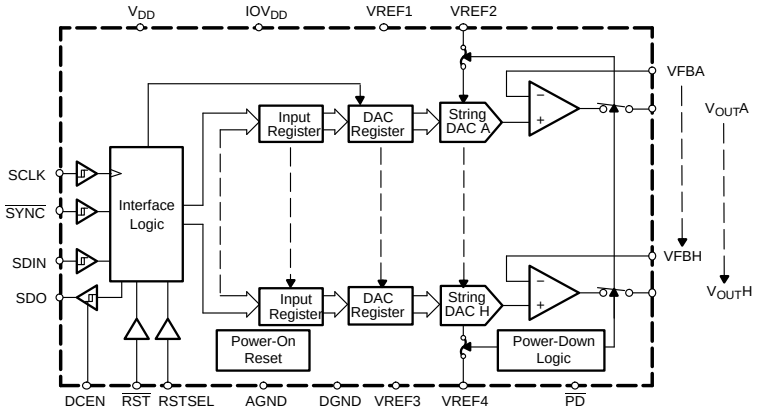
The DAC7558 is a 12-bit, octal-channel, voltage output DAC with exceptional linearity and monotonicity. Its proprietary architecture minimizes undesired transients such as code to code glitch and channel to channel crosstalk. The low-power DAC7558 operates from a single 2.7-V to 5.5-V supply. The DAC7558 output amplifiers can drive a 2-kΩ, 200-pF load rail-to-rail with 5-µs settling time; the output range is set using an external voltage reference.

The 3-wire serial interface operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire™, and DSP interface standards. The outputs of all DACs may be updated simultaneously or sequentially. The parts incorporate a power-on-reset circuit to ensure that the DAC outputs power up to zero volts and remain there until a valid write cycle to the device takes place. The parts contain a power-down feature that reduces the current consumption of the device to under 2 µA.

The small size and low-power operation makes the DAC7558 ideally suited for battery-operated portable applications. The power consumption is typically 7.5 mW at 5 V, 3.7 mW at 3 V, and reduces to 1 µW in power-down mode.

The DAC7558 is available in a 32-lead QFN package and is specified over –40°C to 105°C.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Microwire is a trademark of National Semiconductor Corp..

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC7558	32 QFN	RHB	–40°C TO 105°C	D758	DAC7558IRHBT	250-piece Tape and Reel
					DAC7558IRHBR	3000-piece Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
V_{DD} to GND	–0.3 V to 6 V
Digital input voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{out} to GND	–0.3 V to V_{DD}+ 0.3 V
Operating temperature range	–40°C to 105°C
Storage temperature range	–65°C to 150°C
Junction temperature (T_J Max)	150°C

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, VREF = VDD, R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to 105°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE(1)					
Resolution			12		Bits
Relative accuracy			±0.35	±1	LSB
Differential nonlinearity	Specified monotonic by design		±0.08	±0.5	LSB
Offset error				±12	mV
Zero-scale error	All zeroes loaded to DAC register			±12	mV
Gain error	V_{DD} = 5 V, V_{REF} = 4.096 V			±0.15	%FSR
Full-scale error	V_{DD} = 5 V, V_{REF} = 4.096 V			±0.5	%FSR
Zero-scale error drift			7		µV/°C
Gain temperature coefficient			3		ppm of FSR/°C
PSRR	V_{DD} = 5 V		0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output voltage range		0		VREF	V
Output voltage settling time	R_L = 2 kΩ; 0 pF < C_L < 200 pF			5	µs
Slew rate			1.8		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2 kΩ		1000		
Digital-to-analog glitch impulse	1 LSB change around major carry		0.1		nV-s
Channel-to-channel crosstalk	1-kHz full-scale sine wave, outputs unloaded		–100		dB
Digital feedthrough			0.1		nV-s
Output noise density (10-kHz offset frequency)			120		nV/rtHz
Total harmonic distortion	F_{OUT} = 1 kHz, F_S = 1 MSPS, BW = 20 kHz		–85		dB
DC output impedance			1		Ω
Short-circuit current	V_{DD} = 5 V		50		mA
	V_{DD} = 3 V		20		
Power-up time	Coming out of power-down mode, V_{DD} = 5 V		15		µs
	Coming out of power-down mode, V_{DD} = 3 V		15		
REFERENCE INPUT					
V_{REF} Input range		0		V_{DD}	V
Reference input impedance	V_{REF}1 through V_{REF}4 shorted together		12.5		kΩ
Reference current	V_{REF} = V_{DD} = 5 V, V_{REF}1 through V_{REF}4 shorted together		400	650	µA
	V_{REF} = V_{DD} = 3 V, V_{REF}1 through V_{REF}4 shorted together		240	425	
LOGIC INPUTS(2)					
Input current				±1	µA
V_{IN_L}, Input low voltage	IOV_{DD} ≥ 2.7 V			0.3 IOV_{DD}	V
V_{IN_H}, Input high voltage	IOV_{DD} ≥ 2.7 V	0.7 IOV_{DD}			V
Pin capacitance				3	pF

(1) Linearity tested using a reduced code range of 30 to 4065; output unloaded.
(2) Specified by design and characterization, not production tested. For 1.8 V < IOV_{DD} < 2.7 V, it is recommended that V_{IH} = IOV_{DD} , V_{IL} = GND.

ELECTRICAL CHARACTERISTICS (Continued)

V_{DD} = 2.7 V to 5.5 V, VREF = VDD, R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to 105°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS					
V_{DD}, IOV_{DD} (1)		2.7		5.5	V
I_{DD}(normal operation)	DAC active and excluding load current				
V_{DD} = 3.6 V to 5.5 V	V_{IH} = IOV_{DD} and V_{IL} = GND		1.1	1.8	mA
V_{DD} = 2.7 V to 3.6 V			1	1.7	
I_{DD} (all power-down modes)					
V_{DD} = 3.6 V to 5.5 V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.2	2	µA
V_{DD} = 2.7 V to 3.6 V			0.05	2	
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2 mA, V_{DD} = 5 V		93%		

(1) IOV_{DD} operates down to 1.8 V with slightly degraded timing, as long as V_{IH} = IOV_{DD} and V_{IL} = GND.

TIMING CHARACTERISTICS[1][2]

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND; all specifications –40°C to 105°C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_1[3]	SCLK cycle time	V_{DD} = 2.7 V to 3.6 V	20			ns
		V_{DD} = 3.6 V to 5.5 V	20			
t_2	SCLK HIGH time	V_{DD} = 2.7 V to 3.6 V	10			ns
		V_{DD} = 3.6 V to 5.5 V	10			
t_3	SCLK LOW time	V_{DD} = 2.7 V to 3.6 V	10			ns
		V_{DD} = 3.6 V to 5.5 V	10			
t_4	$\overline{SYNC}$ falling edge to SCLK falling edge setup time	V_{DD} = 2.7 V to 3.6 V	4			ns
		V_{DD} = 3.6 V to 5.5 V	4			
t_5	Data setup time	V_{DD} = 2.7 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	V_{DD} = 2.7 V to 3.6 V	4.5			ns
		V_{DD} = 3.6 V to 5.5 V	4.5			
t_7	SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7 V to 3.6 V	20			ns
		V_{DD} = 3.6 V to 5.5 V	20			
t_9	SCLK falling edge to SDO valid	V_{DD} = 2.7 V to 3.6 V	10			ns
		V_{DD} = 3.6 V to 5.5 V	10			
t_{10}	$\overline{CLR}$ pulse width low	V_{DD} = 2.7 V to 3.6 V	10			ns
		V_{DD} = 3.6 V to 5.5 V	10			

(1) All input signals are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Serial Write Operation timing diagram Figure 1.
(3) Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V.

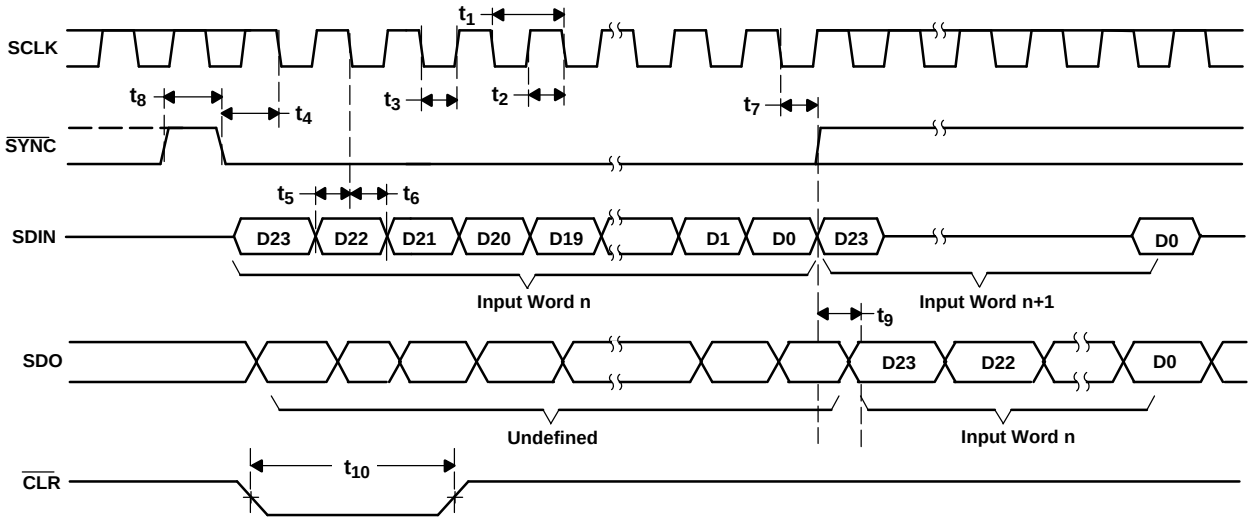
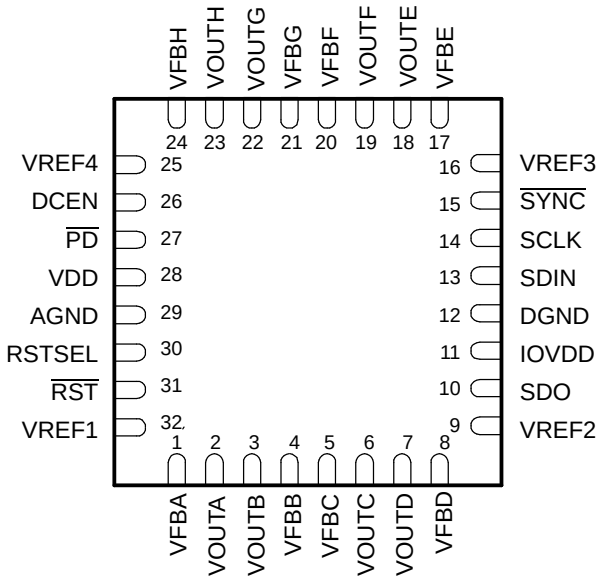


Figure 1. Serial Write Operation

PIN DESCRIPTION

RHB PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		DESCRIPTION
NO.	NAME	
1	VFBA	DAC A amplifier sense input
2	VOUTA	Analog output voltage from DAC A
3	VOUTB	Analog output voltage from DAC B
4	VFBB	DAC B amplifier sense input
5	VFBC	DAC C amplifier sense input
6	VOUTC	Analog output voltage from DAC C
7	VOUTD	Analog output voltage from DAC D
8	VFBD	DAC D amplifier sense input
9	VREF2	Positive reference voltage input for DAC C and DAC D
10	SDO	Serial data output
11	IOVDD	I/O voltage supply input
12	DGND	Digital ground
13	SDIN	Serial data input
14	SCLK	Serial clock input
15	$\overline{\text{SYNC}}$	Frame synchronization input. The falling edge of the $\overline{\text{SYNC}}$ pulse indicates the start of a serial data frame shifted out to the DAC7558.
16	VREF3	Positive reference voltage input for DAC E and DAC F
17	VFBE	DAC E amplifier sense input
18	VOUTE	Analog output voltage from DAC E
19	VOUTF	Analog output voltage from DAC F
20	VFBF	DAC F amplifier sense input
21	VFBG	DAC G amplifier sense input
22	VOUTG	Analog output voltage from DAC G
23	VOUTH	Analog output voltage from DAC H
24	VFBH	DAC H amplifier sense input

PIN DESCRIPTION (continued)

Terminal Functions (continued)

25	VREF4	Positive reference voltage input for DAC G and DAC H
26	DCEN	Daisy-chain enable
27	$\overline{PD}$	Power down
28	VDD	Analog voltage supply input
29	AGND	Analog ground
30	RSTSEL	Reset select. If this pin is low, input coding is binary; if high, then 2s compliment.
31	$\overline{RST}$	Asynchronous reset. Active low. If $\overline{RST}$ pin is low, all DAC channels reset either to zero scale (RSTSEL = 0) or to midscale (RSTSEL = 1).
32	VREF1	Positive reference voltage input for DAC A and DAC B

TYPICAL CHARACTERISTICS

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

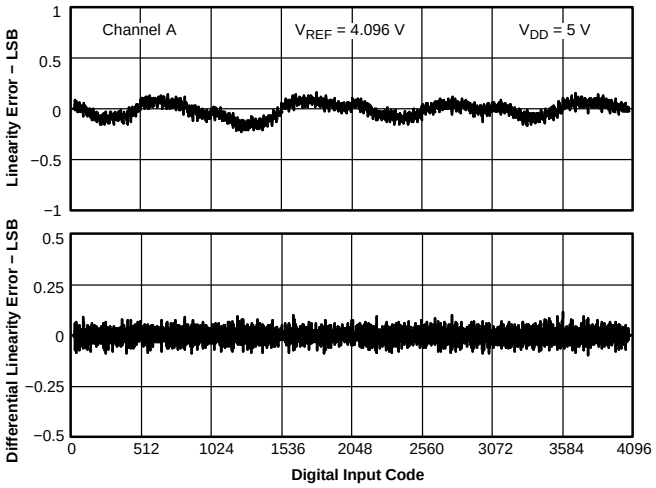


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

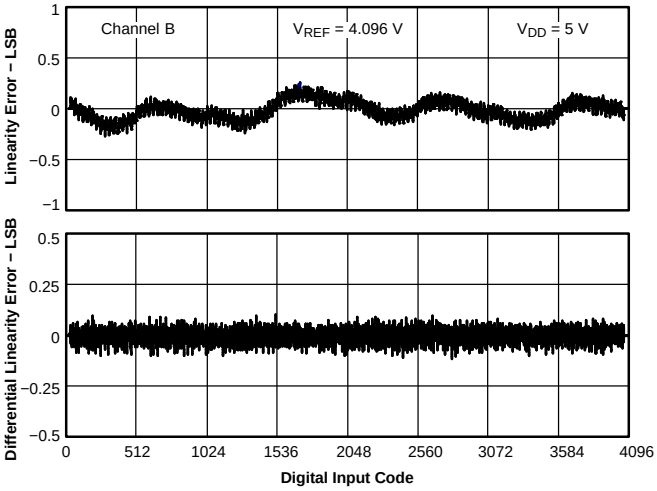


Figure 3.

TYPICAL CHARACTERISTICS (continued)

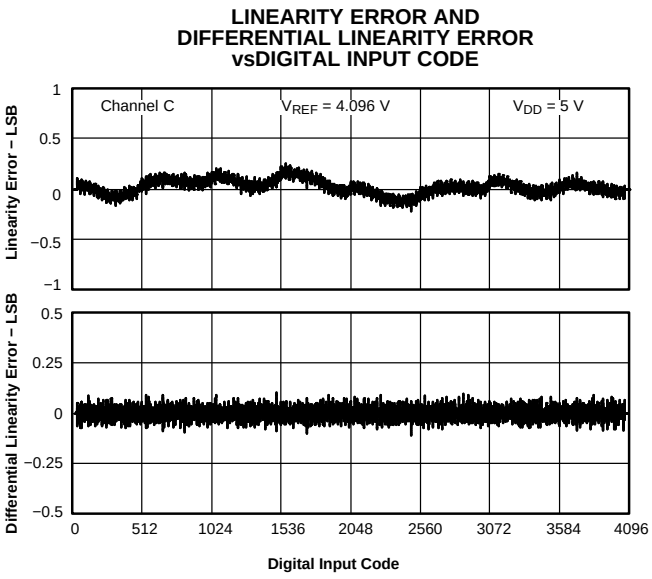


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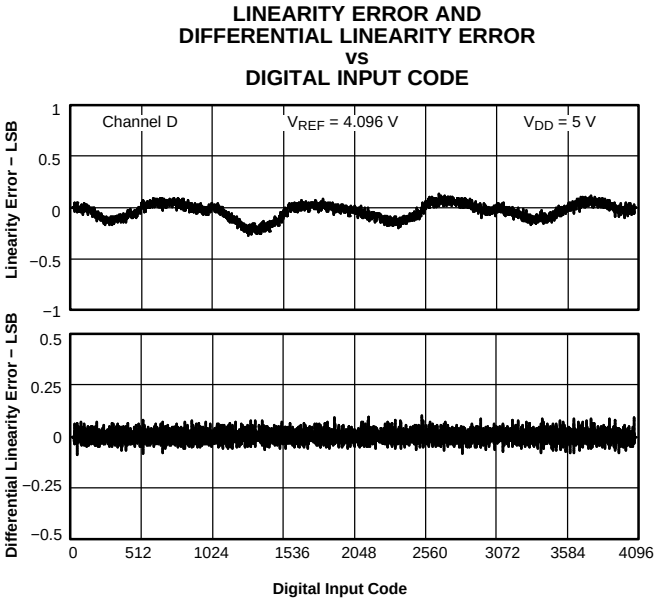


Figure 5.

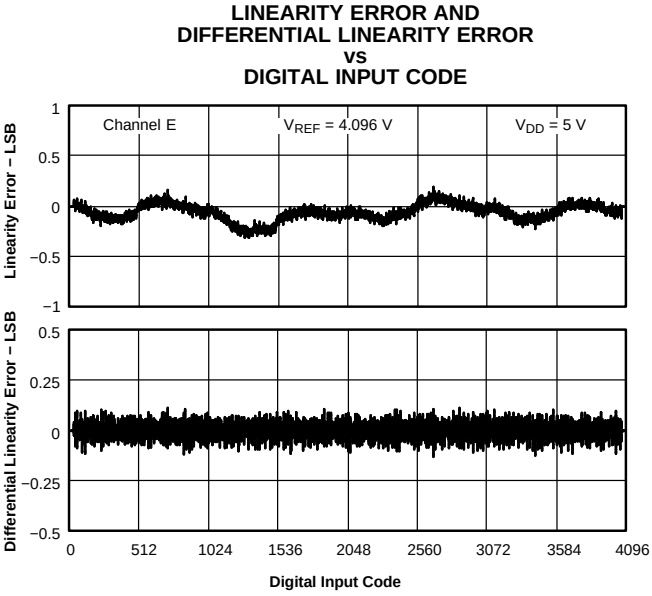


Figure 6.

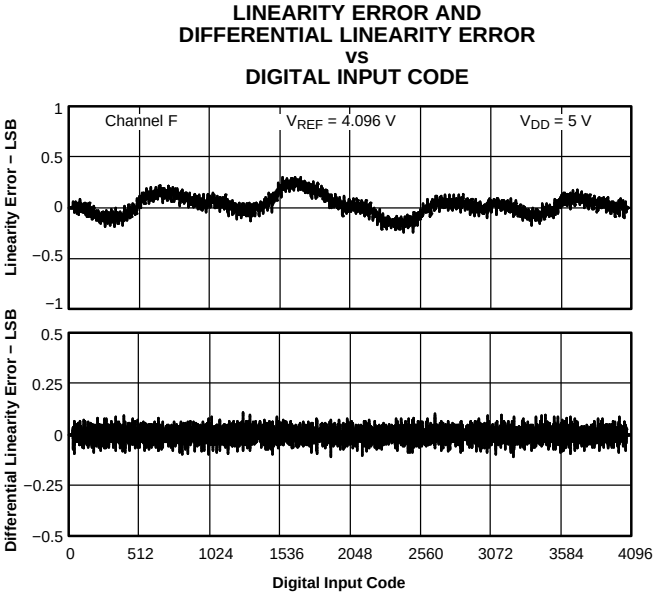


Figure 7.

TYPICAL CHARACTERISTICS (continued)

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

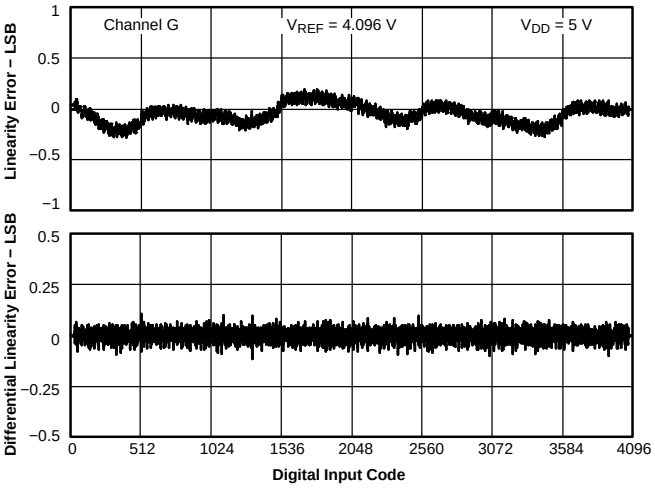


Figure 8.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

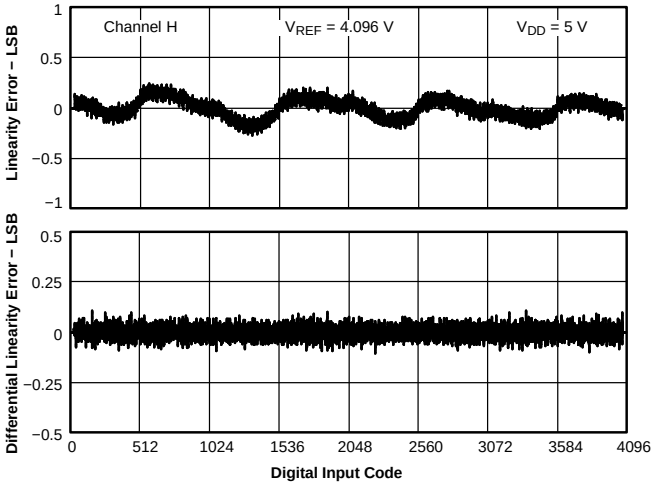


Figure 9.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

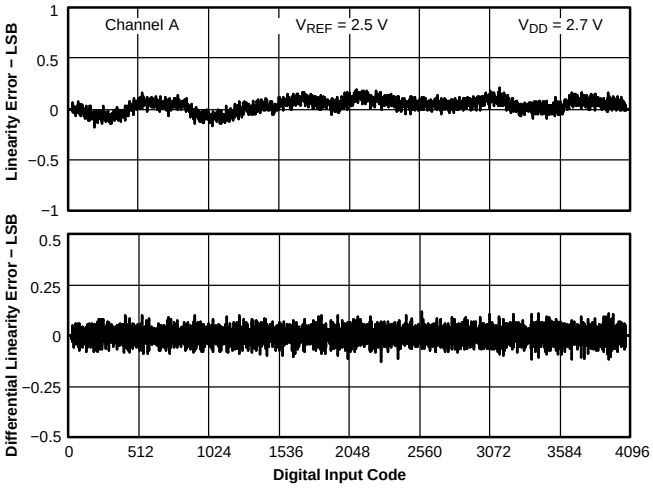


Figure 10.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

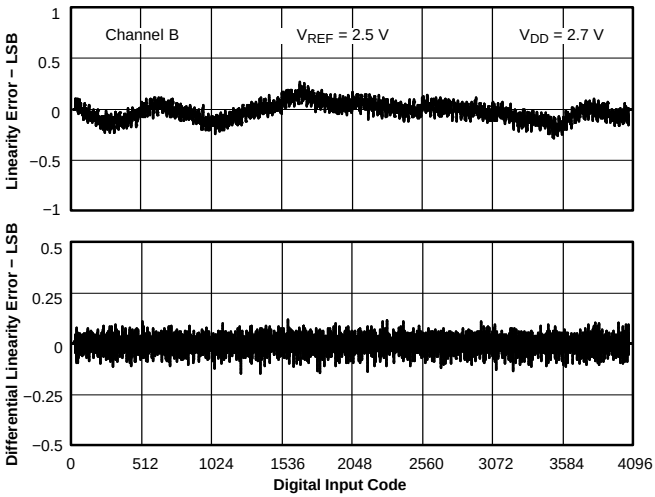


Figure 11.

TYPICAL CHARACTERISTICS (continued)

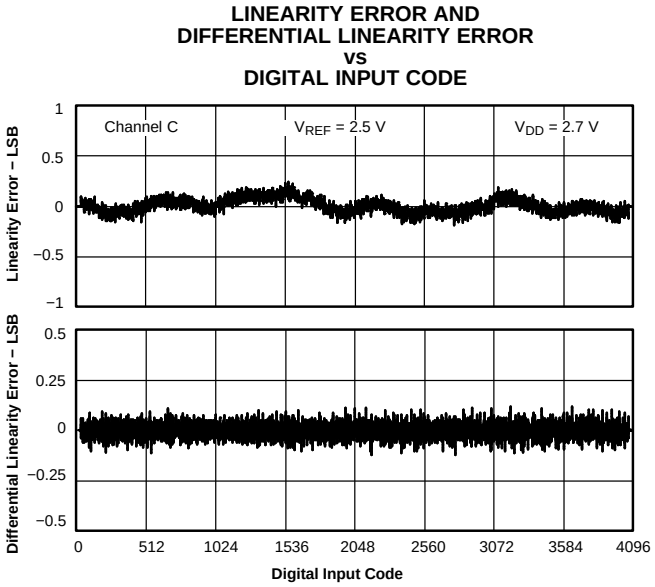


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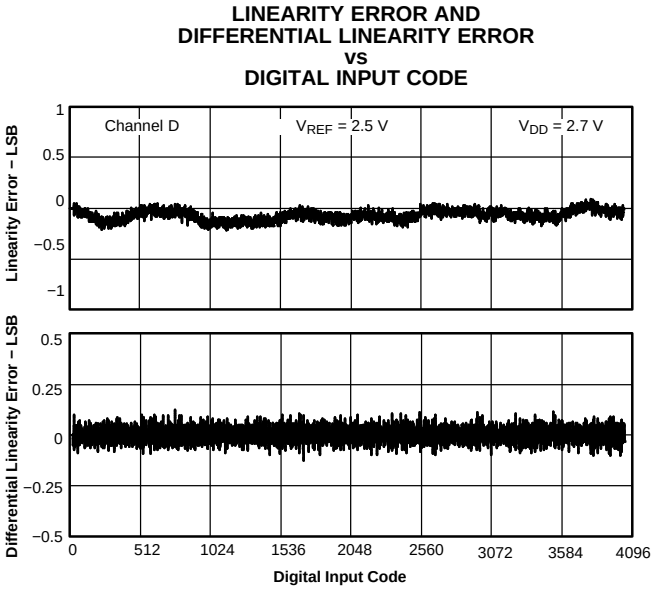


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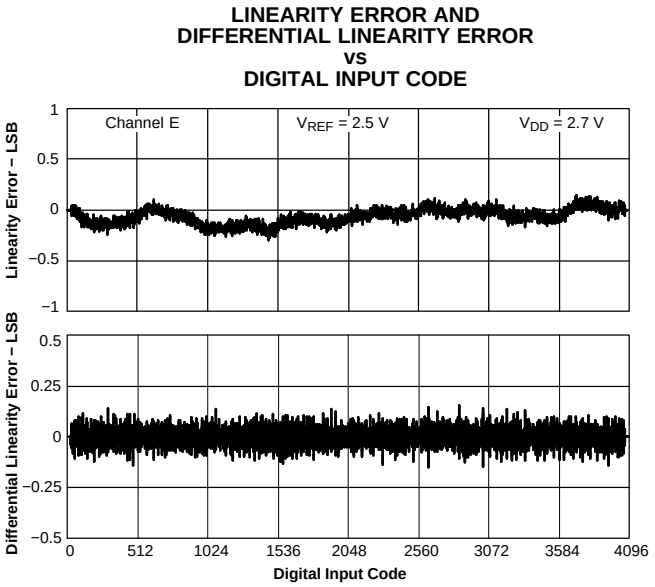


Figure 14.

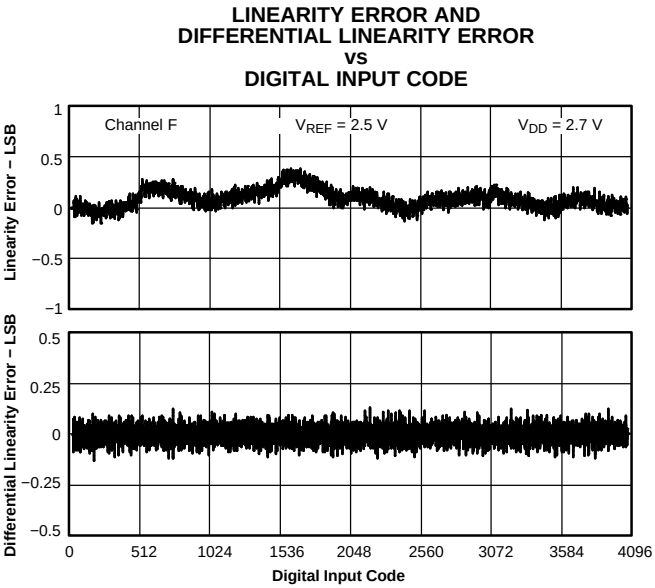


Figure 15.

TYPICAL CHARACTERISTICS (continued)

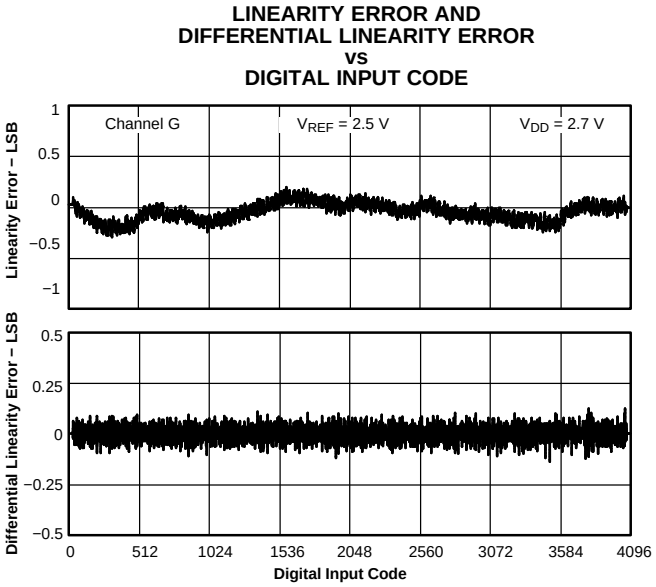


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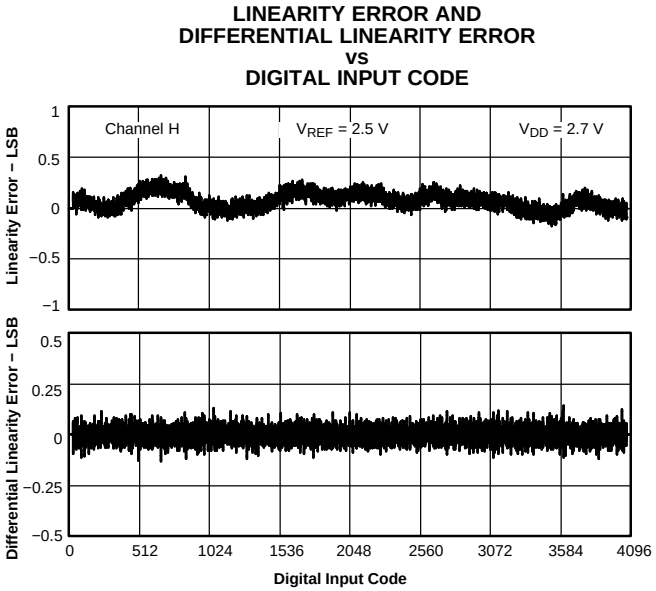


Figure 17.

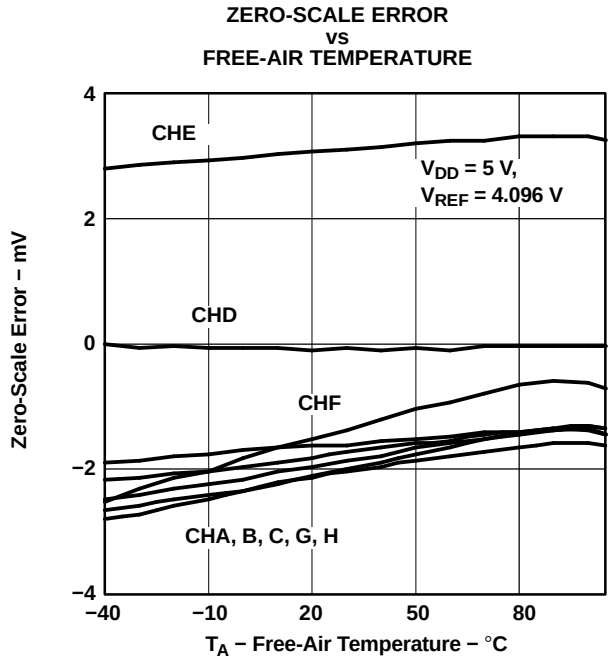


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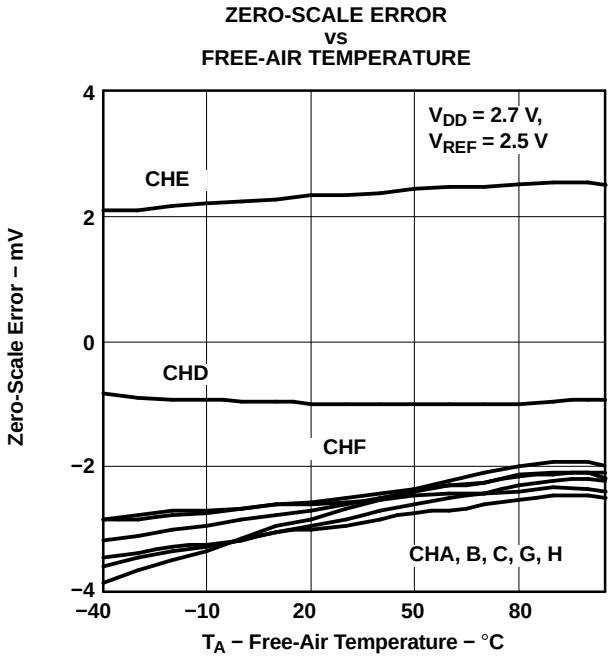


Figure 19.

TYPICAL CHARACTERISTICS (continued)

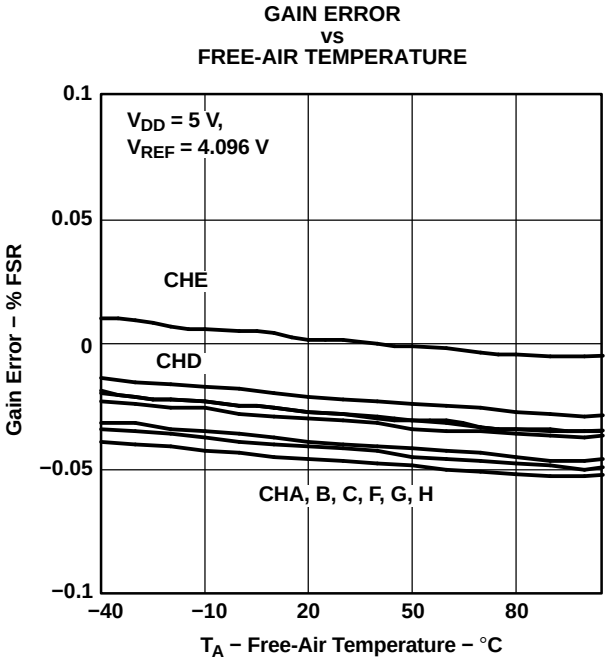


Figure 20.

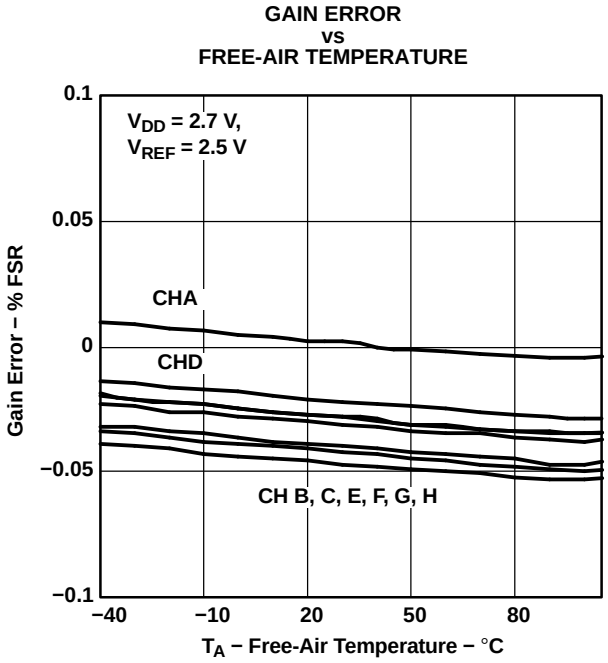


Figure 21.

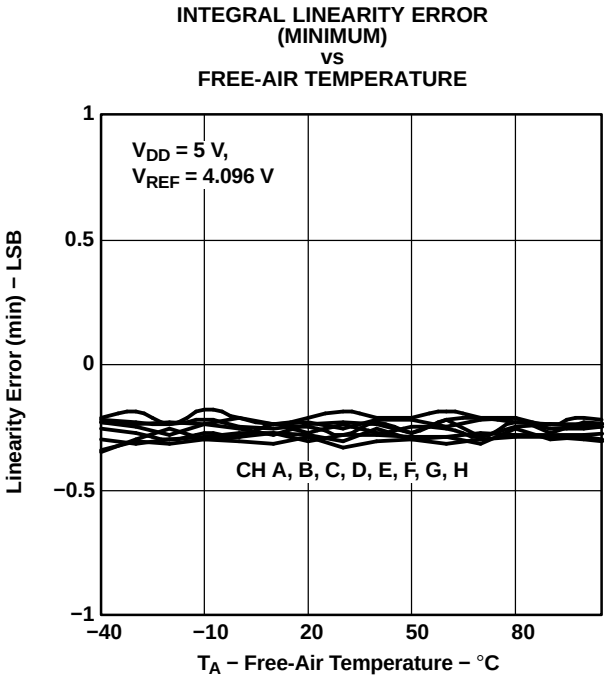


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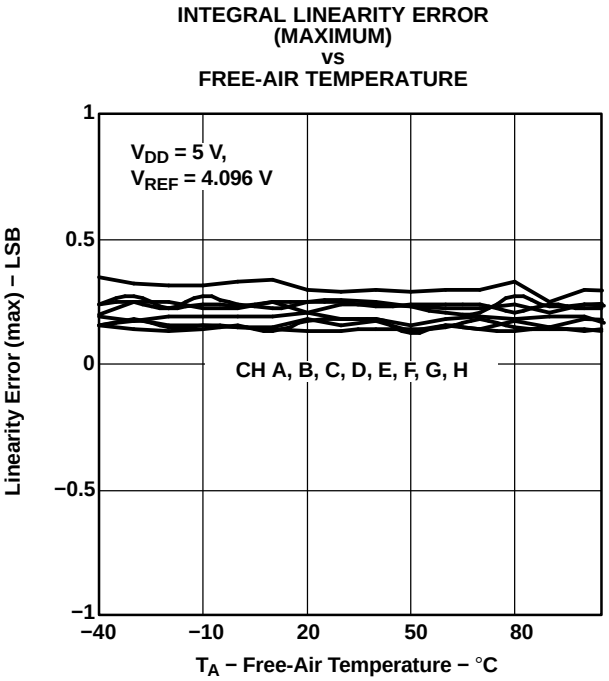


Figure 23.

TYPICAL CHARACTERISTICS (continued)

SINK CURRENT AT NEGATIVE RAIL

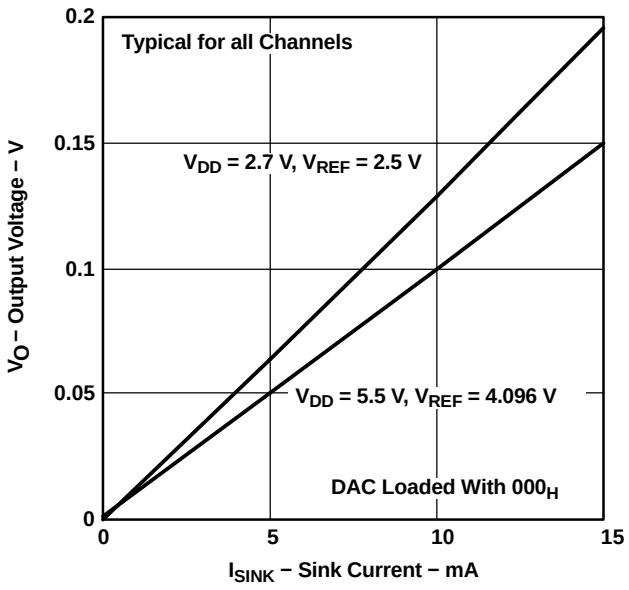


Figure 24.

SOURCE CURRENT AT POSITIVE RAIL

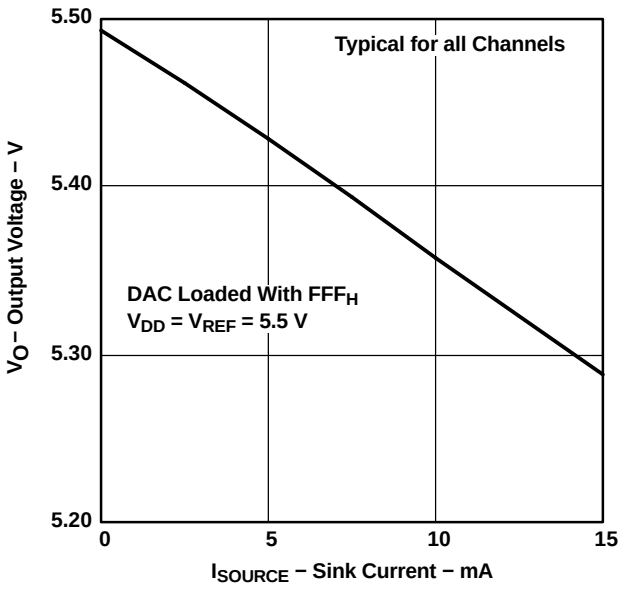


Figure 25.

SOURCE CURRENT AT POSITIVE RAIL

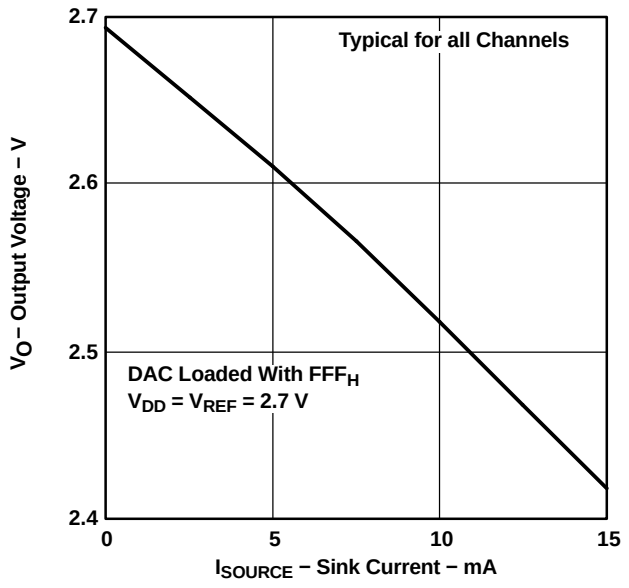


Figure 26.

SUPPLY CURRENT
vs
DIGITAL INPUT CODE

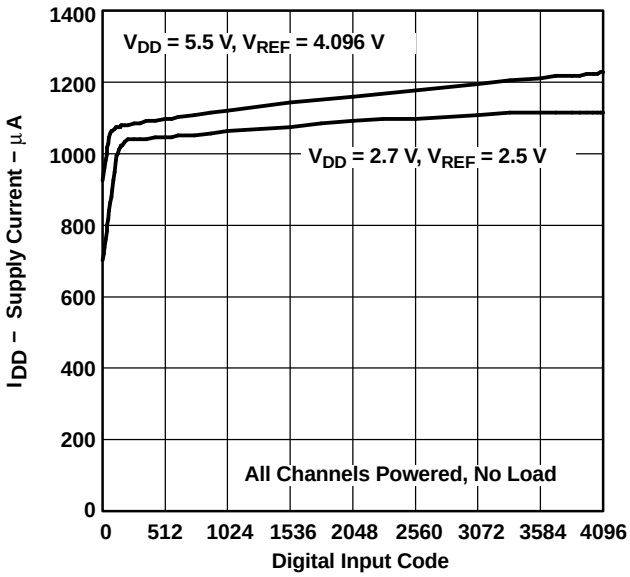


Figure 27.

TYPICAL CHARACTERISTICS (continued)

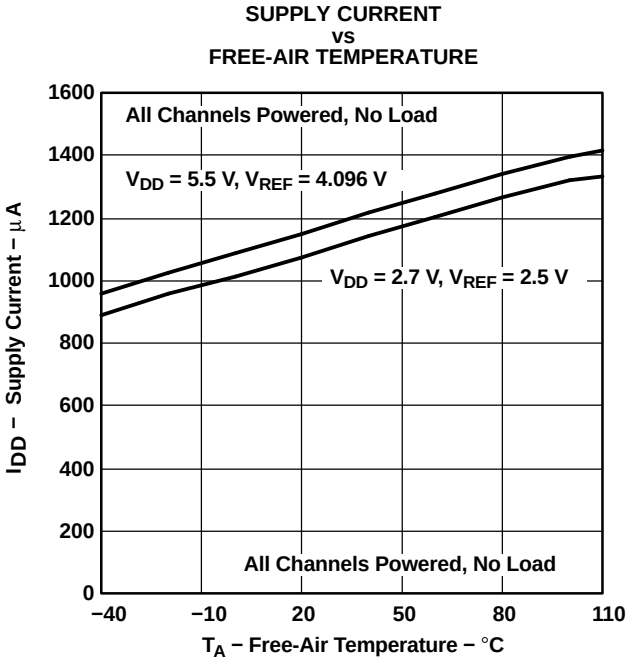


Figure 28.

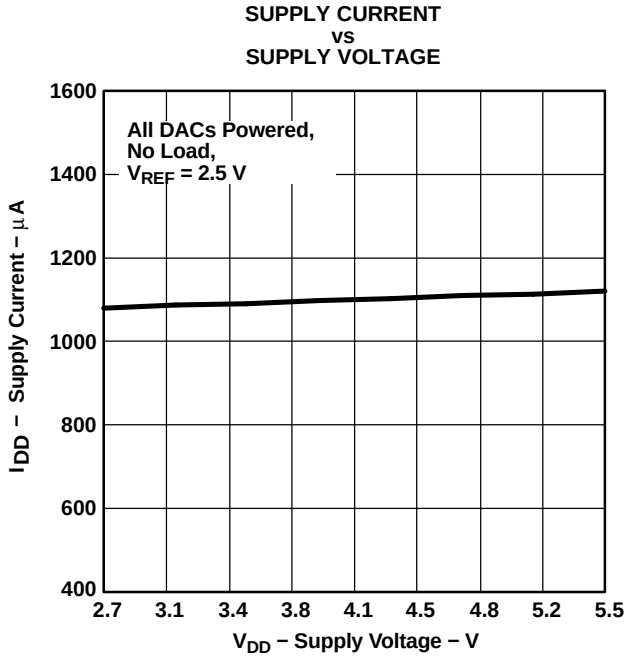


Figure 29.

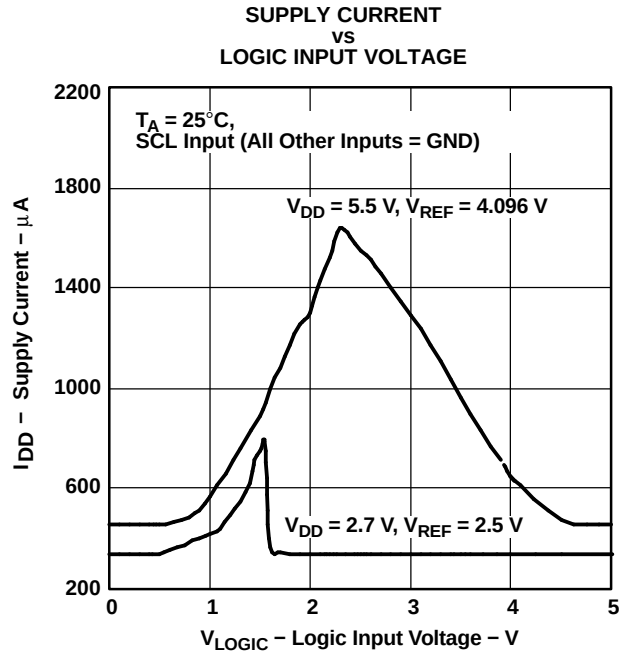


Figure 30.

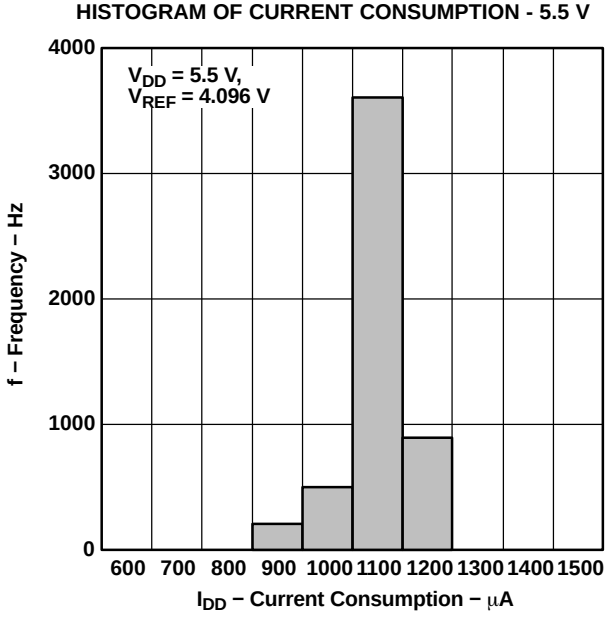


Figure 31.

TYPICAL CHARACTERISTICS (continued)

HISTOGRAM OF CURRENT CONSUMPTION - 2.7 V

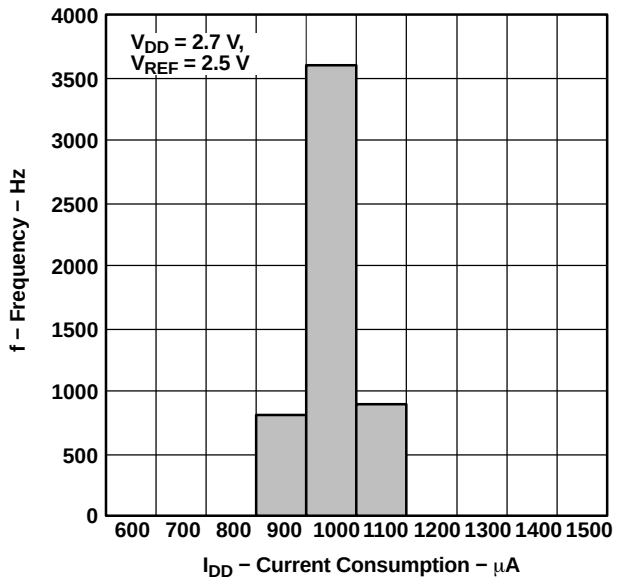


Figure 32.

TOTAL ERROR - 5 V

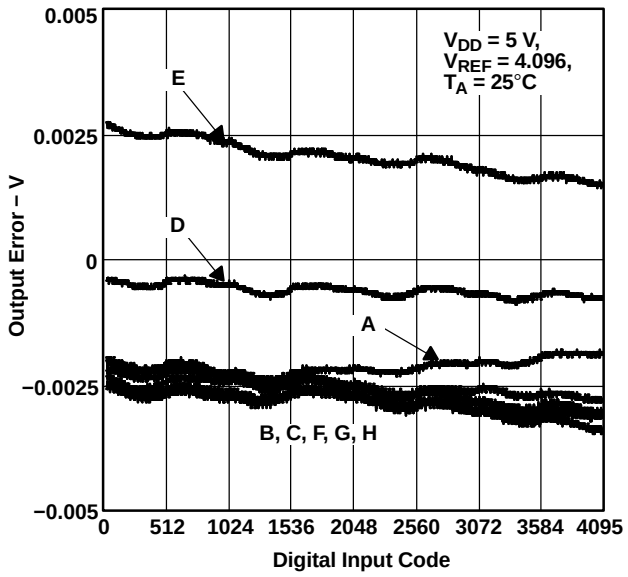


Figure 33.

TOTAL ERROR - 2.7 V

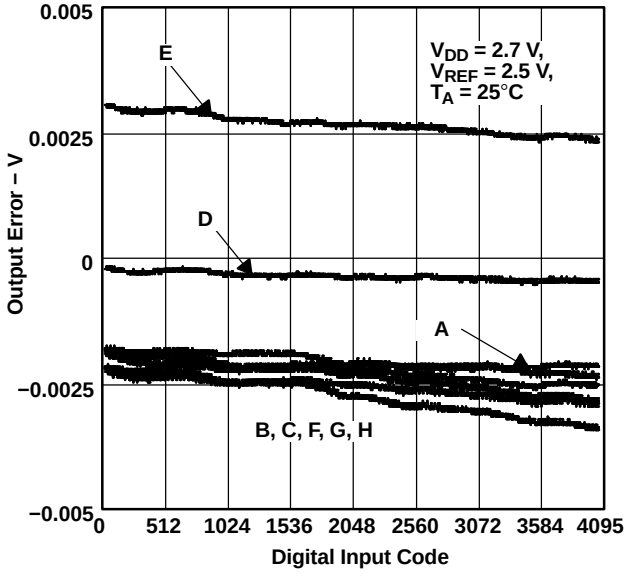


Figure 34.

EXITING POWER-DOWN MODE

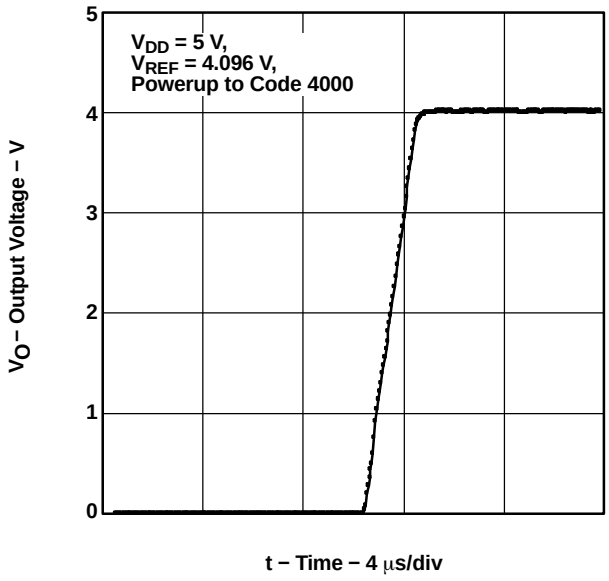
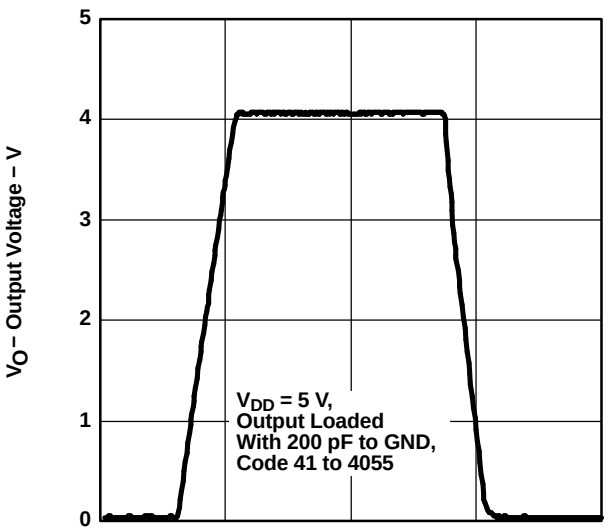


Figure 35.

TYPICAL CHARACTERISTICS (continued)

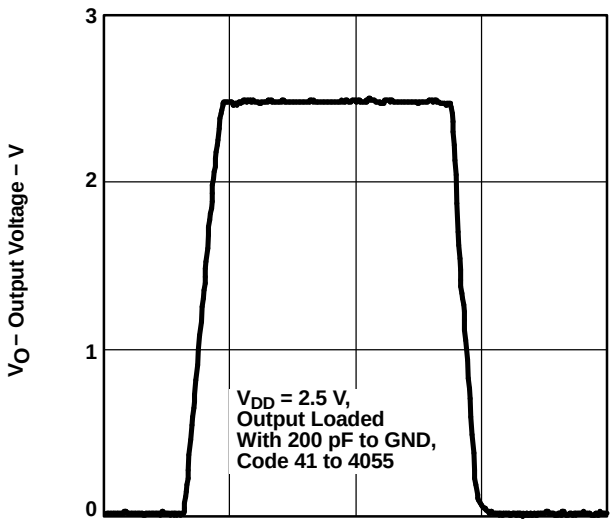
LARGE-SIGNAL SETTLING TIME - 5 V



t – Time – 5 μs/div

Figure 36.

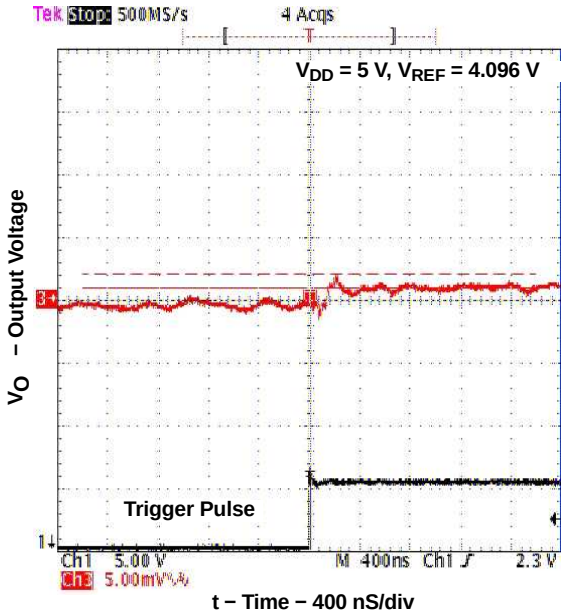
LARGE-SIGNAL SETTLING TIME - 2.7 V



t – Time – 5 μs/div

Figure 37.

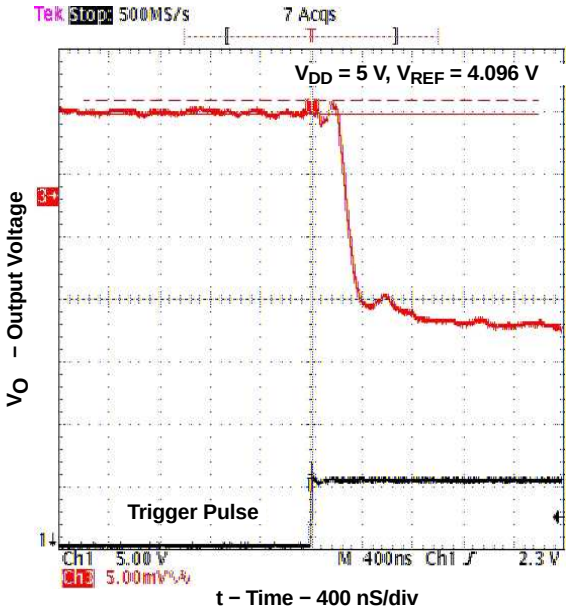
MIDSCALE GLITCH



t – Time – 400 nS/div

Figure 38.

WORST-CASE GLITCH



t – Time – 400 nS/div

Figure 39.

TYPICAL CHARACTERISTICS (continued)

DIGITAL FEEDTHROUGH ERROR

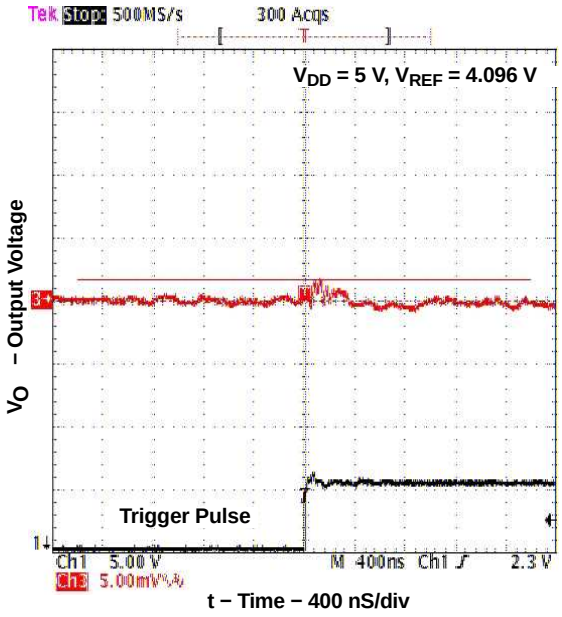


Figure 40.

CHANNEL-TO-CHANNEL CROSSTALK
FOR A FULL-SCALE SWING

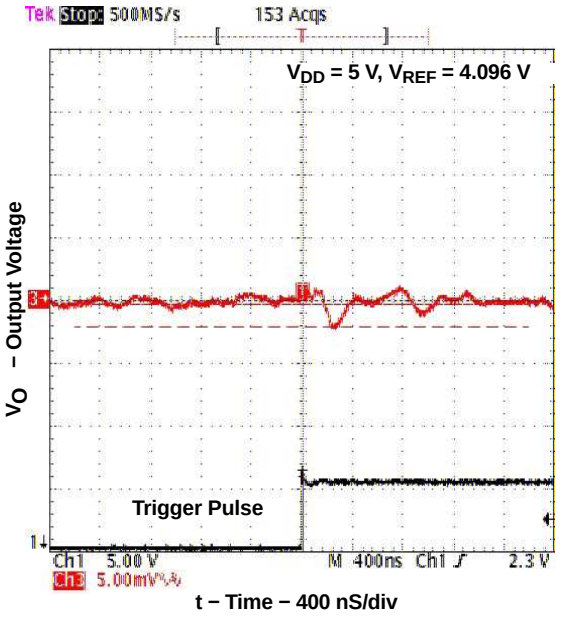


Figure 41.

TOTAL HARMONIC DISTORTION
vs
OUTPUT FREQUENCY

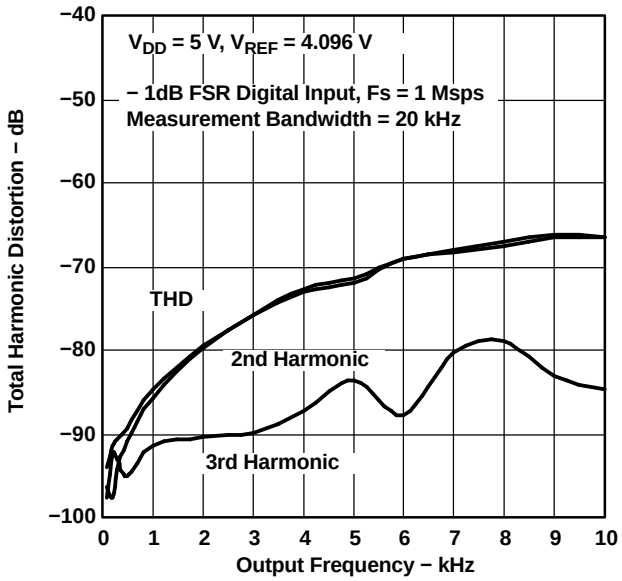


Figure 42.

3-Wire Serial Interface

The DAC7558 digital interface is a standard 3-wire SPI/QSPI/Microwire/DSP-compatible interface.

Table 1. Serial Interface Programming

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15–DB4	DB3–DB0	DESCRIPTION
A1	A0	LD1	LD0	SEL2	SEL1	SEL0	PWD	MSB–LSB	Don't Care	
0	0	0	0	0	0	0	0	Data	X	Write to buffer A with data
(Both A1 and A0 should be set to zero for normal device operation. DAC(s) do not respond if any other combination is used)		0	0	0	0	1	0	Data	X	Write to buffer B with data
		0	0	0	1	0	0	Data	X	Write to buffer C with data
		0	0	0	1	1	0	Data	X	Write to buffer D with data
		0	0	1	0	0	0	Data	X	Write to buffer E with data
		0	0	1	0	1	0	Data	X	Write to buffer F with data
		0	0	1	1	0	0	Data	X	Write to buffer G with data
		0	0	1	1	1	0	Data	X	Write to buffer H with data
		0	1	(000, 001, 010, 011, 100, 101, 110, 111)			0	Data	X	Write to buffer with data and load DAC (selected by DB19, DB18, and DB17)
		1	0	(000, 001, 010, 011, 100, 101, 110, 111)			0	Data	X	Write to buffer with data and load DAC (selected by DB19, DB18, and DB17) and load all other DACs with buffer data
		1	1	0	0	0	0	Data	X	Load DACs A and B with current buffer data
		1	1	0	0	1	0	Data	X	Load DACs A, B, C, and D with current buffer data
		1	1	0	1	0	0	Data	X	Load DACs A, B, C, D, E, and F with current buffer data
		1	1	0	1	1	0	Data	X	Load DACs A, B, C, D, E, F, G, and H with current buffer data
		1	1	1	0	0	0	Data	X	Write to buffer with new data and load DACs A and B simultaneously
		1	1	1	0	1	0	Data	X	Write to buffer with new data and load DACs A, B, C, and D simultaneously
		1	1	1	1	0	0	Data	X	Write to buffer with new data and load DACs A, B, C, D, E, and F simultaneously
		1	1	1	1	1	0	Data	X	Write to buffer with new data and load DACs A, B, C, D, E, F, G, and H simultaneously
		X	0	(000, 001, 010, 011, 100, 101, 110, 111)			1	See Table 2	X	Write to buffer and load DAC with Power-Down command to individual channel (selected by DB19, DB18, and DB17)
		X	1	(000, 001, 010, 011, 100, 101, 110, 111)			1	See Table 2 and Table 3	X	Write to buffer and load DACs with Power-Down command to multiple channels (selected by DB19, DB18, and DB17)

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC7558 consists of a string DAC followed by an output buffer amplifier. Figure 43 shows a generalized block diagram of the DAC architecture.

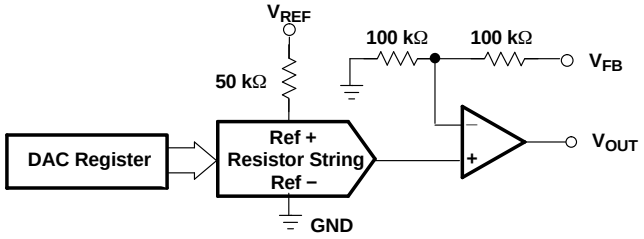


Figure 43. Typical DAC Architecture

The input coding to the DAC7558 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = V_{REF} \times D/4096$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register which can range from 0 to 4095.

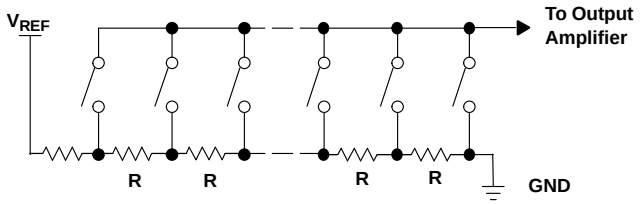


Figure 44. Typical Resistor String

RESISTOR STRING

The resistor string section is shown in Figure 44. It is simply a string of resistors, each of value R. The DAC7558 uses eight separate resistor strings. Each VREFx input pin provides the external reference voltage for two resistor strings. A resistor string has 100 kΩ total resistance to ground, including a 50 kΩ divide-by-two resistor. Since each VREFx pin connects to two resistor strings, the resistance seen by each VREFx pin is approximately 50 kΩ. The divide-by-two function provided by the resistor string is compensated by a gain-of-two amplifier configuration. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is specified monotonic. The DAC7558 architecture uses eight separate resistor strings to minimize channel-to-channel crosstalk.

OUTPUT BUFFER AMPLIFIERS

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with up to 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/µs with a half-scale settling time of 3 µs with the output unloaded.

DAC External Reference Input

Four separate reference pins are provided for eight DACs, providing maximum flexibility. VREF1 serves DAC A and DAC B, VREF2 serves DAC C and DAC D, VREF3 serves DAC E and DAC F, and VREF4 serves DAC G and DAC H. VREF1 through VREF4 can be externally shorted together for simplicity.

It is recommended to use a buffered reference in the external circuit (e.g., REF3140). The input impedance is typically 50 kΩ for each reference input pin.

Amplifier Sense Input

The DAC7558 contains eight amplifier feedback input pins, VFBA ... VFBH. For voltage output operation, VFBA ... VFBH must externally connect to VOUTA ... VOUTH respectively. For better DC accuracy, these connections should be made at load points. The VFBA ... VFBH pins are also useful for a variety of applications, including digitally controlled current sources. Each feedback input pin is internally connected to the DAC amplifier's negative input terminal through a 100-kΩ resistor; and, the amplifier's negative input terminal internally connects to ground through another 100-kΩ resistor (See Figure 43). This forms a gain-of-two, non-inverting amplifier configuration. Overall gain remains one because the resistor string has a divide-by-two configuration. The resistance seen at each VFBx pin is approximately 200 kΩ to ground.

Power-On Reset

On power up, all internal registers are cleared and all channels are updated with zero-scale voltages. Until valid data is written, all DAC outputs remain in this state. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up. In order not to turn on ESD protection devices, V_{DD} should be applied before any other pin is brought high.

During power up, all digital input pins should be set at logic-low voltages. Shortly after power up, if RSTSEL pin is low, then all DAC outputs are at their zero-scale voltages. If RSTSEL pin is brought high, then all DAC outputs are at their mid-scale voltages.

Power Down

The DAC7558 has a flexible power-down capability as described in Table 2 and Table 3. Individual channels can be powered down separately, or multiple channels can be powered down simultaneously. During a power-down condition, the user has flexibility to select the output impedance of each channel. If the $\overline{PD}$ pin is brought low, then all channels can simultaneously be powered down, with the output at high impedance state (High-Z).

The DAC7558 has DB16 as a power-down flag. If this flag is set, then DB11 and DB10 select one of the three power-down modes of the device as described in Table 2.

Table 2. DAC7558 Power-Down Modes

DB11	DB10	OPERATING MODE
0	0	PWD Hi-Z
0	1	PWD 1 kΩ
1	0	PWD 100 kΩ
1	1	PWD Hi-Z

The DAC7558 can also be powered down using the PD pin. When the PD pins is brought low, all channels simultaneously power down and all outputs become high impedance. When the PD pin is brought high, the device resumes its state before the power down condition.

The DAC7558 also has an option to power down individual channels, or multiple channels simultaneously selected by DB20. If DB20 = 0, then the user can power down the selected individual channels. If DB20 = 1, then the user can power down the multiple channels simultaneously as explained in Table 3. Power-down mode is selected by DB11 and DB10.

Table 3. DAC7558 Power-Down Modes for Multiple Channels

DB19	DB18	DB17	OPERATING MODE
0	0	0	PWD Channel A-B
0	0	1	PWD Channel A-C
0	1	0	PWD Channel A-D
0	1	1	PWD Channel A-E
1	0	0	PWD Channel A-F
1	0	1	PWD Channel A-G
1	1	0	PWD Channel A-H
1	1	1	PWD Channel A-H

Asynchronous Clear

The DAC7558 output is asynchronously set to zero-scale voltage immediately after the $\overline{RST}$ pin is brought low. The $\overline{RST}$ signal resets all internal registers, and therefore behaves like the Power-On Reset. The DAC7558 updates at the first rising edge of the $\overline{SYNC}$ signal that occurs after the $\overline{RST}$ pin is brought back to high.

If the RSTSEL pin is high, RST signal going low resets all outputs to midscale. If the RSTSEL pin is low, RST signal going low resets all outputs to zero-scale.

Input Data Format Selection

DAC7558 can use unsigned binary (USB) or binary twos complement (BTC) input data formats. Format selection is done by the RSTSEL pin. If the RSTSEL is kept low, the 12-bit input data is assumed to have USB format, and any asynchronous clear operation generates zero-scale outputs. If the RSTSEL pin is kept high, the 12-bit input data is assumed to have BTC format and any asynchronous clear operation generates mid-scale outputs.

SERIAL INTERFACE

The DAC7558 is controlled over a versatile 3-wire serial interface, which operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards.

24-Bit Word and Input Shift Register

The input shift register is 24 bits wide. DAC data is loaded into the device as a 24-bit word under the control of a serial clock input, SCLK, as shown in the Figure 1 timing diagram. The 24-bit word, illustrated in Table 1, consists of 8 control bits, followed by 12 data bits and 4 don't care bits. Data format is straight binary (RSTSEL pin = 0) or binary twos complement (RSTSEL = 1), where the most significant DAC data bit is DB15. Data is loaded MSB first (DB23) where the first two bits (DB23 and DB22) should be set to zero for DAC7558 to work. The DAC7558 does not respond to any other combination other than 00. DB21 and DB20 (LD1 and LD0) determine if the input register, DAC register, or both are updated with shift register input data. DB19, DB18, and DB17 (SEL2, SEL1, and SEL0) bits select the desired DAC(s). DB16 is the power-down bit. If DB16 = 0, then it is a normal operation, if DB16 = 1, then DB11 and DB10 determine the power-down mode (Hi-Z, 1 kΩ, or 100 kΩ). DB20 bit also gives the user the option of powering down either a single channel or multiple channels at the same time. See Power Down section for more details.

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame-synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$-to-SCLK

falling-edge setup time, t4. After $\overline{\text{SYNC}}$ goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 24 clock pulses. Any data and clock pulses after the twenty-fourth falling edge of SCLK are ignored. No further serial data transfer occurs until SYNC is taken high and low again.

$\overline{\text{SYNC}}$ may be taken high after the falling edge of the twenty-fourth SCLK pulse, observing the minimum SCLK Loop falling-edge to SYNC rising-edge time, t7.

After the end of serial data transfer, data is automatically transferred from the input shift register to the input register of the selected DAC. If $\overline{\text{SYNC}}$ is taken high before the twenty-fourth falling edge of SCLK, the data transfer is aborted and the DAC input registers are not updated.

When DCEN is low, the SDO pin is brought to a Hi-Z state. The first 24 data bits that follow the falling edge of $\overline{\text{SYNC}}$ are stored in the shift register. The rising edge of $\overline{\text{SYNC}}$ that follows the 24th data bit updates the DAC(s). If $\overline{\text{SYNC}}$ is brought high before the 24th data bit, no action occurs.

In daisy-chain mode (DCEN = 1) the DAC7558 requires a falling SCLK edge after the rising $\overline{\text{SYNC}}$, in order to initialize the serial interface for the next update.

When DCEN is high, data can continuously be shifted into the shift register, enabling the daisy-chain operation. The SDO pin becomes active and outputs SDIN data with 24 clock-cycle delay. A rising edge of $\overline{\text{SYNC}}$ loads the shift register data into the DAC(s). The loaded data consists of the last 24 data bits received into the shift register before the rising edge of $\overline{\text{SYNC}}$.

If daisy-chain operation is not needed, DCEN should permanently be tied to a logic-low voltage.

Daisy-Chain Operation

When the DCEN pin is brought high, daisy chaining is enabled. Serial data output (SDO) pin is provided to daisy-chain multiple DAC7558 devices in a system. As long as $\overline{\text{SYNC}}$ is high or DCEN is low the SDO pin is in a high-impedance state. When $\overline{\text{SYNC}}$ is brought low the output of the internal shift register is tied to the SDO pin. As long as $\overline{\text{SYNC}}$ is low and DCEN is high, SDO duplicates the SDIN signal with 24-cycle delay. To support multiple devices in a daisy-chain, SCLK and $\overline{\text{SYNC}}$ signals are shared across all devices and SDO of one DAC7558 should be tied to the SDIN of the next DAC7558. For *n* devices in such a daisy chain, 24*n* SCLK cycles are required to shift the entire input data stream. After 24*n* SCLK falling edges are received (following a falling $\overline{\text{SYNC}}$), the data stream becomes complete, and $\overline{\text{SYNC}}$ can be brought high to update *n* devices simultaneously. SDO operation is specified at a maximum SCLK speed of 10 MHz.

Daisy-chain operation is also possible between octal-channel DAC7558, dual-channel DAC7552, and single-channel DAC7551 devices. Dasy chaining enables communication with any number of DAC channels using a single serial interface. As long as the correct number of bits are shifted using a daisy-chain setting, a rising edge of SYNC properly updates all chips in the system. Following a rising edge of SYNC, all devices on the daisy chain respond according to the control bits they receive.

IOVDD and Level Shifters

The DAC7558 can be used with different logic families that require a wide range of supply voltages (from 1.8 V to 5.5 V). To enable this useful feature, the IOVDD pin must be connected to the logic supply voltage of the system. All DAC7558 digital input and output pins are equipped with level-shifter circuits. Level shifters at the input pins ensure that external logic high voltages are translated to the internal logic high voltage, with no additional power dissipation. Similarly, the level shifter for the SDO pin translates the internal logic high voltage (AVDD) to the external logic high level (IOVDD). For single supply operation, the IOVDD pin can be tied to the AVDD pin.

INTEGRAL AND DIFFERENTIAL LINEARITY

The DAC7558 uses precision thin-film resistors providing exceptional linearity and monotonicity. Integral linearity error is typically within (+/-) 0.35 LSBs, and differential linearity error is typically within (+/-) 0.08 LSBs.

GLITCH ENERGY

The DAC7558 uses a proprietary architecture that minimizes glitch energy. The code-to-code glitches are so low, they are usually buried within the wide-band noise and cannot be easily detected. The DAC7558 glitch is typically well under 0.1 nV-s. Such low glitch energy provides more than 10X improvement over industry alternatives.

CHANNEL-TO-CHANNEL CROSSTALK

The DAC7558 architecture is designed to minimize channel-to-channel crosstalk. The voltage change in one channel does not affect the voltage output in another channel. The DC crosstalk is in the order of a few microvolts. AC crosstalk is also less than –100 dBs. This provides orders of magnitude improvement over certain competing architectures.

APPLICATION INFORMATION

Waveform Generation

Due to its exceptional linearity, low glitch, and low crosstalk, the DAC7558 is well suited for waveform generation (from DC to 10 kHz). The DAC7558 large-signal settling time is 5 µs, supporting an update rate of 200 KSPS. However, the update rates can exceed 1 MSPS if the waveform to be generated consists of small voltage steps between consecutive DAC updates. To obtain a high dynamic range, REF3140 (4.096 V) or REF02 (5.0 V) are recommended for reference voltage generation.

Generating ±5-V, ±10-V, and ± 12-V Outputs For Precision Industrial Control

Industrial control applications can require multiple feedback loops consisting of sensors, ADCs, MCUs, DACs, and actuators. Loop accuracy and loop speed are the two important parameters of such control loops.

Loop Accuracy:

In a control loop, the ADC has to be accurate. Offset, gain, and the integral linearity errors of the DAC are not factors in determining the accuracy of the loop. As long as a voltage exists in the transfer curve of a monotonic DAC, the loop can find it and settle to it. On the other hand, DAC resolution and differential linearity do determine the loop accuracy, because each DAC step determines the minimum incremental change the loop can generate. A DNL error less than –1 LSB (non-monotonicity) can create loop instability. A DNL error greater than +1 LSB implies unnecessarily large voltage steps and missed voltage targets. With high DNL errors, the loop looses its stability, resolution, and accuracy. Offering 12-bit ensured monotonicity and ± 0.08 LSB typical DNL error, 755X DACs are great choices for precision control loops.

Loop Speed:

Many factors determine control loop speed. Typically, the ADC's conversion time, and the MCU's computation time are the two major factors that dominate the time constant of the loop. DAC settling time is rarely a dominant factor because ADC conversion times usually exceed DAC conversion times. DAC offset, gain, and linearity errors can slow the loop down only during the start-up. Once the loop reaches its steady-state operation, these errors do not affect loop speed any further. Depending on the ringing characteristics of the loop's transfer function, DAC glitches can also slow the loop down. With its 1 MSPS (small-signal) maximum data update rate, DAC7558 can support high-speed control loops. Ultra-low glitch energy of the DAC7558 significantly improves loop stability and loop settling time.

Generating Industrial Voltage Ranges:

For control loop applications, DAC gain and offset errors are not important parameters. This could be exploited to lower trim and calibration costs in a high-voltage control circuit design. Using a quad operational amplifier (OPA4130), and a voltage reference (REF3140), the DAC7558 can generate the wide voltage swings required by the control loop.

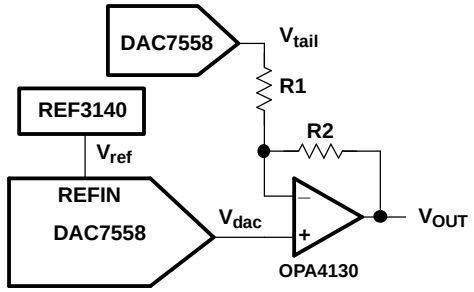


Figure 45. Low-cost, Wide-swing Voltage Generator for Control Loop Applications

The output voltage of the configuration is given by:

$$V_{OUT} = V_{REF}\left(\frac{R2}{R1} + 1\right)\frac{Din}{4096} - V_{tail}\,\frac{R2}{R1} \quad (1)$$

Fixed R1 and R2 resistors can be used to coarsely set the gain required in the first term of the equation. Once R2 and R1 set the gain to include some minimal over-range, four DAC7558 channels could be used to precisely set the required offset voltages. Residual errors are not an issue for loop accuracy because offset and gain errors could be tolerated. Four DAC7558 channels can provide the V_{tail} voltages to minimize offset error, while the other four DAC7558 channels provide Vdac voltages to generate four high-voltage outputs.

For ±5-V operation: R1=10 kΩ, R2 = 15 kΩ, V_{tail} = 3.33 V, V_{REF} = 4.096 V

For ±10-V operation: R1=10 kΩ, R2 = 39 kΩ, V_{tail} = 2.56 V, V_{REF} = 4.096 V

For ±12-V operation: R1=10 kΩ, R2 = 49 kΩ, V_{tail} = 2.45 V, V_{REF} = 4.096 V

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7558IRHBR	ACTIVE	QFN	RHB	32	3000	TBD	CU NIPDAU	Level-2-235C-1 YEAR
DAC7558IRHBT	ACTIVE	QFN	RHB	32	250	TBD	CU NIPDAU	Level-2-235C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

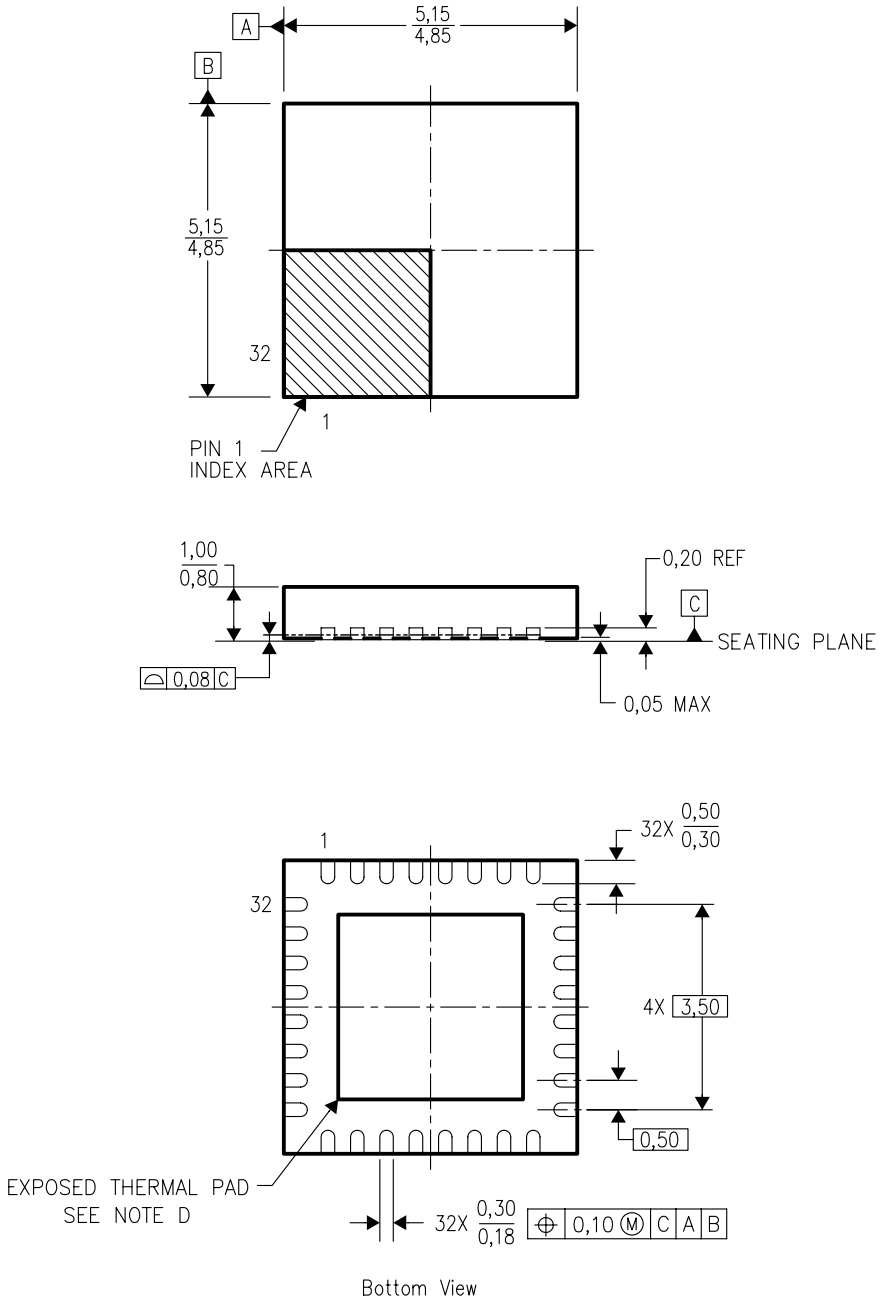
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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