Silicon NPN Power Transistors NS50B

DESCRIPTION

·With TO-220C package
·Complement to type NS50A

APPLICATIONS

·For medium power linear switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

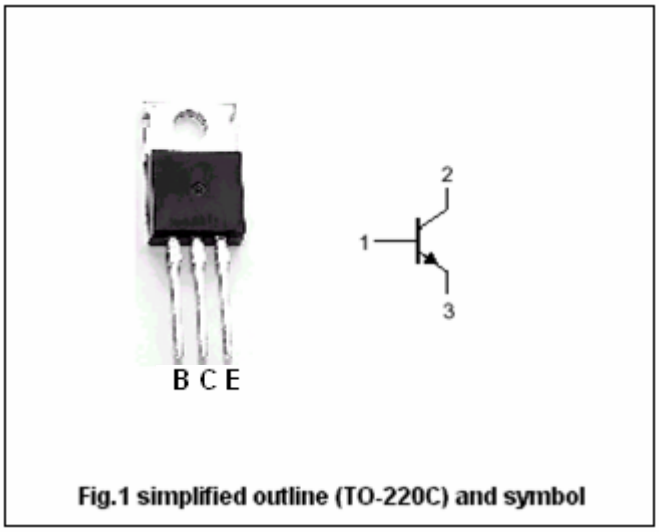


Fig.1 simplified outline (TO-220C) and symbol

ABSOLUTE MAXIMUM RATINGS(T_C=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	100	V
V_{CEO}	Collector-emitter voltage	Open base	60	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current (DC)		6	A
I_{CM}	Collector current-Pulse		10	A
P_C	Collector power dissipation	T_C=25□	65	W
		T_a=25□	2	
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-65~150	□

Silicon NPN Power Transistors NS50B

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	I_C=30mA; I_B=0	60			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C=4A; I_B=0.4A			1.0	V
$V_{BE(sat)}$	Base-emitter saturation voltage	I_C=4A; I_B=0.4A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=100V; I_E=0			10	μA
I_{CEO}	Collector cut-off current	V_{CE}=60V; I_B=0			0.1	mA
I_{EBO}	Emitter cut-off current	V_{EB}=6V; I_C=0			10	μA
h_{FE}	DC current gain	I_C=1A ; V_{CE}=5V	100		160	
f_T	Transition frequency	I_C=0.5A ; V_{CE}=10V	3			MHz

PACKAGE OUTLINE

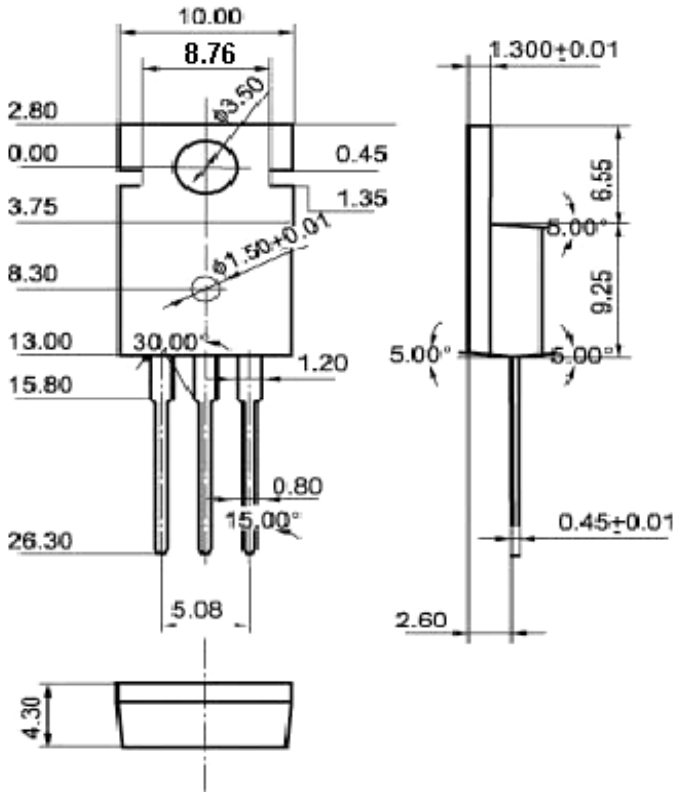


Fig.2 Outline dimensions