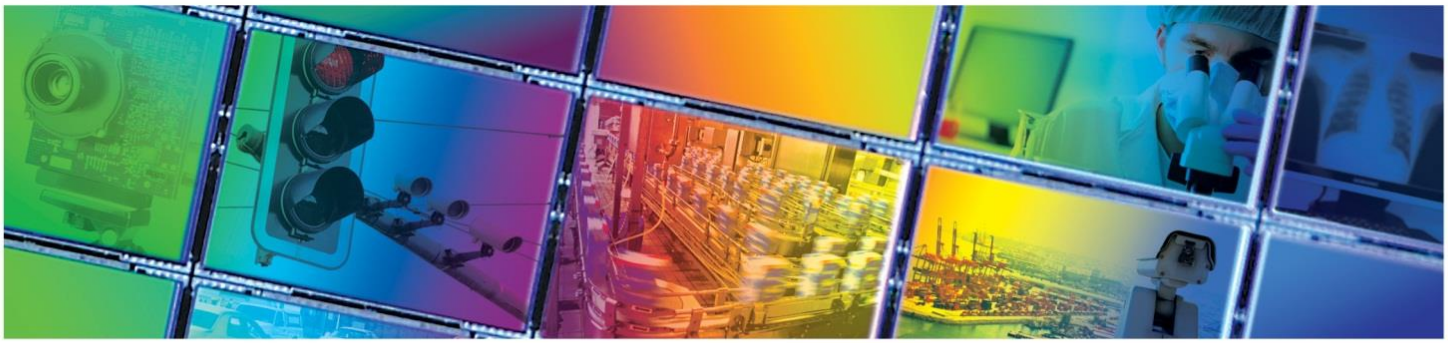
ON Semiconductor®

KAI-18000 IMAGE SENSOR

4320 (H) X 4144 (V) INTERLINE CCD IMAGE SENSOR



JUNE 4, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 3.0 PS0067

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Summary Specification

KAI-18000 Image Sensor

Description

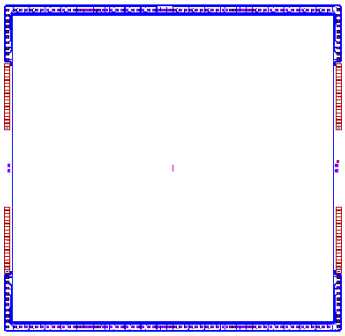
The KAI-18000 Image Sensor is a high-performance 18-million pixel sensor designed for 30 frames/sec video applications. The 8.0 µm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The forty outputs and with binning capabilities allow for 30 frames per second (fps) progressive scan video images at a pixel rate of 17 Mhz. The vertical overflow drain structure provides antiblooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

Features

- 30 frames per second
- 17 MHz data rate
- Progressive scan

Applications

- Customer restricted



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	4320 (H) x 4224 (V) = approx. 18.2 M
Number of Effective Pixels	4320 (H) x 4144 (V) = approx. 17.9 M
Number of Active Pixels	4320 (H) x 4160 (V) = approx. 18.0 M
Number of Outputs	40
Pixel Size	8.0 µm (H) x 8.0 µm (V)
Imager Size	47.89 mm (diagonal)
Chip Size	37.00 mm (H) x 36.00 mm (V)
Aspect Ratio	1:1
Saturation Signal	50,000 e^-
Peak Quantum Efficiency (QE)	55%
Solar Weighted Average QE 400 to 900 nm	31%
Output Sensitivity	30 µV/e^-
Total Sensor Noise (at 17 MHz)	<25 e^-
VCCD Capacity	60,000 e^-
Dark Current at 20 °C	< 0.5 nA/cm^2
Dark Current Doubling Temperature	7 °C
Dynamic Range	60 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	200X
Smear	-85 dB
Image Lag	<10 e^-
Maximum Data Rate	20 MHz

All parameters above are specified at T = 20 °C

Ordering Information

Catalog Number	Product Name	Description
4H2259	KAI-18000-AAA-XR-AE-CUST PROPRIETARY PKG-RAD	Monochrome, PGA Package, Taped Clear Cover Glass with AR coating (both sides), RAD
4H0260	KAI-18000-ABA-XR-AE- CUST PROPRIETARY PKG-EM	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), EM
4H0261	KAI-18000-ABA-XR-AM- CUST PROPRIETARY PKG-MECH	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Mech Sample
4H0402	KAI-18000-ABA-XR-AA- CUST PROPRIETARY PKG-FM	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), FM

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

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Device Description

ARCHITECTURE

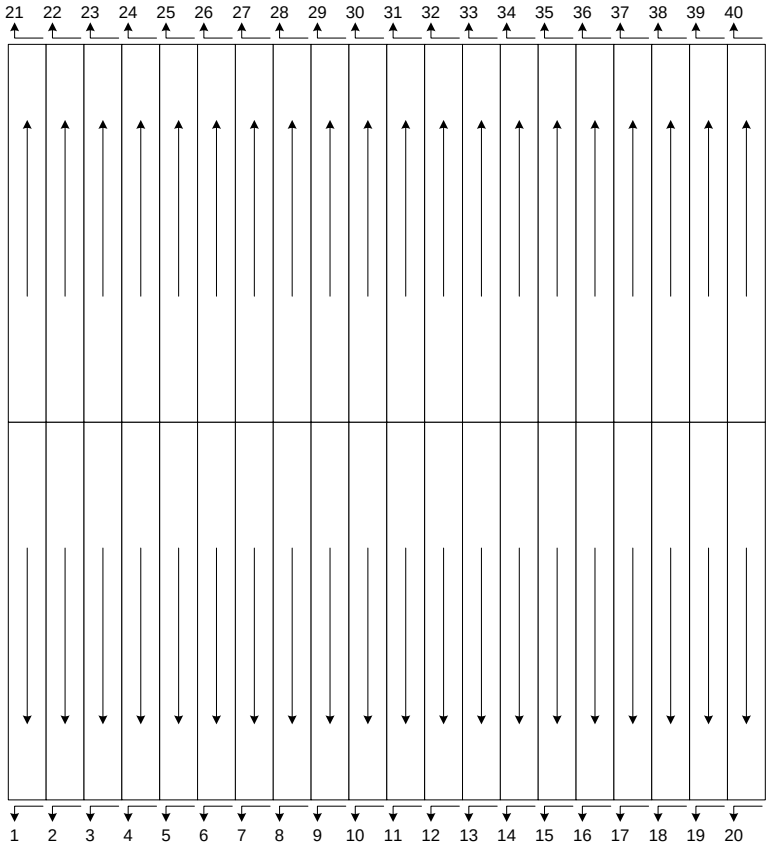


Figure 1: Sensor Architecture

To allow for 30 fps video with a 17 MHz pixel rate, there must be 40 outputs. There are twenty outputs across the top and twenty outputs across the bottom of the image sensor. The vertical CCD (VCCD) is split in half. The pixel design in the top half is an exact mirror image of the bottom half pixel design. The horizontal CCD (HCCD) on each half is split into 20 blocks, each 216 columns wide. The end of each block turns within the space of one column towards an output amplifier. There are six dummy HCCD pixels between the output amplifier and the imaging array. After each VCCD clock cycle one line will be transferred into each HCCD block. Once the HCCD clocks are started after the VCCD line transfer, the first six clock cycles will transfer empty charge packets to the output amplifier. Those are then followed by 216 clock cycles containing valid image data.

There is no dead space between each HCCD block. There also are no dark columns on the image sensor. Dark columns are not possible on a HCCD with more than two outputs.

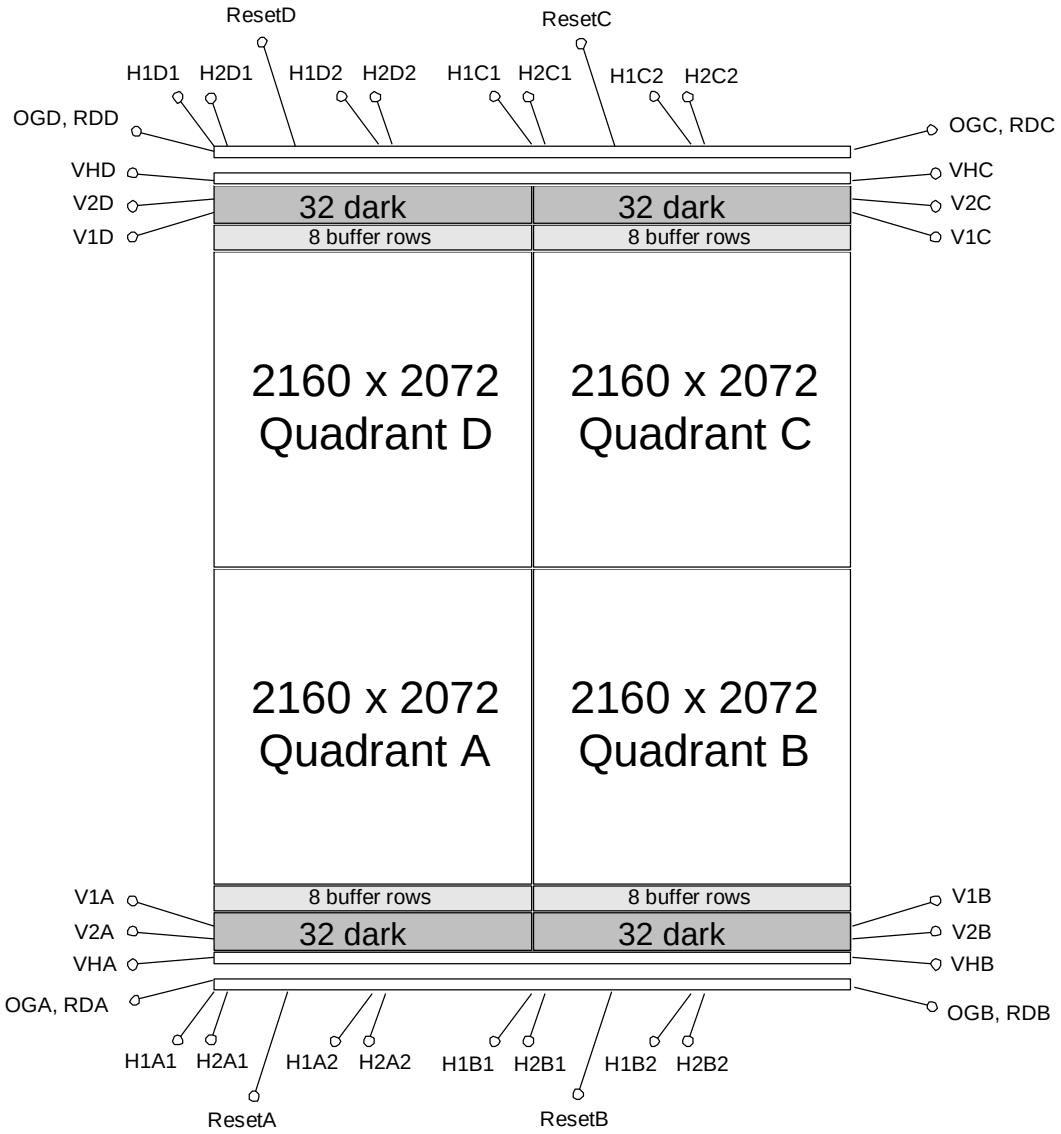


Figure 2: Sensor Architecture

The clock inputs of KAI-18000 are separated into four quadrants. There is no dead space between each quadrant. The wiring is such that if some portion of the image sensor fails, the clock drivers and biases for that quadrant may be powered down while the other quadrants still image. Each quadrant has 32 dark rows adjacent to the HCCD. The dark rows are pixels where the transfer gate between the photodiode and VCCD is permanently turned off. These dark rows will only contain VCCD dark current and image smear signal. They will not contain photodiode dark current. In between the dark rows and imaging pixels are 8 photoactive buffer rows. The buffer rows are a zone to account for larger than normal manufacturing variations in micro-lens formation near the edges of the imaging area. There are buffer columns on the left and right sides of the image sensor. The buffer columns do not transfer into any HCCD so they will not appear at any output amplifier.

PIXEL

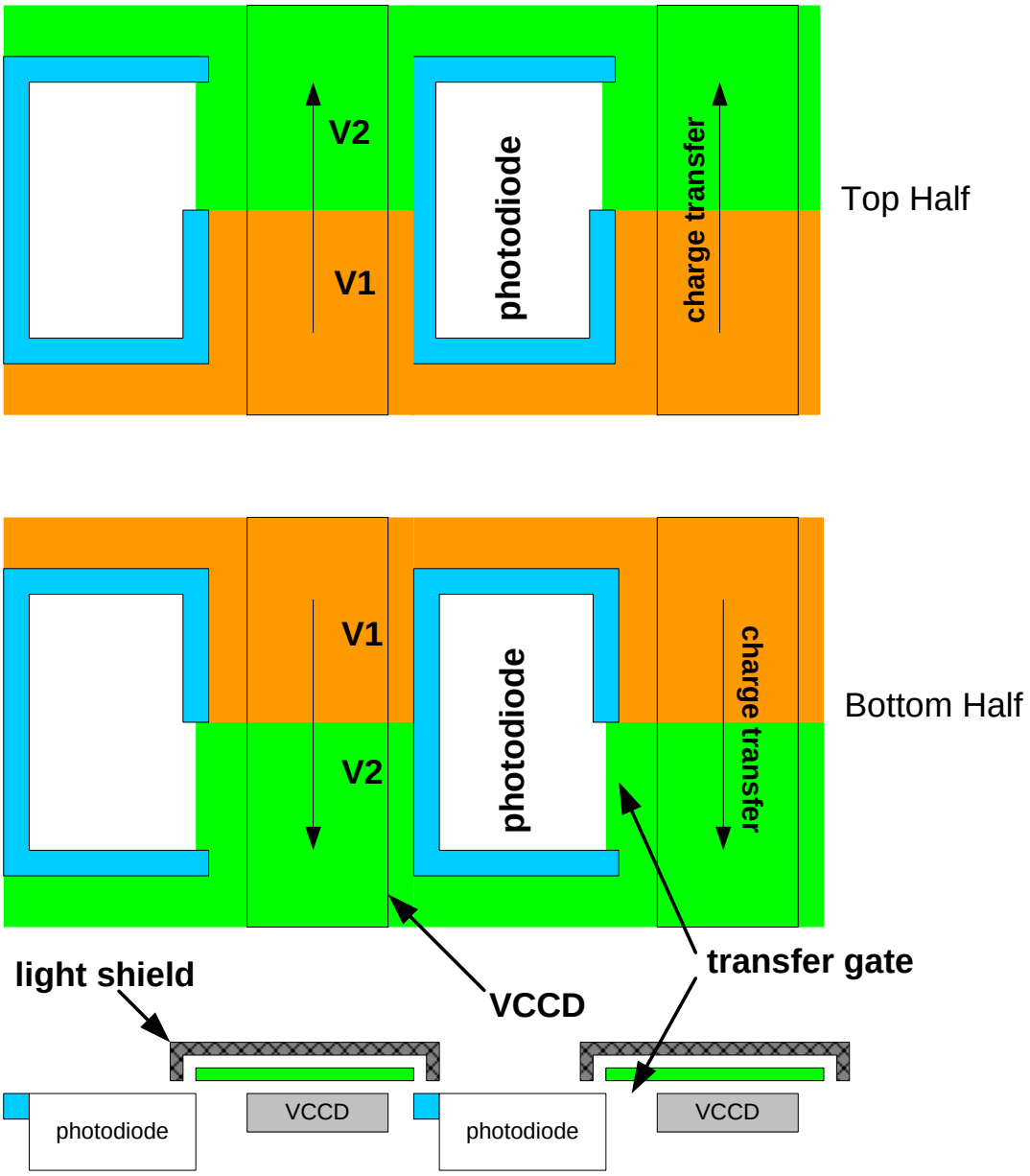


Figure 3: Pixel Architecture, Top and Side View

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time. When the photodiodes' charge capacity is reached, excess electrons overflow into the substrate to prevent blooming. Charge is transferred from the photodiodes to the VCCD when the V2 gate is pulsed above +9V. The pixel array layout of the imager is symmetrically mirrored about the middle center seam. The pixel operation is the same for pixels in the top and the bottom of the array.

Quadrant Boundaries

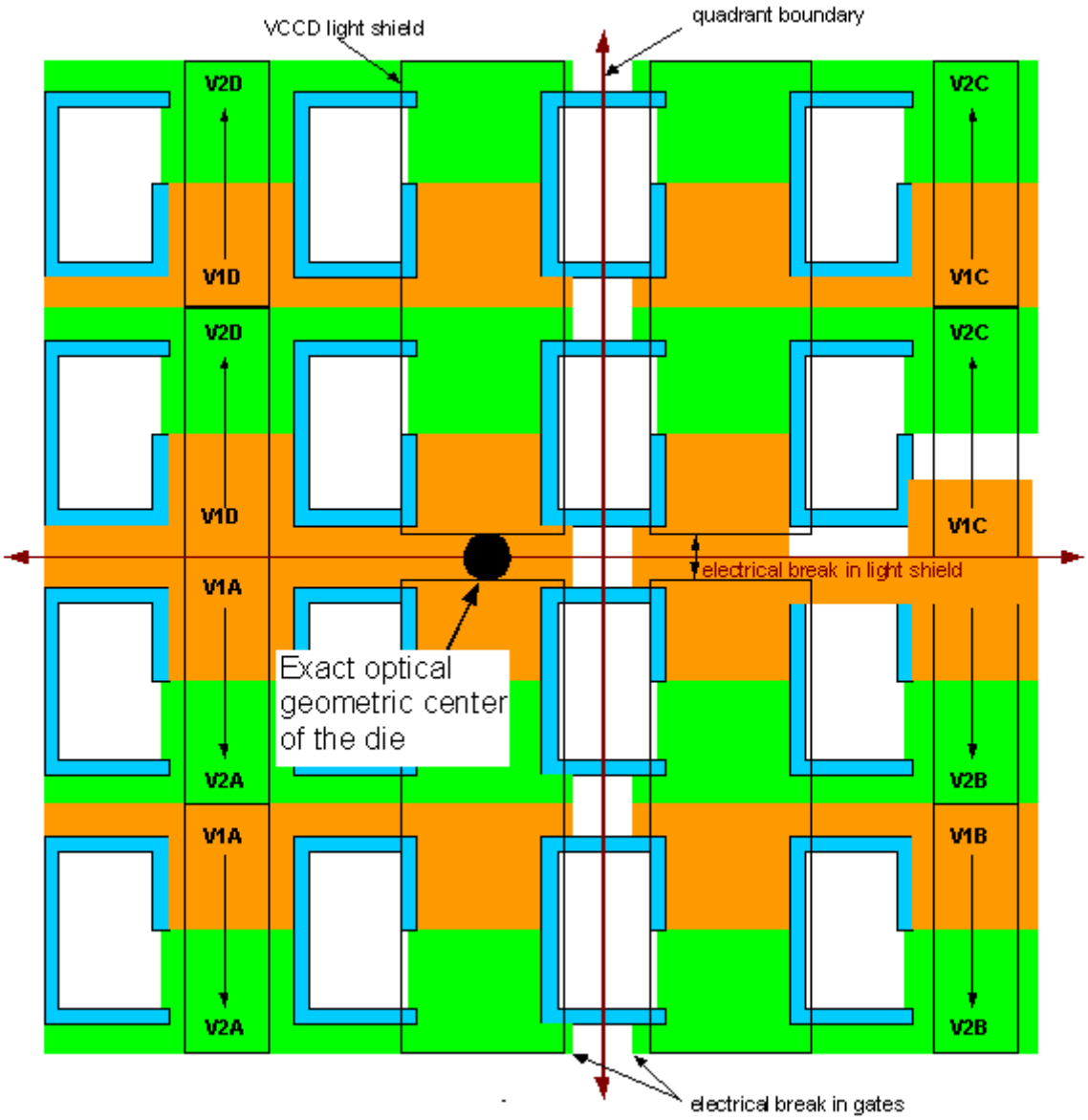


Figure 4: 4-Quadrant Intersection Pixels

The design requirement for KAI-18000 was to allow for a quadrant to be de-activated should something go wrong with that quadrant. This requirement for independent quadrant clock signals necessitates an electrical break in the poly silicon gates along a vertical boundary between the A/B and C/D quadrants. The light shield is used to carry the V1 and V2 clock voltages from the perimeter of the sensor to the center poly silicon gates. Thus, an electrical break in the light shield at the A/D and B/C quadrant boundaries is required. These electrical breaks will affect the photo-response of the pixels bordering the quadrant boundaries. The quantum efficiency is expected to be different by 10 to 20% relative to the rest of the pixel array.

VERTICAL TO HORIZONTAL TRANSFER

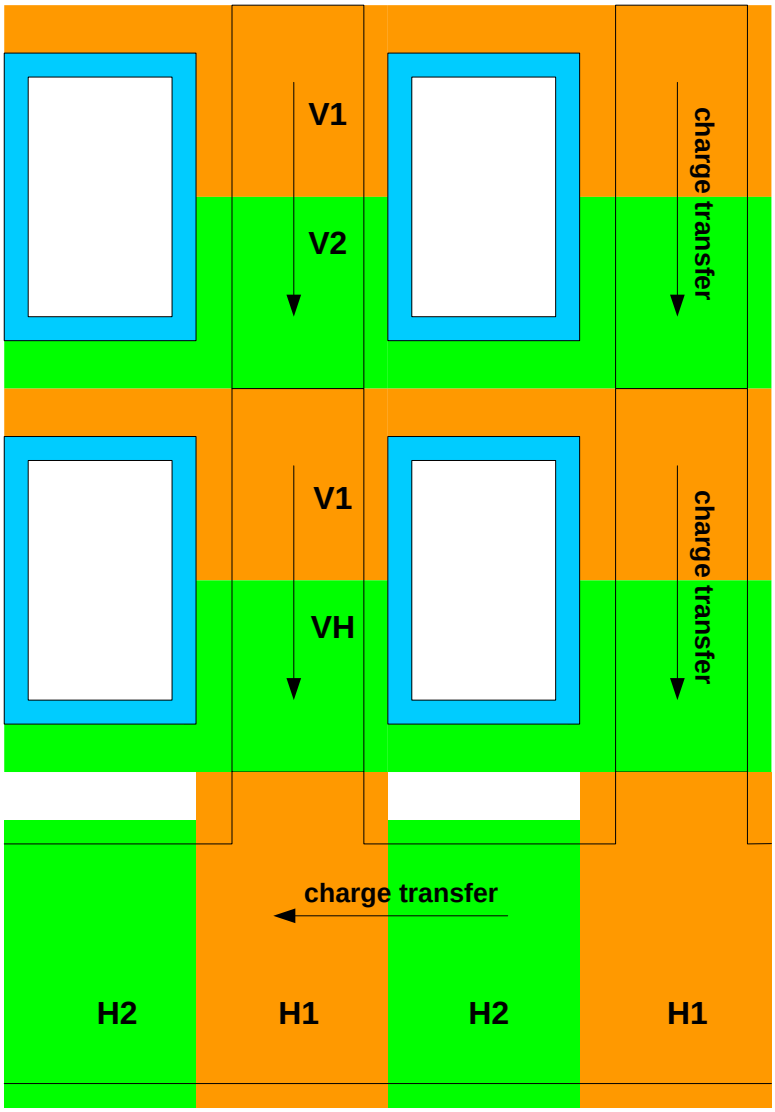


Figure 5: Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are clocked, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row of gates next to the HCCD has a separate clock line, VH. The timing requirements to meet 30 frames/sec mandate a very short horizontal retrace time which is insufficient to allow a complete VCCD transfer across the entire pixel array. To allow enough time for VCCD charge transfer the V1 and V2 clocks are operated during HCCD read out. This extends the V1 and V2 charge transfer times out to the length of one line time. To prevent charge from the VCCD from transferring into the HCCD during HCCD readout the last gate, VH, is clocked separately. VH is normally held low to block transfer from the VCCD to the HCCD. When an entire line has been read out of the HCCD and V1 is low and V2 is high, then VH is rapidly clocked from low to high and back low again in less than 1 µs. The short pulse on VH transfers the next row into the HCCD. H1 must be high and H2 must be low during the VH transfer time from the VCCD to the HCCD.

Horizontal Register to Floating Diffusion

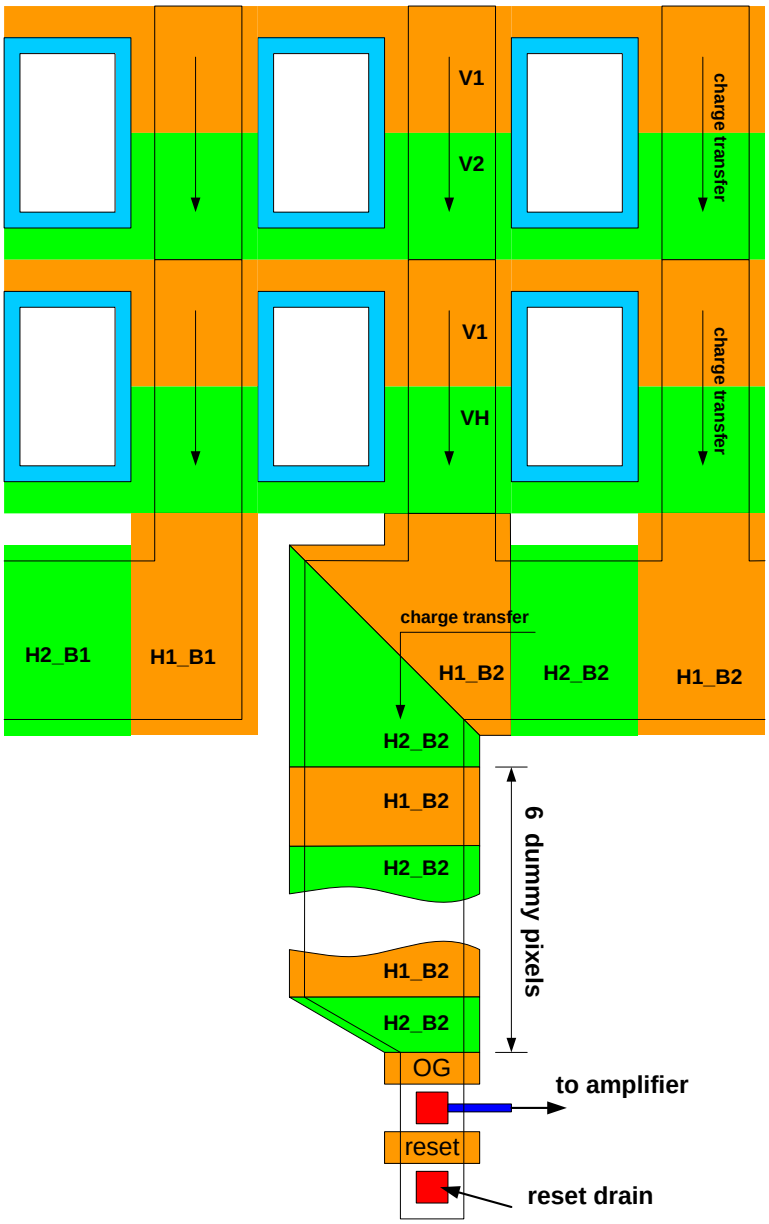


Figure 6: Horizontal Register to Floating Diffusion Architecture

The HCCD for each output block has a total of 222 pixels. 216 of those pixels receive valid image data directly from the VCCD. The remaining 6 pixels are between the floating diffusion and the first valid image pixel. The dummy pixels are required to provide space for wiring connections and the amplifier. Charge is transferred across OG to the floating diffusion on the falling edge of H2. The reset gate should be pulsed on the rising edge of H2.

OUTPUT

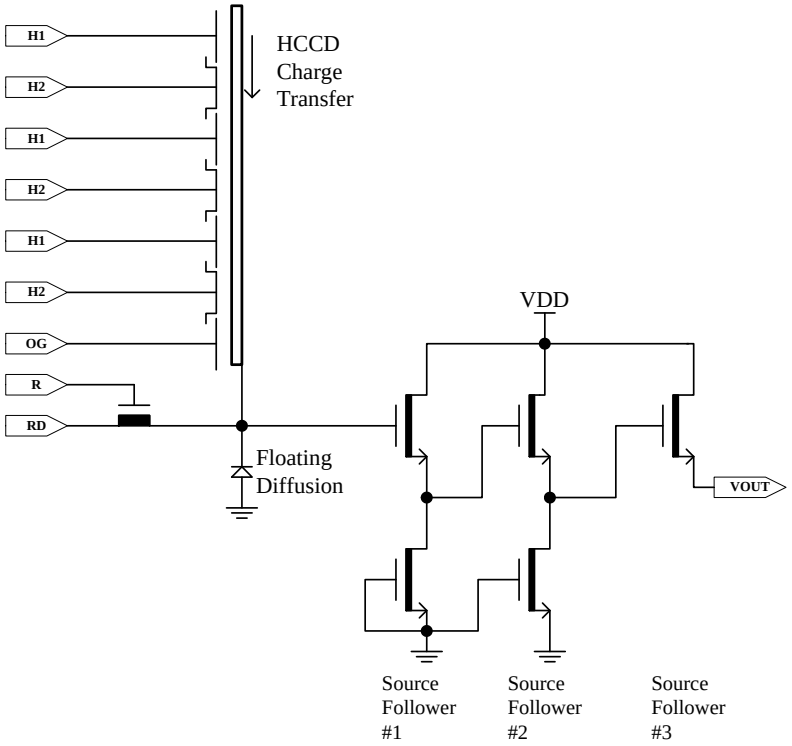


Figure 7: Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression $\Delta Vfd=\Delta Q/Cfd$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets the fd potential to the reset drain voltage (RD). When the image sensor is operated in the binned or summed modes there may be more than 50,000 electrons in the output signal. The image sensor is designed with a 30 μV/e charge to voltage conversion on the output. This means a full signal of 50,000 electrons will produce a 1500 mV change on the output amplifier. The output amplifier was designed to handle an output swing of 1500 mV at a pixel rate of 17 MHz. The output amplifier will not be able to swing more than 1500 mV in the binned or summed interlaced modes. The HCCD will also not hold more than 65,000 electrons. If signal clipping or blooming of the HCCD is to be avoided the photodiode charge capacity should be reduced below 50,000 electrons by increasing the substrate voltage.

OUTPUT SPICE MODEL

These spice model parameters are measured values for DC conditions. All transistor model parameters are for NMOS transistors SPICE level 1.

The video output bond pad has an estimated capacitance of 3pF.

	Load Transistors		Drive Transistors		
	1st stage	2nd stage	1st stage	2nd stage	3rd stage
VTO	-2.3	-2.3	-2.74	-2.74	-2.74
LAMBDA	0.0179	0.0179	0.0672	0.0672	0.0672
GAMMA	0.96	0.96	0.68	0.68	0.68
KP	2.51E-05	2.51E-05	2.84E-05	2.84E-05	2.84E-05
PHI	0.34	0.34	0.09	0.09	0.09
W (µm)	13	96	4.6	37	352
L (µm)	5	5	2	2	2

At 17 MHz, the video output bandwidth will be determined entirely by the 3rd stage drive transistor loading. The complete behavior of the KAI-18000 Image Sensor cannot be fully and accurately modeled with a SPICE model. Rather, these parameters can be used to help estimate the imager's performance along with actual data from the test and characterization system.

ESD Protection

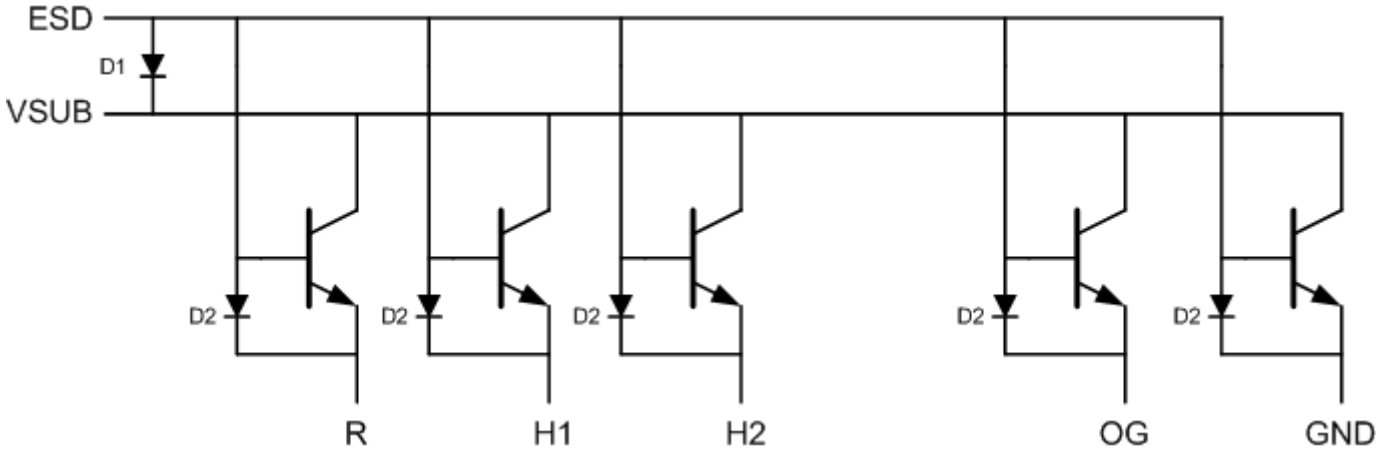


Figure 8: ESD Protection

The ESD protection circuitry for KAI-18000 is shown in Figure 8. It is mandatory that the pin voltages conform always to this range: ESD < Pin Voltage < ESD + 15. There are no exceptions. Only Reset, OG, GND, H1 and H2 pins are connected to ESD circuit.

Any power up, power down or other transient pulses, even less than 1 nsec pulse width, can cause the circuitry to latch up. In addition, please refer to the specific bond pad locations of ESD protection stated in Figure 12: Bond Pad Assignment Table. Please note that Schottky diode D1 is an externally mounted component which the system designer may choose to include.

Refer to the section on Power Up Sequence for more details.

BOND PADS (LEFT HALF)

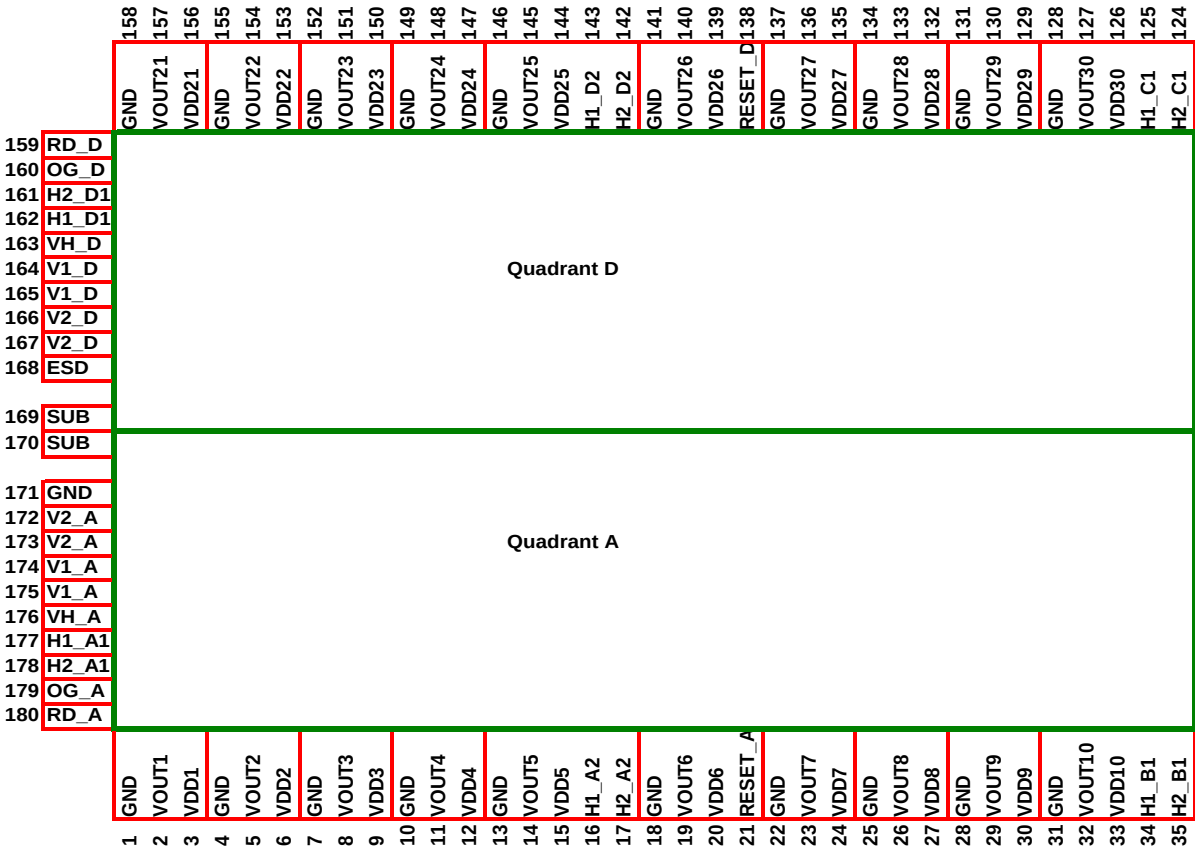


Figure 9: Bond Pad Schematic (left half)

All pins with identical labels are connected internally on the image sensor. Those pins must be wired together externally. All GND pins are connected internally on the image sensor. The VDD pins are independent to each output. An individual output amplifier may be deactivated by setting VDD to zero volts and disabling the output load current sink. Each quadrant has two independent HCCD clock inputs. The inputs, V1, V2, VH, OG, RD, and Reset are all separated by quadrant.

BOND PADS (RIGHT HALF)

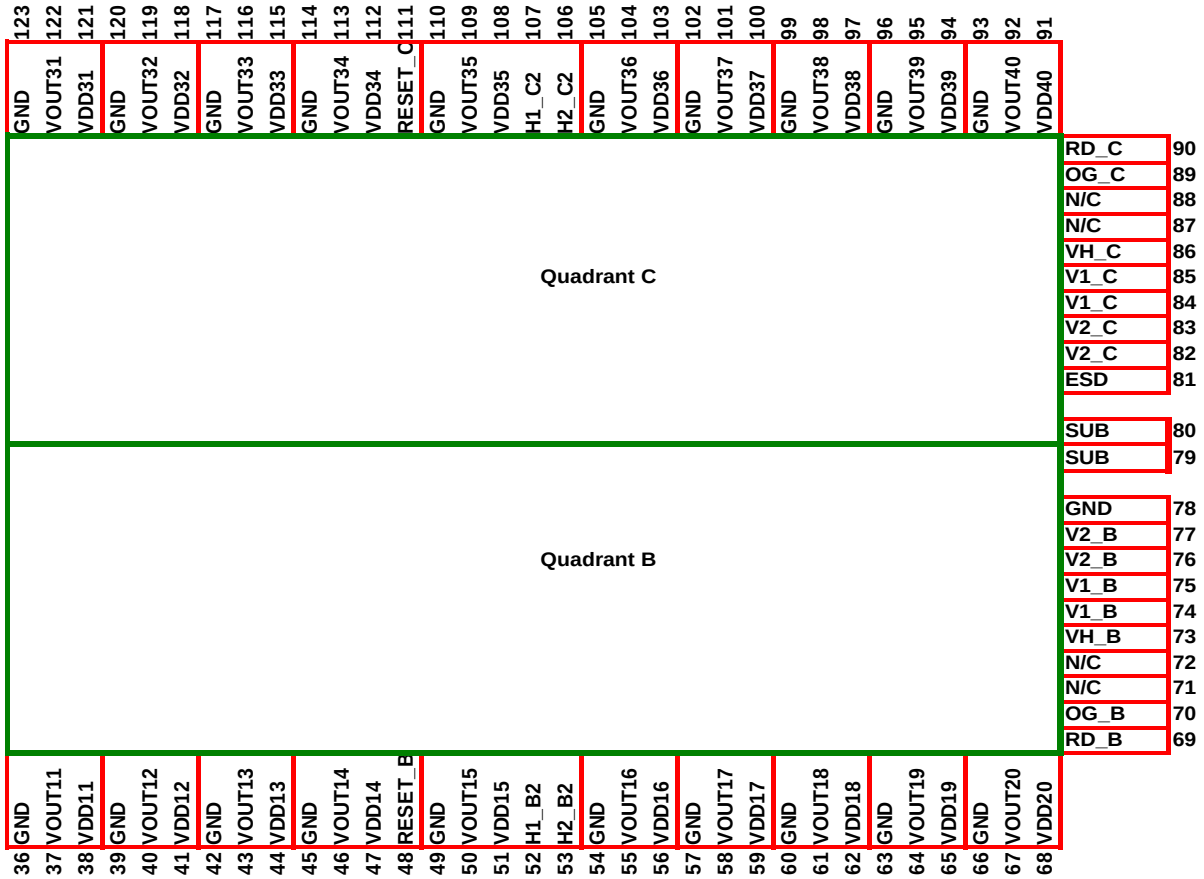


Figure 10: Bond Pad Schematic (right half)

Bond Pad Design

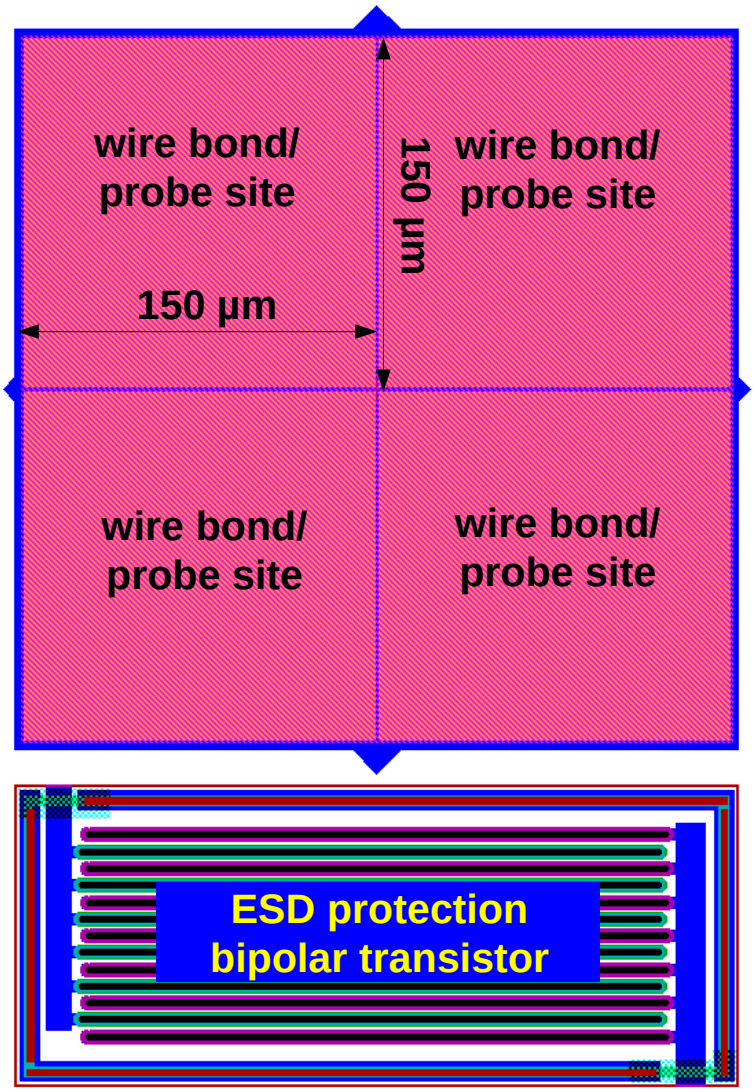


Figure 11: Bond Pad Design

Each bond pad is 300 µm square with 4 wire bond / wafer probe sites. The four sites are delineated by a 2 µm gap in a poly silicon layer underneath the metal pad. It will appear in a microscope as a shallow trench in the metal layer. A metal triangle is located at the center of each side of the bond pad. Each bond pad has an ESD protection transistor located nearby. Not all bond pads will have an ESD protection transistor connected. The pads with ESD protection are listed in the pad location list in Figure 12: Bond Pad Assignment Table.

Bond Pad Locations

Pad	Pad Name	Function	ESD	X (µm)	Y (µm)
1	GND	GND	YES	-17062	-17240
2	VOUT1	VOUT	NO	-16482	-17240
3	VDD1	VDD	NO	-15902	-17240
4	GND	GND	YES	-15334	-17240
5	VOUT2	VOUT	NO	-14754	-17240
6	VDD2	VDD	NO	-14174	-17240
7	GND	GND	YES	-13606	-17240
8	VOUT3	VOUT	NO	-13026	-17240
9	VDD3	VDD	NO	-12446	-17240
10	GND	GND	YES	-11878	-17240
11	VOUT4	VOUT	NO	-11298	-17240
12	VDD4	VDD	NO	-10718	-17240
13	GND	GND	YES	-10200	-17240
14	VOUT5	VOUT	NO	-9860	-17240
15	VDD5	VDD	NO	-9520	-17240
16	H1_A2	H1	YES	-9180	-17240
17	H2_A2	H2	YES	-8840	-17240
18	GND	GND	YES	-8391	-17240
19	VOUT6	VOUT	NO	-7991	-17240
20	VDD6	VDD	NO	-7591	-17240
21	RESET_A	R	YES	-7191	-17240
22	GND	GND	YES	-6694	-17240
23	VOUT7	VOUT	NO	-6114	-17240
24	VDD7	VDD	NO	-5534	-17240
25	GND	GND	YES	-4966	-17240
26	VOUT8	VOUT	NO	-4386	-17240
27	VDD8	VDD	NO	-3806	-17240
28	GND	GND	YES	-3238	-17240
29	VOUT9	VOUT	NO	-2658	-17240
30	VDD9	VDD	NO	-2078	-17240
31	GND	GND	YES	-1560	-17240
32	VOUT10	VOUT	NO	-1220	-17240
33	VDD10	VDD	NO	-880	-17240
34	H1_B1	H1	YES	-540	-17240
35	H2_B1	H2	YES	-200	-17240
36	GND	GND	YES	218	-17240
37	VOUT11	VOUT	NO	798	-17240
38	VDD11	VDD	NO	1378	-17240
39	GND	GND	YES	1946	-17240
40	VOUT12	VOUT	NO	2526	-17240
41	VDD12	VDD	NO	3106	-17240
42	GND	GND	YES	3674	-17240
43	VOUT13	VOUT	NO	4254	-17240
44	VDD13	VDD	NO	4834	-17240
45	GND	GND	YES	5433	-17240

Pad	Pad Name	Function	ESD	X (µm)	Y (µm)
158	GND	GND	YES	-17062	17240
157	VOUT21	VOUT	NO	-16482	17240
156	VDD21	VDD	NO	-15902	17240
155	GND	GND	YES	-15334	17240
154	VOUT22	VOUT	NO	-14754	17240
153	VDD22	VDD	NO	-14174	17240
152	GND	GND	YES	-13606	17240
151	VOUT23	VOUT	NO	-13026	17240
150	VDD23	VDD	NO	-12446	17240
149	GND	GND	YES	-11878	17240
148	VOUT24	VOUT	NO	-11298	17240
147	VDD24	VDD	NO	-10718	17240
146	GND	GND	YES	-10200	17240
145	VOUT25	VOUT	NO	-9860	17240
144	VDD25	VDD	NO	-9520	17240
143	H1_D2	H1	YES	-9180	17240
142	H2_D2	H2	YES	-8840	17240
141	GND	GND	YES	-8391	17240
140	VOUT26	VOUT	NO	-7991	17240
139	VDD26	VDD	NO	-7591	17240
138	RESET_D	R	YES	-7191	17240
137	GND	GND	YES	-6694	17240
136	VOUT27	VOUT	NO	-6114	17240
135	VDD27	VDD	NO	-5534	17240
134	GND	GND	YES	-4966	17240
133	VOUT28	VOUT	NO	-4386	17240
132	VDD28	VDD	NO	-3806	17240
131	GND	GND	YES	-3238	17240
130	VOUT29	VOUT	NO	-2658	17240
129	VDD29	VDD	NO	-2078	17240
128	GND	GND	YES	-1560	17240
127	VOUT30	VOUT	NO	-1220	17240
126	VDD30	VDD	NO	-880	17240
125	H1_C1	H1	YES	-540	17240
124	H2_C1	H2	YES	-200	17240
123	GND	GND	YES	218	17240
122	VOUT31	VOUT	NO	798	17240
121	VDD31	VDD	NO	1378	17240
120	GND	GND	YES	1946	17240
119	VOUT32	VOUT	NO	2526	17240
118	VDD32	VDD	NO	3106	17240
117	GND	GND	YES	3674	17240
116	VOUT33	VOUT	NO	4254	17240
115	VDD33	VDD	NO	4834	17240
114	GND	GND	YES	5433	17240

Pad	Pad Name	Function	ESD	X (µm)	Y (µm)
46	VOUT14	VOUT	NO	5833	-17240
47	VDD14	VDD	NO	6233	-17240
48	RESET_B	R	YES	6633	-17240
49	GND	GND	YES	7080	-17240
50	VOUT15	VOUT	NO	7420	-17240
51	VDD15	VDD	NO	7760	-17240
52	H1_B2	H1	YES	8100	-17240
53	H2_B2	H2	YES	8440	-17240
54	GND	GND	YES	8858	-17240
55	VOUT16	VOUT	NO	9438	-17240
56	VDD16	VDD	NO	10018	-17240
57	GND	GND	YES	10586	-17240
58	VOUT17	VOUT	NO	11166	-17240
59	VDD17	VDD	NO	11746	-17240
60	GND	GND	YES	12314	-17240
61	VOUT18	VOUT	NO	12894	-17240
62	VDD18	VDD	NO	13474	-17240
63	GND	GND	YES	14042	-17240
64	VOUT19	VOUT	NO	14622	-17240
65	VDD19	VDD	NO	15202	-17240
66	GND	GND	YES	15770	-17240
67	VOUT20	VOUT	NO	16350	-17240
68	VDD20	VDD	NO	16930	-17240
69	RD_B	RD	NO	17957	-17240
70	OG_B	OG	YES	17957	-16640
71	N/C	-	NO	17957	-16040
72	N/C	-	NO	17957	-15440
73	VH_B	VH	NO	17957	-14840
74	V1_B	V1	NO	17957	-14240
75	V1_B	V1	NO	17957	-13640
76	V2_B	V2	NO	17957	-13040
77	V2_B	V2	NO	17957	-12440
78	GND	GND	YES	17957	-11840
79	SUB	SUB	NO	17808	-300
80	SUB	SUB	NO	17808	300
81	ESD	ESD	YES	17957	11840
82	V2_C	V2	NO	17957	12440
83	V2_C	V2	NO	17957	13040
84	V1_C	V1	NO	17957	13640
85	V1_C	V1	NO	17957	14240
86	VH_C	VH	NO	17957	14840
87	N/C	-	NO	17957	15440
88	N/C	-	NO	17957	16040
89	OG_C	OG	YES	17957	16640
90	RD_C	RD	NO	17957	17240

Pad	Pad Name	Function	ESD	X (µm)	Y (µm)
113	VOUT34	VOUT	NO	5833	17240
112	VDD34	VDD	NO	6233	17240
111	RESET_C	R	YES	6633	17240
110	GND	GND	YES	7080	17240
109	VOUT35	VOUT	NO	7420	17240
108	VDD35	GND	NO	7760	17240
107	H1_C2	VOUT	YES	8100	17240
106	H2_C2	VDD	YES	8440	17240
105	GND	GND	YES	8858	17240
104	VOUT36	VOUT	NO	9438	17240
103	VDD36	VDD	NO	10018	17240
102	GND	GND	YES	10586	17240
101	VOUT37	VOUT	NO	11166	17240
100	VDD37	VDD	NO	11746	17240
99	GND	GND	YES	12314	17240
98	VOUT38	VOUT	NO	12894	17240
97	VDD38	VDD	NO	13474	17240
96	GND	GND	YES	14042	17240
95	VOUT39	VOUT	NO	14622	17240
94	VDD39	VDD	NO	15202	17240
93	GND	GND	YES	15770	17240
92	VOUT40	VOUT	NO	16350	17240
91	VDD40	VDD	NO	16930	17240
159	RD_D	RD	NO	-17960	17240
160	OG_D	OG	YES	-17960	16640
161	H2_D1	H2	YES	-17960	16040
162	H1_D1	H1	YES	-17960	15440
163	VH_D	VH	NO	-17960	14840
164	V1_D	V1	NO	-17960	14240
165	V1_D	V1	NO	-17960	13640
166	V2_D	V2	NO	-17960	13040
167	V2_D	V2	NO	-17960	12440
168	ESD	ESD	YES	-17960	11840
169	SUB	SUB	NO	-17808	300
170	SUB	SUB	NO	-17808	-300
171	GND	GND	YES	-17960	-11840
172	V2_A	V2	NO	-17960	-12440
173	V2_A	V2	NO	-17960	-13040
174	V1_A	V1	NO	-17960	-13640
175	V1_A	V1	NO	-17960	-14240
176	VH_A	VH	NO	-17960	-14840
177	H1_A1	H1	YES	-17960	-15440
178	H2_A1	H2	YES	-17960	-16040
179	OG_A	OG	YES	-17960	-16640
180	RD_A	RD	NO	-17960	-17240

Figure 12: Bond Pad Assignment Table

Die Orientation

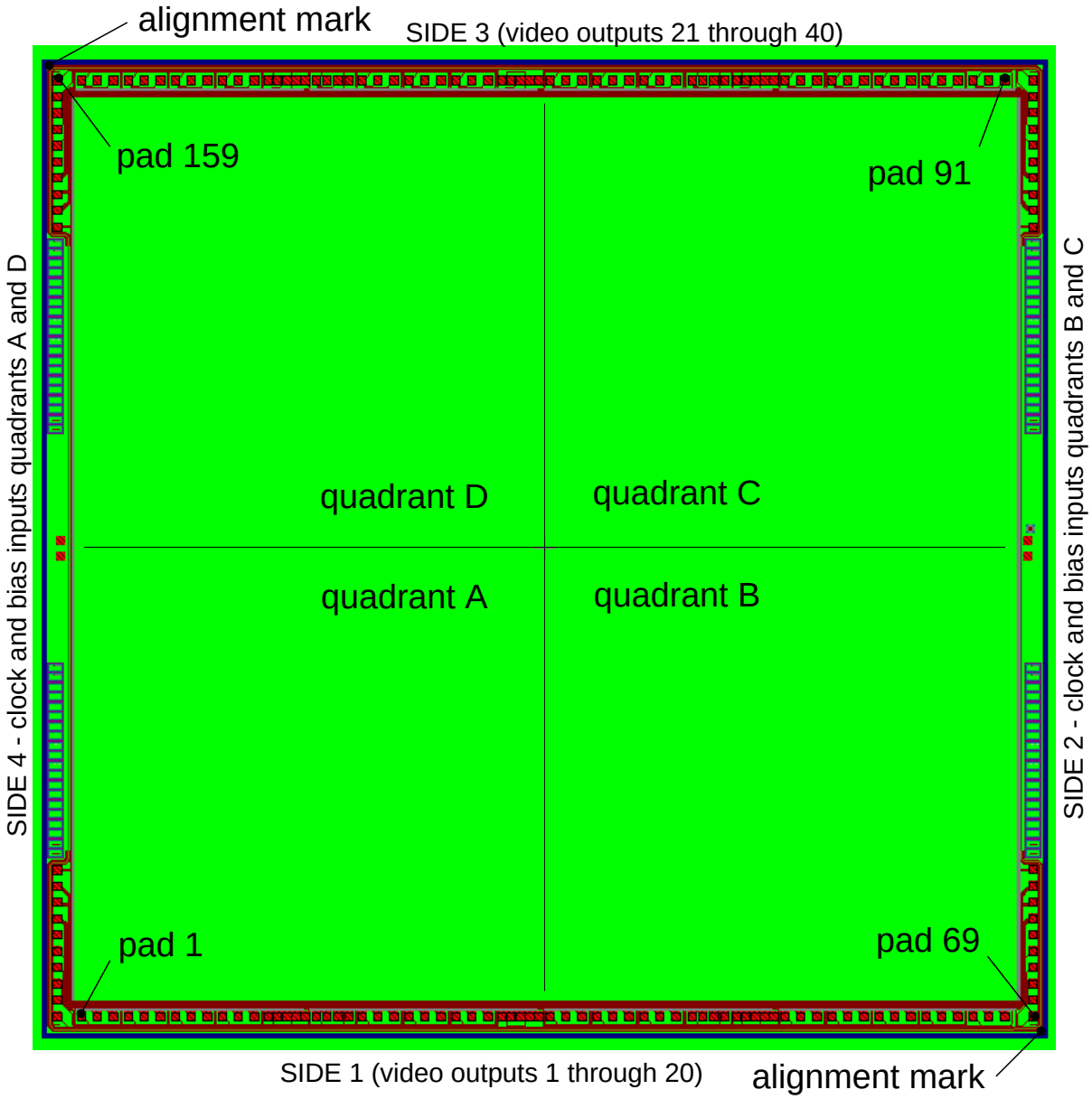


Figure 13: Die Orientation

Pad One Mark

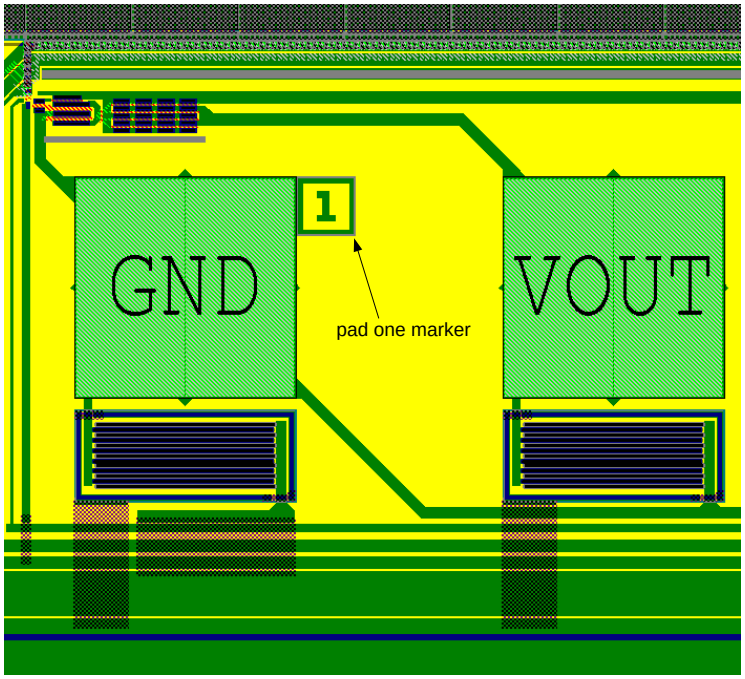


Figure 14: Pad One Marker

Die Alignment Mark

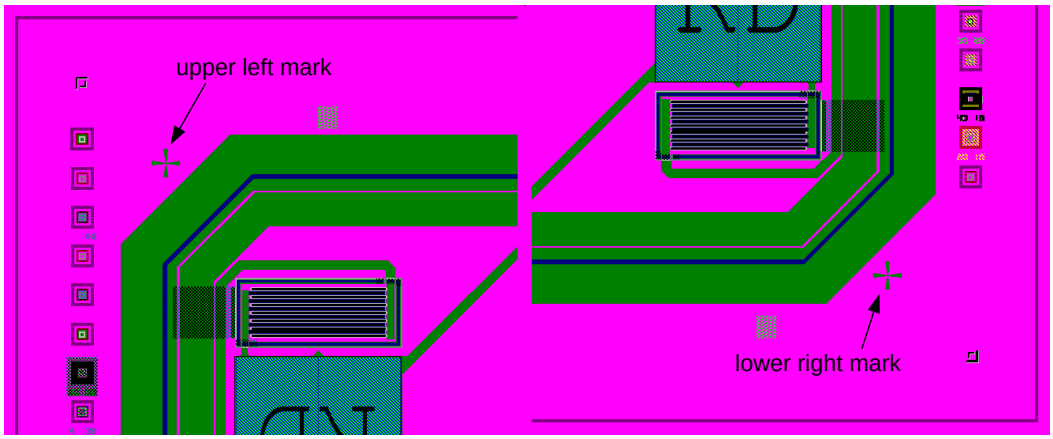


Figure 15: Die Alignment Marks

The alignment marks are on a diagonal line passing through the optical and geometric center of the die.

Mark Location	X (µm)	Y (µm)
Top Left	-18229.9	17737.2
Bottom Right	18229.9	-17737.2

Performance

Power – Estimated

Amplifier	1st & 2nd	3rd
Current (mA)	0.75	5
Voltage (V)	15	7
Outputs	40	40
Power (mW)	450	1400

Parameter	VCCD (GND)	VCCD (V1-V2)	HCCD (GND)	HCCD (H1-H2)
Capacitance (nF)	400	24	0.8	0.2
Voltage (V)	9	18	5	10
Frequency (MHz)	0.071	0.071	17	17
Power (mW)	2305	553	340	340

Total estimated power is 5.4W.

This power estimate uses a simple model of fCV^2. This is will overestimate the power dissipated by the CCDs. The output amplifier power values are expected to be accurate.

Imaging Performance

Image Performance Operational Conditions

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions:

Description	Condition	Notes
Frame time	33 msec	1
Horizontal clock frequency	20 MHz	
Light source (LED)	green illumination centered 530 nm	2
Operation	Nominal operating voltages and timing	

Notes:
1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.

Imaging Performance Specifications

Description	Symbol	Min.	Nom.	Max.	Units	Sample Plan	Test Temp (°C)	Notes
Dark Current			<200	<500	pA/cm^2	Die	20	1
Maximum Photoresponse Nonlinearity	NL		2	3	%	Die	20	2, 3
Maximum Gain Difference Between Outputs	ΔG		4	10	%	Die	20	2, 3
Horizontal CCD Charge Capacity	HNe	60	65		ke^-	Design	20	
Vertical CCD Charge Capacity	VNe	54	60		ke^-	Die	20	
Photodiode Charge Capacity	PNe	45	50		ke^-	Die	20	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99997				Design	20	
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999				Design	20	
Photoresponse Non-Uniformity	PRNU	1	-	3	%	Die	20	
Photodiode Dark Current	Ipd		60		e/p/s	Die	20	
Photodiode Dark Current	Ipd		0.05	0.2	nA/cm^2	Die	20	
Vertical CCD Dark Current	Ivd		280		e/p/s	Die	20	
Vertical CCD Dark Current	Ivd		0.2	0.5	nA/cm^2	Die	20	
Image Lag	Lag		<10	50	e^-	Die	20	
Antiblooming Factor	Xab	100	200			Device	20	
Vertical Smear	Smr		85		db	Device	20	
Sensor Read Noise	ne-T		23	25	e^- rms	Design	20	4
Output Amplifier DC Offset	Vodc	4	8.5	14	V	Die	20	
Output Amplifier Impedance	ROUT	100	130	200	Ohms	Die	20	
Output Amplifier Sensitivity	ΔV/ΔN	30	32	-	$\mu V/e^-$	Die	20	
Solar Weighted Average Quantum Efficiency	QEmin	29	31		%	Device	20	
Modulation Transfer Function	MTF	55	58		%	FM device	20	

Notes:
1. Before irradiation.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning
4. The value does not directly include the system noise. The system electronics noise (at 20MHz) is subtracted out in quadrature.

Typical Performance Curves

Quantum Efficiency

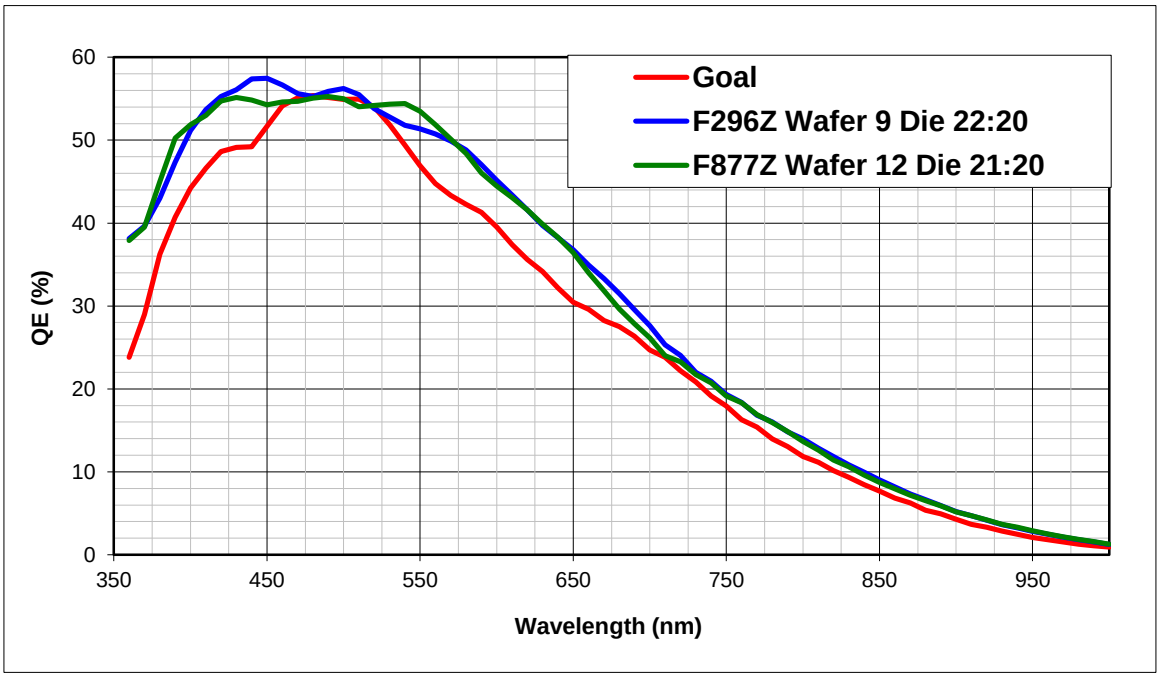


Figure 16: Monochrome Quantum Efficiency

Angular Quantum Efficiency

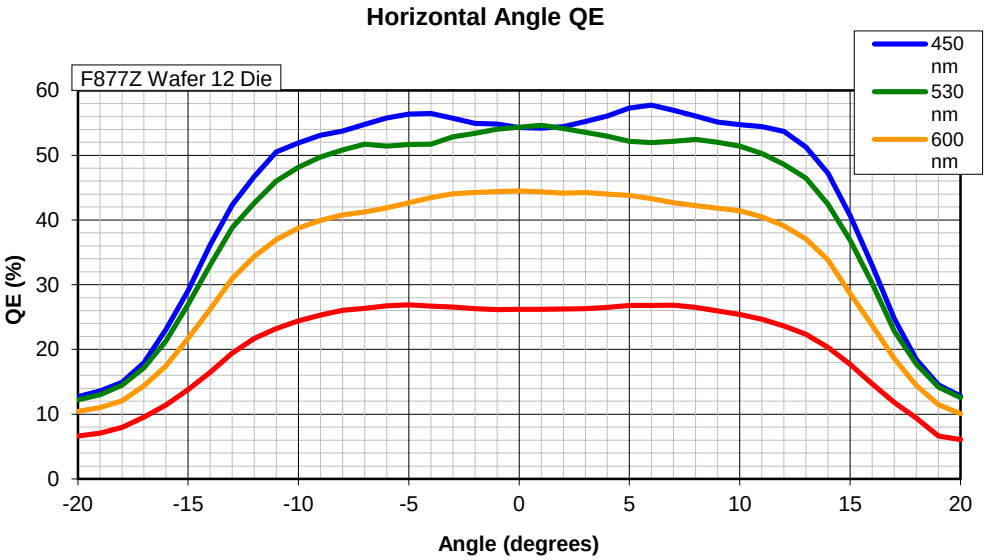


Figure 17: Angular Quantum Efficiency

Horizontal and Vertical MTF

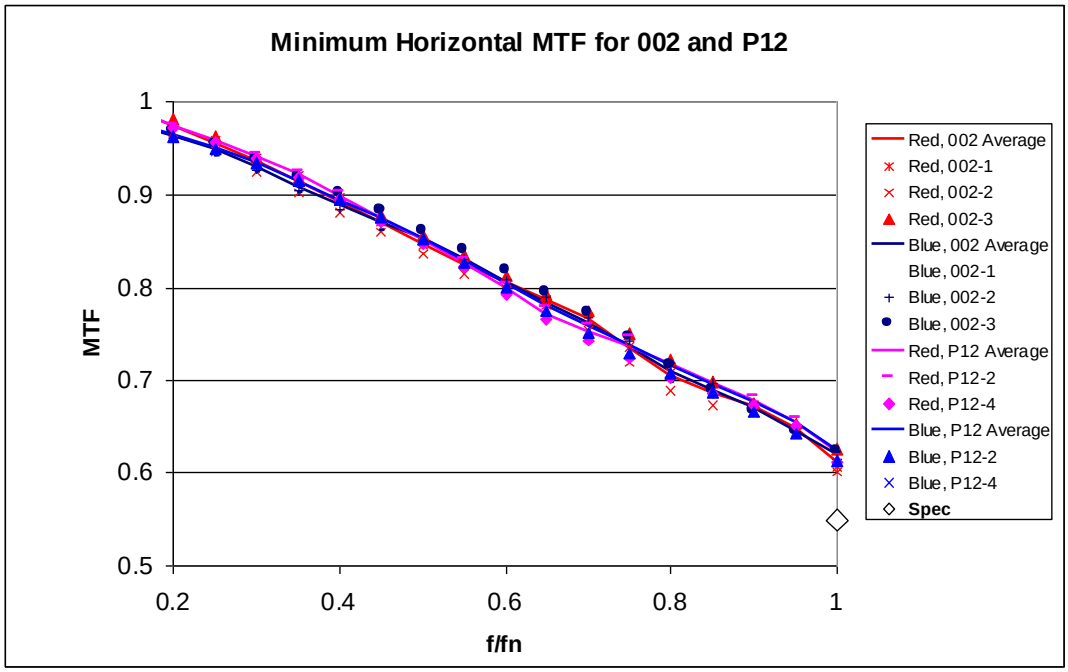


Figure 18: KAI-18000 Horizontal MTF

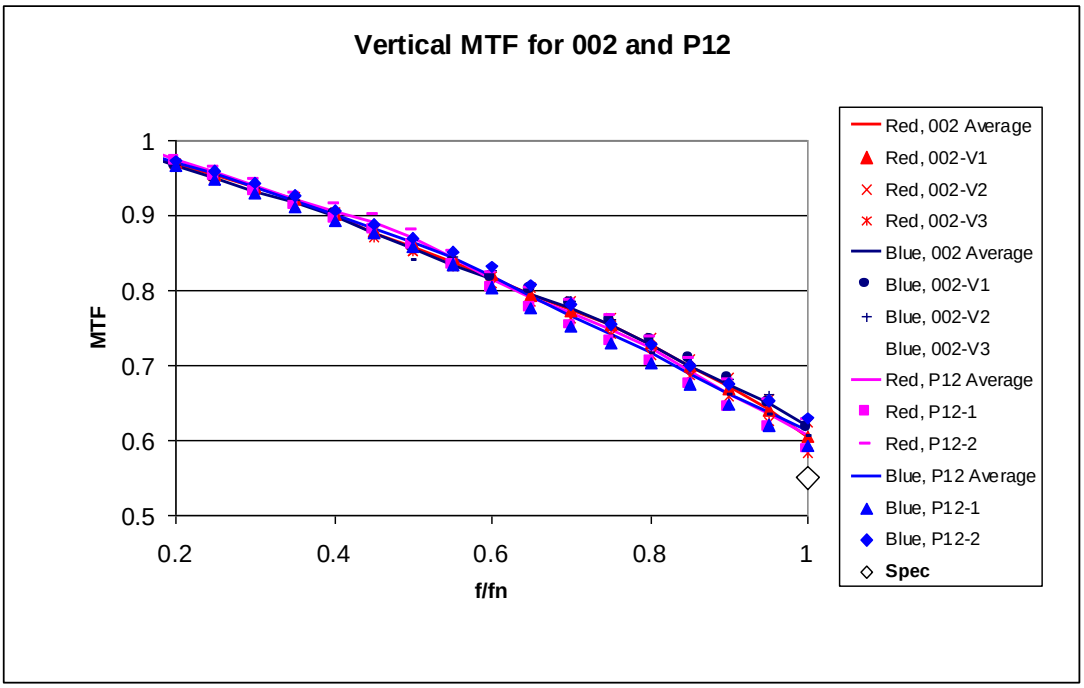


Figure 19: KAI-18000 Vertical MTF

Defect Definitions

SPECIFICATIONS

Description	Definition	Monochrome with Microlens Only
Major dark field defective bright pixel	Defect ≥ 25 mV	200
Major bright field (80% Saturation) defective dark pixel	Defect ≥ 15%	
Minor dark field defective bright pixel	Defect ≥ 8 mV	2000
Cluster defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally	80
Column defect	A group of more than 10 contiguous major defective pixels along a single column	≤1

Notes:

1. Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Operation

Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Temperature	T	-50	50	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	Iout	0.0	6.0	mA	3
Off-chip Load	C_L		25	pF	4

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25 °C. Excessive humidity will degrade MTTF.
3. Total for both outputs. Current is 5 mA for each output. Note that the current bias affects the amplifier bandwidth.
4. With the maximum clock frequency of 17 MHz.

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Maximum Voltage Ratings Between Pin (or Function)

Description	Minimum	Maximum	Units	Notes
R, VH, H1, H2, OG, and GND to ESD	0	17	V	
Pin to Pin with ESD Protection	-17	17	V	1
VDD to GND	0	25	V	

Notes:
1. Pin functions with ESD protection are: R, VH, H1, H2, and OG.

Expected Range of DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Gate	OG	-3.25	-3.0	-2.75	V	0.001	
Reset Drain	RD	12.25	12.5	12.75	V	0.001	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	0.8	3
Ground	GND	0.0	0.0	0.0	V		
Substrate	SUB	8.0	Vab	15.0	V		1
ESD Protection	ESD	-9.5	-9.0	-8.5	V	1.0	2

Notes:
1. The operating value of the substrate voltage, Vab, will be marked on the shipping container for each device. The value Vab is set such that the photodiode charge capacity is still linear; 0.5 volt away from peak value.
2. VESD must be more negative than H1, H2, OG, GND, and R during sensors operation AND during camera power turn on.
3. One output, unloaded.

AC Operating Conditions

Expected Range of Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V2H	9.75	10.0	10.25	V	
Vertical CCD Clock Midlevel	V1M, V2M	-0.25	0.0	0.25	V	1
Vertical CCD Clock Low	V1L, V2L	-9.25	-9.0	-8.75	V	2
Horizontal CCD Clock High	H1H, H2H	0.25	0.5	0.75	V	3
Horizontal CCD Clock Low	H1L, H2L	-5.25	-5.0	-4.75	V	
Horizontal CCD Clock Amplitude	H1, H2		5		V	4
Reset Clock Low - Specified Value	RL	-2.9	-2.8	-2.7	V	6
Reset Clock Amplitude	Ramp	5.5V				7
Electronic Shutter Voltage	Vshutter	37	40	44	V	
Vertical-Horizontal High	VHH	2	2.25	2.5	V	5
Vertical-Horizontal Low	VHL	-9.25	-9	-8.75	V	2

Notes:
1. V1M and V2M must be the same voltage
2. V1L, V2L, and VHL must be the same voltage
3. H1H and H2H must be the same voltage
4. H1 and H2 must have the same offset and amplitude
5. For improved radiation durability set VHH 1V higher than V1M, V2M
6. The Reset Clock Low Voltage will be specified for each KAI-18000 image sensor delivered to the customer. The tolerance allowed for the *actual* Reset Clock Low Voltage.
7. A minimum level for the Reset Clock Amplitude is specified. The Reset Clock High level (RH) can be defined as the *actual* Reset Clock Low level plus a fixed minimum amplitude (Ramp). See Figure 33: Reset and HCCD Timing Detail.

Power Up Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

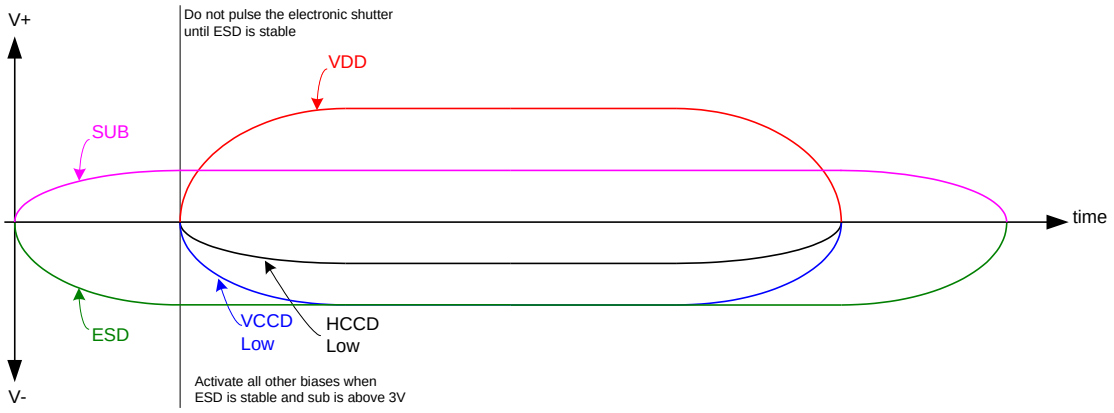


Figure 20: Power Up and Power Down Sequence

Notes:

1. Activate all other biases when ESD is stable and SUB is above 3V
2. Do not pulse the electronic shutter until ESD is stable
3. VDD cannot be +15V when SUB is 0V
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.
5. An acceptable power-up sequence can be energize VSUB followed by ESD, then, when ESD is stable, energize RD, VDD, OG. The remaining clock levels can be activated in any order.

The VCCD clock waveform must not have a negative overshoot more than 0.4V below the ESD voltage.

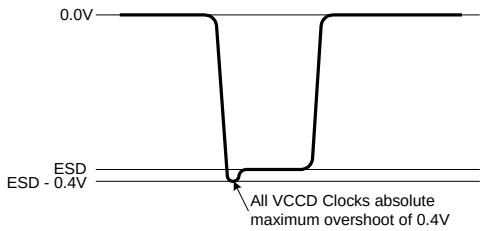


Figure 21: VCCD clock negative overshoot

Example of external diode protection for SUB, VDD and ESD. α denotes 1-40.

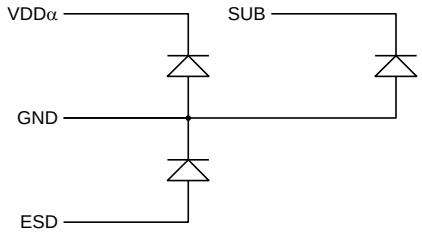


Figure 22: External Diode Protection recommendation

Clock Line Capacitances

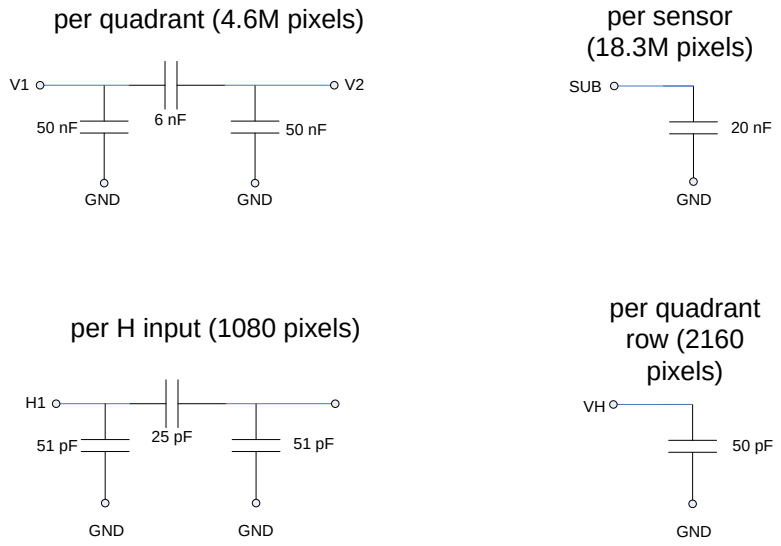


Figure 23: Clock Line Capacitance

All bond pads have a capacitance of 3.1pF not included in this figure.

Notes:

1. The clock line capacitances do not include all input impedance characteristics of the KAI-18000 device. As such, they do not fully represent a valid equivalent circuit model. The capacitance drawings are only provided to help estimate the current drive requirements on the respective V and H clocks.

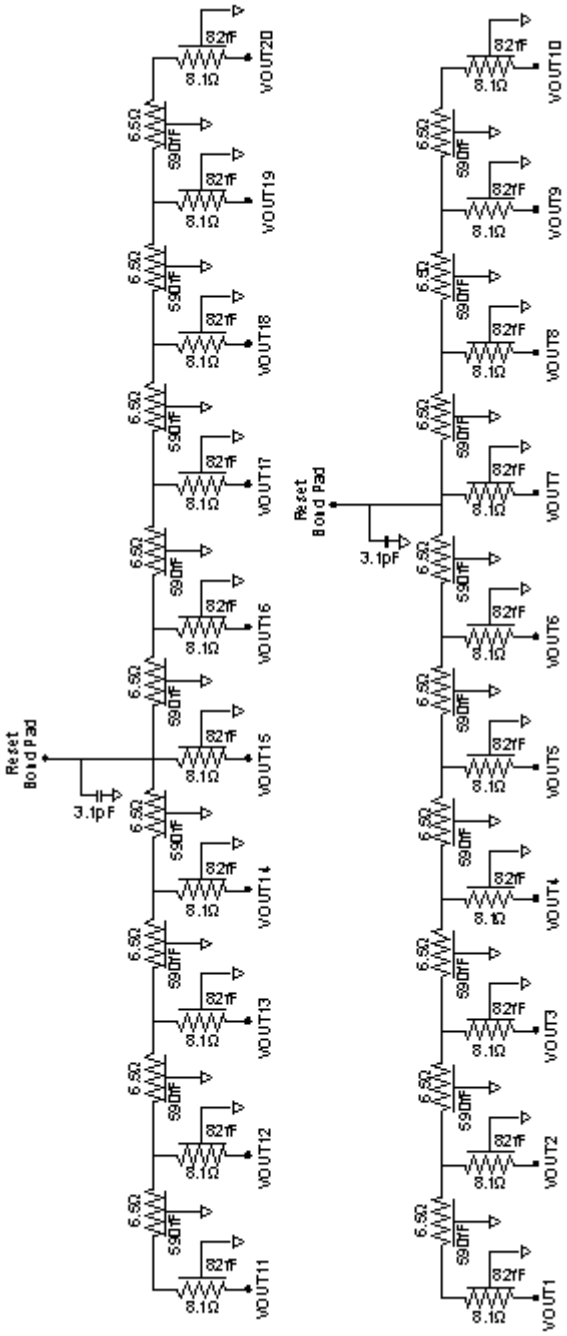


Figure 24: Reset Clock Line Capacitance

Notes:

1. The clock line capacitances do not include all input impedance characteristics of the KAI-18000 device. As such, they do not fully represent a valid equivalent circuit model. The capacitance drawings are only provided to help estimate the current drive requirements on the respective Reset clocks.

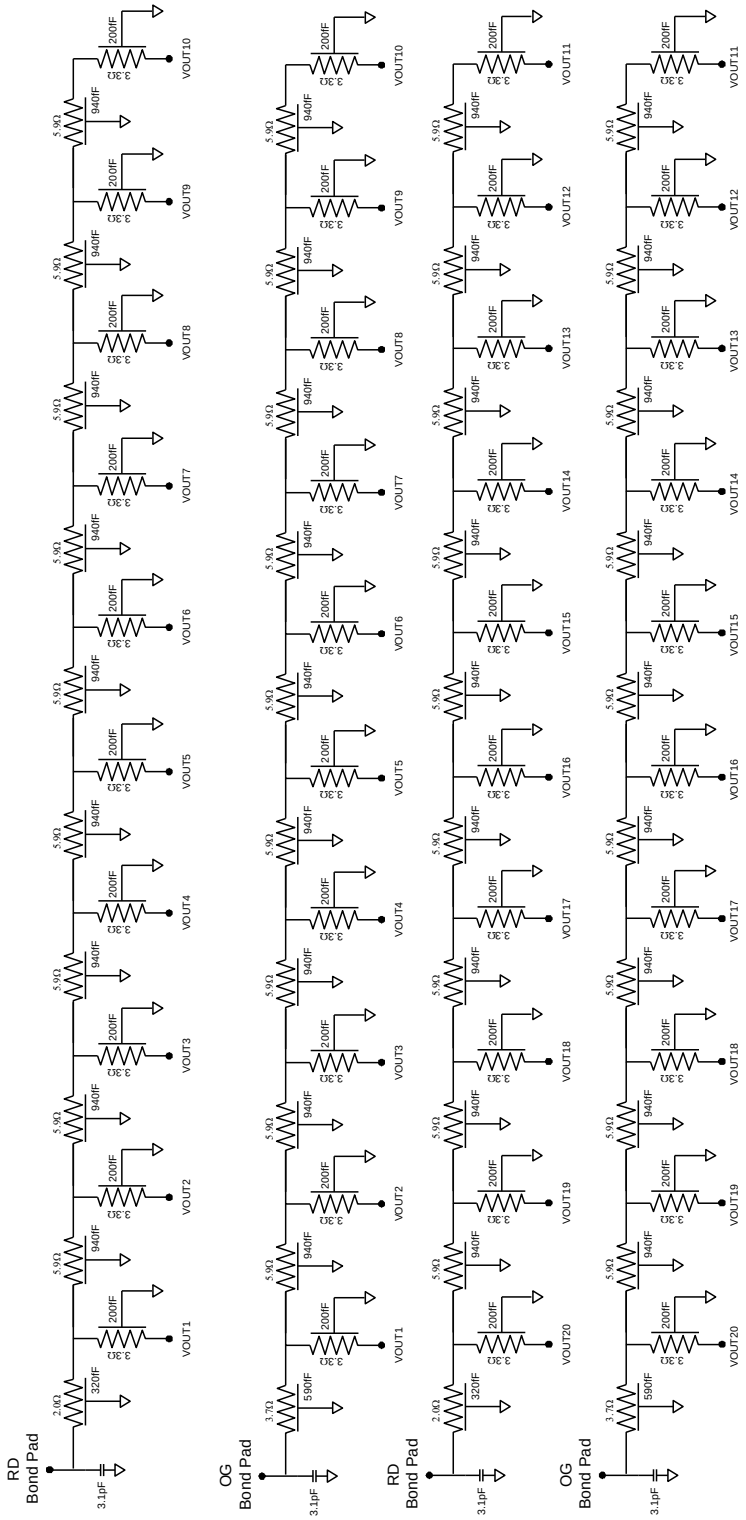


Figure 25: RD and OG Line Capacitances

Timing Requirements (For 17 MHz Operation)

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
VCCD Delay	TVD		2.0		µs	
Horizontal Retrace Time	TVT		1.0		µs	
VH Transfer time high	TVHM		0.25		µs	
VH Transfer time low	TVHL		0.50		µs	
VCCD Transfer time high	TVM		3		µs	
VCCD Transfer rise/fall time	TVS		4.029		µs	
Line Time	TL		14.058		µs	
VCCD Transfer rise/fall time	TVS		4.029		µs	
Photodiode Transfer time	TV2H		10.0		µs	
VCCD Pedestal time	TVPD		20		µs	
VCCD Delay	TVST		200		µs	
Reset Pulse time	TR	6		8	ns	
Reset Pulse Rise Time	TRT	0		4	ns	
Reset/HCCD alignment	THR	0	2	4		
HCCD Clock Level Time	TH		21.4			
HCCD Clock Rise Time	THT	0	8	10		
Shutter Pulse time	TSH		5		µs	
Pixel Clock Period	TPIX		58.82353		ns	

TIMING

Image Readout Flow

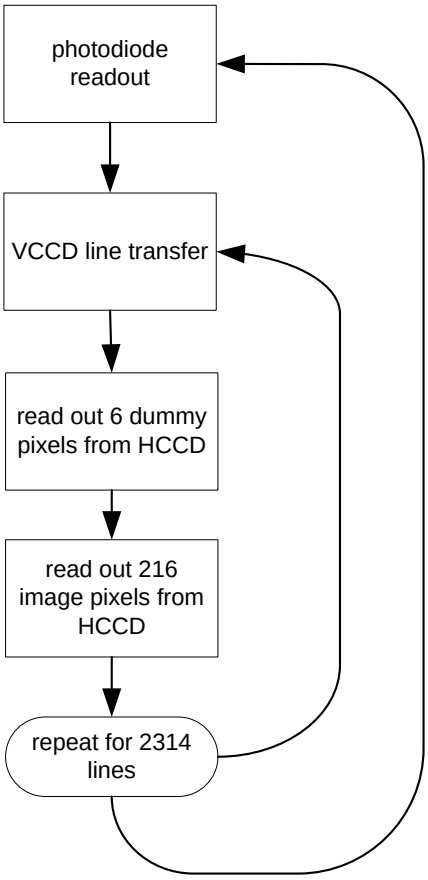


Figure 26: Image Readout Flow

The image readout sequence begins with the photodiode to VCCD transfer. The transfer gate is turned on by raising the V2 gate voltage above 9 V. The integration time ends on the falling edge transition from the V2 high level to the V2 midlevel voltage. Each VCCD clock cycle transfers the entire image one line towards the HCCD. The first 32 lines will contain only VCCD dark current and smear signal. The next 2080 lines will contain data from photoactive pixels. While the VCCD is emptied in 2112 lines, 2314 lines are needed to stretch out the total frame time to 33.3 ms. The VCCD should be clocked continuously. Stopping the VCCD clock will cause non-uniformities in dark current and smear signal.

Electronic Shutter Timing Flow

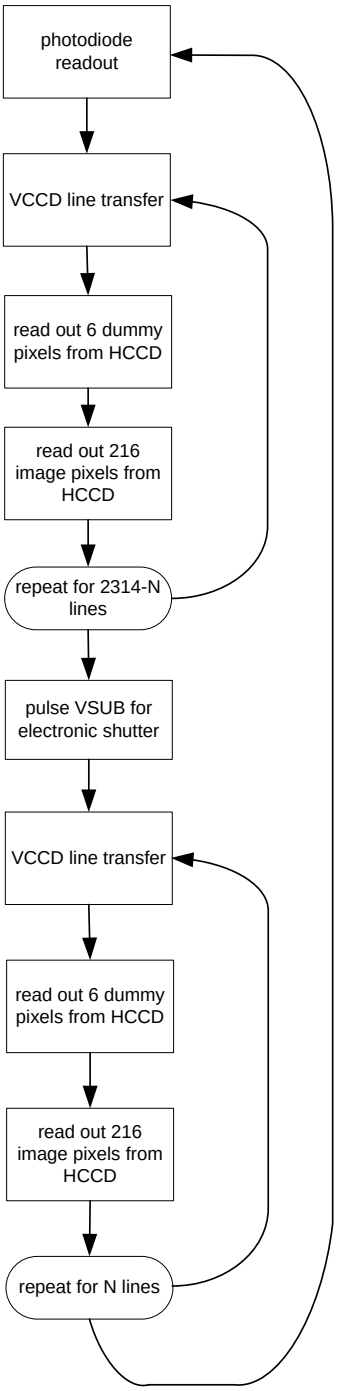


Figure 27: Electronic Shutter Timing Flow

Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 45 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 45 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-18000 VCCD has a charge capacity of 60,000 electrons (60 ke^-). If the SUB voltage is set such that the photodiode holds more than 60 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles (or more) in size. The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded (for example, by a very bright light source). it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity.

This results in blooming. The amount of antiblooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is specified separately for each KAI-18000 image sensor. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 50 ke^- of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of T_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 40 volts T_{INT} seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

Large Signal Output

The charge handling capacity of the output amplifier is set by the reset clock voltage levels. The reset clock driver circuit is very simple if an amplitude of 5 V is used. The low level of the reset clock determines the maximum amount of charge that can be sampled by the output amplifier. The high level determines how stable the video DC offset level will be. The large signal output of KAI-18000 (1.5 V) requires that the low level voltage of the reset clock be fine-tuned for each KAI-18000 image sensor. This will ensure the maximum amount of reliability from channel potential shifts caused by radiation damage.

Line Timing

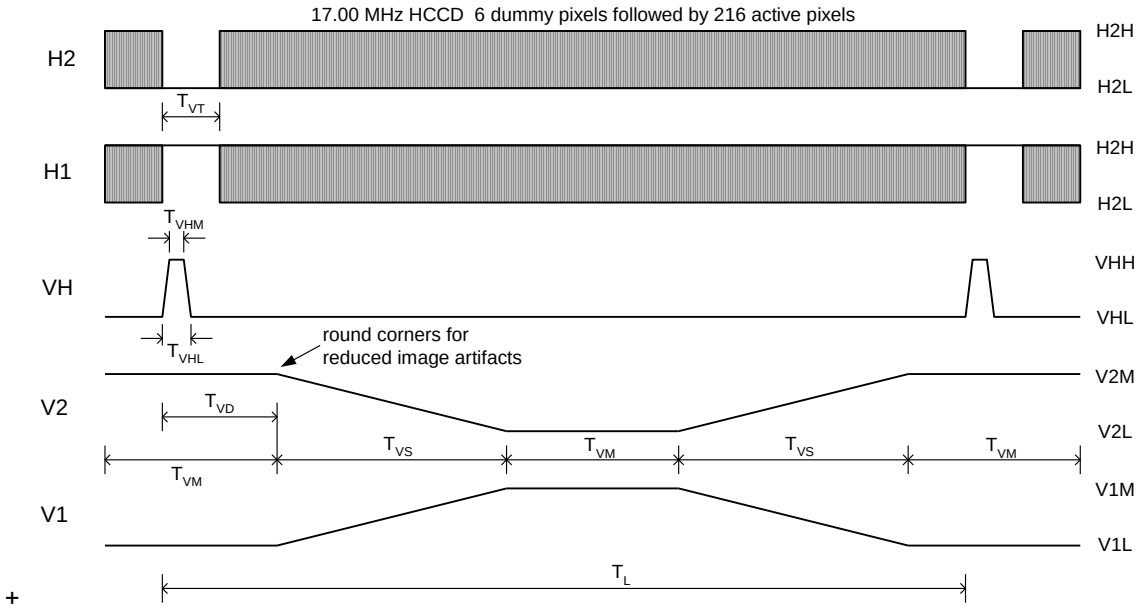


Figure 28: Line Timing

Charge begins to transfer from the vertical to the horizontal CCD on the rising edge of the VH clock. The transfer is completed 500 ns after the falling edge of the VH clock. The H1 and H2 clocks must be stopped during the VH transfer time. The main VCCD in the pixel array cannot transfer in 1 µs so the V1 and V2 clock transitions are spread out over the entire 14.058 µs line time. The V1 and V2 clocks have a large capacitive coupling to the GND (p-well) of the image sensor. Any rapid changes or glitches on the V1 or V2 clocks will likely couple into the video output and degrade image quality. Image artifacts are best avoided by ensuring a smooth, and as slow as possible clock waveform that will fit into 14.058 µs.

The line timing should be repeated continuously even after the last photoactive line has been read out. This will ensure a uniform dark current and smear signal background level. The only exception is when the sensor is in stand-by mode. In standby mode the V1, V2, VH, H1, and H2 clocks are set at 0 V. At the end of standby mode clock the VCCD for at least 100 ms before acquiring the first image.

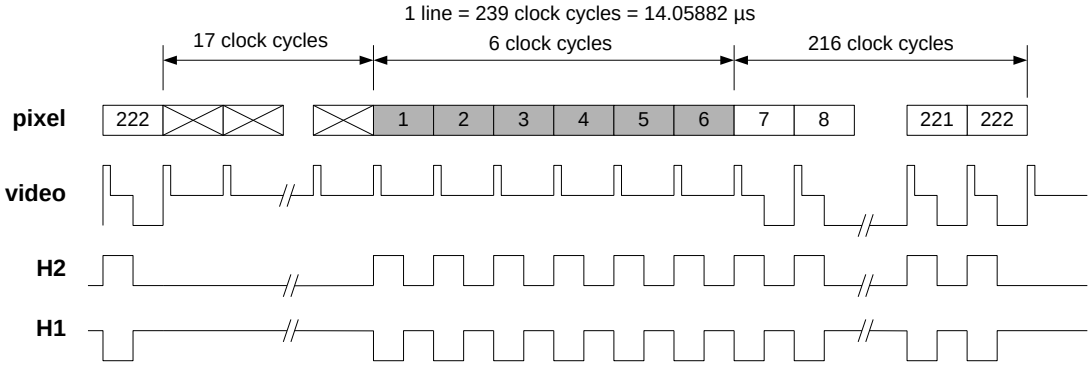


Figure 29: Line Timing Detail

Edge Alignment V1 and V2 clock

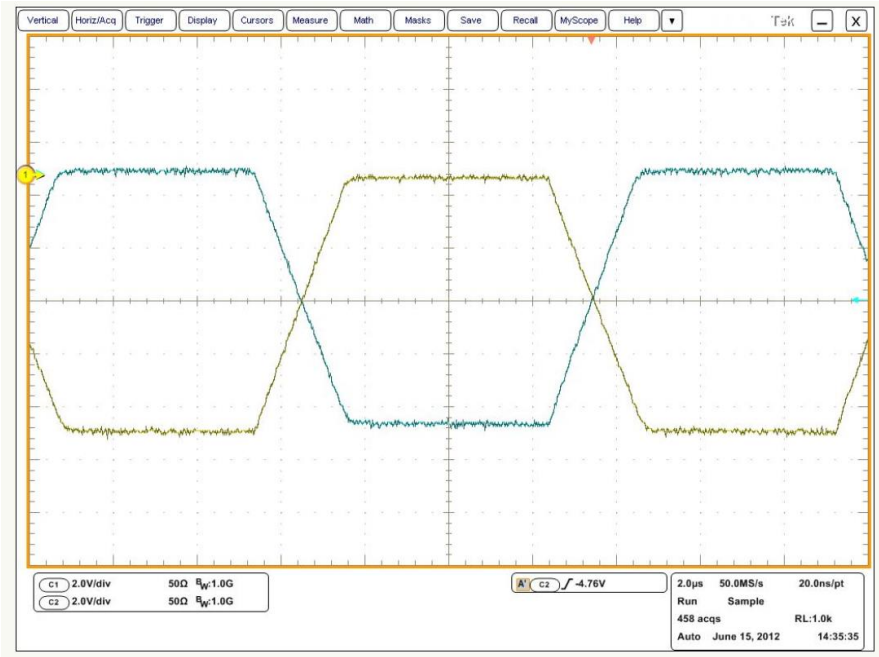


Figure 30: Example of Vertical Clock Crossover - targeted at 50%

Notes:

1. Trace 1: V1 Clock
2. Trace 2: V2 Clock

For good video waveforms the circuit design should target a V1-V2 crossover at 50%.

Frame Timing

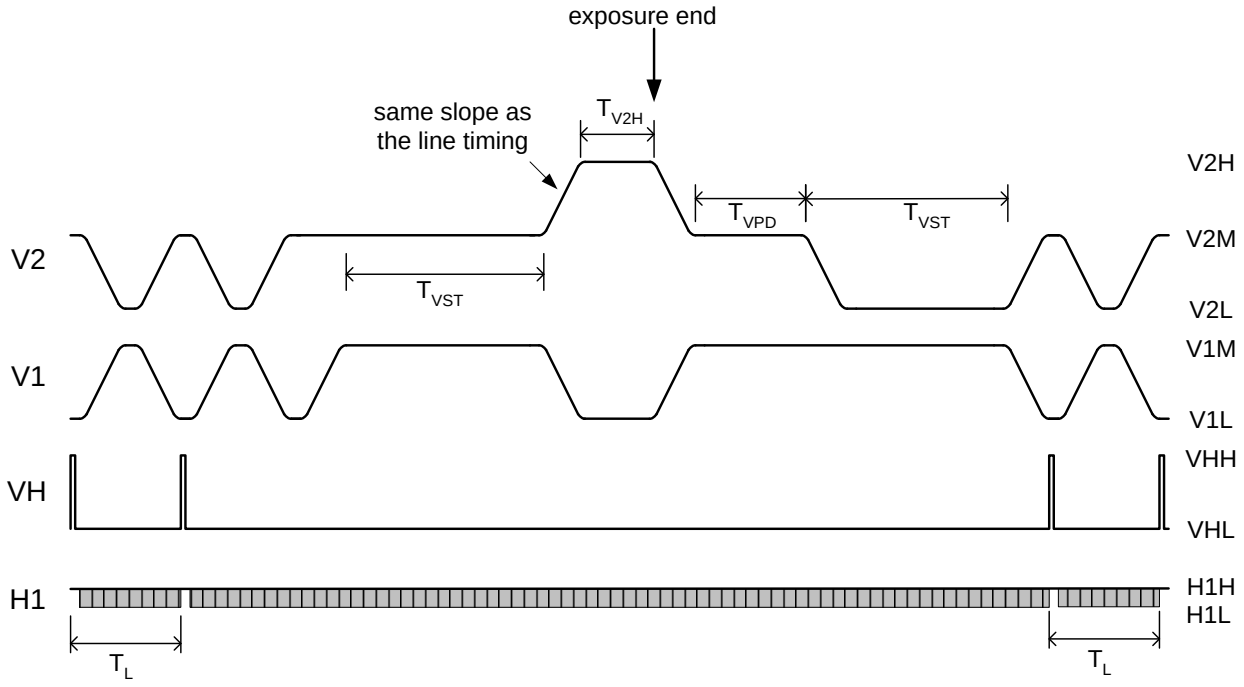


Figure 31: Frame Timing

The frame timing sequence causes all photodiodes to transfer their charge to the VCCD. The transfer completes on the falling edge of V2 from V2H to V2M. The V2 clock must be at the V2H level for at least TV2H time. The sloped edges are not critical in the frame timing because valid image data is not being sampled. The V2M to V2H rising and falling edges must be compensated by equal slopes on the V1 clock transitioning between V1M and V1L. Failure to compensate those edges will result in incomplete photodiode to VCCD charge transfer.

Pixel Timing

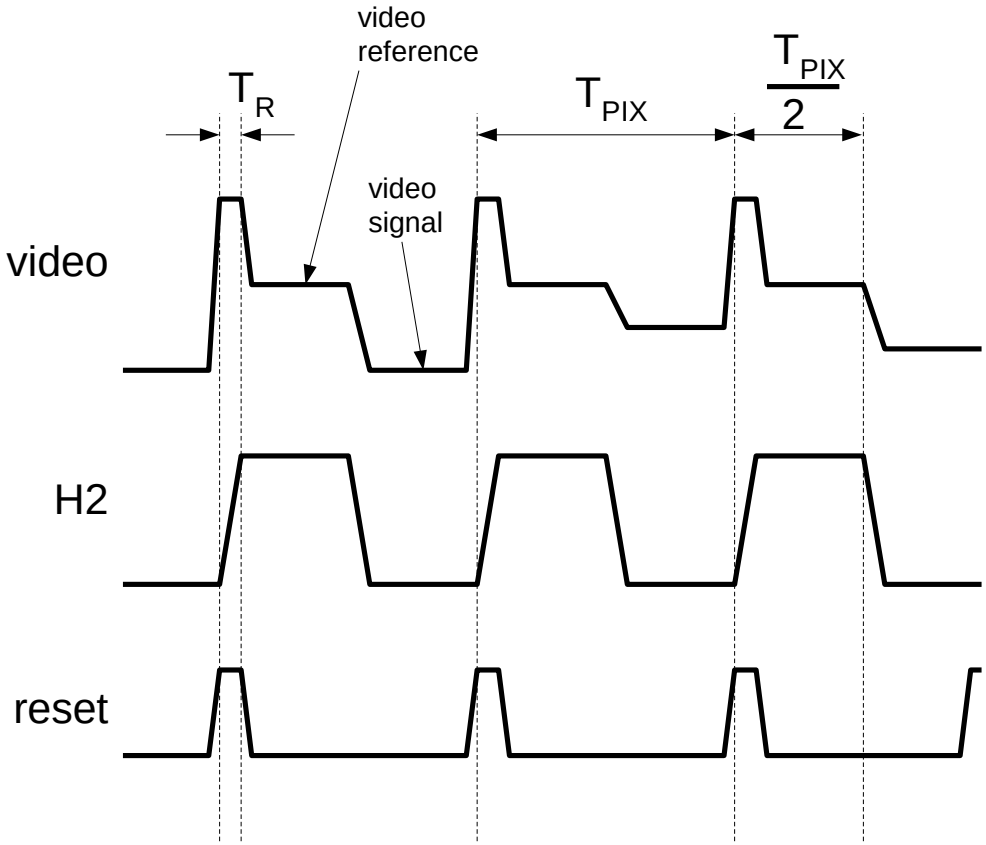
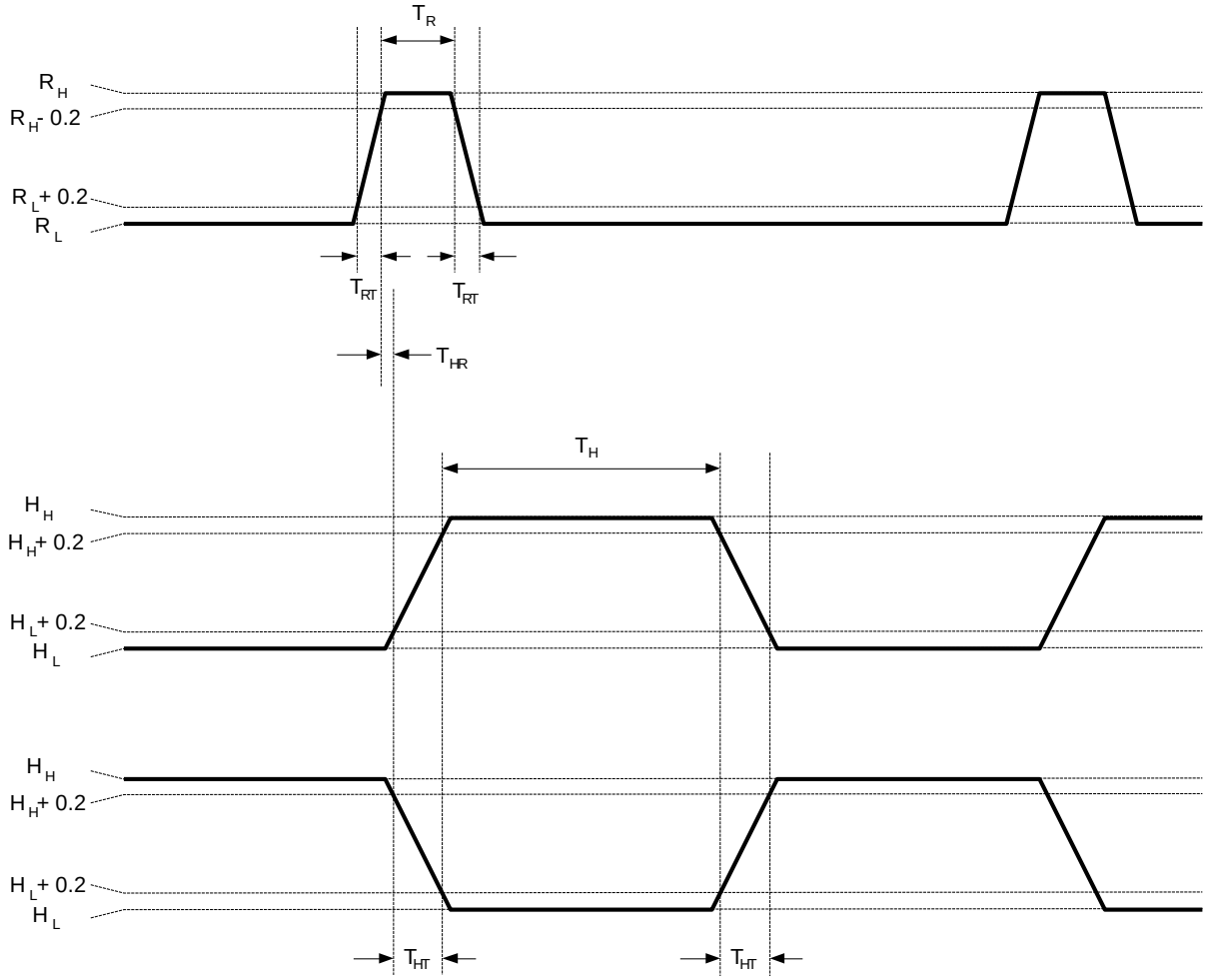


Figure 32: Pixel Timing

The reset clock should be coincident with the rising edge of the H2 clock. There is no minimum time for the rise and fall times of the clocks. The maximum rise and fall times are determined by how much time the correlated double sampling circuit needs for its sampling operations.



Note: R_L is assigned at delivery. R_H, as shown , is the peak value for this signal and is defined as $R_L + R_{amp}$

Figure 33: Reset and HCCD Timing Detail

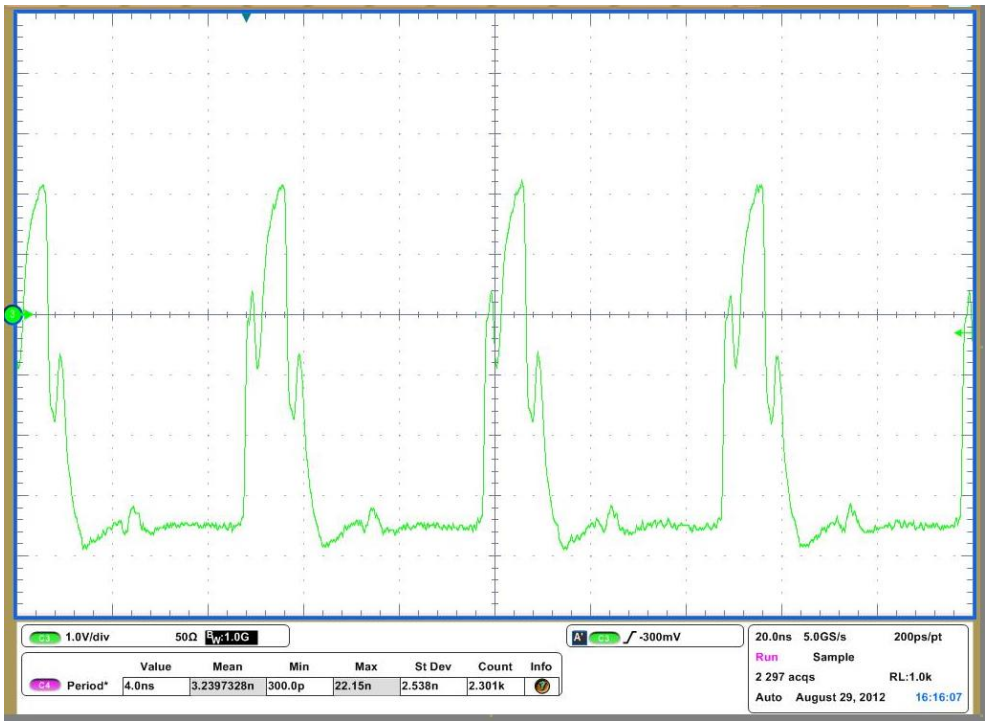


Figure 34: Reset Clock Waveform

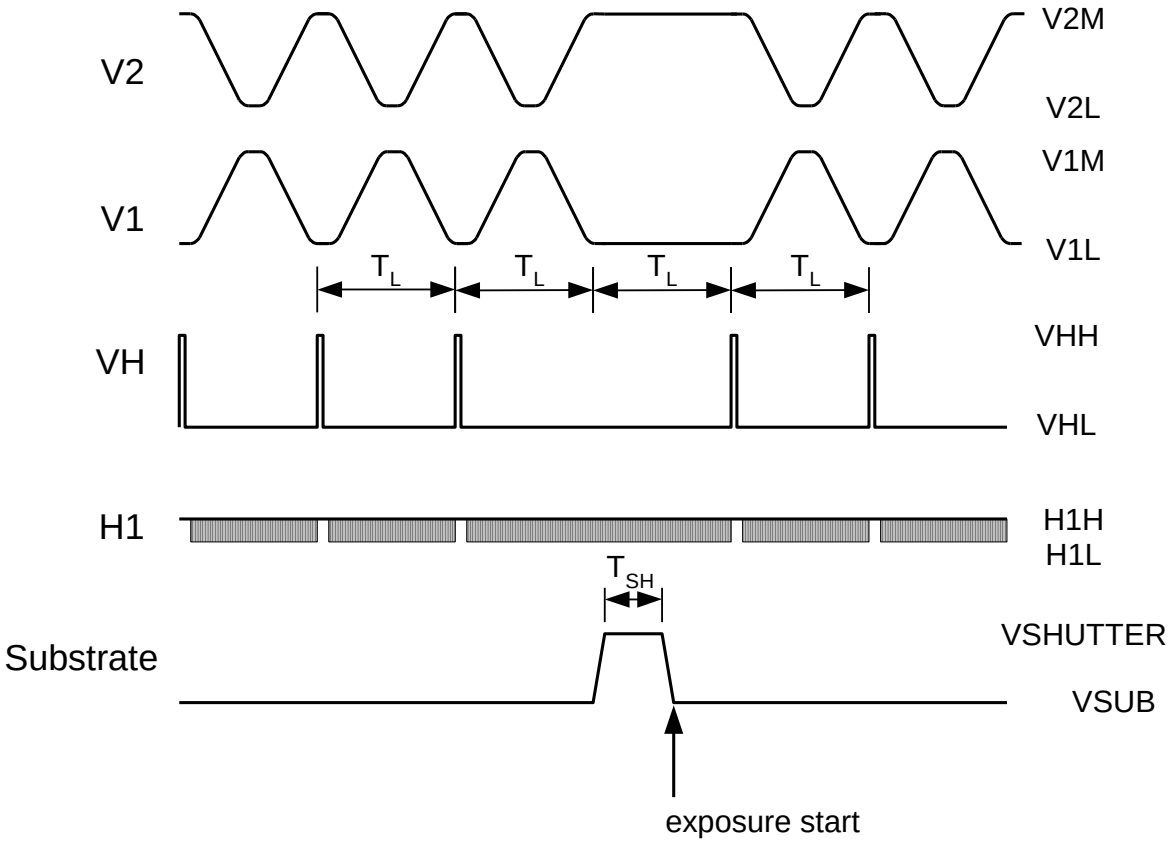


Figure 35: Electronic Shutter Timing

All charge in the photodiodes is discharged to the substrate when the substrate connection is pulsed above 40 V. The photodiode begin collecting photo-signal (exposure start) on the falling edge of the substrate pulse. The substrate pulse should come after the last valid pixel of a line has been read out and sampled from the HCCD. Hold the VCCD clocks idle during the substrate pulse period. Do not pulse the substrate while reading out valid image data from the HCCD. Continue clocking the reset clock and HCCD during the electronic shuttering.

Video Loading

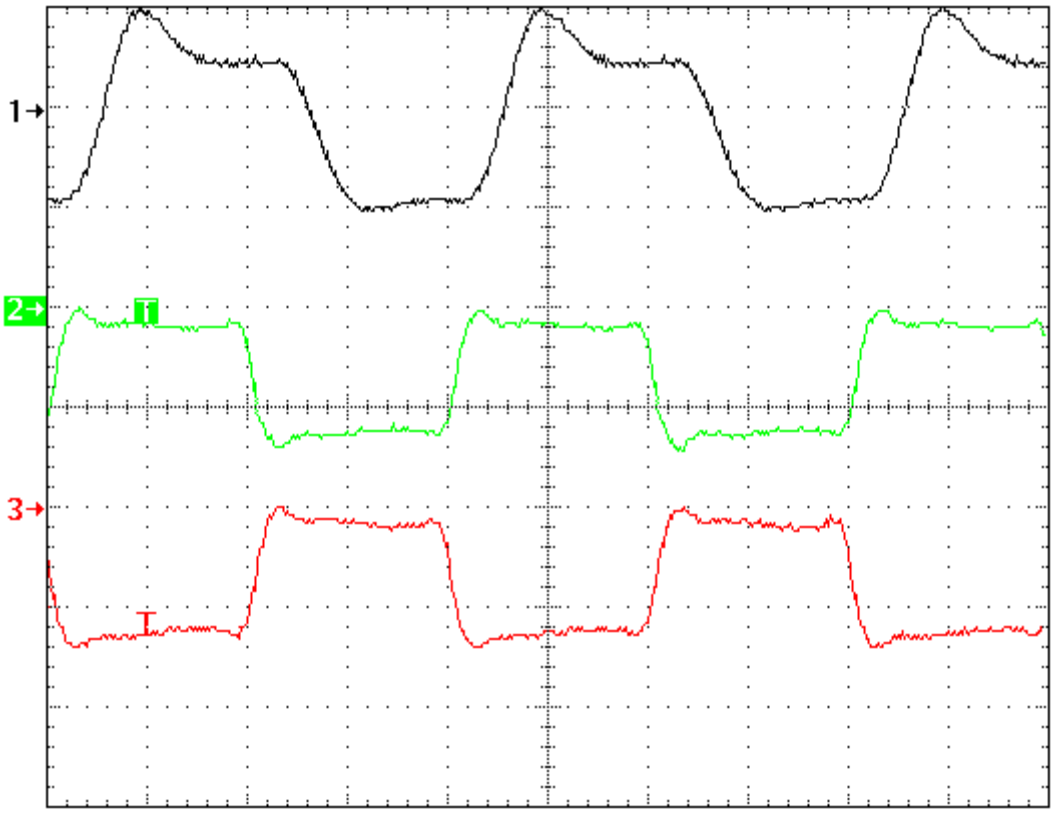


Figure 36: Video Output Waveform

Notes:

3. Trace 1: Video KAI-18000 Waveform
4. Trace 2: H Clock
5. Trace 3: H Clock

For good video waveforms the total load on the image sensor video output bond pad should be less than 30 pF for a 17 MHz pixel clock. This is with a 5 mA load current on the output amplifier bond pad.

Noise Factors

The following list ranks the input pins of the image sensor in order of their importance to noise performance.

1. OG
2. Reset (clock level and timing jitter)
3. GND
4. VDD
5. H2 (timing jitter)
6. H1 (timing jitter)
7. RD
8. V1, V2, VH
9. SUB
10. ESD

OG and Reset will couple noise onto the output with about a 5 to 1 ratio. A 5 µV change on OG or Reset will produce approximately a 1 µV change on the output. For H1 and H2 timing stability is more important than clock level stability.

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	50	°C	1
Humidity	RH	5	90	%	2

Notes:
Long-term storage toward the maximum temperature will accelerate color filter degradation.
T = 25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions.*
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long term storage (>1 year) should be avoided.

Mechanical Drawings

Completed Assembly

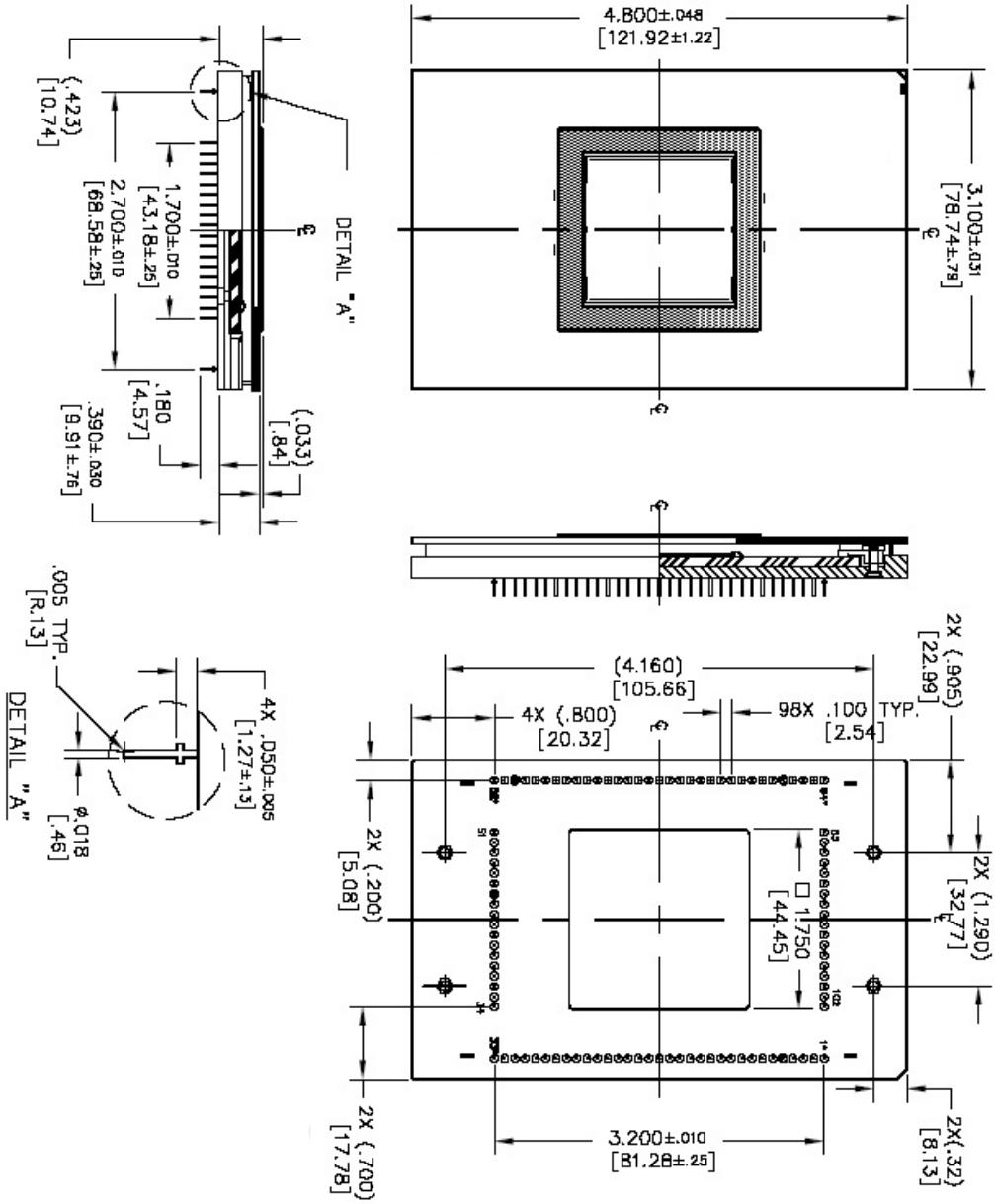


Figure 37: Completed Assembly

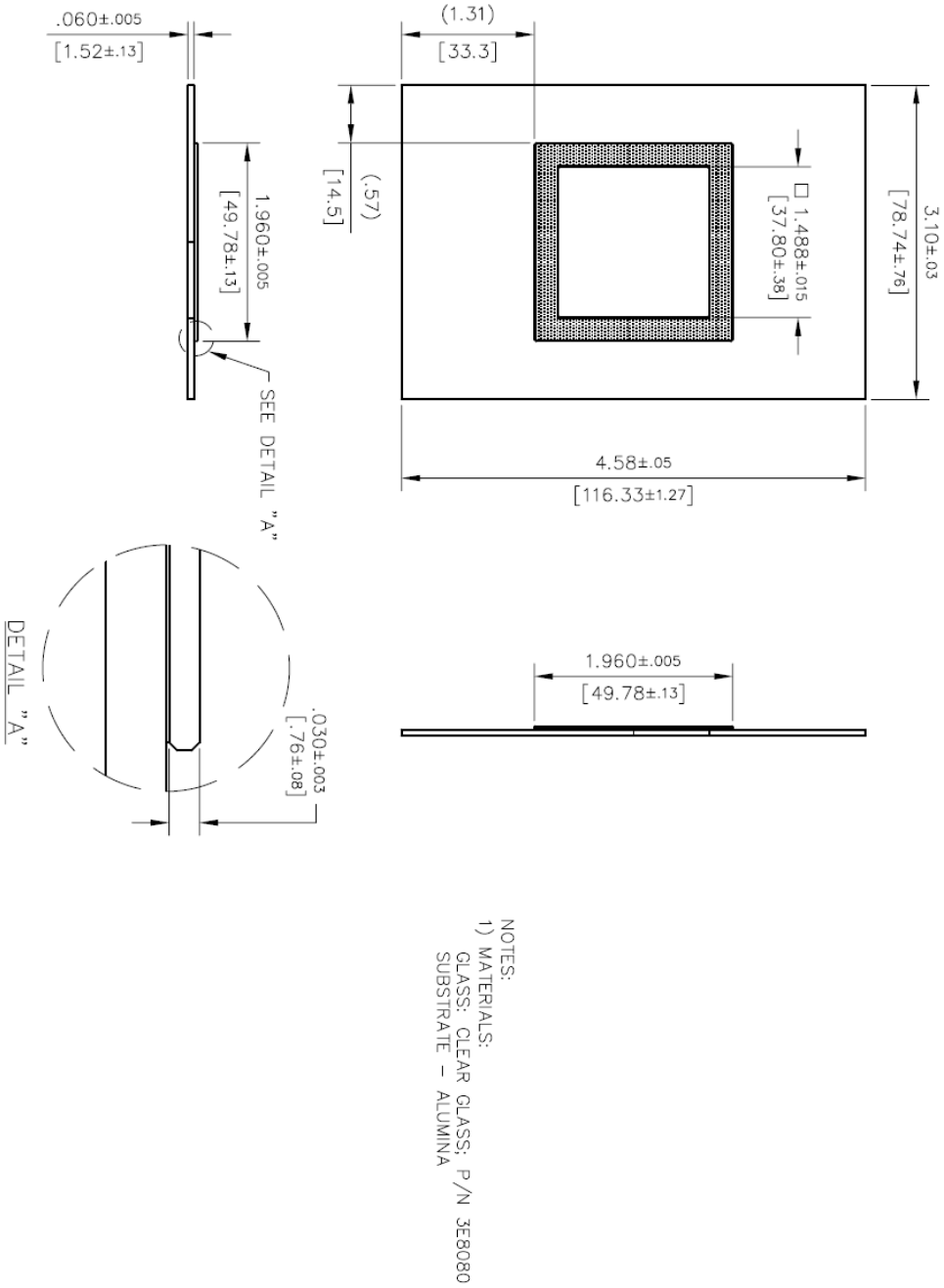


Figure 38: Glass Drawing

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-1416

Revision Number	Description of Changes
1.0	• Formal reissue (previous format version was labeled as revision 2.0).
3.0	• Resequence the revision to match historical releases. • This revision release had an update to the ESD circuit and the power up sequence. • A defect specification section is included. • Change to Applications use on front page. • Rename part number for proprietary package type in Ordering Information section. • Maximum Ratings table added
3.0_2	• Updated corrections and formatting in Summary Specification; title, size of imager, etc. • Removal of "ISS" references throughout • Updated miscellaneous formatting items. • Updated contact information under Ordering Information section. • Updated pixel array layout description in Device Description - Architecture section • Corrected reference to ESD pin descriptions as contained in Bond Pad Assignment Table • Removal of Class reference in Defect Definitions table. • Updating company referenced in Life Support Applications Policy and Specification Liability statement.

PS0067

Revision Number	Date	Description of Changes
1.0	9/21/12	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections • Updated limits for Output Amplifier, QE, MTF, and Total Read Noise • Added Microlens to the description of the 4H0402 version in Ordering Information. • Revised definition of Reset Clock waveform. Components specified are Reset Clock Low level and Reset Clock Amplitude. • Added a clock signal waveform, See Figure 34: Reset Clock Waveform. • Corrected the ordering information section to reflect four part number version. • Left VR line items in specification parameter table to be TBD (To Be Reviewed) • Sensor Read Noise entry created. Replaces Read Noise. • Removed marking code on ordering information • Added a scope trace to show 50% crossover example of the vertical clock.
2.0	10/1/12	• Correction to ordering information – part names.
3.0	5/30/13	• Update to final TBR values associated with Reset clock swing level. Remove the requirement for VH to be managed as other pins for ESD protection (that is not applicable to VH).
3.1	6/4/14	• Updated branding

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