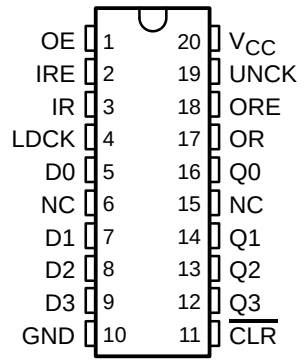
- **Independent Synchronous Inputs and Outputs**
- **16 Words by 4 Bits Each**
- **3-State Outputs Drive Bus Lines Directly**
- **Data Rates up to 10 MHz**
- **Fall-Through Time 50 ns Typical**
- **Data Terminals Arranged for Printed Circuit Board Layout**
- **Expandable, Using External Gating**
- **Packaged in Standard Ceramic (J) 300-mil DIPs**

J PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54LS222A 64-bit, low-power Schottky memory is organized as 16 words by 4 bits each. It can be expanded in multiples of 15m + 1 words or 4n bits, or both (where n is the number of packages in the vertical array, and m is the number of packages in the horizontal array); however, some external gating is required. For longer words, the input-ready (IR) signals of the first-rank packages and output-ready (OR) signals of the last-rank packages must be ANDed for proper synchronization.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written to and read from its array at independent data rates. These FIFOs are designed to process data at rates up to 10 MHz in a bit-parallel format, word by word.

The load clock (LDCK) normally is held low, and data is written into memory on the high-to-low transition of LDCK. The unload clock (UNCK) normally is held high, and data is read out on the low-to-high transition of UNCK. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the IR and OR flags that indicate not-full and not-empty conditions. IR is high only when the memory is not full and LDCK is low. OR is high only when the memory is not empty and UNCK is high.

A low level on the clear ($\overline{\text{CLR}}$) input resets the internal stack-control pointers and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the IR and OR outputs.

The SN54LS222A is characterized over the full military temperature range of –55°C to 125°C.



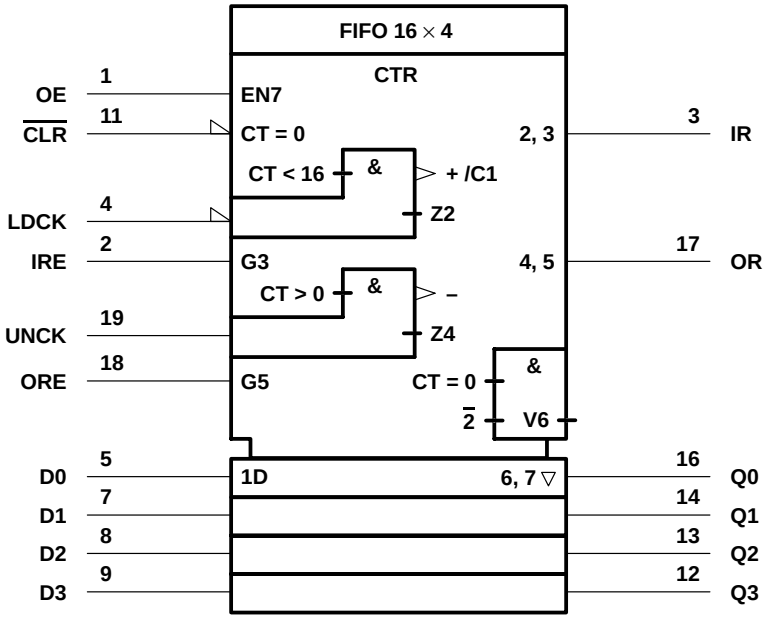
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated

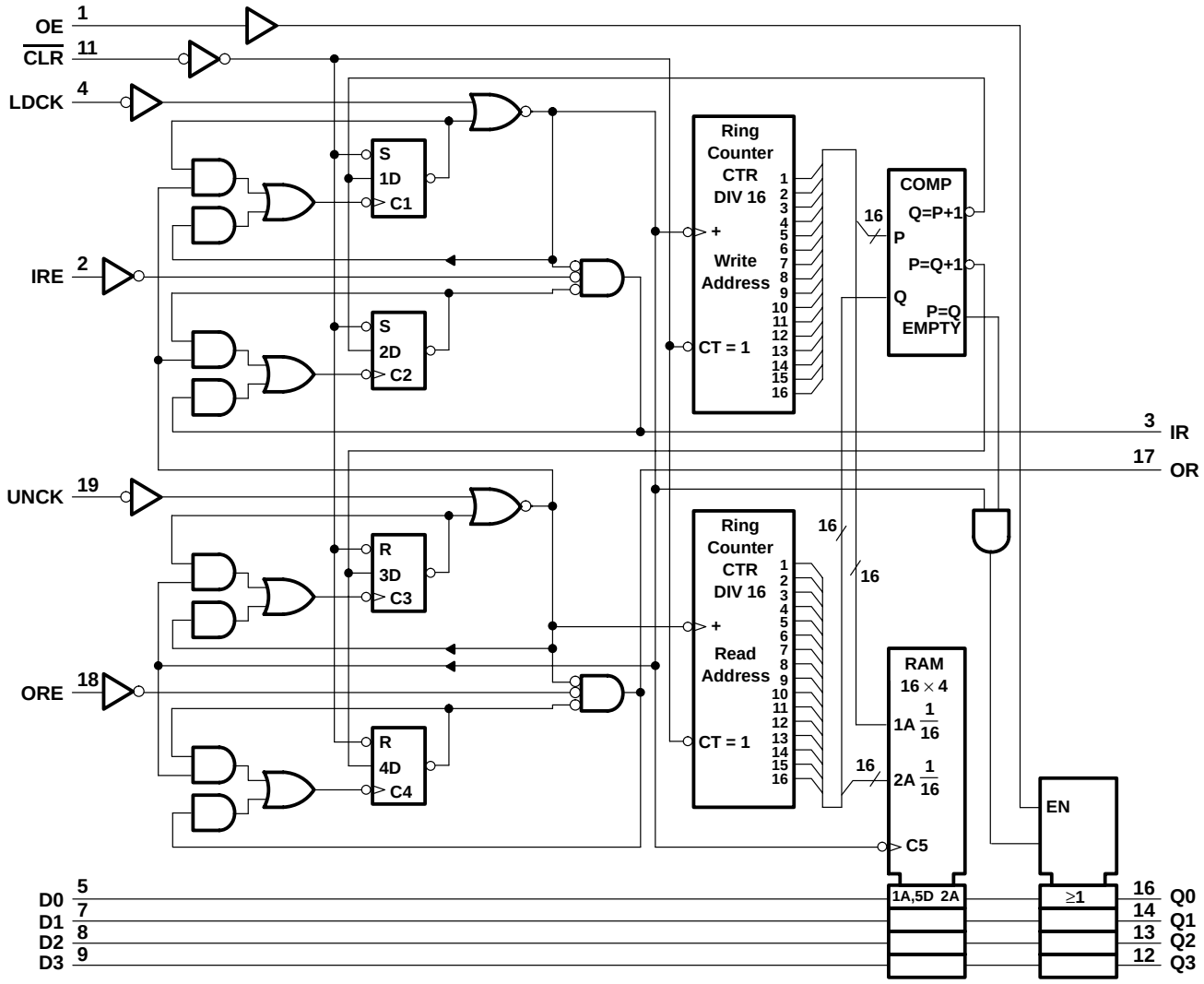
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

logic symbol†

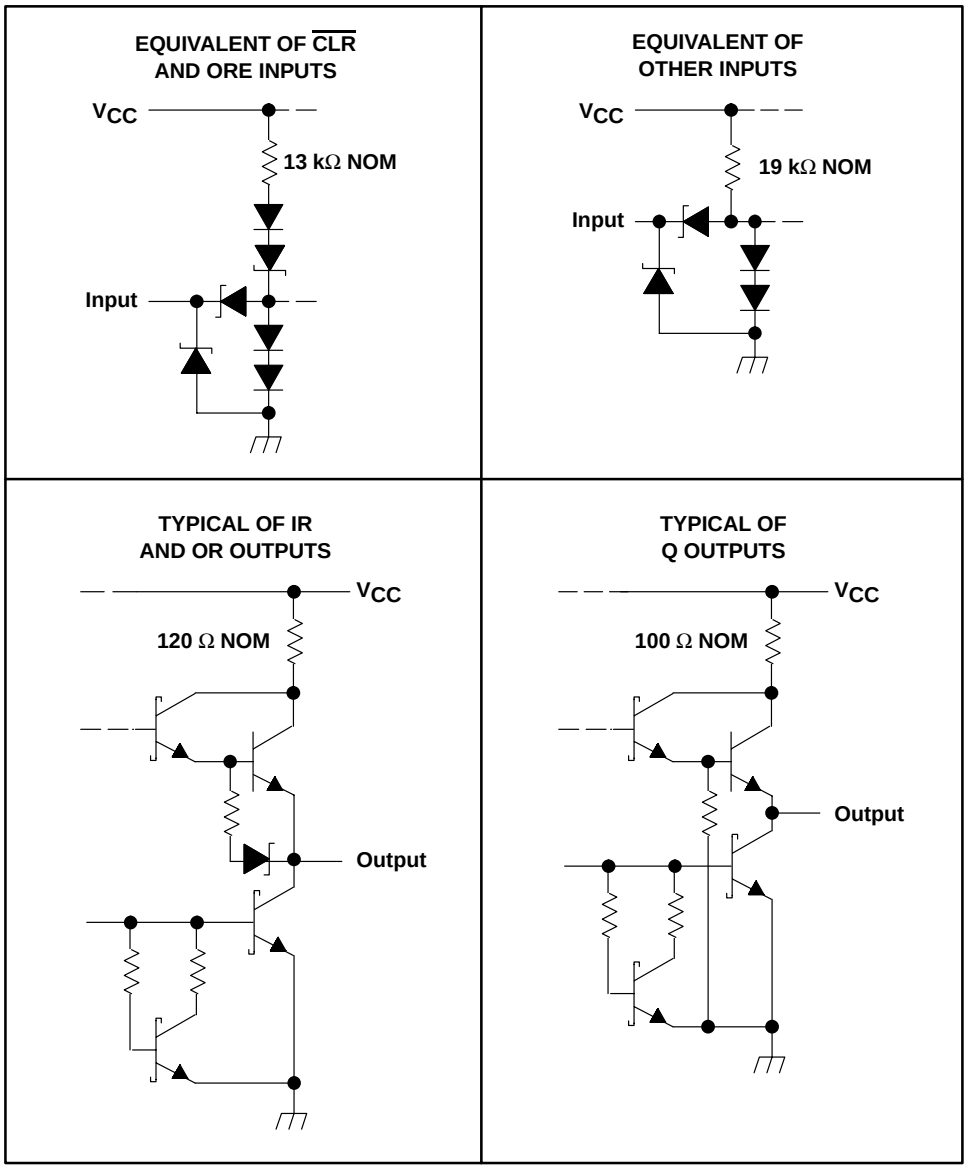


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. This symbol is functionally accurate, but does not show the details of implementation; for these details, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

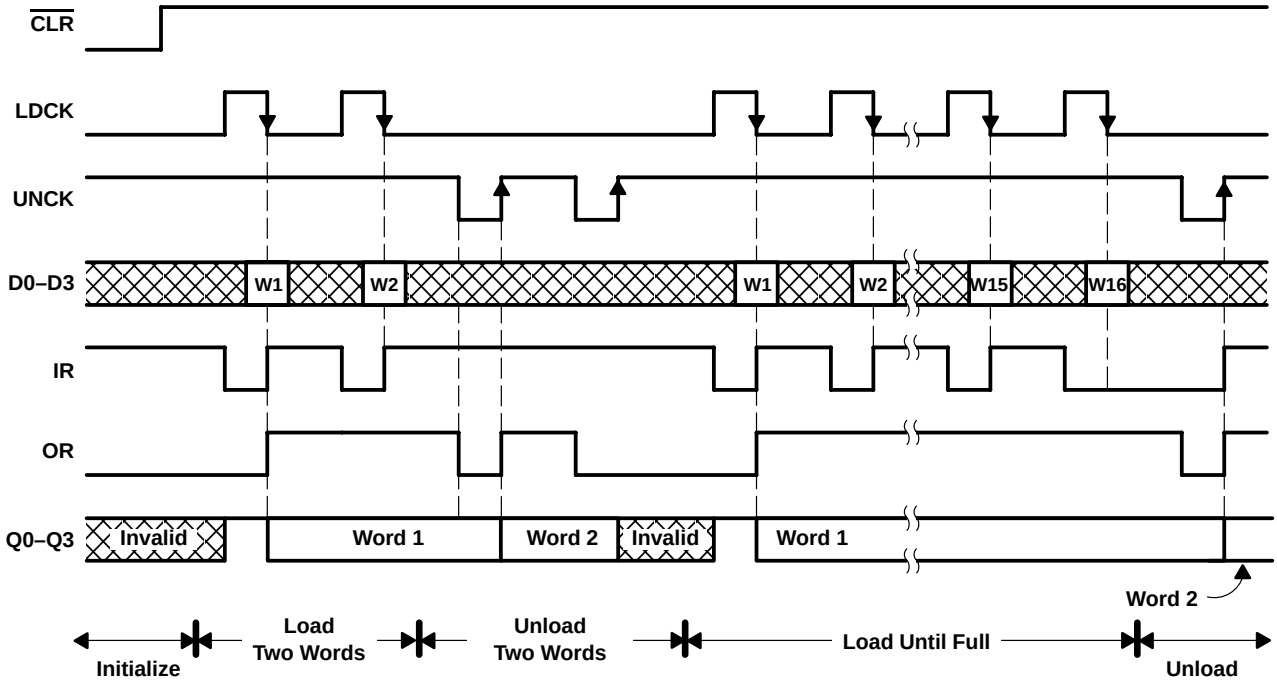
logic diagram (positive logic)



schematics of inputs and outputs



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Off-state output voltage range, V_O . . . . . –0.5 V to 5.5 V
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.7	V
I_{OH}	High-level output current	Q outputs			–1	mA
		IR, OR			–0.4	
I_{OL}	Low-level output current	Q outputs			12	mA
		IR, OR			4	
T_A	Operating free-air temperature		–55		125	°C

NOTE 2: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = MIN,	I_I = –18 mA			–1.5	V
V_{OH}	Q outputs	V_{CC} = MIN,	I_{OH} = –1 mA	2.4	3.3		V
	IR, OR	V_{CC} = MIN,	I_{OH} = –0.4 mA	2.5	3.4		
V_{OL}	Q outputs	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4	V
	IR, OR	V_{CC} = MIN,	I_{OL} = 4 mA		0.25	0.4	
I_{OZH}	Q outputs	V_{CC} = MAX,	V_O = 2.7 V			20	µA
I_{OZL}	Q outputs	V_{CC} = MAX,	V_O = 0.4 V			–20	µA
I_I		V_{CC} = MAX,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			–0.4	mA
I_{OS}§	Q outputs	V_{CC} = MAX		–30		–130	mA
	IR, OR			–20		–100	
I_{CC}		V_{CC} = MAX	Outputs high		84	135	mA
			Outputs low		87	155	
			Outputs disabled		89	155	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

timing requirements over recommended operating conditions (see Note 2 and Figure 2)

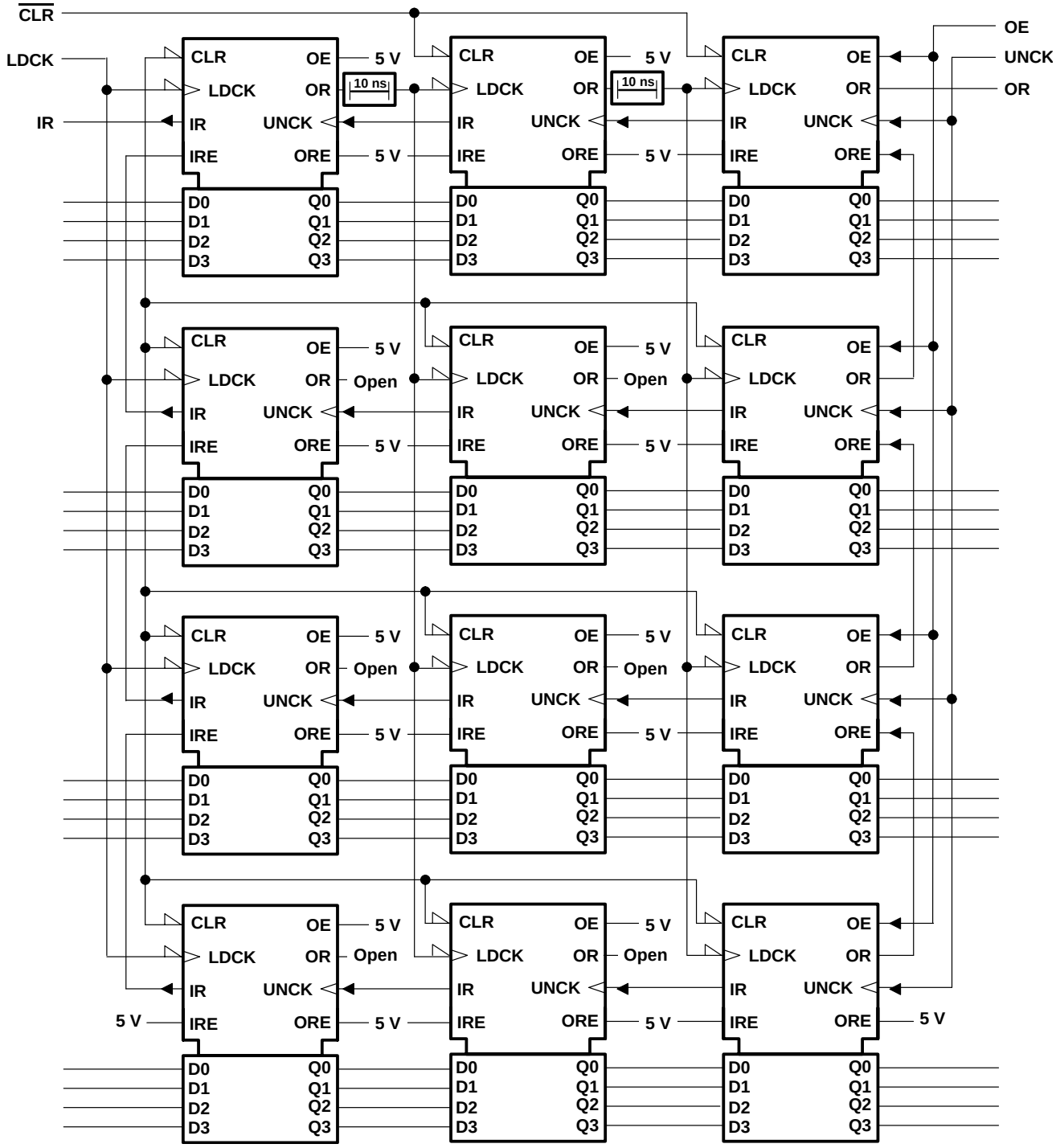
			MIN	MAX	UNIT
t_w	Pulse duration	LDCK high	60		ns
		LDCK low	15		
		UNCK low	30		
		UNCK high	30		
		$\overline{CLR}$ low	20		
t_{su}	Setup time	Data to LDCK↓	50		ns
		LDCK↓ before UNCK↓	50		
		UNCK↑ before LDCK↑	50		
t_h	Hold time	Data from LDCK↓	10		ns

NOTE 2: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	IRE↑	IR	R_L = 2 kΩ, C_L = 15 pF		23	35	ns
t_{PHL}	IRE↓				9	15	
t_{PLH}	ORE↑	OR	R_L = 2 kΩ, C_L = 15 pF		22	35	ns
t_{PHL}	ORE↓				9	15	
t_{PLH}	LDCK↓	IR	R_L = 2 kΩ, C_L = 15 pF		25	40	ns
t_{PHL}	LDCK↑				36	50	
t_{PLH}	LDCK↓	OR	R_L = 2 kΩ, C_L = 15 pF		48	70	ns
t_{PLH}	UNCK↑	OR	R_L = 2 kΩ, C_L = 15 pF		29	45	ns
t_{PHL}	UNCK↓				28	45	
t_{PLH}	UNCK↑	IR	R_L = 2 kΩ, C_L = 15 pF		49	70	ns
t_{PLH}	$\overline{CLR}$↓	IR	R_L = 2 kΩ, C_L = 15 pF		36	55	ns
t_{PHL}		OR			25	40	
t_{PHL}	LDCK↓	Q	R_L = 667 Ω, C_L = 45 pF		34	50	ns
t_{PLH}	UNCK↑	Q	R_L = 667 Ω, C_L = 45 pF		54	80	ns
t_{PHL}					45	70	
t_{PZL}	OE↑	Q	R_L = 667 Ω, C_L = 45 pF		22	35	ns
t_{PZH}					21	35	
t_{PLZ}	OE↓	Q	R_L = 667 Ω, C_L = 5 pF		16	30	ns
t_{PHZ}					18	30	

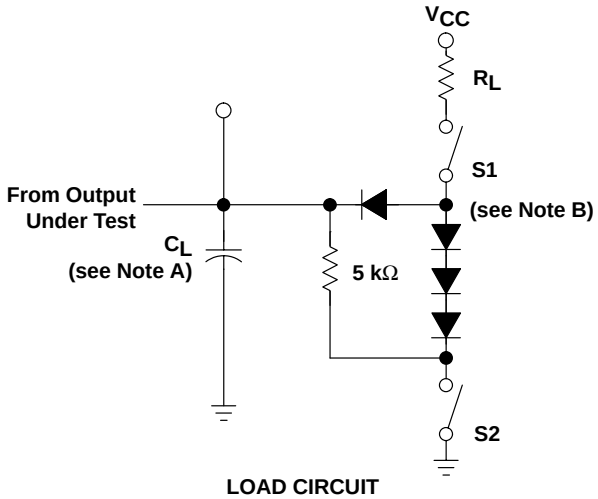
APPLICATION INFORMATION



10 ns ≡ Noninverting delay ≥10 ns (e.g., two stages of 'LS04), two places

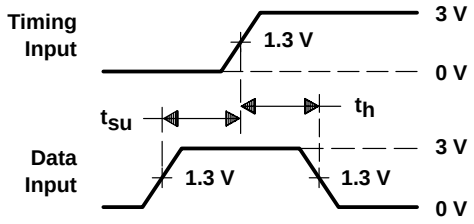
Figure 1. 48-Word by 16-Bit Expansion Using SN54LS222A

PARAMETER MEASUREMENT INFORMATION

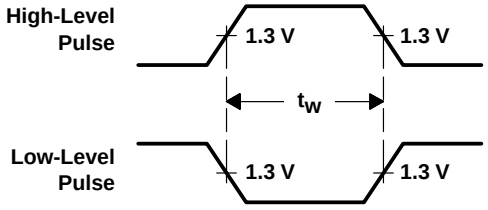


LOAD CIRCUIT

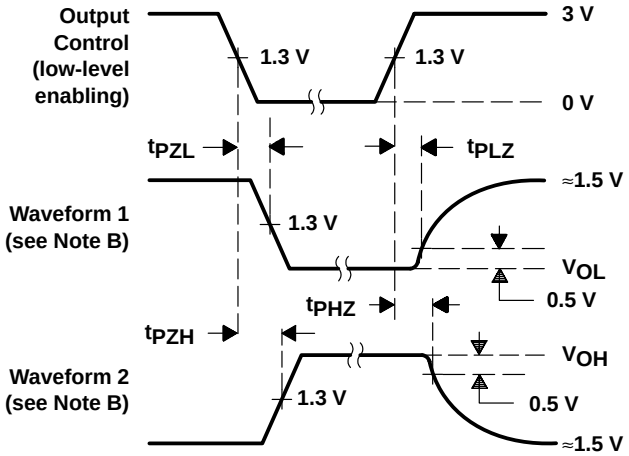
TEST	S1	S2
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed
t_{PLZ}/t_{PHZ}	Closed	Closed
t_{PLH}/t_{PHL}	Closed	Closed



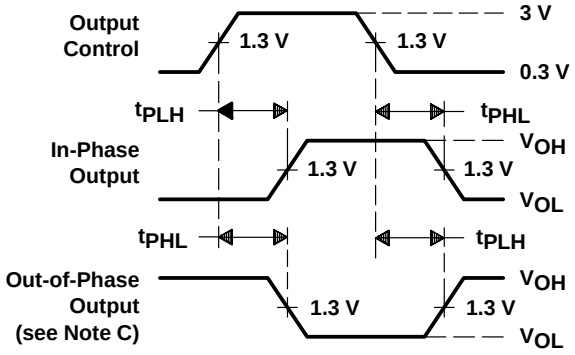
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r < 15 ns, t_f < 6 ns, Z_O ≈ 50 Ω.
D. All diodes are 1N916 or 1N3064.
E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN54LS222AJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SNJ54LS222AJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

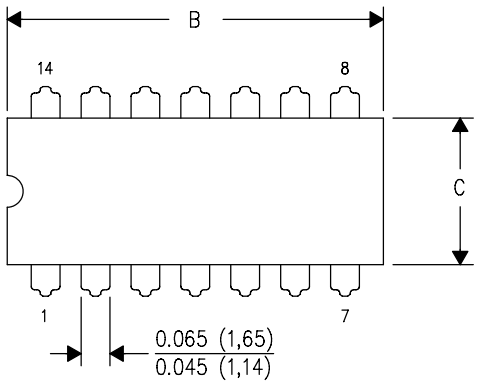
OTHER QUALIFIED VERSIONS OF SN54LS222A :
- Catalog: SN74LS222A

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

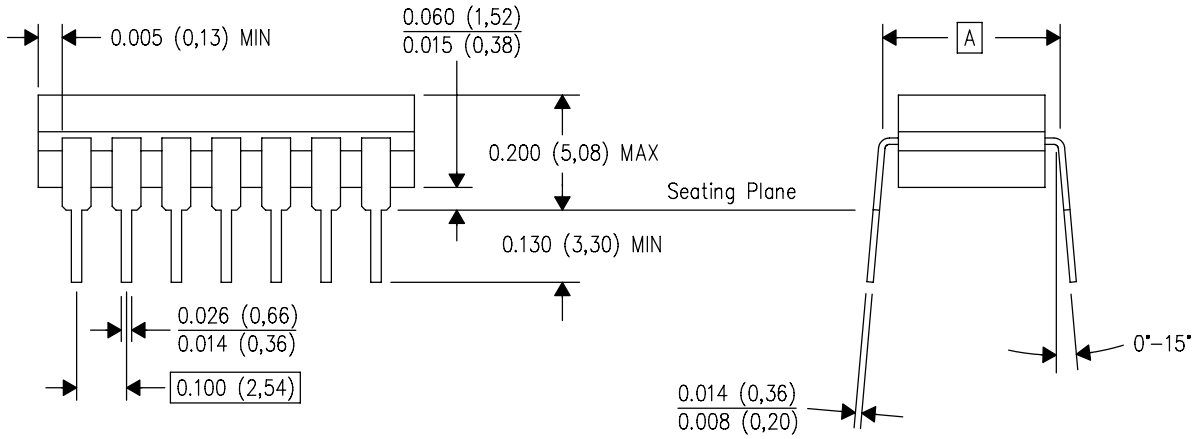
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated