340KHz, 2A, Asynchronous Step-Down Regulator

Halogen Free

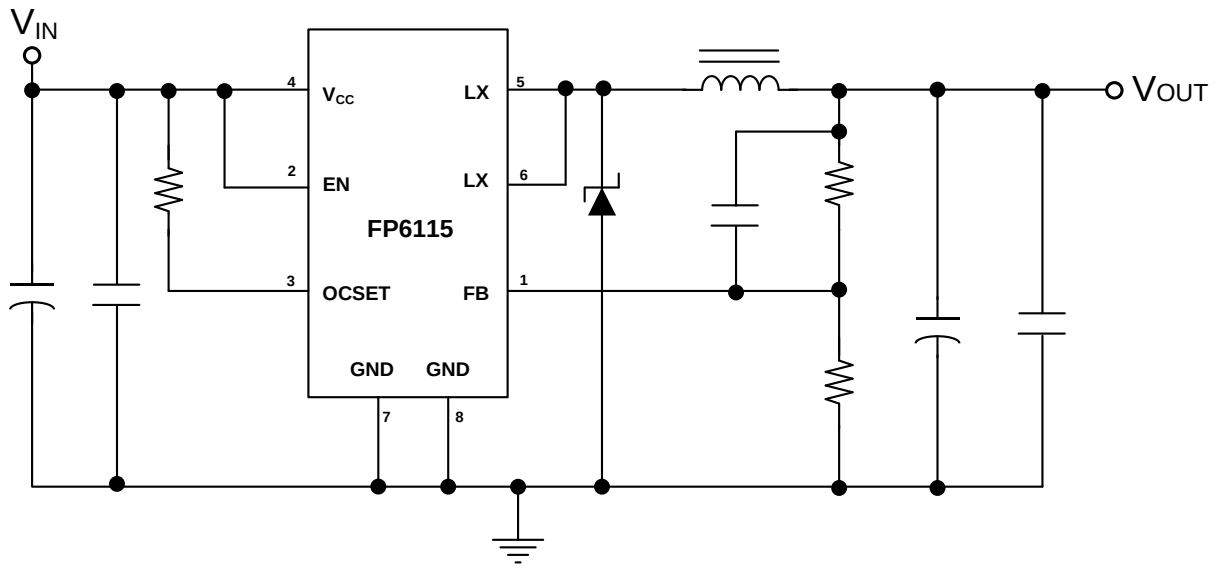
General Description

The FP6115 is a buck switching regulator for wide operating voltage application fields. The FP6115 includes a high current P-MOSFET, a high precision reference (0.8V) for comparing output voltage with a feedback amplifier, an internal soft start timer and dead-time controller. The oscillator is for controlling the maximum duty cycle and PWM frequency.

Features

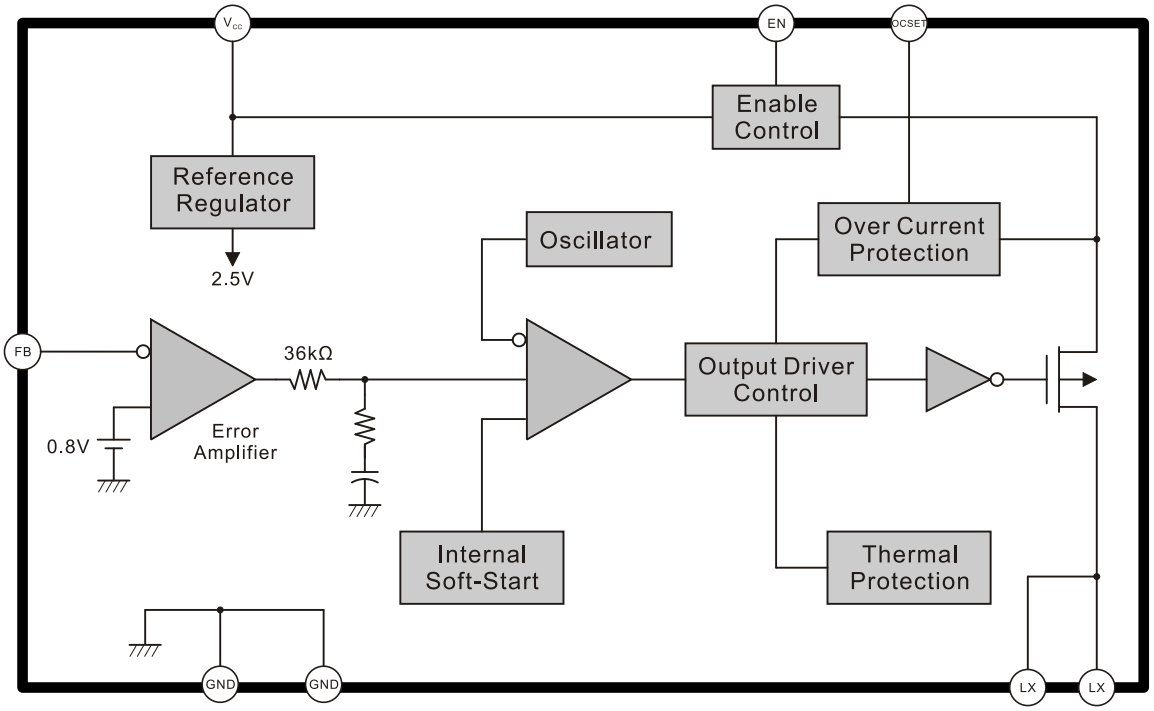
- Precision Feedback Reference Voltage: 0.8V (2%)
- Wide Supply Voltage Operating Range: 3.6 to 23V
- Output Adjustable From 0.8V to 16V
- Low Current Consumption: 3mA
- Internal Fixed Oscillator Frequency: 340KHz (Typ.)
- Internal Soft-Start Function (SS)
- Built-In P-MOSFET for 2A Output Loading
- Over Current Protection
- Package: SOP-8L

Typical Application Circuit



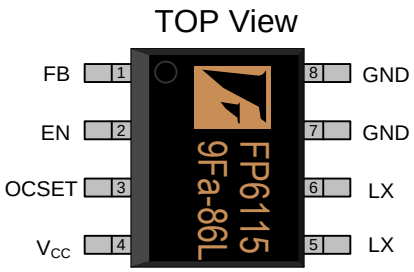
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Function Block Diagram



Pin Descriptions

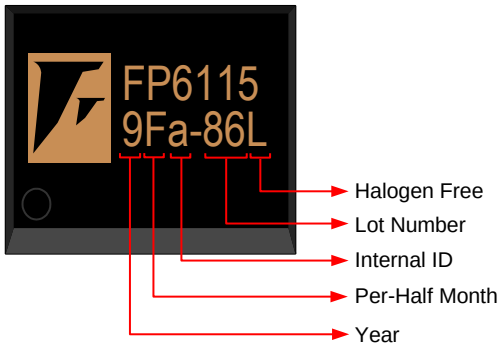
SOP-8L



Name	No.	I / O	Description
FB	1	I	Error Amplifier Inverting Input
EN	2	I	Enable Control
OCSET	3	I	Set Switch Output Over Current
V_{CC}	4	P	IC Power Supply (PMOS Source)
LX	5	O	PMOS High Current Output
LX	6	O	PMOS High Current Output
GND	7	P	IC Ground
GND	8	P	IC Ground

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Marking Information



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

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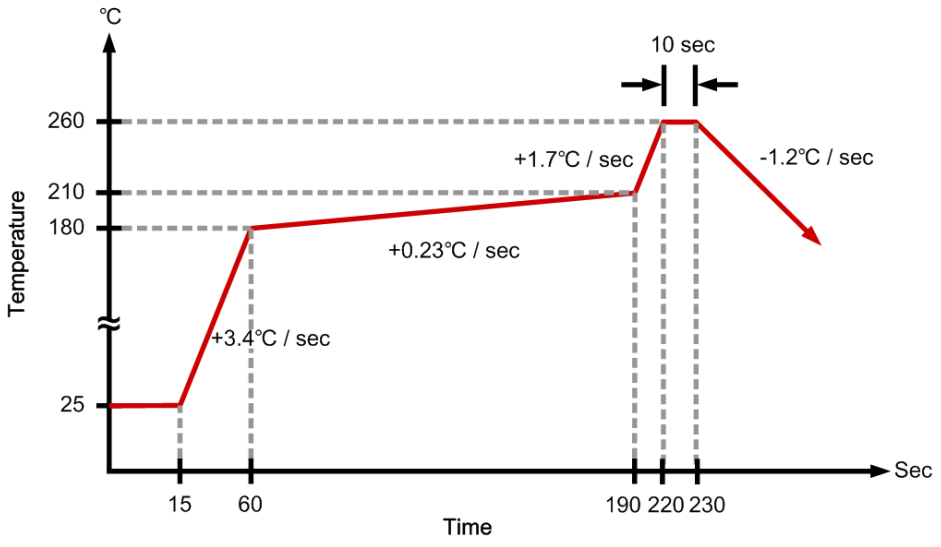
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6115DR-G1	-25°C ~ +85°C	SOP-8L	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				23	V
Output Source Current					3.5	A
Error Amplifier Inverting Input			-0.3		1.2	V
Allowable Power Dissipation	P_D	SOP-8L $T_A \leqq +25°C$			650	mW
Thermal Resistance	θ_{JA}	SOP-8L			+110	°C / W
	θ_{JC}				+55	°C / W
Operating Temperature			-25		+85	°C
ESD Susceptibility		HBM (Human Body Mode)			2	KV
		MM (Machine Mode)			200	V
Junction Temperature	T_J				+150	°C
Storage Temperature	T_S	SOP-8L	-55		+150	°C
SOP-8L Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



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Recommended Operating Conditions

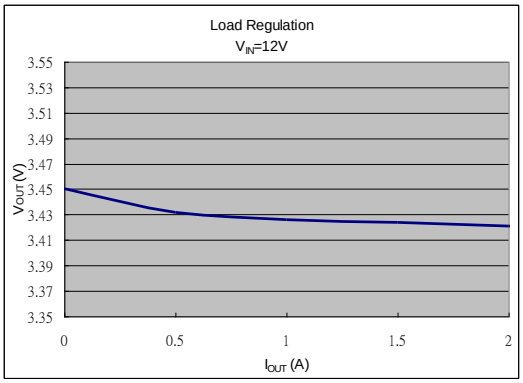
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3.6		23	V
Operating Temperature			-25		85	°C

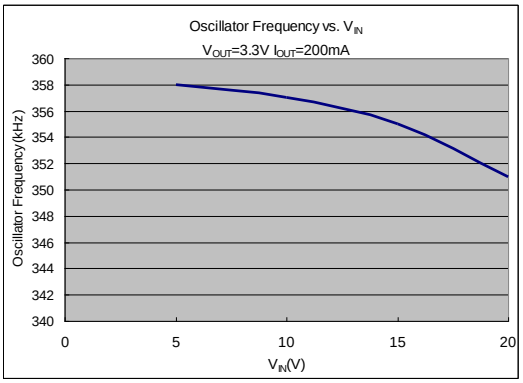
DC Electrical Characteristics (V_{CC}=6V,T_A = 25°C, unless otherwise noted)

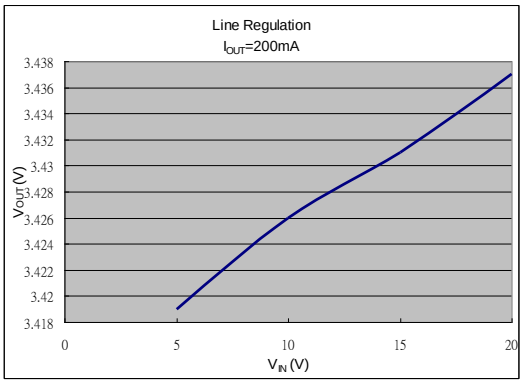
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference						
Feedback Voltage	V_{REF}		0.784	0.8	0.816	V
Line Regulation	$\Delta V_{REF} / V_{REF}$	V_{CC}=3.6V to 23V		1	2	%
Load Regulation	$\Delta V_{REF} / V_{REF}$	I_{OUT}=0A to 2A		2		%
Feedback Voltage Change with Temperature	$\Delta V_{REF} / V_{REF}$	T_A=- -25°C to +85°C		1	2	%
Oscillator Section						
Oscillation Frequency	f	Measured from LX pin waveform		340		KHz
Short Circuit or Over Current Oscillation Frequency	f_{SC}	Measured from LX pin waveform		50		KHz
Frequency Change with Voltage	$\Delta f / \Delta V$	V_{CC}=3.6V to 23V		5		%
Frequency Change with Temperature	$\Delta f / \Delta T$	T_A = -25°C to +85°C		5		%
Idle Period Adjustment Section						
Maximum Duty Cycle	T_{DUTY}	V_{FB} =0.2V		80		%
Output Section						
PMOS Switch Current	I_{LX}		-2			A
PMOS On Resistance	$R_{DS\ (ON)}$	V_{CC}=4.5V		70	95	mΩ
		V_{CC}=10V		50	60	mΩ
Thermal Shutdown Section						
Thermal Shutdown Temperature				+150		°C
Over Current Protection Section						
OCSET Bias Current	I_{OCSET}			40		µA
Total Device Section						
EN Pin Input Current	I_{EN}	V_{EN}=2.5V			20	µA
EN Pin On Threshold	V_{UPPER}	EN pin upper		1.1		V
EN Pin Off Threshold	V_{LOW}	EN pin low		0.85		V
EN Pin Hysteresis	V_{HYS}		150	250		mV
Supply Shutdown Current	I_{SD}	V_{EN}=0V		2	10	µA
Supply Average current	I_{AVE}			3	6	mA

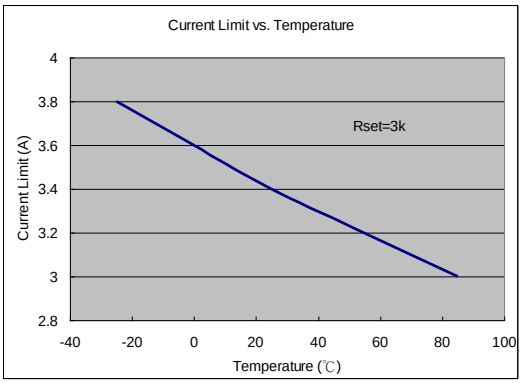
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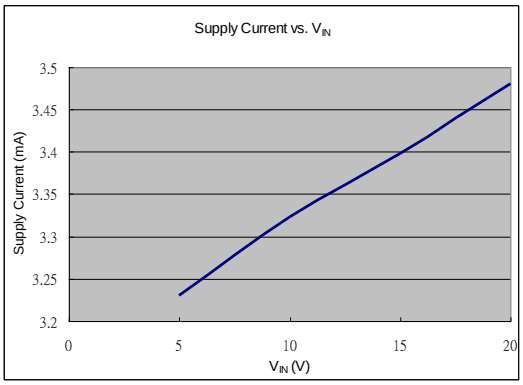
Typical Operating Characteristics

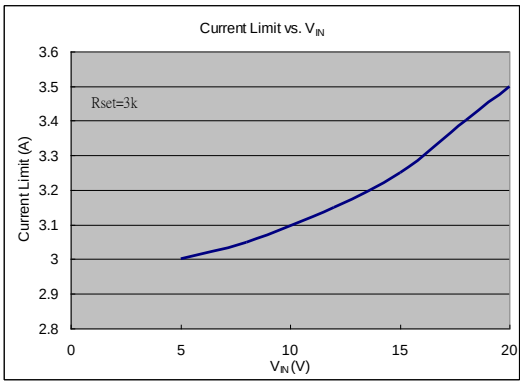


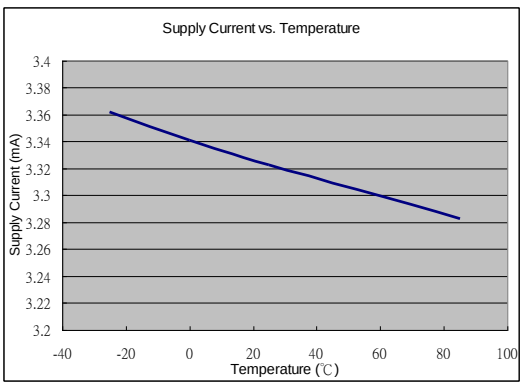


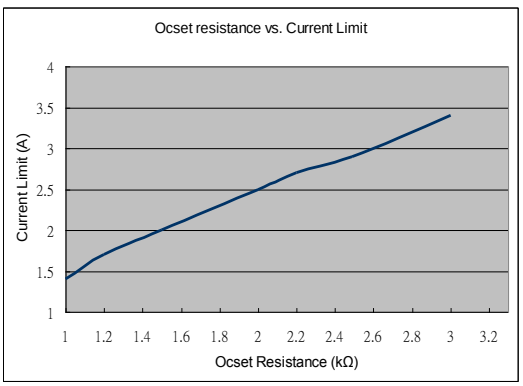






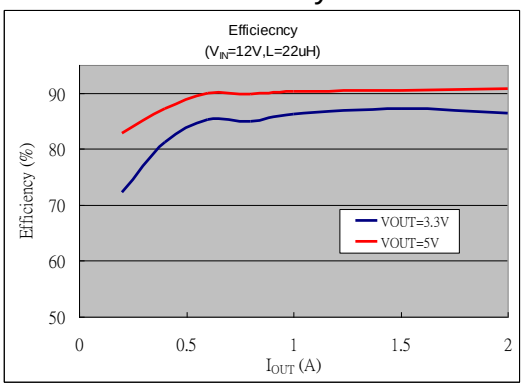




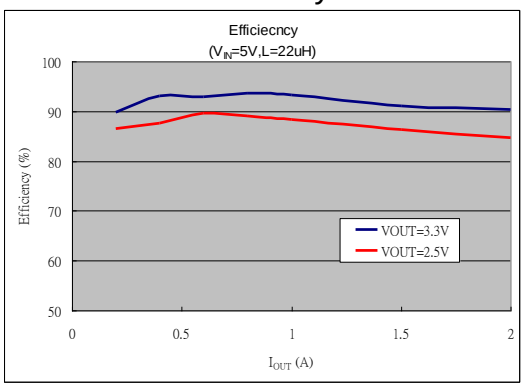


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Efficiency

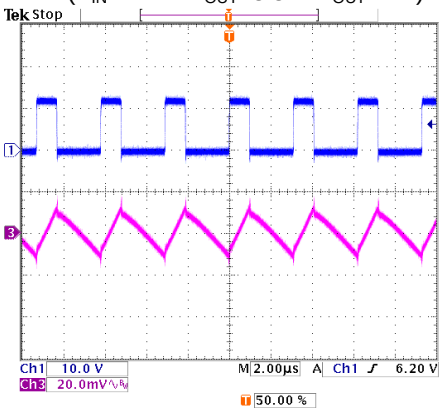


Efficiency



Output Ripple

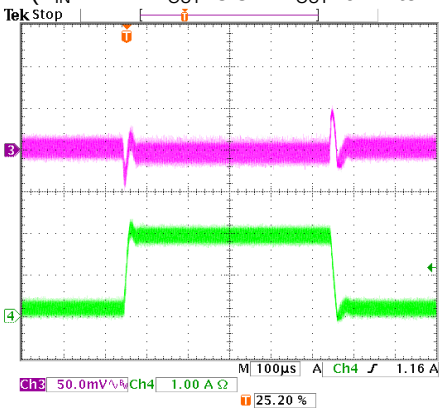
(V_{IN}=12V，V_{OUT}=3.3V，I_{OUT}= 2A)



Ch1 LX Ch2 V_{OUT}

Transient Response

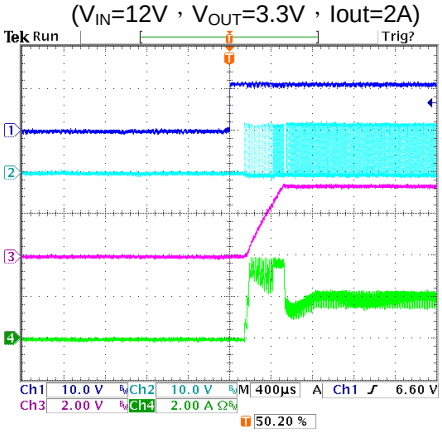
(V_{IN}=12V，V_{OUT}=3.3V，I_{OUT}=0.2A to 2A)



Ch3 V_{OUT} Ch4 I_{LX}

EN on Test

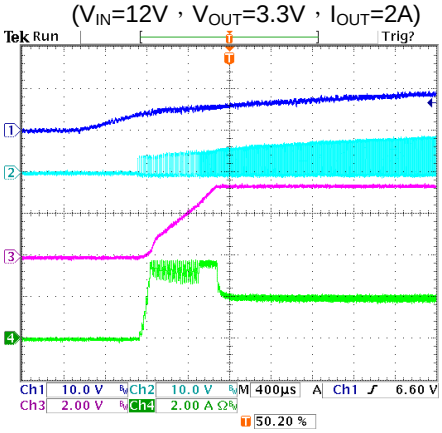
(V_{IN}=12V，V_{OUT}=3.3V，Iout=2A)



Ch1 EN Ch2 LX Ch3 V_{OUT} Ch4 I_{LX}

Power on Test

(V_{IN}=12V，V_{OUT}=3.3V，I_{OUT}=2A)



Ch1 V_{IN} Ch2 LX Ch3 V_{OUT} Ch4 I_{LX}

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Function Description

Voltage Reference

A 2.5V reference regulator supplies FP6115 internal circuits and uses a resistive divider to provide 0.8V precision reference voltage on the non-inverting terminal of error amplifier.

Error Amplifier

The error amplifier compares a sample of the DC-DC converter output voltage to the 0.8V (V_{REF}) reference and generates an error signal for the PWM comparator. Output voltage of the DC-DC converter is setting by the resistor divider with following expression (see Fig. 1)

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \times V_{REF}$$

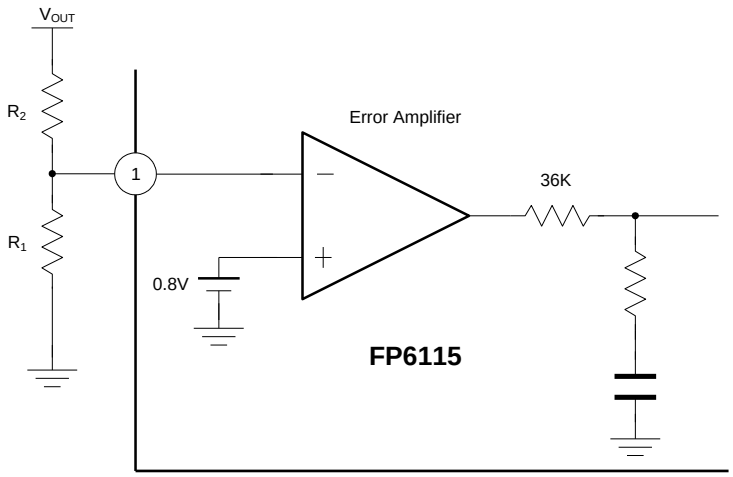


Figure 1. Error Amplifier with Feedback Resistance Divider

The recommended resistor value is summarized below:

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)
1.8	2.4k	3k
2.5	3.2k	6.8k
3.3	1.5k	4.7k
5	2k	10.5k

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Oscillator

The fixed frequency is generated by an internal RC oscillator. Its typical values is 340KHz in normal operation and 50KHz in short circuit condition.

Thermal Protection

When a heavy loading draws current from the regulator, the chip temperature will rise. Once the junction temperature exceeds 150℃, FP6115 thermal protection function will be triggered and the LX output will be turned off. When junction temperature is lower, FP6115 starts again and enable LX pin output.

Over Current Protection

The FP6115 uses cycle-by-cycle current limit to protect the internal power switch. During each switching cycle, a current limit comparator detects if the power switch current exceeds the external setting current or not. Once over current occurs, chip will decrease the oscillator frequency to prevent from thermal issue. The current limit threshold is setting by external resistor (R_3) which is connecting from V_{CC} to OCSET pin. An internal 40μA current sink which draws current from the resistor sets the voltage at pin OCSET. Please refer to the following formula for setting the current limit value:

$$I_{OCP} = \frac{I_{OCSET} \times R_3}{35m\Omega}$$

Here, 35mΩ is internal sense resistance.

Example：

$$I_{OCP} = \frac{40\mu A \times 2.49k}{35m\Omega} = 2.85A$$

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Application Information

Input Capacitor Selection

The input capacitor must be connected to the V_{CC} pin and GND pin of the FP6115 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

In switch mode, the input current is discontinuous in a buck converter. The source current of the high-side MOSFET is a square wave. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{RMS} = I_{O_MAX}\sqrt{\frac{V_O}{V_{IN}}\left(1-\frac{V_O}{V_{IN}}\right)}$$

It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is I_{O_MAX} / 2.

Inductor Selection

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance result in high ripple current. However, the larger value inductor usually has a larger physical size, higher series resistance, and lower saturation current. On the experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN}-V_O)}{f\times\Delta I_L}\frac{V_O}{V_{IN}} = \frac{(V_{IN}-V_O)}{f\times[2\times(10\%\sim 20\%)I_O]}\frac{V_O}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_L = \frac{V_O}{f\times L}\times\left(1-\frac{V_O}{V_{IN}}\right)$$

Choose an inductor that does not saturate under the worst-case load conditions, which is the load current plus half the peak-to-peak inductor ripple current, even at the highest operating temperature. The peak inductor current is:

$$I_{L_PEAK} = I_O + \frac{\Delta I_L}{2}$$

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The inductors in different shape and style are available from manufacturers. Shielded inductors are small and radiate less EMI issue. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Inductor Value (μH)	Dimensions(mm)	Component Supplier	Model
10	10.3×10.3×4.0	FENG-JUI	TPRH10D40-10R
10	10.1×10.1×3.0	Sumida	CDRH104R
15	10.3×10.3×4.0	FENG-JUI	TPRH10D40-15R

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_O = \Delta I_L \times \left(ESR_{C_{OUT}} + \frac{1}{8 \times f \times C_{OUT}} \right)$$

Where f = operating frequency, C_{OUT}= output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

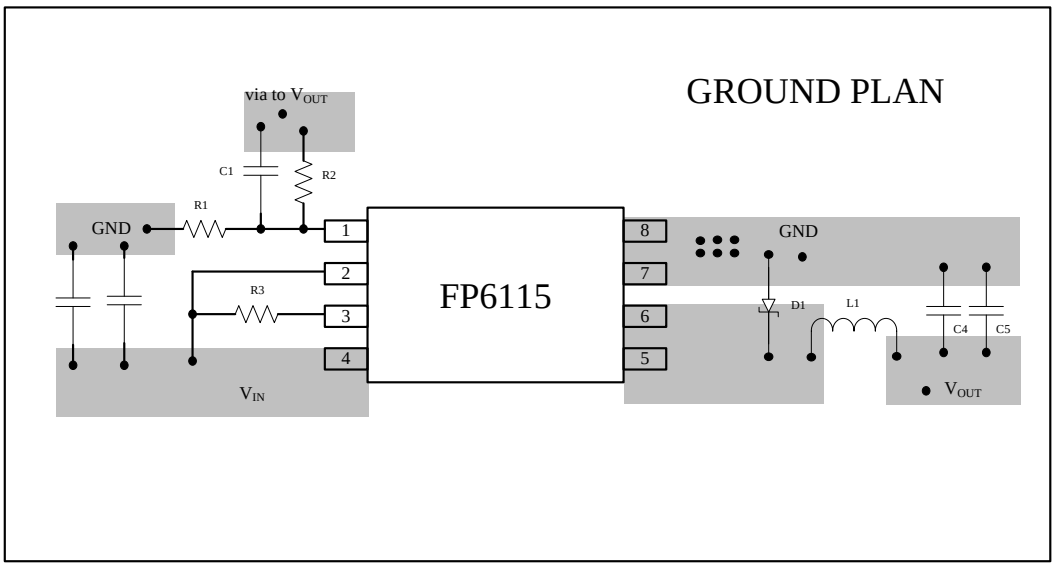
Using Ceramic Input and Output Capacitors

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. In best condition, this ringing can couple to the output and be mistaken as loop instability. In worst condition, a sudden inrush of current through the long wires can potentially generate a voltage spike at V_{IN}, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the one with X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

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PC Board Layout Checklist

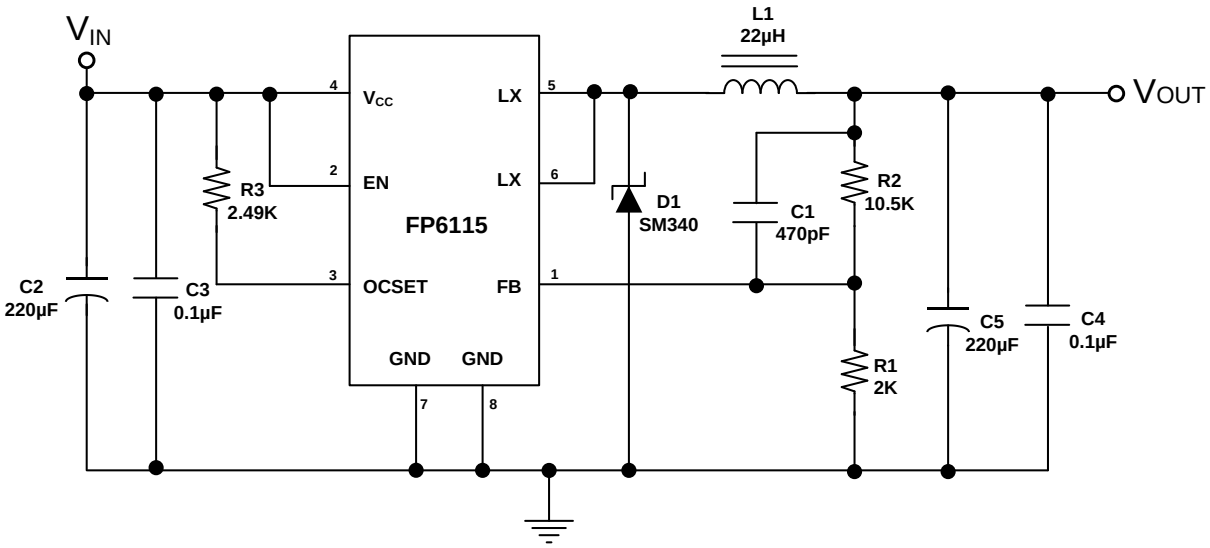
1. The power traces, consisting of the GND trace, the LX trace and the V_{IN} trace should be kept short, direct and wide.
2. Place C_{IN} near V_{CC} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
3. The resistive divider $R_1$and R_2 must be connected to FB pin directly as closely as possible.
4. FB is a sensitive node. Please keep it away from switching node, LX. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and the layer on which the feedback trace is routed. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.
5. Keep the GND plates of C_{IN} and C_{OUT} as close as possible. Then connect this to the ground plane (if one is used) with several vias. This reduces ground plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the FP6115 GND pin by giving it a low impedance ground connection.



Suggested Layout

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Typical Application



FP6115 Basic DC-DC Regulator Circuits

For example:

The V_{IN} power supply is 12V and the V_{OUT} is designed for 5.0V / 2A solution.

The output voltage formula is:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \times V_{REF} = \left(1 + \frac{10.5K\Omega}{2K\Omega}\right) \times 0.8V = 5.0V$$

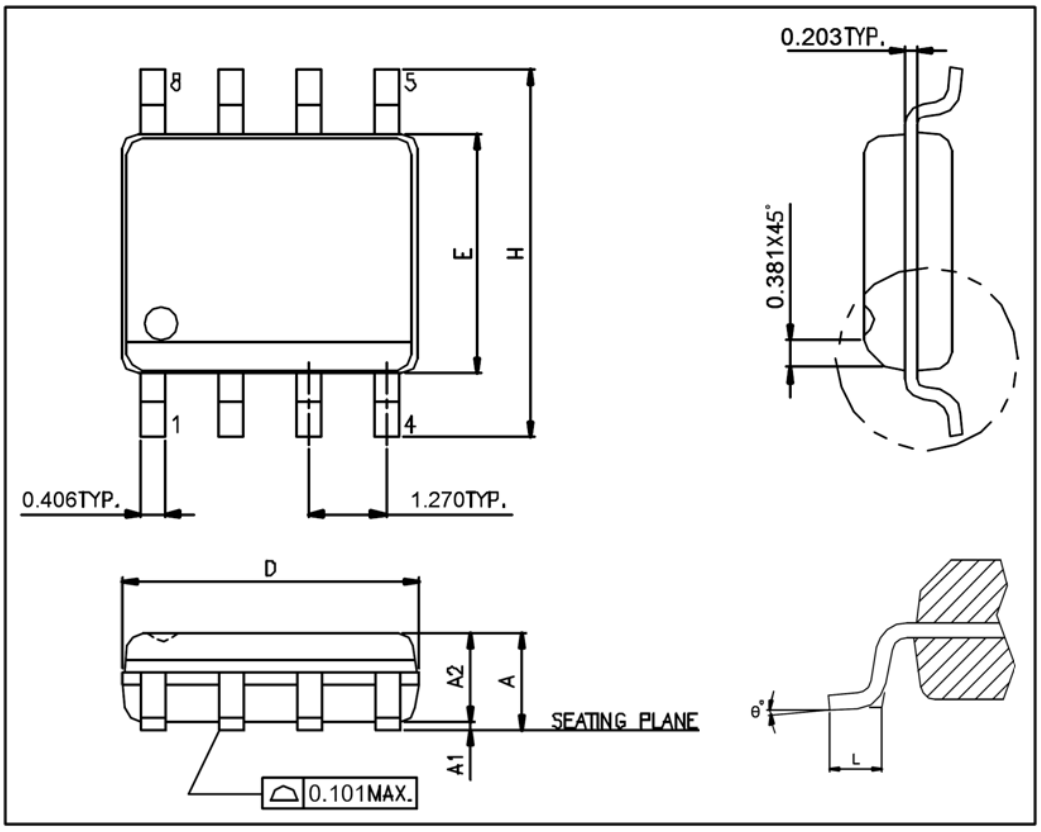
Notice:

1. **Tapping reel aluminum foil bags after unpacking must be stored at ≤10% RH environment.**
2. **Tapping reel aluminum foil bags after unpacking must sure surface-mount is completed within 168 hours.**

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Package Outline

SOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC Outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions gate burrs.
3. Dimension “E” does not include inter-lead flash, or protrusions.

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